Dual-Channel 16-Bit, 10MSPS, SAR ADC with Analog Front End

FEATURES

- Integrated fully-differential ADC drivers
  - Wide input common-mode voltage range
  - High common-mode rejection
  - Single-ended to differential conversion
- Gain options include: 1.03, 1.25, 1.53, 2.03, 2.74, 4.11, and 5.77
  - Integrated gain-setting resistors
- High performance
  - 16-bit resolution, no missing codes
  - Throughput: 10MSPS per channel
  - Conversion latency: 131.25ns
  - INL: 3ppm (typical), 4.6ppm (maximum)
  - SNR/THD
    - 92dBFS (typical)/-118dBc (typical) at f_{IN} = 1kHz
    - 91.1dBFS (typical)/-109dBc (typical) at f_{IN} = 500kHz
  - Noise spectral density: -158.8dBFS/Hz
- Low power
  - 88.9mW per channel typical at 10MSPS
- Integrated, low-drift reference buffers and decoupling
- Integrated V_{CM} generation
- Digital features and data interface
  - Conversion result FIFO, 16k samples per channel
  - Digital averaging filter with up to 2^{10} decimation
- SPI configuration per channel
- Configurable data interface per channel
  - Single lane, DDR, serial LVDS, 160Mbps per lane
  - Dual lane, DDR, serial LVDS, 80Mbps per lane
  - Single/quad lane SPI data interface
- Package
  - 196-ball, 10mm × 10mm CSP_BGA, 0.65mm pitch
  - Integrated supply decoupling capacitors
- Operating temperature range: −40°C to +85°C

APPLICATIONS

- Digital imaging
- Cell analysis
- Spectroscopy
- High-speed data acquisition
- Digital control loops, hardware in the loop
- Power quality analysis
- Source measurement units
- Nondestructive test

GENERAL DESCRIPTION

The AD4885 is a dual-channel, low noise, low power, high-speed, 16-bit, successive approximation register (SAR) analog-to-digital converter (ADC) with integrated fully-differential drivers (FDA) and gain-setting resistors. The two channels can be sampled either simultaneously or independently, which offers flexibility for a wide range of applications.

The integration of the ADC drivers, low drift reference buffers, low dropout (LDO) regulators along with all critical decoupling capacitors greatly simplifies analog front-end design challenges. Specified performance is easier to achieve, which requires a simpler and more compact printed circuit board (PCB) layout.

Optimized for input signals up to 1MHz, the AD4885 delivers low noise and exceptional linearity at remarkably low power consumption, which makes it ideal for many precision data acquisition systems.

Anti-aliasing filter requirements can be relaxed by taking advantage of the high sample rate to oversample, then apply integrated digital filtering and decimation to reduce noise and deliver an increase in dynamic range for applications where ultra-low latency is not required.

The AD4885 features a SAR architecture that results in a conversion latency of just 131.25ns. Therefore, it is a good fit for wide bandwidth applications that have multiplexed input signals, applications that require extremely low latency, or both. Such high throughput and low-latency applications can benefit from the two independent, multilane low-voltage differential signaling (LVDS) interfaces. Alternatively, the load on the digital host can be eased by storing the captured data in the on-chip, 16k samples per channel, first in, first out (FIFO) memory, then asynchronously accessing it via the serial-peripheral interface (SPI) data interfaces.

TYPICAL APPLICATION DIAGRAM

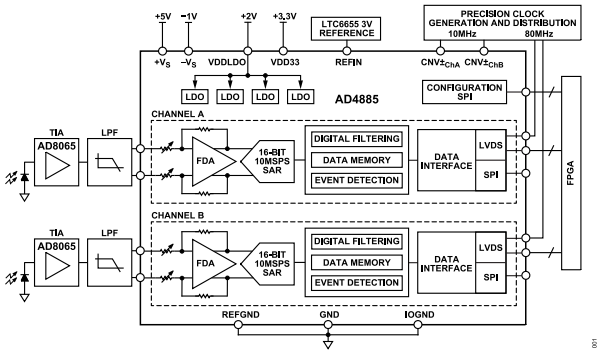

Figure 1. Typical Application Diagram

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REVISION HISTORY

10/2026—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

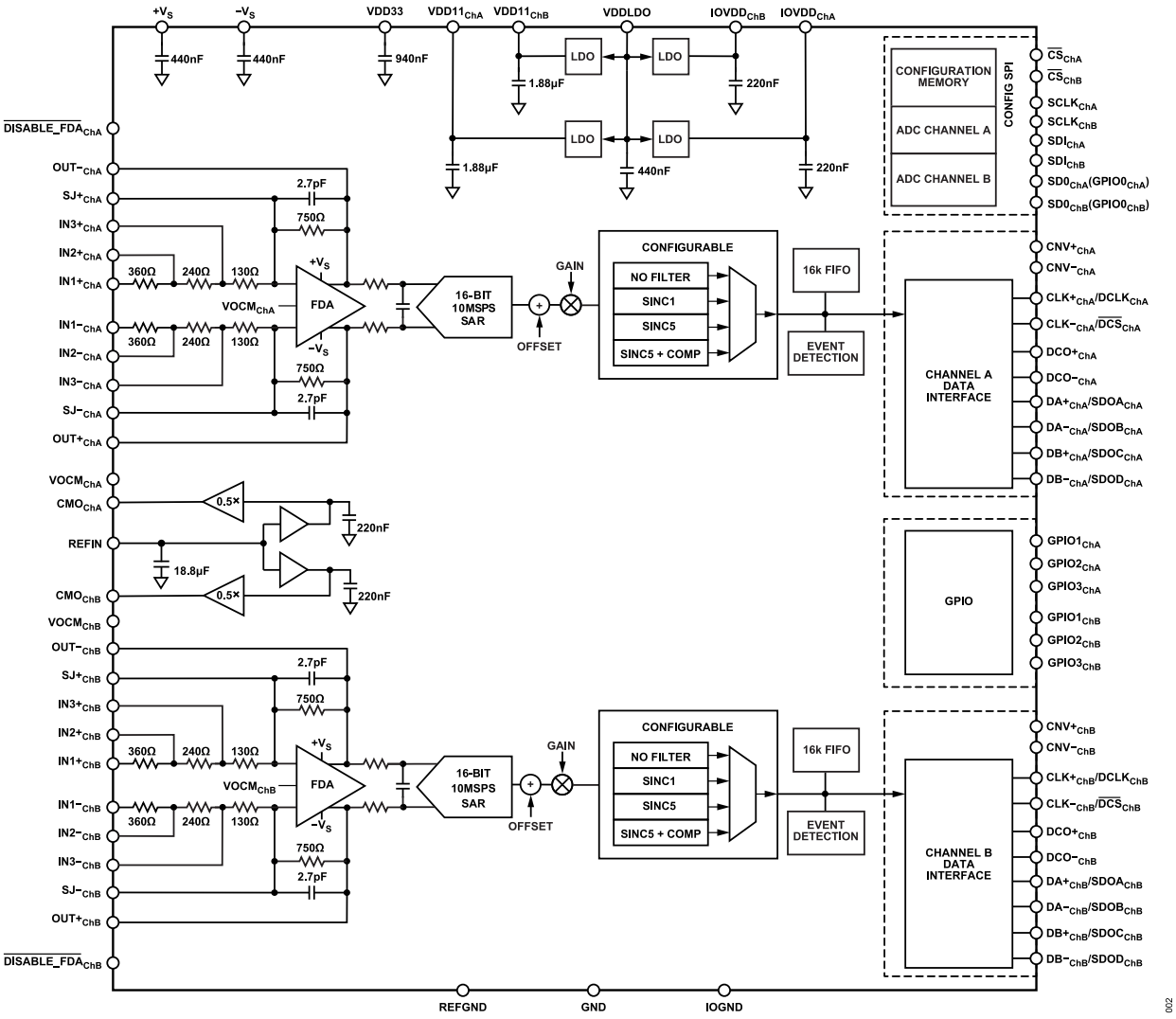

Figure 2. AD4885 Functional Block Diagram

SPECIFICATIONS

VDD33 = 3.3V ± 5%, VDDLDO = 1.4V to 2.7V, $VDD11_{ChA}$ = $VDD11_{ChB}$ = 1.1V ± 5%, $IOVDD_{ChA}$ = $IOVDD_{ChB}$ = 1.1V − 5% to 1.2V + 5%, voltage reference input (V_{REFIN}) = 3.0V, $+V_S$ = 5V ± 5%, $-V_S$ = −1V ± 5%, sampling frequency (f_S) = 10MHz, differential input drive with 1.5V common mode. Unless otherwise noted, T_A = T_{MIN} to T_{MAX}, Gain (G) = 1.03, no external FDA feedback capacitors (C_{fb} = 0pF).

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION		16			Bits
ANALOG INPUT					
Input Impedance	Differential drive configuration[1]				
	G = 1.03, $IN1+_{ChX}$ to $IN1-_{ChX}$		1460		Ω
	G = 1.25, $IN1+_{ChX}$ to $IN1-_{ChX}$		1200		Ω
	G = 1.53, $IN1+_{ChX}$ to $IN1-_{ChX}$		980		Ω
	G = 2.03, $IN1+_{ChX}$ to $IN1-_{ChX}$		740		Ω
	G = 2.74, $IN2+_{ChX}$ to $IN2-_{ChX}$		548		Ω
	G = 4.11, $IN2+_{ChX}$ to $IN2-_{ChX}$		365		Ω
	G = 5.77, $IN1+_{ChX}$ to $IN1-_{ChX}$		260		Ω
Input Capacitance	$IN1+_{ChX}$ to $IN1-_{ChX}$		4		pF
	$IN2+_{ChX}$ to $IN2-_{ChX}$		8		pF
	$IN3+_{ChX}$ to $IN3-_{ChX}$		10		pF
	$SJ+_{ChX}$ to $SJ-_{ChX}$		13		pF
Differential Input Voltage Range (V_{IN})	V_{IN} = ±3V/Gain				
	G = 1.03		±2.91		V
	G = 2.03		±1.48		V
	G = 5.77		±0.52		V
FDA Input Common-Mode Voltage (V_{CM}) Functional Range	At FDA pins $SJ+_{ChX}$, $SJ-_{ChX}$	$-V_S$		$+V_S$ − 1.3	V
DC ACCURACY					
No Missing Codes		16			Bits
Differential Nonlinearity (DNL)			±0.15	±0.25	LSB
Integral Nonlinearity (INL)	C_{fb} = 0pF (full signal bandwidth)		±3	±6	ppm
	C_{fb} = 220pF (<1MHz signal bandwidth)		±3	±4.6	ppm
Transition Noise	Numerically derived from dynamic range				
	C_{fb} = 0pF		0.9		LSB RMS
	C_{fb} = 220pF		0.59		LSB RMS
Gain Error	T_A = 25°C		0.2		%FS
Gain Error Drift	T_A = −40°C to +85°C		10		ppm/°C
Zero Error	T_A = 25°C		−41		µV
Zero Error Drift	T_A = −40°C to +85°C		2.8		ppm/°C
DC Power Supply Rejection					
$+V_S$			−95		dB
$-V_S$			−97		dB
VDD33			−90		dB
$VDD11_{ChA}$, $VDD11_{ChB}$			−75		dB
Low Frequency Noise	Bandwidth = 0.1Hz to 10Hz		290		nV RMS
AC PERFORMANCE					
Dynamic Range	Shorted input test				
	C_{fb} = 0pF		88.3		dBFS
	C_{fb} = 220pF		91.9		dBFS
Noise Spectral Density (NSD)	Numerically derived from dynamic range, C_{fb} = 0pF				
	Logarithmic units		−155.3		dBFS/Hz
	Linear units		36.7		nV/√Hz

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Total RMS Noise	Numerically derived from dynamic range				
	C_{fb} = 0pF		82		µV RMS
	C_{fb} = 220pF		54.2		µV RMS
Signal-to-Noise Ratio (SNR)	C_{fb} = 220pF, input frequency (f_{IN}) = 1kHz, voltage magnitude (V_{MAG}) = −0.5dBFS				
	G = 1.03		92		dBFS
	G = 1.25		91.9		dBFS
	G = 1.53		91.9		dBFS
	G = 2.03		91.9		dBFS
	G = 2.74		91.8		dBFS
	G = 4.11		91.6		dBFS
	G = 5.77		91.4		dBFS
	G = 7.02		91.2		dBFS
	C_{fb} = 220pF, f_{IN} = 500kHz, V_{MAG} = −1dBFS, G = 1.03		91.1		dBFS
	C_{fb} = 0pF, f_{IN} = 1kHz, V_{MAG} = −0.5dBFS				
	G = 1.03	87.3	88.3		dBFS
	G = 2.03	87.0	87.9		dBFS
	G = 5.77	84.9	85.7		dBFS
	G = 7.02		85.1		dBFS
	C_{fb} = 0pF, f_{IN} = 500kHz, V_{MAG} = −1dBFS, G = 1.03		87.8		dBFS
	C_{fb} = 220pF, f_{IN} = 1kHz, Sinc5 + compensation filter, decimate by 8, V_{MAG} = −0.5dBFS, G = 1.03		97.0		dBFS
Total Harmonic Distortion (THD)	C_{fb} = 220pF, f_{IN} = 1kHz, V_{MAG} = −0.5dBFS				
	G = 1.03		−118		dBc
	G = 1.25		−120.2		dBc
	G = 1.53		−120		dBc
	G = 2.03		−120		dBc
	G = 2.74		−117.6		dBc
	G = 4.11		−114.8		dBc
	G = 5.77		−111.6		dBc
	G = 7.02		−111.5		dBc
	C_{fb} = 220pF, f_{IN} = 500kHz, V_{MAG} = −1dBFS, G = 1.03		−109		dBc
	C_{fb} = 0pF, f_{IN} = 1kHz, V_{MAG} = −0.5dBFS				
	G = 1.03		−112	−104.4	dBc
	G = 2.03		−114.1	−105.7	dBc
	G = 5.77		−111.2	−102	dBc
	G = 7.02		−111.8		dBc
	C_{fb} = 0pF, f_{IN} = 500kHz, V_{MAG} = −1dBFS, G = 1.03		−107.2		dBc
Signal-to-Noise and Distortion (SINAD)	C_{fb} = 220pF, f_{IN} = 1kHz, V_{MAG} = −0.5dBFS, G = 1.03		92		dBFS
	C_{fb} = 220pF, f_{IN} = 500kHz, V_{MAG} = −1dBFS, G = 1.03		91.1		dBFS
	C_{fb} = 0pF, f_{IN} = 1kHz, V_{MAG} = −0.5dBFS, G = 1.03		87.8		dBFS
	C_{fb} = 0pF, f_{IN} = 500kHz, V_{MAG} = −1dBFS, G = 1.03		87.8		dBFS
Spurious-Free Dynamic Range (SFDR)	C_{fb} = 220pF, f_{IN} = 1kHz, V_{MAG} = −0.5dBFS, G = 1.03		132.7		dBFS
	C_{fb} = 220pF, f_{IN} = 500kHz, V_{MAG} = −1dBFS, G = 1.03		105		dBFS
	C_{fb} = 0pF, f_{IN} = 1kHz, V_{MAG} = −0.5dBFS, G = 1.03		128.7		dBFS
	C_{fb} = 0pF, f_{IN} = 500kHz, V_{MAG} = −1dBFS, G = 1.03		103.8		dBFS
AC Power Supply Rejection					
$+V_S$	Ripple voltage = $1V_{p-p}$, f = 1kHz		112		dB
$-V_S$	Ripple voltage = $1V_{p-p}$, f = 1kHz		100		dB

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VDD33	Ripple voltage = 50mV$_{p-p}$, f = 1kHz		83		dB
VDD11$_{ChA}$, VDD11$_{ChB}$	Ripple voltage = 50mV$_{p-p}$, f = 1kHz		81		dB
IOVDD$_{ChA}$, IOVDD$_{ChB}$	Ripple voltage = 50mV$_{p-p}$, f = 1kHz		88		dB
VDDLDO	Ripple voltage = 50mV$_{p-p}$, f = 1kHz		89		dB
Channel-to-Channel Crosstalk	V_{IN} = 3V$_{p-p}$				
	f_{IN} = 10kHz		−131		dB
	f_{IN} = 700kHz		−96		dB
−3dB Small Signal Bandwidth	$V_{IN,dm}$ = 60mV$_{p-p}$, G = 1.03, C_{fb} = 0pF		40		MHz
Slew Rate	$V_{OUT,dm}$ = 4V step		500		V/µs
Settling Time to 16-Bits	$V_{OUT,dm}$ = 4V step		40		ns
CHANNEL-TO-CHANNEL MATCHING					
Phase Angle Mismatch	1kHz sine wave				
	G = 1.03		6		m°
	G = 2.03		5		m°
	G = 5.77		3		m°
VOCM$_{ChX}$ CHARACTERISTICS					
Input Voltage		1.5 − 0.05	1.5	1.5 + 0.05	V
Input Resistance			125		kΩ
Offset Voltage	Common-mode offset $V_{OS,cm,ChX}$ = $V_{OUT,cm,ChX}$ − VOCM$_{ChX}$ Positive Input (V_{IP}) = Negative Input (V_{IN}) = V_{OCM} = 0V				
	T_A = 25°C		±5	±50	mV
	T_A = −40°C to +85°C		±20	±55	mV
Input Bias Current	T_A = 25°C		−330		nA
Input Bias Current Drift	T_A = −40°C to +85°C		−1.5		nA/°C
FDA OUTPUT CLAMPS					
V_{CLAMP+} Clamping Voltage			V_{CLAMP+} + 0.5	V_{CLAMP+} + 0.6	V
V_{CLAMP-} Clamping Voltage		V_{CLAMP-} − 0.6	V_{CLAMP-} − 0.5		V
Recovery Time			100		ns
Input Resistance	Resistance between +V_{CLAMP} and −V_{CLAMP}		240		kΩ
DISABLE ($\overline{DISABLE_FDA}_{ChX}$ PIN) MODE					
Input Voltage	Disabled	−V_S − 0.3		GND + 1	V
	Enabled	GND + 1.4		+V_S + 0.3	V
Turn Off Time	Static full-scale FDA output falling to 10% amplitude after $\overline{DISABLE_FDA}_{ChX}$ assertion		20		µs
Turn On Time	Static full-scale FDA output reaching 90% amplitude after $\overline{DISABLE_FDA}_{ChX}$ deassertion		1.2		µs
$\overline{DISABLE_FDA}_{ChX}$ Pin Bias Current					
Enabled	$\overline{DISABLE_FDA}_{ChX}$ = 5V		110		nA
Disabled	$\overline{DISABLE_FDA}_{ChX}$ = 0V		−900		nA
REFERENCE INPUT (REFIN)					
Input Voltage (V_{REFIN})		2.995	3.0	3.005	V
Current Draw		−0.6		+2	µA/MSPS
	T_A = 25°C	−14		+14	µA
Leakage Current	Converters idle	−10		+10	µA
COMMON-MODE OUTPUT (CMO$_{ChX}$)					
Absolute Output Voltage	V_{REFIN} = 3.0V	1.47	V_{REFIN}/2	1.51	V
Noise	Bandwidth = 7.4MHz		71		µV RMS
Noise Spectral Density			26.1		nV/√Hz

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LOW DROPOUT REGULATORS ($VDD11_{ChX}$, $IOVDD_{ChX}$)					
Input Voltage Range		1.4		2.7	V
Output Voltage	T_A = 25°C, VDDLDO = 1.8V		1.1		V
Start-Up Time			10		µs
LOW VOLTAGE DIFFERENTIAL SIGNALING (LVDS) INPUT AND OUTPUT (EIA-644)					
Data Format	Serial LVDS data output	Twos complement			
LVDS Inputs (CLK_{ChX}± and CNV_{ChX}±)	$IOVDD_{ChX}$ supply domain inputs.				
Common-Mode Input Voltage (V_{ICM})	Default setting	700		1400	mV
Differential Input Voltage (V_{IDIFF})	Default setting	100		600	mV
LVDS Outputs (DCO_{ChX}±, DA_{ChX}±, and DB_{ChX}±)	$IOVDD_{ChX}$ supply domain outputs, differential termination, load resistance (R_L) = 100 Ω				
Common-Mode Output Voltage (V_{OCM})	LVDS_VOD = 001b	910	928	940	mV
	LVDS_VOD = 010b (default)	832	851	867	mV
	LVDS_VOD = 100b	687	706	722	mV
Differential Output Voltage (V_{ODIFF})	LVDS_VOD = 001b	353	395	445	mV
	LVDS_VOD = 010b (default)	471	530	594	mV
	LVDS_VOD = 100b	700	785	880	mV
DIGITAL INPUTS (CNV_{ChX}, $\overline{CS}_{ChX}$, $SCLK_{ChX}$, and SDI_{ChX})	$VDD11_{ChX}$ supply domain inputs				
Input Voltage Tolerance		0		2.5	V
Logic Levels					
Input Low Voltage (V_{IL})		0		0.36 × $VDD11_{ChX}$	V
Input High Voltage (V_{IH})		0.92		2.5	V
DIGITAL INPUTS ($GPIOx_{ChX}$, $\overline{DCS}_{ChX}$, and $DCLK_{ChX}$)	$IOVDD_{ChX}$ supply domain inputs				
Input Voltage Tolerance		0		1.26	V
Logic Levels					
V_{IL}		0		0.36 × $IOVDD_{ChX}$	V
V_{IH}		0.92		$IOVDD_{ChX}$	V
Input Current					
Input Low Current (I_{IL})		−1		+1	µA
Input High Current (I_{IH})		−1		+1	µA
Input Pin Capacitance			4.5		pF
DIGITAL OUTPUTS ($GPIOx_{ChX}$)	$IOVDD_{ChX}$ supply domain outputs				
Logic Levels					
Output Low Voltage (V_{OL})	Sink current (I_{SINK}) = 500µA	0		0.15	V
Output High Voltage (V_{OH})	Source current (I_{SOURCE}) = 500µA	$IOVDD_{ChX}$ − 0.115		$IOVDD_{ChX}$	V
DIGITAL OUTPUTS ($SDOx_{ChX}$)	$IOVDD_{ChX}$ supply domain outputs.				
Data Format	Configured as serial data output	Twos complement			
Logic Levels					
V_{OL}	I_{SINK} = 500µA			0.15	V
V_{OH}	I_{SOURCE} = 500µA	$IOVDD_{ChX}$ − 0.115		$IOVDD_{ChX}$	V
POWER SUPPLIES					
±V_S		3	+V_S = 5V −V_S = −1V	10	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VDD33		3.135	3.30	3.465	V
VDDLDO		1.4		2.7	V
$VDD11_{ChX}$	Applied externally, LDO disabled	1.045	1.10	1.155	V
$IOVDD_{ChX}$	Applied externally, LDO disabled	1.045	1.10	1.26	V
Operating Current	LVDS_CNV_EN = 0				
Static	Converters and interfaces idle, FIFO disabled				
$\pm V_S$	$+V_S - -V_S$ = 10V		8.2	9.88	mA
VDD33			11.6	15.2	mA
VDDLDO	Both $VDD11_{ChX}$ LDO disabled		0.01	0.045	mA
$VDD11_{ChX}$	Combined draw of both rails		34	46.5	mA
$IOVDD_{ChX}$	Combined draw of both rails		10.9	12.5	mA
VDDLDO	Both $VDD11_{ChX}$ LDO enabled		47.5	60.4	mA
Dynamic	DC input signal				
$\pm V_S$	$+V_S - -V_S$ = 10V		10	11.4	mA
VDD33			17	22	mA
VDDLDO	Both $VDD11_{ChX}$ LDO disabled		0.01	0.049	mA
$VDD11_{ChX}$	Combined draw of both rails		37	52	mA
$IOVDD_{ChX}$	Combined draw of both rails		16.9	19.1	mA
VDDLDO	Both $VDD11_{ChX}$ LDO enabled		63.4	77.5	mA
Dynamic	−0.5dBFS sine wave input signal				
$\pm V_S$	$+V_S - -V_S$ = 10V		10.4	11.8	mA
VDD33			17	22	mA
VDDLDO	$VDD11_{ChX}$ LDO disabled		0.01	0.049	mA
$VDD11_{ChX}$	Combined draw of both rails		37	52	mA
$IOVDD_{ChX}$	Combined draw of both rails		16.9	19.3	mA
VDDLDO	Both $VDD11_{ChX}$ LDO enabled		62.8	77	mA
Standby Mode					
$\pm V_S$	$\overline{DISABLE_FDA}_{ChA}$ = 0V, $\overline{DISABLE_FDA}_{ChB}$ = 0V, $+V_S - -V_S$ = 10V		0.07	0.4	mA
VDD33			3	3.8	mA
VDDLDO	Both $VDD11_{ChX}$ LDO disabled		0.01	0.045	mA
$VDD11_{ChX}$	Combined draw of both rails		3.2	9	mA
$IOVDD_{ChX}$	Combined draw of both rails		0.14	0.7	mA
VDDLDO	Both $VDD11_{ChX}$ LDO enabled		4.2	12.1	mA
Sleep Mode					
$\pm V_S$	$\overline{DISABLE_FDA}_{ChA}$ = 0V, $\overline{DISABLE_FDA}_{ChB}$ = 0V, $+V_S - -V_S$ = 10V		0.07	0.4	mA
VDD33			1.42	1.88	mA
VDDLDO	Both $VDD11_{ChX}$ LDO disabled		0.01	0.045	mA
$VDD11_{ChX}$	Combined draw of both rails		2.5	9	mA
$IOVDD_{ChX}$	Combined draw of both rails		0.12	0.69	mA
VDDLDO	Both $VDD11_{ChX}$ LDO enabled		3.5	11.2	mA
Power Dissipation Per Channel	Both $VDD11_{ChX}$ LDO disabled $+V_S$ = 5V, $-V_S$ = −1V For typ values: VDD33 = 3.3V, $VDD11_{ChX}$ = 1.1V, $IOVDD_{ChX}$ = 1.1V For max values: VDD33 = 3.456V, $VDD11_{ChX}$ = 1.155V, $IOVDD_{ChX}$ = 1.26V				
Static	Converters and interfaces idle, FIFO disabled		68.4	87.2	mW
Dynamic	DC input signal		87.7	109.6	mW

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Dynamic	−0.5dBFS sine wave input signal		88.9	110.9	mW
Standby Mode	$\overline{DISABLE_FDA}_{ChX}$ = 0V		7	12.8	mW
Sleep Mode	$\overline{DISABLE_FDA}_{ChX}$ = 0V		4.0	9.6	mW
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+85	°C

[1] For more details and for impedance under single-ended driving condition, see the Analog Inputs Drive and Gain section.

SPECIFICATIONS

TIMING SPECIFICATIONS

VDD33 = 3.3V ± 5%, VDDLDO = 1.5V to 2.7V, $VDD11_{ChX}$ = 1.1V ± 5%, $IOVDD_{ChX}$ = 1.1V − 5% to 1.2V + 5%, V_{REFIN} = 3.0V, f_S = 10MHz, and T_A = T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2. Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Sampling Frequency	f_S	1.25[1]		10	MHz
Conversion Time	t_{CONV}	100		800	ns
Acquisition Phase	t_{ACQ}	t_{CYC}			ns
Conversion Cycle Period	t_{CYC}	t_{CONV}			ns
LVDS Data Interface					
Data Interface Clock Count	N			8	
Active Data Lane Count	L			2	
$CNV\pm_{ChX}$ High Time	t_{CNVH}	t_{CLK}	4 × t_{CLK}	t_{CYC} − t_{CNVL}	ns
$CNV\pm_{ChX}$ Low Time	t_{CNVL}	t_{CLK}	4 × t_{CLK}	t_{CYC} − t_{CNVH}	ns
$CNV\pm_{ChX}$ Edge to CLK± Rising Edge Alignment	t_{CCA}			535	ps
$CNV\pm_{ChX}$ to $Dx\pm_{ChX}$ (MSB) Ready	t_{MSB}				
Gain Error Correction Enabled			20.5	22.4	ns
Gain Error Correction Disabled			15.7	18	ns
$CLK\pm_{ChX}$ Period	t_{CLK}	12.5		t_{CYC} × L/N	ns
$CLK\pm_{ChX}$ Frequency	f_{CLK}		1/t_{CLK}	80	MHz
$CLK\pm_{ChX}$ to $Dx\pm_{ChX}$ Delay	t_{CLKD}	1		2.1	ns
$CLK\pm_{ChX}$ to $DCO\pm_{ChX}$ Delay (Echo Clock Mode)	t_{DCO}	1		2	ns
$DCO\pm_{ChX}$ to $Dx\pm_{ChX}$ Delay (Echo Clock Mode)	t_{DCOD}	0.02		0.55	ns
SPI Data Interface					
Data Interface Clock Count, Single Conversion Result	M			24	
Active Data Lane Count	C		1	4	
Data Interface Chip-Select Falling Edge ($\overline{DCS}_{ChX}$) to $SDOB_{ChX}$ Data Valid	t_{DEN}	5	6		ns
Data Interface Clock Period ($DCLK_{ChX}$)	t_{DCK}	20			ns
Data Interface Clock Low-Pulse Width ($DCLK_{ChX}$)	t_{DCKL}	t_{DCK} × 0.45			ns
Data Interface Clock High-Pulse Width ($DCLK_{ChX}$)	t_{DCLKH}	t_{DCK} × 0.45			ns
Data Interface Clock Falling Edge to Data Remains Valid Delay	t_{DHSDO}	5			ns
Data Interface Clock Falling Edge to Data Valid Delay	t_{DDSDO}			9.6	ns
$DCLK_{ChX}$ Rising to Data Interface Chip Select Falling	t_{DCKEN}	0			ns
Data Interface Chip-Select High to DCLK Disabled	$t_{DCLKDIS}$	0			ns
Data Interface Chip-Select High Between Frames	t_{DCSMIN}		(t_{DCKEN} + $t_{DCLKDIS}$) + 0.5 × t_{DCLK}		ns
Serial Configuration Interface					
$SCLK_{ChX}$ Period	t_{SCK}	20			ns
$SCLK_{ChX}$ Low-Pulse Width	t_{SCKL}	t_{SCK} × 0.45			ns
$SCLK_{ChX}$ High-Pulse Width	t_{SCKH}	t_{SCK} × 0.45			ns
$SCLK_{ChX}$ Falling Edge to Data Remains Valid Delay	t_{HSDO}	0.7			ns
$SCLK_{ChX}$ Falling Edge to Data Valid Delay	t_{DSDO}			14.5	ns
$\overline{CS}_{ChX}$ Falling Edge to $SCLK_{ChX}$	t_{CSSCK}	0			ns
Last SCLK to $\overline{CS}_{ChX}$ Rising	t_{SCKCS}	0			ns
SDI_{ChX} Valid Setup Time Before $SCLK_{ChX}$ Rising Edge	t_{SSDI}	1			ns
SDI Valid Hold Time After SCLK Rising Edge	t_{HSDI}	0			ns
SCLK Rising to Data Interface Chip-Select Falling	t_{SCKEN}	0			ns
Data Interface Chip-Select High to $SCLK_{ChX}$ Disabled	t_{SCKDIS}	0			ns
Data Interface Chip-Select High to SDO_{ChX} Disabled	t_{CSDIS}			10.3	ns
Data Interface Chip-Select High Between Frames	t_{CSMIN}		(t_{SCKEN} + t_{SCKDIS}) + 0.5 × t_{SCK}		ns

SPECIFICATIONS

Table 2. Timing Specifications (Continued)

Parameter	Symbol	Min	Typ	Max	Unit
Digital Filter					
$\overline{FILT_SYNC}_{ChX}$ Rising Edge to CNV Rising Edge	$t_{SYNC\ MAX}$		t_{CYC} − 5		ns
CNV Rising Edge to $\overline{FILT_SYNC}_{ChX}$ Falling Edge	$t_{SYNC\ MIN}$		3		ns
Event Detection					
Input Threshold Crossed to $\overline{ALERT}$ Asserted	t_{EVT}	2 × t_{CYC}		3 × t_{CYC}	ns

[1] The requirement for a minimum sampling frequency has the implication that the first two samples acquired after power up or after a sleep or standby period are not guaranteed to be correct, and therefore must be discarded.

ABSOLUTE MAXIMUM RATINGS

Table 3. Absolute Maximum Ratings

Parameter	Rating
Analog Inputs	
$SJ+_{ChA}$ to $SJ-_{ChA}$, $SJ+_{ChB}$ to $SJ-_{ChB}$	±1V
$IN3+_{ChA}$ to $IN3-_{ChA}$, $IN3+_{ChB}$ to $IN3-_{ChB}$	±2V
$IN2+_{ChA}$ to $IN2-_{ChA}$, $IN2+_{ChB}$ to $IN2-_{ChB}$	±4V
$IN1+_{ChA}$ to $IN1-_{ChA}$, $IN1+_{ChB}$ to $IN1-_{ChB}$	±7V
V_{OCM_ChX} to GND	$-V_S$ to $+V_S$ + 0.3V
$OUT+_{ChX}$, $OUT-_{ChX}$[1] to GND	−0.3V to +3.6V
Supply Voltage	
$+V_S$ to $-V_S$	11V
REFIN, VDD33 to GND	−0.3V to +3.6V
VDDLDO to GND	−0.3V to +2.75V
$VDD11_{ChX}$ to GND	−0.3V to +1.26V
$IOVDD_{ChX}$ to GND	−0.3V to +1.26V
Digital Inputs and Outputs	
Inputs ($CNV\pm_{ChX}$, $CLK\pm_{ChX}$) to GND	−0.3V to +2.75V
LVDS OUTPUT ($DCO\pm_{ChX}$, $DA\pm_{ChX}$, $DB\pm_{ChX}$) to GND	−0.3V to +1.26V
$\overline{CS}_{ChX}$, $SCLK_{ChX}$, SDI_{ChX} to GND	−0.3V to +2.75V
$GPIOn_{ChX}$ to GND	−0.3V to +1.26V
$\overline{DISABLE_FDA}_{ChXA}$ to GND	$-V_S$ − 0.3V to $+V_S$ + 0.3V
$SDOA_{ChX}$, $SDOB_{ChX}$, $SDOC_{ChX}$, $SDOD_{ChX}$ to GND	−0.3V to 1.26V
Temperature	
Storage Range	−55°C to +150°C
Operating Range	−40°C to +85°C
Maximum T_J	105°C
Maximum Reflow (Package) as per JEDEC J-STD-020	260°C

[1] The FDA output pins $OUT+_{ChX}$ and $OUT-_{ChX}$ have the consideration of analog inputs since they drive the inputs of the ADC. The voltage into these nodes is indirectly driven by the user via the FDA, which means that respecting this Absolute Maximum Rating involves limiting the differential input voltage to the FDA, taking into account the configured FDA gain.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction-to-case thermal resistance. θ_{JB} is the junction-to-board thermal resistance. Ψ_{JT} is the junction-to-top thermal characterization.

Thermal resistance values specified in Table 4 are simulated based on JEDEC specs (unless specified otherwise) and must be used in compliance with JESD51-12.

Table 4. Thermal Resistance[1]

Package Type	θ_{JA}	θ_{JC}	θ_{JB}	Ψ_{JT}	Unit
BC-196-20	37.3	23	23	3.6	°C/W

[1] Thermal resistance values are based on simulation of a 2S2P JEDEC PCB with vias, except for θ_{JC}, which is based on a 1S0P JEDEC PCB simulation.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged-device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the AD4885

Table 5. AD4885, 196-Ball CSP_BGA

ESD Model	Withstand Threshold (V)	Class
HBM	±1000	1C
FICDM	±500	C2a

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

TOP VIEW
(Not to Scale)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	IN2+$_{ChB}$	IN2+$_{ChB}$	IN1+$_{ChB}$	IN1−$_{ChB}$	IN2−$_{ChB}$	IN2−$_{ChB}$	GND	IN2+$_{ChA}$	IN2+$_{ChA}$	IN1+$_{ChA}$	IN1−$_{ChA}$	IN2−$_{ChA}$	IN2−$_{ChA}$	GND
B	IN3+$_{ChB}$	IN3+$_{ChB}$	SJ+$_{ChB}$	SJ−$_{ChB}$	IN3−$_{ChB}$	IN3−$_{ChB}$	−VS	IN3+$_{ChA}$	IN3+$_{ChA}$	SJ+$_{ChA}$	SJ−$_{ChA}$	IN3−$_{ChA}$	IN3−$_{ChA}$	−VS
C	−VS	−VS	−VS	−VS	−VS	−VS	−VS	−VS	−VS	−VS	−VS	−VS	−VS	−VS
D	+VS	+VS	+VS	+VS	+VS	+VS	+VS	+VS	+VS	+VS	+VS	+VS	+VS	+VS
E	+V_{CLAMP}	OUT−$_{ChB}$	OUT−$_{ChB}$	OUT+$_{ChB}$	OUT+$_{ChB}$	+VS	−V_{CLAMP}	+V_{CLAMP}	OUT−$_{ChA}$	OUT−$_{ChA}$	OUT+$_{ChA}$	OUT+$_{ChA}$	+VS	−V_{CLAMP}
F	V_{OCM_ChB}	CMO$_{ChB}$	DNC	DNC	GND	$\overline{DISABLE_FDA}_{ChB}$	GND	V_{OCM_ChA}	CMO$_{ChA}$	DNC	DNC	GND	$\overline{DISABLE_FDA}_{ChA}$	GND
G	GND	GND	GND	REFGND	REFGND	REFGND	VDD11$_{ChB}$	GND	GND	GND	REFGND	REFGND	REFGND	VDD11$_{ChA}$
H	GND	VDD33	VDD33	REFGND	REFGND	VDDLDO	VDD11$_{ChB}$	GND	VDD33	VDD33	REFGND	REFGND	VDDLDO	VDD11$_{ChA}$
J	REFGND	REFGND	GND	GND	GND	GND	VDD11$_{ChB}$	REFGND	REFGND	GND	GND	GND	GND	VDD11$_{ChA}$
K	REFGND	REFGND	GND	GND	GND	IOGND	IOVDD$_{ChB}$	REFGND	REFGND	GND	GND	GND	IOGND	IOVDD$_{ChA}$
L	GND	REFIN	GND	GND	GND	CNV−$_{ChB}$	CNV+$_{ChB}$	GND	REFIN	GND	GND	GND	CNV−$_{ChA}$	CNV+$_{ChA}$
M	GND	REFIN	GND	GND	GND	CLK+$_{ChB}$/ DCLK$_{ChB}$	CLK−$_{ChB}$/ $\overline{DCS}_{ChB}$	GND	REFIN	GND	GND	GND	CLK+$_{ChA}$/ DCLK$_{ChA}$	CLK−$_{ChA}$/ $\overline{DCS}_{ChA}$
N	GPIO0$_{ChB}$	GPIO1$_{ChB}$	GPIO2$_{ChB}$	GPIO3$_{ChB}$	DCO−$_{ChB}$	DB+$_{ChB}$/ SDOC$_{ChB}$	DB−$_{ChB}$/ SDOD$_{ChB}$	GPIO0$_{ChA}$	GPIO1$_{ChA}$	GPIO2$_{ChA}$	GPIO3$_{ChA}$	DCO−$_{ChA}$	DB+$_{ChA}$/ SDOC$_{ChA}$	DB−$_{ChA}$/ SDOD$_{ChA}$
P	DNC	SCLK$_{ChB}$	SDI$_{ChB}$	$\overline{CS}_{ChB}$	DCO+$_{ChB}$	DA+$_{ChB}$/ SDOA$_{ChB}$	DA−$_{ChB}$/ SDOB$_{ChB}$	DNC	SCLK$_{ChA}$	SDI$_{ChA}$	$\overline{CS}_{ChA}$	DCO+$_{ChA}$	DA+$_{ChA}$/ SDOA$_{ChA}$	DA−$_{ChA}$/ SDOB$_{ChA}$

GROUND PINS
ANALOG INPUT PINS
ANALOG OUTPUT PINS
DIGITAL I/O PINS
POWER SUPPLY PINS
DO NOT CONNECT

003

Figure 3. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic	Type[1]	Description
A1, A2	IN2+$_{ChB}$	AI	Channel B Positive Analog Input 2.
A3	IN1+$_{ChB}$	AI	Channel B Positive Analog Input 1.
A4	IN1−$_{ChB}$	AI	Channel B Negative Analog Input 1.
A5, A6	IN2−$_{ChB}$	AI	Channel B Negative Analog Input 2.
A7, A14, F5, F7, F12, F14, G1 to G3, G8 to G10, H1, H8, J3 to J6, J10 to J13, K3 to K5, K10 to K12, L1, L3 to L5, L8, L10 to L12, M1, M3 to M5, M8, M10 to M12	GND	P	Grounds. All ground pins must be connected to a PCB GND plane.
A8, A9	IN2+$_{ChA}$	AI	Channel A Positive Analog Input 2.
A10	IN1+$_{ChA}$	AI	Channel A Positive Analog Input 1.
A11	IN1−$_{ChA}$	AI	Channel A Negative Analog Input 1.
A12, A13	IN2−$_{ChA}$	AI	Channel A Negative Analog Input 2.
B1, B2	IN3+$_{ChB}$	AI	Channel B Positive Analog Input 3.
B3	SJ+$_{ChB}$	AI	Channel B FDA Summing Junction Positive Node. Sensitive pin, see the Layout Guidelines section.
B4	SJ−$_{ChB}$	AI	Channel B FDA Summing Junction Negative Node. Sensitive pin, see the Layout Guidelines section.
B5, B6	IN3−$_{ChB}$	AI	Channel B Negative Analog Input 3.
B7, B14, C1 to C14	−V_S	P	FDA Negative Supply Rail. These supply pins are internally decoupled by two 220nF capacitors to GND. These pins must be shorted externally.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Type[1]	Description
B8, B9	$IN3+_{ChA}$	AI	Channel A Positive Analog Input 3.
B10	$SJ+_{ChA}$	AI	Channel A FDA Summing Junction Positive Node. Sensitive pin, see the Layout Guidelines section.
B11	$SJ-_{ChA}$	AI	Channel A FDA Summing Junction Negative Node. Sensitive pin, see the Layout Guidelines section.
B12, B13	$IN3-_{ChA}$	AI	Channel A Negative Analog Input 3.
D1 to D14, E6, E13	$+V_S$	P	FDA Positive Supply Rail. These supply pins are internally decoupled by two 220nF capacitors to GND. These pins must be shorted externally.
E1, E8	$+V_{CLAMP}$	AI	FDA Output Positive Clamp. These pins must be shorted externally and connected to the reference input pin REFIN.
E2, E3	$OUT-_{ChB}$	AO	Channel B FDA Negative Output.
E4, E5	$OUT+_{ChB}$	AO	Channel B FDA Positive Output.
E7, E14	$-V_{CLAMP}$	AI	FDA Output Negative Clamp. These pins must be shorted externally and connected to ground.
E9, E10	$OUT-_{ChA}$	AO	Channel A FDA Negative Output.
E11, E12	$OUT+_{ChA}$	AO	Channel A FDA Positive Output.
F1	V_{OCM_ChB}	AI	Channel B FDA Output Common-Mode Voltage.
F2	CMO_{ChB}	AO	Channel B ADC Common-Mode Voltage Output.
F3, F4, F10, F11, P1, P8	DNC	DNC	Do Not Connect. Do not connect to these pins.
F6	$\overline{DISABLE_FDA}_{ChB}$	DI	Channel B FDA Disable Pin. Contains internal pull-up network, can be left floating for normal operation.
F8	V_{OCM_ChA}	AI	Channel A FDA Output Common-Mode Voltage.
F9	CMO_{ChA}	AO	Channel A ADC Common-Mode Voltage Output.
F13	$\overline{DISABLE_FDA}_{ChA}$	DI	Channel A FDA Disable Pin. Contains internal pull-up network, can be left floating for normal operation.
G4 to G6, G11 to G13, H4, H5, H11, H12, J1, J2, J8, J9, K1, K2, K8, K9	REFGND	P	Reference Grounds. Connect any external reference decoupling capacitors across REFIN and REFGND. All REFGND pins must be connected with a low impedance path to GND.
G7, H7, J7	$VDD11_{ChB}$	P	Channel B ADC 1.1V Core Supplies. These supply pins are internally decoupled by four 470nF capacitors to GND. When power is supplied to VDDLDO (H6, H13), an internal LDO voltage regulator produces the 1.1V required at these pins. The voltage regulator is automatically powered on when VDDLDO is driven with a voltage between 1.4V and 2.7V. If VDDLDO is left disconnected, the required 1.1V must be supplied to these pins from an external source.
G14, H14, J14	$VDD11_{ChA}$	P	Channel A ADC 1.1V Core Supplies. These supply pins are internally decoupled by four 470nF capacitors to GND. When power is supplied to VDDLDO (H6, H13), an internal LDO voltage regulator produces the 1.1V required at these pins. The voltage regulator is automatically powered on when VDDLDO is driven with a voltage between 1.4V and 2.7V. If VDDLDO is left disconnected, the required 1.1V must be supplied to these pins from an external source.
H2, H3, H9, H10	VDD33	P	3.3V Supply Rail Inputs for ADCs. These supply pins are internally decoupled by two 470nF capacitors to GND. These pins must be shorted externally.
H6, H13	VDDLDO	P	LDO Supply Rail Input. This supply rail is internally decoupled by two 220nF capacitors to GND. Four internal, 1.1V, LDO voltage regulators (two per ADC) can be supplied from a source connected to this input in the 1.4V to 2.7V range. If this pin is left open, all four internal regulators automatically power off and $VDD11_{ChA}$, $VDD11_{ChB}$, $IOVDD_{ChA}$, and $IOVDD_{ChB}$ must be connected with an external voltage source within their allowed specification limits. If VDDLDO is connected to a voltage source, $VDD11_{ChA}$, $VDD11_{ChB}$, $IOVDD_{ChA}$, and $IOVDD_{ChB}$ must not be connected to any external voltage source. These pins must be shorted externally.
K6, K13	IOGND	P	Digital Interface Supply Ground Reference. These pins must be connected to the same ground plane as all other GND pins. All pins specified as type DI, DO, or DI/O must use this ground reference.
K7	$IOVDD_{ChB}$	P	Channel B ADC 1.1V Digital Interface Supply Rail. This supply is internally decoupled by a 220nF capacitor to IOGND.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Type[1]	Description
			When power is supplied to VDDLDO (H6, H13), an internal LDO voltage regulator produces the 1.1V required at this pin. The voltage regulator is automatically powered on when VDDLDO is driven with a voltage between 1.4V and 2.7V. If VDDLDO is left disconnected, the required 1.1V must be supplied to this pin from an external source (typically the host controller interface supply).
K14	$IOVDD_{ChA}$	P	Channel A ADC 1.1V Digital Interface Supply Rail. This supply is internally decoupled by a 220nF capacitor to IOGND. When power is supplied to VDDLDO (H6, H13), an internal LDO voltage regulator produces the 1.1V required at this pin. The voltage regulator is automatically powered on when VDDLDO is driven with a voltage between 1.4V and 2.7V. If VDDLDO is left disconnected, the required 1.1V must be supplied to this pin from an external source (typically the host controller interface supply).
L2, L9, M2, M9	REFIN	AI	3.0V Reference Voltage Input for ADCs. These pins must be shorted externally.
L6, L7	$CNV-_{ChB}$, $CNV+_{ChB}$	DI	Channel B ADC Convert Start Inputs. This pin pair serves as the conversion control input, a conversion is initiated on the rising edge of the convert signal. These inputs are by default configured in complementary metal-oxide semiconductor (CMOS) mode, in which $CNV-_{ChB}$ must be connected to IOGND and the convert signal is applied to $CNV+_{ChB}$. In the LVDS data interface mode, the convert start input can be optionally configured in LVDS mode, in which case, the convert signal is applied differentially to $CNV+_{ChB}$ and $CNV-_{ChB}$ and an external 100Ω termination resistor must be placed across these pins. For more details, see the ADC Conversion Control section.
L13, L14	$CNV-_{ChA}$, $CNV+_{ChA}$	DI	Channel A ADC Convert Start Inputs. This pin pair serves as the conversion control input, a conversion is initiated on the rising edge of the convert signal. These inputs are by default configured in CMOS mode, in which $CNV-_{ChA}$ must be connected to IOGND and the convert signal is applied to $CNV+_{ChA}$. In the LVDS data interface mode, the convert start input can be optionally configured in LVDS mode, in which case, the convert signal is applied differentially to $CNV+_{ChA}$ and $CNV-_{ChA}$ and an external 100Ω termination resistor must be placed across these pins. For more details, see the ADC Conversion Control section.
M6	$CLK+_{ChB}/DCLK_{ChB}$	DI	Channel B ADC Data Interface Clock Multifunction Pin. In LVDS data interface mode (default), this pin serves as half of the differential data clock input, and an external 100Ω termination resistor must be present between it and the $CLK-_{ChB}$ pin. In SPI data interface mode, the single-ended data clock signal must be applied to this pin.
M7	$CLK-_{ChB}/\overline{DCS}_{ChB}$	DI	Channel B ADC Data Interface Clock Input ($CLK-_{ChB}$)/Data Interface Chip-Select ($\overline{DCS}_{ChB}$) Multifunction Pin. In LVDS data interface mode (default), this pin serves as half of the differential data clock input, and an external 100Ω termination resistor must be present between it and the $CLK+_{ChB}$ pin. In SPI data interface mode, this pin functions as a chip-select input (data interface chip-select).
M13	$CLK+_{ChA}/DCLK_{ChA}$	DI	Channel A ADC Data Interface Clock Multifunction Pin. In LVDS data interface mode (default), this pin serves as half of the differential data clock input, and an external 100Ω termination resistor must be present between it and the $CLK-_{ChA}$ pin. In SPI data interface mode, the single-ended data clock signal must be applied to this pin.
M14	$CLK-_{ChA}/\overline{DCS}_{ChA}$	DI	Channel A ADC Data Interface Clock Input ($CLK-_{ChA}$)/Data Interface Chip-Select ($\overline{DCS}_{ChA}$) Multifunction Pin. In LVDS data interface mode (default), this pin serves as half of the differential data clock input, and an external 100Ω termination resistor must be present between it and the $CLK+_{ChA}$ pin. In SPI data interface mode, this pin functions as a chip-select input (data interface chip-select).
N1	$GPIO0_{ChB}$	DI/O	Channel B ADC General-Purpose Input and Output 0 Pin. By default, this pin is enabled as an output and functioning as Channel B Configuration SPI SDO.
N2	$GPIO1_{ChB}$	DI/O	Channel B ADC General-Purpose Input and Output 1 Pin.
N3	$GPIO2_{ChB}$	DI/O	Channel B ADC General-Purpose Input and Output 2 Pin.
N4	$GPIO3_{ChB}$	DI/O	Channel B ADC General-Purpose Input and Output 3 Pin.
N5	$DCO-_{ChB}$	DO	Channel B ADC LVDS Echo Clock Negative Output. This output pin, along with $DCO+_{ChB}$, outputs a buffered and delayed version of $CLK+_{ChB}$ and $CLK-_{ChB}$. Data outputs from LVDS Data Lanes ($DA\pm_{ChB}$ and $DB\pm_{ChB}$, if active) are clocked out in alignment with

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Type[1]	Description
			both rising and falling edges of $DCO+_{ChB}$ and $DCO-_{ChB}$. If the echo clock mode is disabled, these pins can be left unconnected.
N6	$DB+_{ChB}/SDOC_{ChB}$	DO	Channel B ADC Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with $DB-_{ChB}$ serves as the optional, secondary LVDS Data Lane B for the ADC. If unused, leave unconnected. When the ADC is in SPI data interface mode, this pin functions as Serial Data Output C ($SDOC_{ChB}$), which is active in a 4-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock ($DCLK_{ChB}$). This pin must be left unconnected if not being used.
N7	$DB-_{ChB}/SDOD_{ChB}$	DO	Channel B ADC Data Interface Output Multifunction Pin. When the ADC is in LVDS data interface mode (default), this output pin along with $DB+_{ChB}$ serves as the optional, secondary LVDS Data Lane B. If unused, leave unconnected. When the ADC is in SPI data interface mode, this pin functions as Serial Data Output D ($SDOD_{ChB}$), which is active in a 4-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock ($DCLK_{ChB}$). Note that this pin does not go into a high impedance state when used in 4-lane SPI mode when $\overline{DCS}_{ChB}$ is high. This pin must be left unconnected if not being used.
N8	$GPIO0_{ChA}$	DI/O	Channel A ADC General-Purpose Input and Output 0 Pin. By default, this pin is enabled as an output and functioning as Channel A Configuration SPI SDO.
N9	$GPIO1_{ChA}$	DI/O	Channel A ADC General-Purpose Input and Output 1 Pin.
N10	$GPIO2_{ChA}$	DI/O	Channel A ADC General-Purpose Input and Output 2 Pin.
N11	$GPIO3_{ChA}$	DI/O	Channel A ADC General-Purpose Input and Output 3 Pin.
N12	$DCO-_{ChA}$	DO	Channel A ADC LVDS Echo Clock Negative Output. This pin, along with $DCO+_{ChA}$, outputs a buffered and delayed version of $CLK+_{ChA}$ and $CLK-_{ChA}$. Data outputs from LVDS Data Lanes ($DA\pm_{ChA}$ and $DB\pm_{ChA}$, if active) are clocked out in alignment with both rising and falling edges of $DCO+_{ChA}$ and $DCO-_{ChA}$. If the echo clock mode is disabled, these pins can be left unconnected.
N13	$DB+_{ChA}/SDOC_{ChA}$	DO	Channel A ADC Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with $DB-_{ChA}$ serves as the optional, secondary LVDS Data Lane B for the ADC. If unused, leave unconnected. When the ADC is in SPI data interface mode, this pin functions as Serial Data Output C ($SDOC_{ChA}$), which is active in a 4-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock ($DCLK_{ChA}$). This pin must be left unconnected if not being used.
N14	$DB-_{ChA}/SDOD_{ChA}$	DO	Channel A ADC Data Interface Output Multifunction Pin. When the ADC is in LVDS data interface mode (default), this output pin along with $DB+_{ChA}$ serves as the optional, secondary LVDS Data Lane B. If unused, leave unconnected. When the ADC is in SPI data interface mode, this pin functions as Serial Data Output D ($SDOD_{ChA}$), which is active in a 4-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock ($DCLK_{ChA}$). Note that this pin does not go into a high impedance state when used in 4-lane SPI mode when $\overline{DCS}_{ChA}$ is high. This pin must be left unconnected if not being used.
P2	$SCLK_{ChB}$	DI	Channel B ADC Configuration Interface Serial Data Clock. This clock input is used to shift data into and out of the device configuration memory.
P3	SDI_{ChB}	DI	Channel B ADC Configuration Interface Serial Data Input. Data is shifted into this input on the rising edge of the serial data clock, $SCLK_{ChB}$.
P4	$\overline{CS}_{ChB}$	DI	Channel B ADC Configuration Interface Chip-Select Input (Active Low). The $\overline{CS}_{ChB}$ input frames serial data transfers over the Configuration SPI.
P5	$DCO+_{ChB}$	DO	Channel B ADC LVDS Echo Clock Positive Output. This output pin, along with $DCO-_{ChB}$, outputs a buffered and delayed version of $CLK+_{ChB}$ and $CLK-_{ChB}$. Data outputs from LVDS Data Lanes ($DA\pm_{ChB}$ and $DB\pm_{ChB}$, if active) are clocked out in alignment with both rising and falling edges of $DCO+_{ChB}$ and $DCO-_{ChB}$. If the echo clock mode is disabled, these pins can be left unconnected.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin Number	Mnemonic	Type[1]	Description
P6	$DA+_{ChB}/SDOA_{ChB}$	DO	Channel B ADC Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with $DA-_{ChB}$ serves as the primary LVDS Data Lane A. In SPI data interface mode, this pin functions as Serial Data Output A ($SDOA_{ChB}$), which is active in a 4-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock ($DCLK_{ChB}$). This pin must be left unconnected if not being used.
P7	$DA-_{ChB}/SDOB_{ChB}$	DO	Channel B ADC Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with $DA+_{ChB}$ serves as the primary LVDS Data Lane A. In SPI data interface mode, this pin functions as Serial Data Output B ($SDOB_{ChB}$), which is active in a 4-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock ($DCLK_{ChB}$). This pin must be left unconnected if not being used.
P9	$SCLK_{ChA}$	DI	Channel A ADC Configuration Interface Serial Data Clock. This clock input is used to shift data into and out of the device configuration memory.
P10	SDI_{ChA}	DI	Channel A ADC Configuration Interface Serial Data Input. Data is shifted into this input on the rising edge of the serial data clock, $SCLK_{ChA}$.
P11	$\overline{CS}_{ChA}$	DI	Channel A ADC Configuration Interface Chip-Select Input (Active Low). The $\overline{CS}_{ChA}$ input frames serial data transfers over the Configuration SPI.
P12	$DCO+_{ChA}$	DO	Channel A ADC LVDS Echo Clock Positive Output. This pin, along with $DCO-_{ChA}$, outputs a buffered and delayed version of $CLK+_{ChA}$ and $CLK-_{ChA}$. Data outputs from LVDS Data Lanes ($DA\pm_{ChA}$ and $DB\pm_{ChA}$, if active) are clocked out in alignment with both rising and falling edges of $DCO+_{ChA}$ and $DCO-_{ChA}$. If the echo clock mode is disabled, these pins can be left unconnected.
P13	$DA+_{ChA}/SDOA_{ChA}$	DO	Channel A ADC Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with $DA-_{ChA}$ serves as the primary LVDS Data Lane A. In SPI data interface mode, this pin functions as Serial Data Output A ($SDOA_{ChA}$), which is active in a 4-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock ($DCLK_{ChA}$). This pin must be left unconnected if not being used.
P14	$DA-_{ChA}/SDOB_{ChA}$	DO	Channel A ADC Data Interface Output Multifunction Pin. In LVDS data interface mode (default), this output pin along with $DA+_{ChA}$ serves as the primary LVDS Data Lane A. In SPI data interface mode, this pin functions as Serial Data Output B ($SDOB_{ChA}$), which is active in a 4-lane configuration only. Result data is shifted out of this pin on the falling edge of the data interface clock ($DCLK_{ChA}$). This pin must be left unconnected if not being used.

[1] AI is analog input, AO is analog output, DI is digital input, DI/O is digital input and output, DO is digital output, and P is power.

TYPICAL PERFORMANCE CHARACTERISTICS

Unless otherwise noted, T_A = 25°C, f_S = 10MSPS, G = 1.03, $+V_S$ = 5V, $-V_S$ = −1V, VDD33 = 3.3V, VDDLDO not connected, $IOVDD_{ChX}$ = 1.1V, $VDD11_{ChX}$ = 1.1V, differential input drive with 1.5V common mode, external FDA feedback capacitors (C_{fb}) = 220pF, and digital filters disabled.

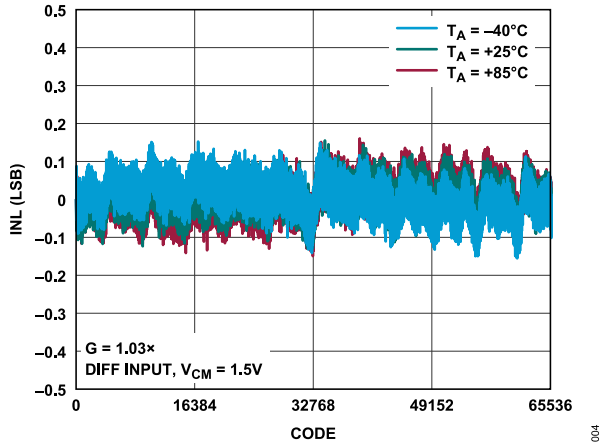

Figure 4. INL vs. Output Code, Differential Input Drive

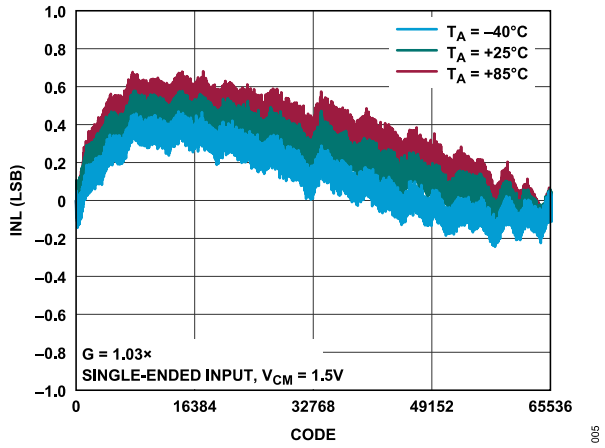

Figure 5. INL vs. Output Code, Single-Ended Input Drive

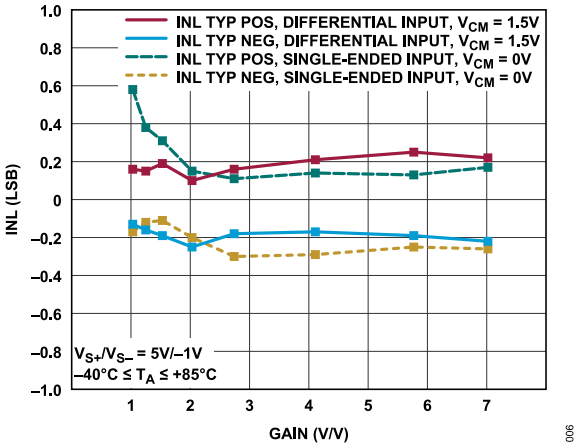

Figure 6. INL vs. Gain

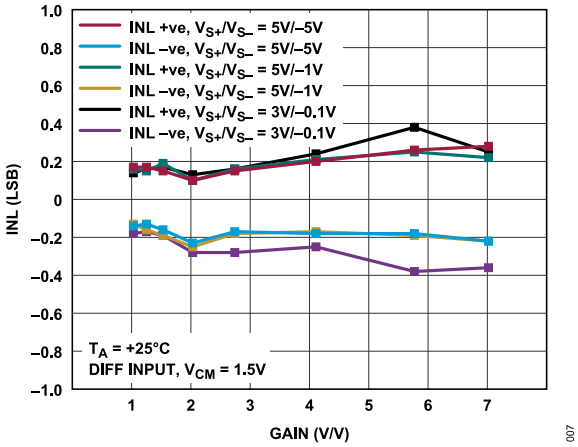

Figure 7. INL vs. Gain for Various FDA Supply Spans

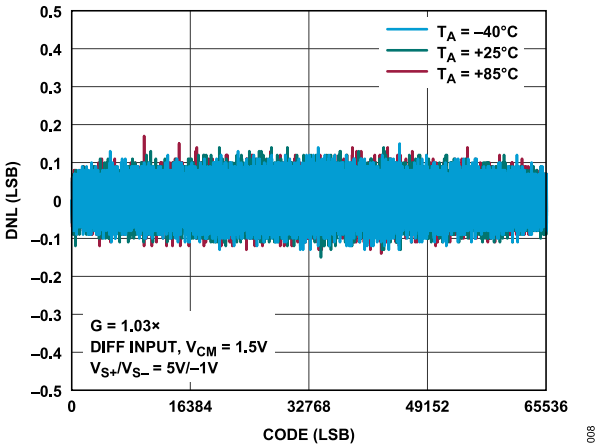

Figure 8. DNL vs. Temperature

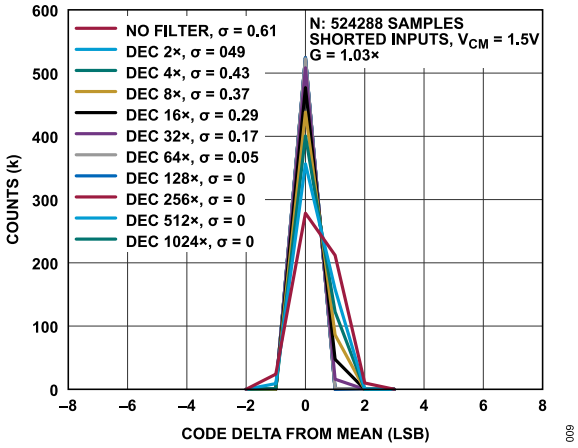

Figure 9. Histogram of Output Codes, Sinc1 Filter

TYPICAL PERFORMANCE CHARACTERISTICS

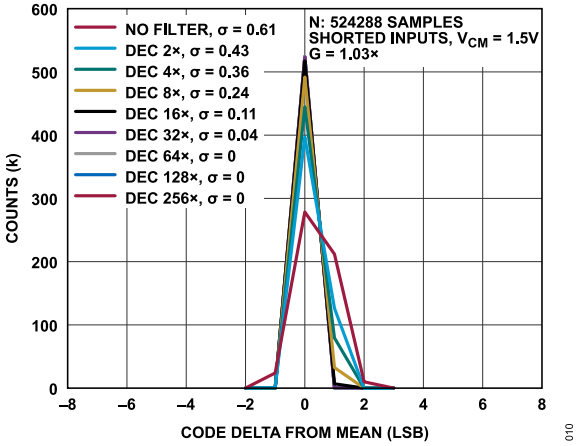

Figure 10. Histogram of Output Codes, Sinc5 Filter

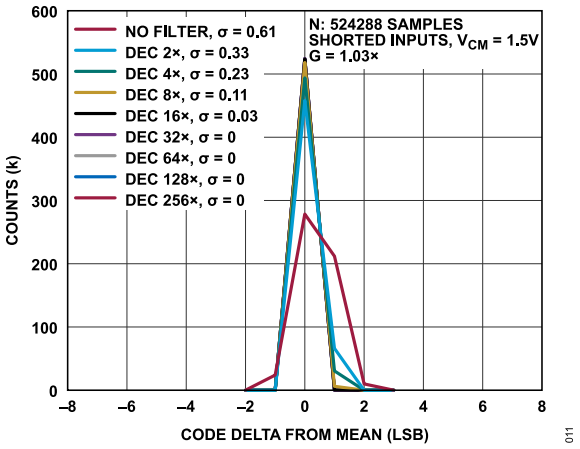

Figure 11. Histogram of Output Codes, Sinc5 + Compensation Filter

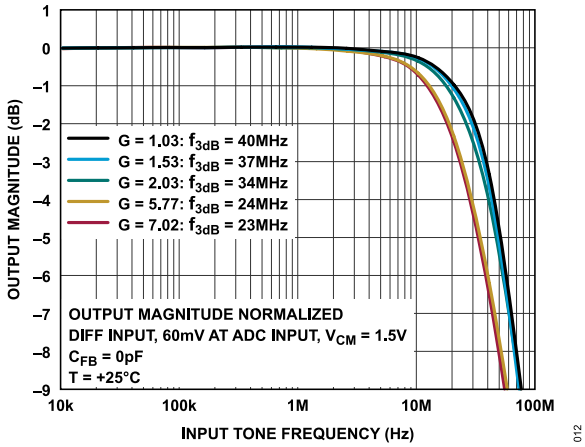

Figure 12. Small Signal Frequency Response, 10MSPS

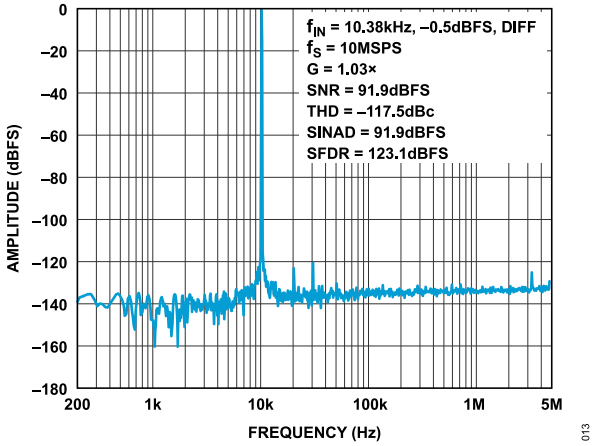

Figure 13. FFT 10MSPS, f_{IN} = 10.38kHz, Differential, −0.5dBFS, G = 1.03

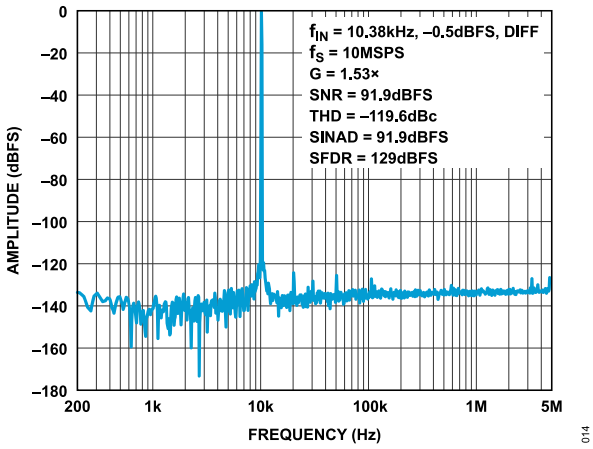

Figure 14. FFT 10MSPS, f_{IN} = 10.38kHz, Differential, −0.5dBFS, G = 1.53

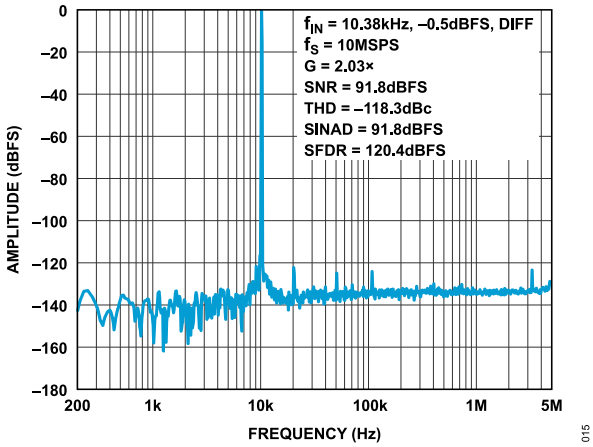

Figure 15. FFT 10MSPS, f_{IN} = 10.38kHz, Differential, −0.5dBFS, G = 2.03

TYPICAL PERFORMANCE CHARACTERISTICS

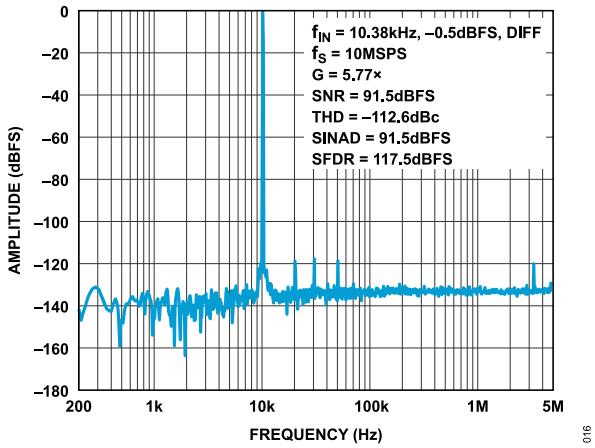

Figure 16. FFT 10MSPS, f_{IN} = 10.38kHz, Differential, −0.5dBFS, G = 5.77

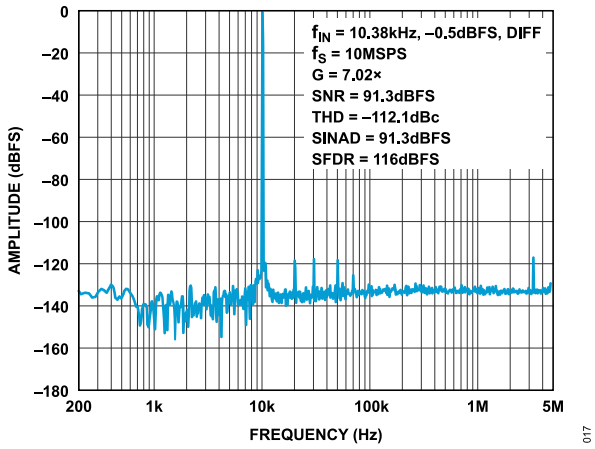

Figure 17. FFT 10MSPS, f_{IN} = 10.38kHz, Differential, −0.5dBFS, G = 7.02

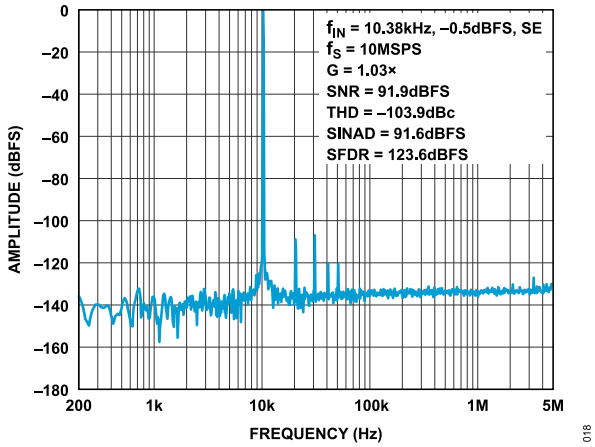

Figure 18. FFT 10MSPS, f_{IN} = 10.38kHz, Single-Ended, −0.5dBFS, G = 1.03

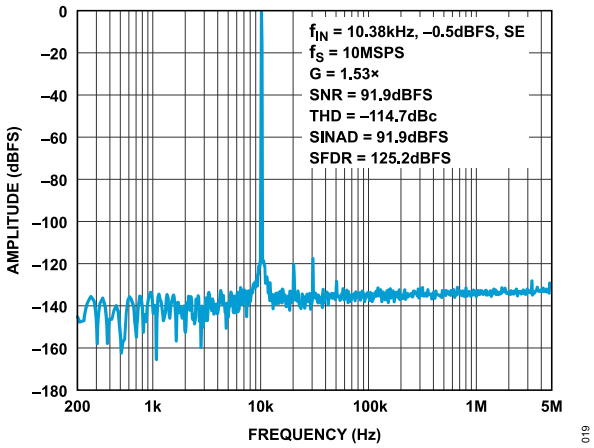

Figure 19. FFT 10MSPS, f_{IN} = 10.38kHz, Single-Ended, −0.5dBFS, G = 1.53

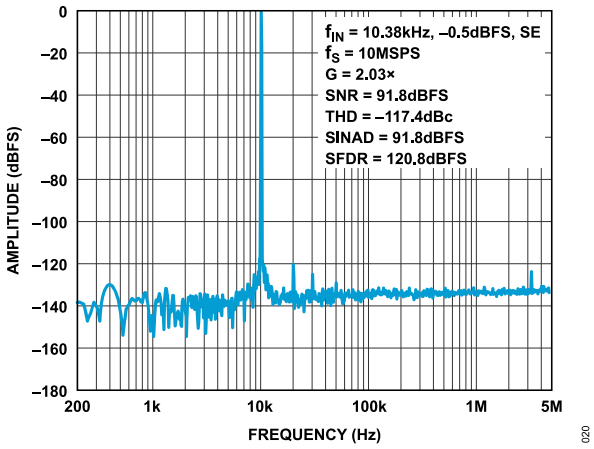

Figure 20. FFT 10MSPS, f_{IN} = 10.38kHz, Single-Ended, −0.5dBFS, G = 2.03

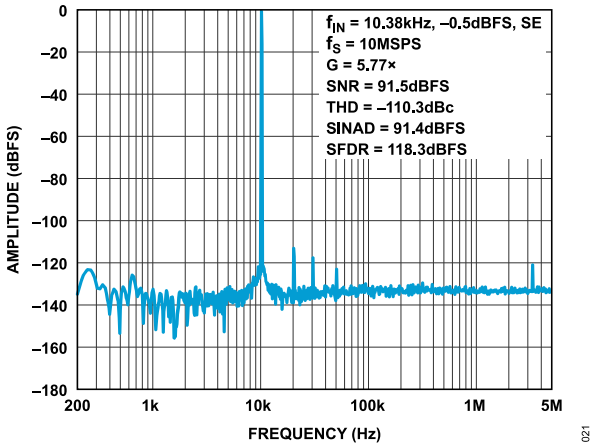

Figure 21. FFT 10MSPS, f_{IN} = 10.38kHz, Single-Ended, −0.5dBFS, G = 5.77

TYPICAL PERFORMANCE CHARACTERISTICS

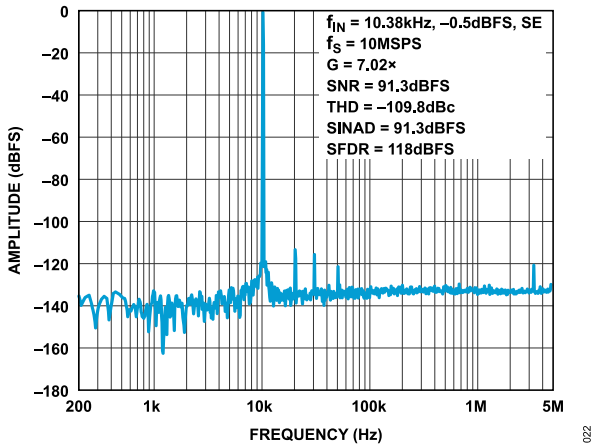

Figure 22. FFT 10MSPS, f_{IN} = 10.38kHz, Single-Ended, −0.5dBFS, G = 7.02

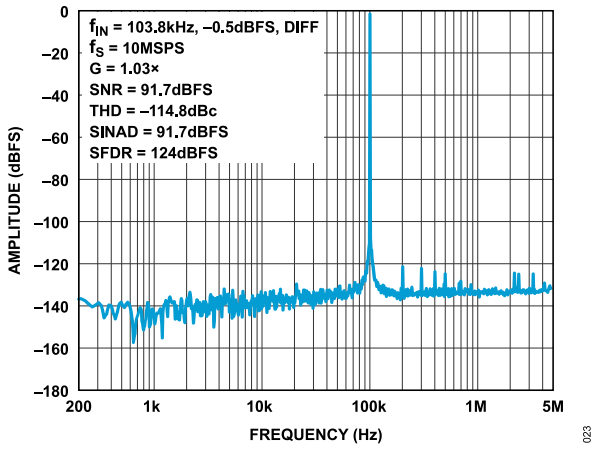

Figure 23. FFT 10MSPS, f_{IN} = 103.8kHz, Differential, −0.5dBFS, G = 1.03

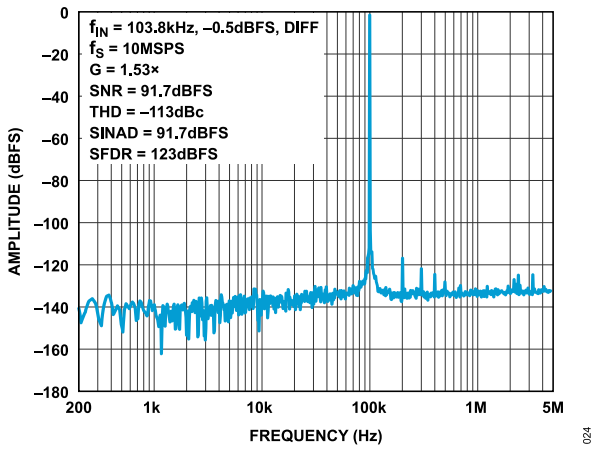

Figure 24. FFT 10MSPS, f_{IN} = 103.8kHz, Differential, −0.5dBFS, G = 1.53

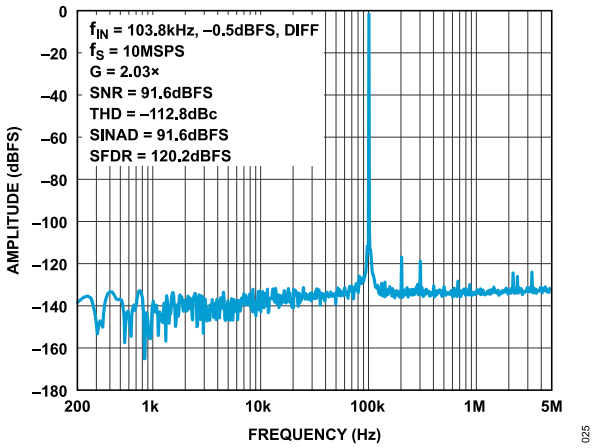

Figure 25. FFT 10MSPS, f_{IN} = 103.8kHz, Differential, −0.5dBFS, G = 2.03

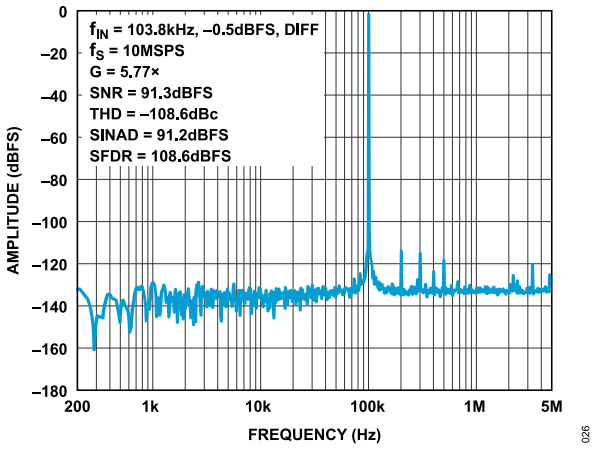

Figure 26. FFT 10MSPS, f_{IN} = 103.8kHz, Differential, −0.5dBFS, G = 5.77

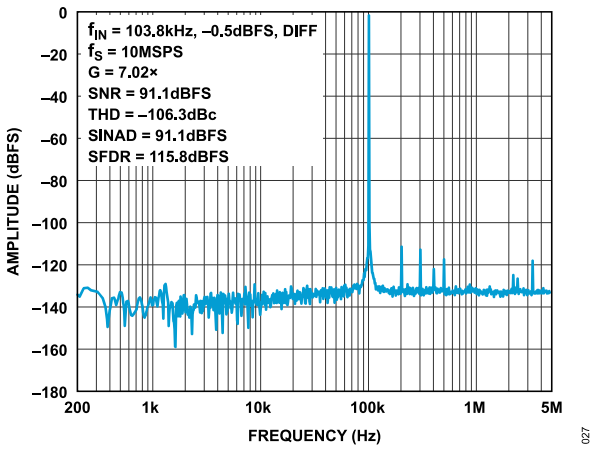

Figure 27. FFT 10MSPS, f_{IN} = 103.8kHz, Differential, −0.5dBFS, G = 7.02

TYPICAL PERFORMANCE CHARACTERISTICS

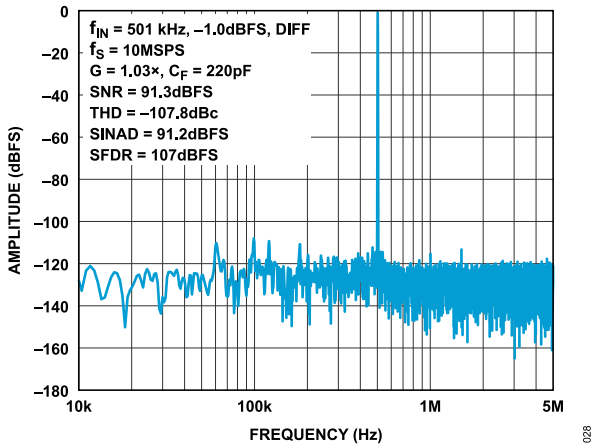

Figure 28. FFT 10MSPS, f_{IN} = 501kHz, Differential, −1dBFS, G = 1.03

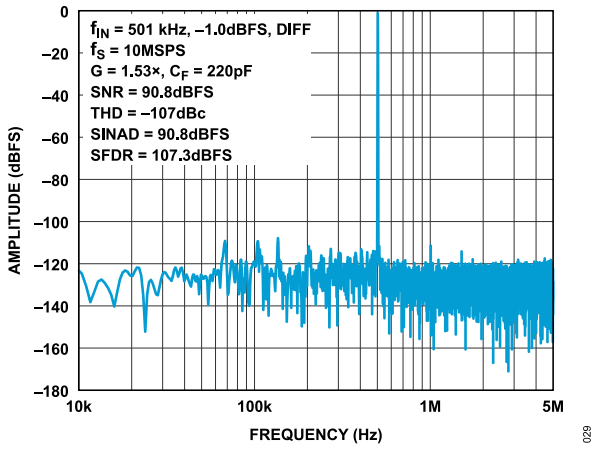

Figure 29. FFT 10MSPS, f_{IN} = 501kHz, Differential, −1dBFS, G = 1.53

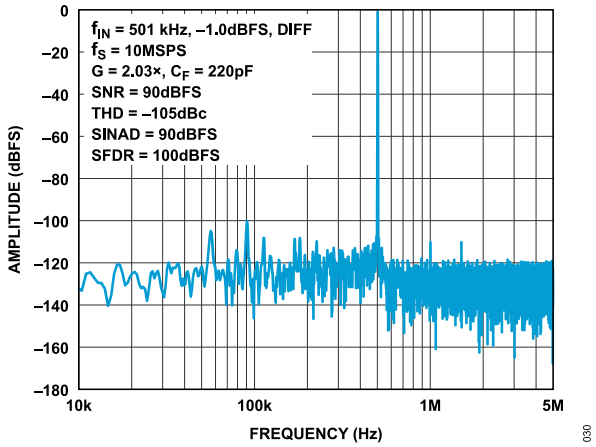

Figure 30. FFT 10MSPS, f_{IN} = 501kHz, Differential, −1dBFS, G = 2.03

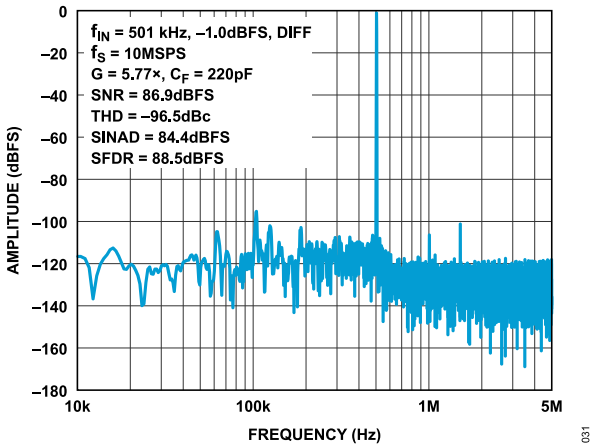

Figure 31. FFT 10MSPS, f_{IN} = 501kHz, Differential, −1dBFS, G = 5.77

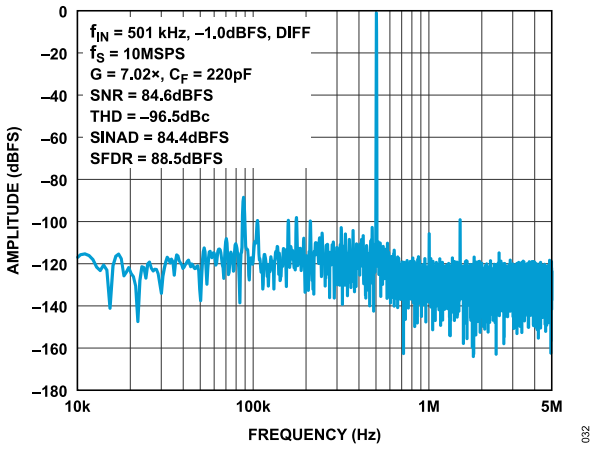

Figure 32. FFT 10MSPS, f_{IN} = 501kHz, Differential, −1dBFS, G = 7.02

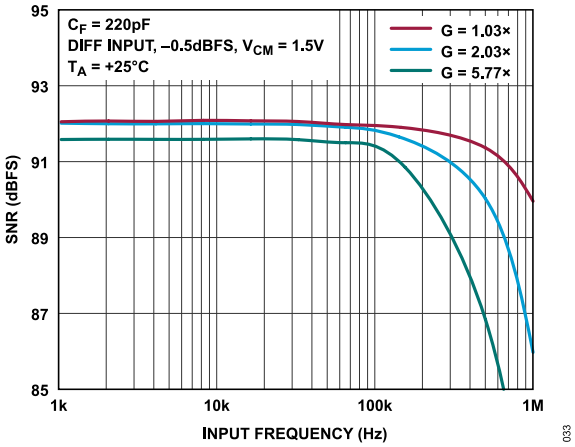

Figure 33. SNR vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

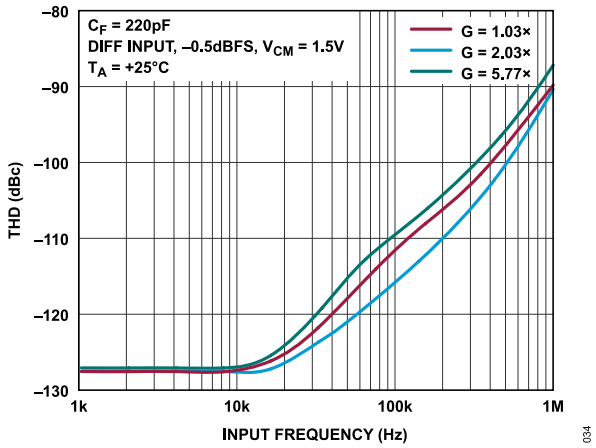

Figure 34. THD vs. Input Frequency

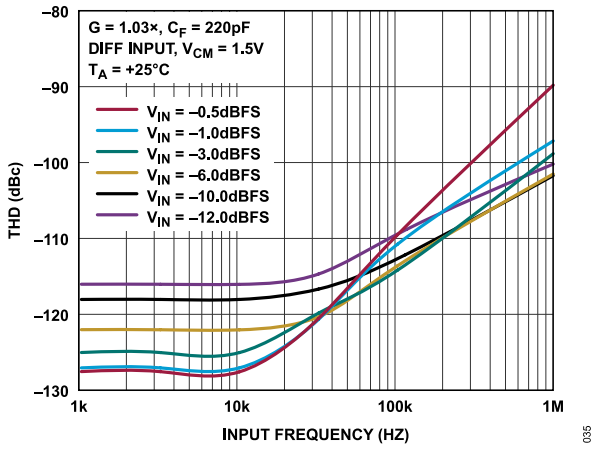

Figure 35. THD vs. Input Frequency for Various Input Tone Levels

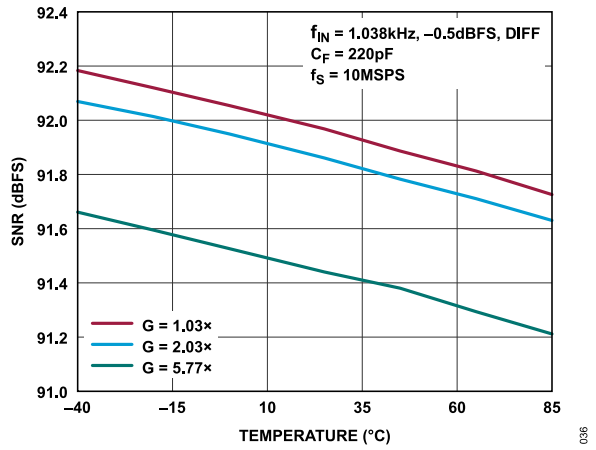

Figure 36. SNR vs. Temperature, f_{IN} = 1kHz, −0.5dBFS

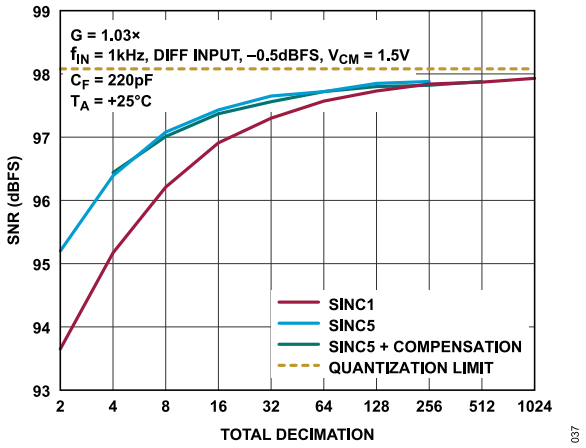

Figure 37. SNR vs. Total Decimation

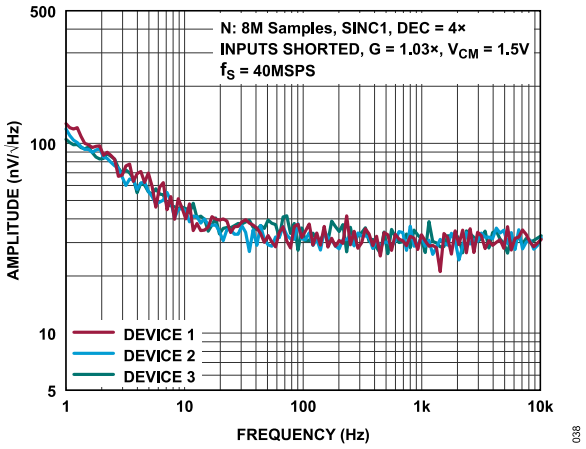

Figure 38. Low Frequency Noise, Inputs Shorted

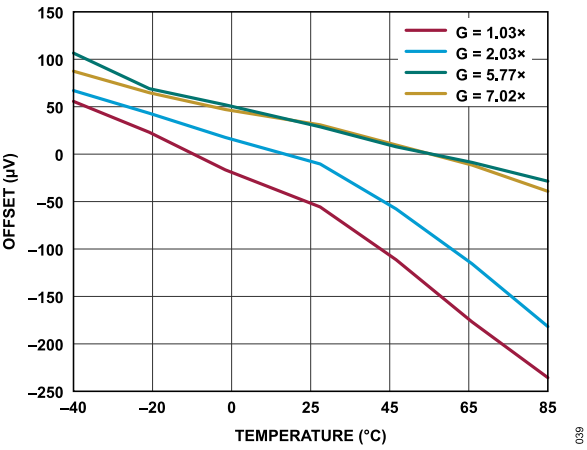

Figure 39. Offset Error vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

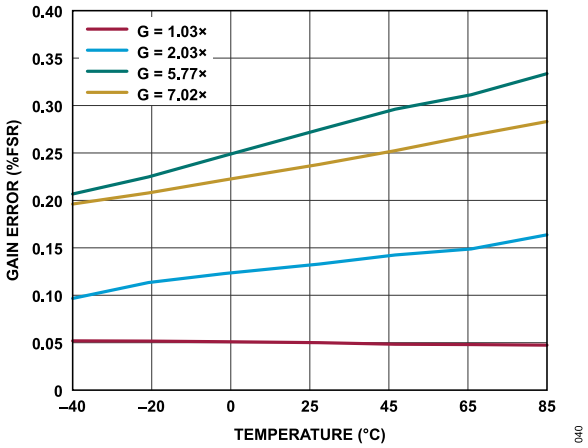

Figure 40. Gain Error vs. Temperature

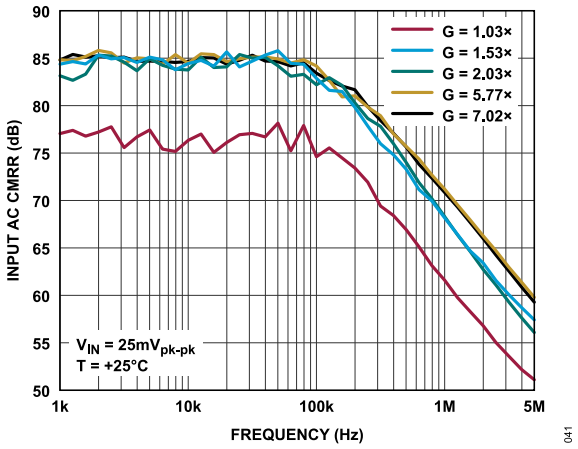

Figure 41. Input AC Common-Mode Rejection Ratio (CMRR) vs. Frequency

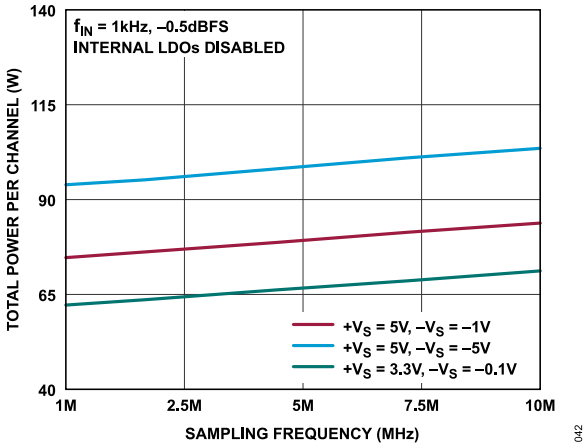

Figure 42. Total Power per Channel vs. Sampling Frequency, LDOs Disabled

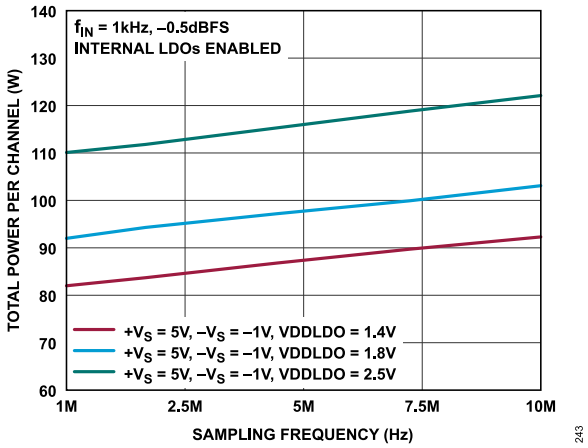

Figure 43. Total Power per Channel vs. Sampling Frequency, LDOs Enabled

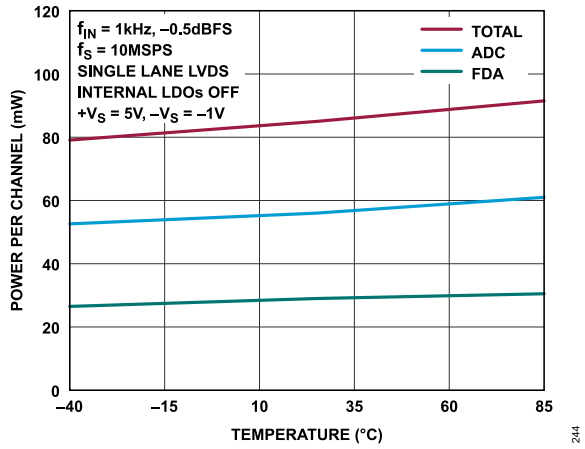

Figure 44. Power per Channel vs. Temperature, Normal Mode

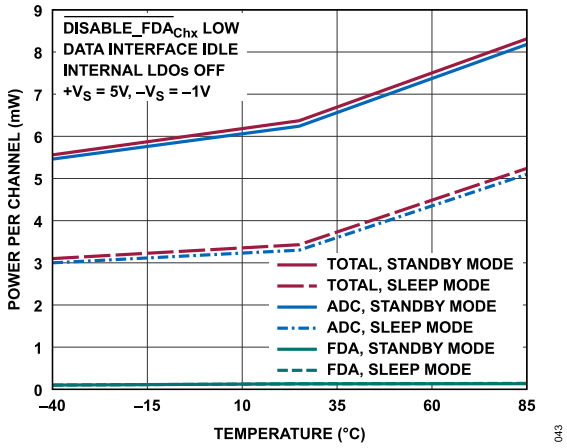

Figure 45. Power per Channel vs. Temperature, Power Saving Modes

TYPICAL PERFORMANCE CHARACTERISTICS

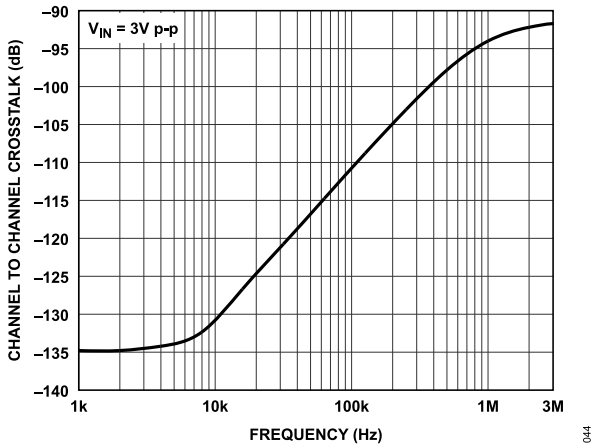

Figure 46. Channel-to-Channel Crosstalk

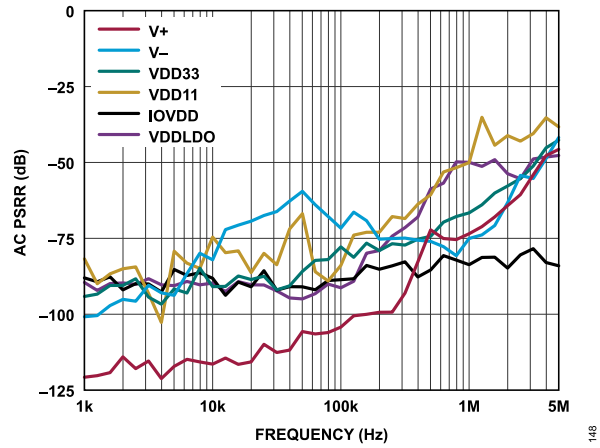

Figure 48. AC Power-Supply Rejection Ratio (PSRR) vs. Frequency

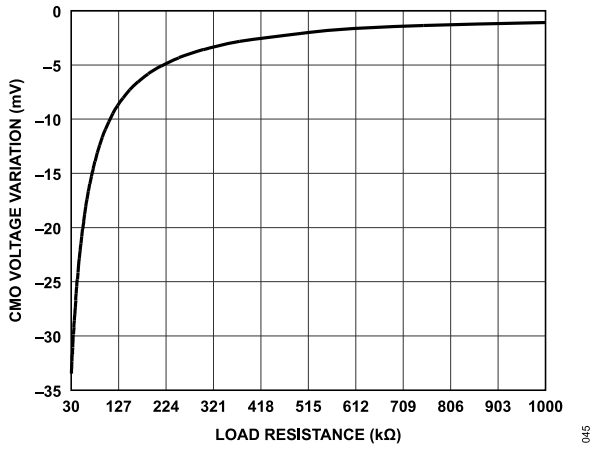

Figure 47. CMO Voltage Variation vs. Load Resistance

TERMINOLOGY

Integral Nonlinearity Error (INL)

INL refers to the deviation of each output code from a line drawn between points at negative full scale and positive full scale. The negative full-scale reference is defined by an input level equivalent to ½ LSB prior to the first code transition. The positive full-scale reference is defined as an input level that is 1½ LSB beyond the last code transition. The deviation is measured from the center of each code relative to the straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions occur at 1 LSB intervals. DNL is a measure of the maximum deviation of any code from the ideal code width. DNL is specified in terms of resolution for which no missing codes are guaranteed.

Zero Error

Zero error is the difference between the ideal midscale voltage, 0V, and the applied voltage producing the midscale output code, 0 LSB.

Gain Error

Gain error is specified as the difference in the slope of the ADC transfer characteristic vs. that of an ideal converter. In an ideal data converter, the first code transition (100 … 00 to 100 … 01) occurs ½ LSB more than the nominal negative full-scale input (−2.999954V for a ±3.0V range at 16 bits) and the last code transition (011 … 10 to 011 … 11) occurs 1½ LSB less than the nominal positive full-scale input (+2.999863V for a ±3.0V range at 16 bits).

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the RMS amplitude of an ADC full scale sine wave to the RMS sum of all other spectral components below the Nyquist frequency, excluding the first five harmonics and DC. The value for SNR is expressed in decibels relative to full scale (dBFS).

Signal-to-Noise and Distortion (SINAD) Ratio

SINAD is the ratio of the RMS amplitude of an ADC full scale sine wave to the root sum of squares of all other spectral components in the Nyquist bandwidth ($f < f_S/2$) including harmonic components but excluding the DC component. The value for SINAD is expressed in decibels relative to full scale (dBFS).

Noise Spectral Density (NSD)

Noise Spectral Density shows the noise power per unit bandwidth measured at the output of the ADC. NSD is numerically derived from the dynamic range (DR) specification of the ADC (which is obtained through a shorted-input test). The derivation assumes that the noise is evenly distributed (that is, white) across the Nyquist bandwidth ($f < f_S/2$):

$$NSD\ \left(\frac{\text{dBFS}}{\text{Hz}}\right) = -DR\ (\text{dB}) - 10 \times \log_{10}\left(\frac{f_S}{2}\right)$$

To convert from the logarithmic dBFS/Hz to linear nV/√Hz units:

$$NSD\ \left(\frac{\text{nV}}{\sqrt{\text{Hz}}}\right) = V_{FullScale,RMS} \times 10^{\left(\frac{NSD\ (\text{dBFS/Hz})}{20}\right)} \times 10^9$$

Note that to obtain the NSD referred to the input of the AD4885, divide the output referred value by the gain of the FDA.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the amplitudes of the first five harmonic components of the input signal to the RMS amplitude of the fundamental frequency (carrier). The value for THD is expressed in decibels relative to carrier (dBc).

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of the RMS amplitude of an ADC full scale sine wave to the peak spurious signal amplitude (excluding input signal harmonic components). The value of SFDR is expressed in decibels relative to full scale (dBFS).

Phase Angle Mismatch

Phase Angle Mismatch quantifies the difference in timing or phase response between the two channels of the device. It is measured by applying the same sine wave to both channels while sampling simultaneously, and calculating the phase shift between the two reconstructed waveforms.

Power-Supply Rejection Ratio (PSRR)

PSRR is a measure of the sensitivity of the ADC to variations in the specified power supply rail vs. frequency. PSRR is computed as the ratio of the observed change in the output code in RMS volts to the RMS magnitude of the perturbing signal coupled to the supply. The resulting ratio is reported in decibels (dB).

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PRODUCT OVERVIEW

The AD4885 is a dual-channel, 16-bit, 10MSPS per channel, SAR ADC with integrated fully-differential drivers. It is built as a system in package (SiP) that contains four separate die (two ADCs and two FDAs) along with gain-setting resistors and critical decoupling capacitors. In-package integrated components minimize the overall solution area, reduce the potential performance errors introduced by factors such as component selection, placement and routing challenges, and in general reduce the engineering effort to first design success.

The combination of a state-of-the-art ADC with a low-noise FDA enables reaching typical SNR figures as high as 92dB, result output latency of 131.25ns, and high signal fidelity for signals up to 1MHz. This parametric performance, throughput, and bandwidth make this product ideal for a variety of high-speed, data-acquisition applications. Accounting for its low power consumption, the product becomes an exceptionally apt choice for applications where channel density and thermal management present a challenge.

The external selection of the gain-setting resistors allows choosing the gain among a set of prefixed values, while the ability to place additional capacitors facilitates bandwidth adjustment. The FDAs can accommodate single-ended or differential input signals, do not require external generation of a common-mode voltage, and generally remove common SAR ADC drive challenges such as PCB layout, kickback settling calculations, and output filter design.

The SiP approach results in complete independence in channel configuration and data access. For each channel, conversion result access occurs via one of its two independent data interfaces: its multilane LVDS port operating at clock rates up to 80MHz or via its multioutput SPI operating at clock rates up to 50MHz.

A rich digital feature set increases the flexibility of the device and can potentially simplify system complexity and reduce the load on the digital host. These features include a 16,384 sample FIFO memory per channel, internal and external event detection, multifunction GPIOs, digital filtering, and system error correction coefficients.

TRANSFER FUNCTION

Each AD4885 channel digitizes the full-scale difference voltage at the input of the SAR ADC of 2 × V_{REFIN} into 2^{16} levels, resulting in an LSB size of 91.55µV with V_{REFIN} = 3.0V. Note that 1 LSB at 16 bits is approximately 15.26ppm. Note also that the transfer function is defined at input of the ADC, not the $INx\pm_{ChX}$ pins at the input of the AFE. The polarity is preserved in the sense that a positive value for $INx+_{ChX} - INx-_{ChX}$ results in a positive voltage measurement.

Table 7 summarizes the mapping of input voltages to differential output codes.

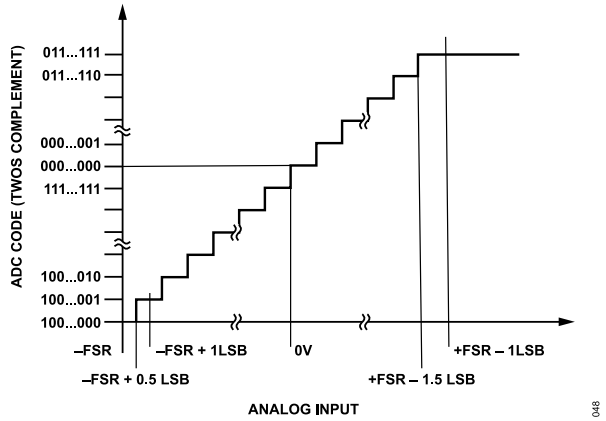

Figure 49. ADC Ideal Transfer Function for the Differential Output Codes (FSR is Full-Scale Range)

Table 7. Input Voltage to Output Code Mapping

Description	ADC Analog Input Voltage Difference (Volts)	Digital Output Code (Twos Complement, Hex)
FS − 1 LSB	$+V_{REFIN} \times (1 - 1/2^{15})$	0x7FFF
Midscale + 1 LSB	$+V_{REFIN}/2^{15}$	0x0001
Midscale	0	0x0000
Midscale − 1 LSB	$-V_{REFIN}/2^{15}$	0xFFFF
−FS + 1 LSB	$-V_{REFIN} \times (1 - 1/2^{15})$	0x8001
−FS	$-V_{REFIN}$	0x8000

REFERENCE BUFFER AND COMMON-MODE OUTPUT

The AD4885 requires an external 3.0V reference to drive the REFIN pin. The REFIN pin integrates a capacitor array totaling 18.8µF ± 20%. The capacitor array is constructed from commercially available, multilayer, high dielectric (X6S), ceramic capacitors, and it serves as the primary charge reservoir, which is shared by the two SAR ADCs.

Additional external capacitance (C_{RSV}) can optionally be placed across the REFIN and REFGND pins for improved charge capacity and noise rejection, as required. As with all precision circuits, the placement of the external reference capacitors must be as close to the device pins as possible on the same side of the PCB. The routing between the capacitor and device pins must minimize the series impedance in each routing path.

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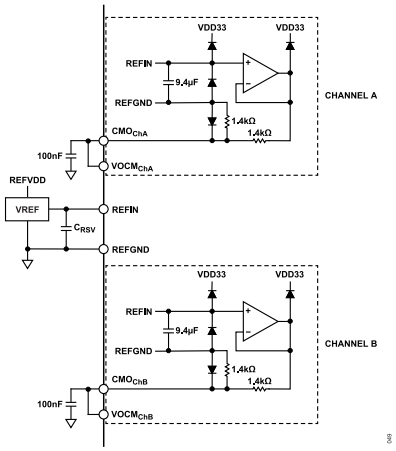

Figure 50. REFIN and CMO Internal Equivalent Circuit and Typical Application

Each AD4885 channel internally generates a common-mode reference voltage of one-half of V_{REFIN}, they are output through the CMO_{ChX} pins. The CMO_{ChX} outputs are used to set the common-mode output voltage of their respective analog front-ends. To achieve this, each CMO_{ChX} output must be directly connected to its corresponding V_{OCM_ChX} and decoupled with a recommended capacitance of 100nF.

Each CMO_{ChX} output is generated using a resistive divider connected to the reference buffer output. The resulting output impedance is typically 700Ω. Due to the limited drive capability, any additional load must be carefully considered to avoid excessive start-up times or absolute errors. In general, consider CMO_{ChX} buffering for the following situations:

- The VDD33 power rail of the AD4885 is frequently cycled.
- Short start-up settling times are required.
- If the external load on a CMO_{ChX} pin exceeds 30µA (R_L < 45kΩ). For the typical load regulation information, see Figure 47.

POWER SUPPLIES

The power requirements for the AD4885 are distributed across the following supply domains:

- AFE supply rails (±V_S)
- 3.3V ADC analog circuit domain (VDD33)
- 1.1V ADC core supplies ($VDD11_{ChA}$, $VDD11_{ChB}$)
- 1.1V domain for the digital interfaces ($IOVDD_{ChA}$, $IOVDD_{ChB}$)
- Optional internal voltage regulators input rail (VDDLDO)

The optional VDDLDO supply rail can be used to supply power to the four integrated voltage regulators used to internally power the 1.1V core ($VDD11_{ChA}$, $VDD11_{ChB}$) and interface ($IOVDD_{ChA}$, $IOVDD_{ChB}$) rails. For all details and design considerations when using the internal voltage regulators, see the Internally Regulated Supply Configuration section. On the other hand, for more details on applications that do not use internal regulators, see the Externally Generated Supply Configuration section.

Power for the VDD33 supply rail must be supplied from an external source and must only be applied once power is supplied to the 1.1V supply rails. For the full description of the activation order of the voltage supplies, see the Power Supply Sequence section.

All supply domains are internally decoupled using multilayer, high dielectric, ceramic capacitors (X6S), which eliminate the need of external decoupling capacitors. However, care must be taken to understand the bulk decoupling requirements for other components in the design, which share the same supply. Integrated supply decoupling capacitors in the AD4885 are listed in Table 6 and Table 8.

Table 8. Supply Rails Integrated Decoupling Summary

Supply Pin	Nominal Capacitance (µF)	Capacitance Tolerance (%)	Return Path
$+V_S$	0.44 (2× 0.22)	±10	GND
$-V_S$	0.44 (2× 0.22)	±10	GND
VDD33	0.94 (2× 0.47)	±10	GND
VDDLDO	0.44 (2× 0.22)	±10	GND
$VDD11_{ChA}$	1.88 (4× 0.47)	±10	GND
$VDD11_{ChB}$	1.88 (4× 0.47)	±10	GND
$IOVDD_{ChA}$	0.22	±10	$IOGND_{ChA}$
$IOVDD_{ChB}$	0.22	±10	$IOGND_{ChB}$

INTERNALLY REGULATED SUPPLY CONFIGURATION

Each channel in AD4885 includes two internal LDO regulators, one to generate the 1.1V $VDD11_{ChX}$ supply rail and another to internally generate the 1.1V $IOVDD_{ChX}$ supply rail. Upon power on or reset of the AD4885 channel registers, both regulators automatically power up when an external voltage source in the range of 1.4V to 2.7V is applied to the VDDLDO pins. Note that it is not allowed to enable the internally regulated supply configuration for one channel only. The regulators are designed to supply the internal load requirement of the AD4885, therefore, no external loading is permitted. Also, when using the internally regulated configuration, the $VDD11_{ChA}$, $VDD11_{ChB}$, $IOVDD_{ChA}$, and $IOVDD_{ChB}$ circuit nodes must be kept separate (that is not shorted in any combination among themselves). Note that, as described in the Power Saving Operating Modes section, the $IOVDD_{ChX}$ rails are disabled in both power saving modes.

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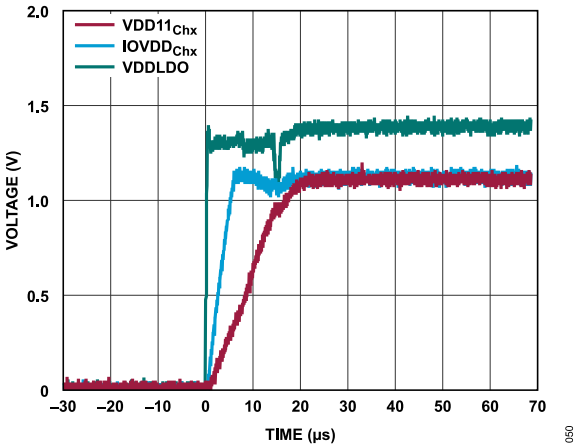

Figure 51. Typical Regulator Start-Up Transient, Converter Idle

The required connectivity when using the internal regulators is shown in Figure 52. As shown in Figure 52, the three $VDD11_{ChA}$ pins (G7, H7, and J7) must be shorted. It is recommended that a thick trace or polygon on the device side of the PCB be used to implement this connection in the physical design to minimize routing impedance. The same shorting indications apply to the $VDD11_{ChB}$ pins (G14, H14, and J14). The VDD33 rail must be powered with an external 3.3V supply. To further minimize power consumption, this supply can be removed when both channels have been put in one of the power saving modes. When this supply is removed, only analog circuitry is held in reset, and the configuration register content remains unaffected. For the applicable input voltage tolerance for each supply rail, see the Specifications section.

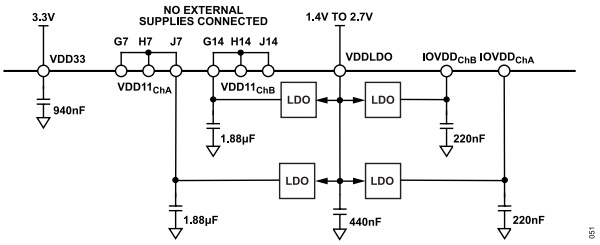

Figure 52. Internally Regulated (1.1V) Supply Configuration

The internally regulated configuration is ideal for use in area constrained applications where the ability to eliminate external regulators is advantageous. However, note that in this configuration the internal regulators introduce additional power dissipation inside AD4885.

EXTERNALLY GENERATED SUPPLY CONFIGURATION

In systems using externally generated supplies, VDDLDO pins must be left unconnected. With VDDLDO unconnected, all four internal LDO regulators powering $VDD11_{ChA}$, $VDD11_{ChB}$, $IOVDD_{ChA}$, and $IOVDD_{ChB}$ are automatically disabled. $VDD11_{ChA}$ and $VDD11_{ChB}$ must be externally supplied with 1.1 V, it is recommended to supply both rails with the same source. $IOVDD_{ChA}$ and $IOVDD_{ChA}$ must be externally supplied with 1.1V to 1.2V, it is recommended to supply both rails with the same source. Note that if $VDD11_{ChX}$ is not present, the corresponding ADC channel is held in a POR state and all its registers reset to their default state after the supply reestablishes. For more details on the POR circuitry, see the Power-On Reset (POR) Monitor section. The VDD33 rail must be powered with an external 3.3V supply. The VDD33 supply can be removed to further reduce power when both channels are in one of the two Power Saving Operating Modes, only analog circuitry is held in reset, and register contents remain unaffected. For the applicable input voltage tolerance for each supply rail, see the Specifications section.

As shown in the example of Figure 53, external voltage sources are applied to $VDD11_{ChA}$, $VDD11_{ChB}$, $IOVDD_{ChA}$, and $IOVDD_{ChB}$ pins.

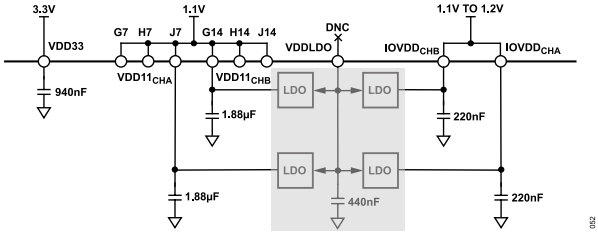

Figure 53. Externally Sourced Supply Configuration

POWER-ON RESET (POR) MONITOR

Each AD4885 channel has an independent power supply monitoring circuit that inhibits the converter functions and resets the configuration memory when supply conditions are outside the specified operating limits. This function ensures that the channel is in a deterministic state after power-up. The power-on function is constructed from two independent voltage monitors, the first measuring the core 1.1V supply ($VDD11_{ChX}$) and a second measuring the voltage at the reference input (REFIN). Each monitor has its own comparator output that is used to decouple the analog and digital block resets, as shown in Figure 54.

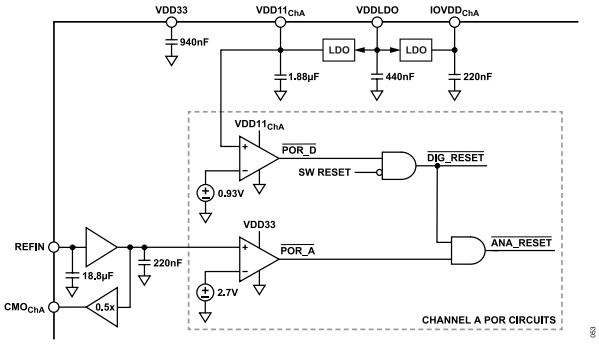

Figure 54. Simplified Diagram of POR Circuit (Shown for Channel A)

The core VDD (1.1V) supply monitor compares the $VDD11_{ChX}$ supply voltage against a preset threshold of 0.93V. If the supply voltage falls to less than this threshold, a reset signal, $\overline{POR_D}$, asserts. The digital logic reset signal, $\overline{DIG_RESET}$, is defined as the logical combination of the $\overline{POR_D}$ signal and (logical AND) the complement of the SPI software reset function. When either

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the $\overline{\text{POR_D}}$ signal (VDD11 < 0.93V) or the SW RESET signal is asserted, the internal digital circuitry is held in reset. When cleared, the contents of the configuration registers of this channel are restored to the factory default settings.

The reference monitor compares the input voltage at the reference input pin, REFIN, against a preset threshold of 2.7V. As shown in Figure 54, power for the reference monitor circuit is supplied from the VDD33 supply. However, it is important to note that a reference voltage below 2.6V causes the part to stop outputting conversion data results. To recover the conversion process, bring the reference voltage to 2.87V. For correct operation of the monitor circuit, the VDD33 supply must be applied to the AD4885 within the specified tolerance of 3.3V ± 5% before the reference source is enabled. Assuming the device is operating within the specified supply conditions, a reference voltage less than 2.7V results in the assertion of an internal reset signal, $\overline{\text{POR_A}}$. The $\overline{\text{POR_A}}$ signal and (logical AND) the $\overline{\text{DIG_RESET}}$ signal are combined to produce a reset ($\overline{\text{ANA_RESET}}$) for the analog circuit blocks including the ADC core, ADC timer, and reference buffer. If this reset signal is asserted, the analog blocks are placed in an inactive state, and the converter functionality is disabled. This event is indicated with a value of 1 in the POR_ANA_FLAG bit from the Device Status Register (Address 0x14). The state of the event detection is persistent until a Logic 1 is written to the POR_ANA_FLAG bit to clear the detection state.

POWER SUPPLY SEQUENCE

Table 9 specifies the recommended supply sequences for both internal and external generation of 1.1V supply rails ($IOVDD_{ChA}$, $IOVDD_{ChB}$, $VDD11_{ChA}$, and $VDD11_{ChB}$). Both methods are shown in Figure 55 and Figure 56, where highlighted in blue are the supplies that must be provided to the AD4885, including the REFIN voltage. In both cases, the AD4885 requires that the supplies are applied in ascending voltage order. As described in the Power-On Reset (POR) Monitor section, the voltage at the reference input pin must only be applied once VDD33 is within the specified supply tolerance to avoid undesired behavior. Therefore, if the selected voltage reference does not provide an enable pin, it is strongly recommended to design the reference circuit to power up after VDD33.

The configuration SPI inputs, $\overline{CS}_{ChX}$, $SCLK_{ChX}$, and SDI_{ChX} are protected with clamps to the VDD33 supply rail to allow the inputs to swing more than $IOVDD_{ChX}$. As a consequence of this architectural decision, it is necessary to drive the SPI inputs to ground, or to otherwise leave the inputs floating until VDD33 is greater than $IOVDD_{ChX}$ − 0.3V. Alternatively, the VDD33 source can be connected to the device using a series power switch, such as the ADP199, configured so that the switch is open when the source is less than $IOVDD_{ChX}$ − 0.3V, which eliminates the parasitic current path through the digital inputs to VDD33.

To power down the application circuit, the power-up sequence specified in Table 9 must be reversed.

Table 9. Recommended Supply Sequence

1.1V Supplies (IOVDD and VDD11) Source	Supply Sequence
Internally Generated	**1.** VDDLDO **2.** VDD33 **3.** Digital inputs **4.** Reference **5.** $\pm V_S$ **6.** Analog inputs
Externally Generated	**1.** IOVDD, VDD11 **2.** VDD33 **3.** Digital inputs **4.** Reference **5.** $\pm V_S$ **6.** Analog inputs

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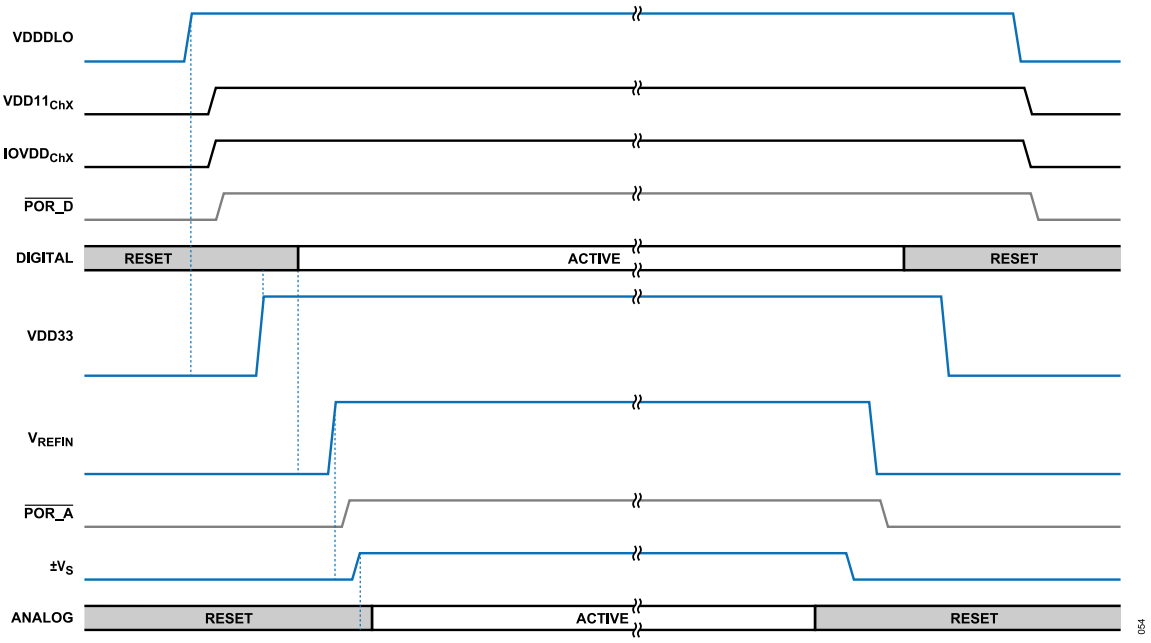

Figure 55. Power Supply Sequence, Internally Generated IOVDD$_{ChX}$ and VDD11$_{ChX}$

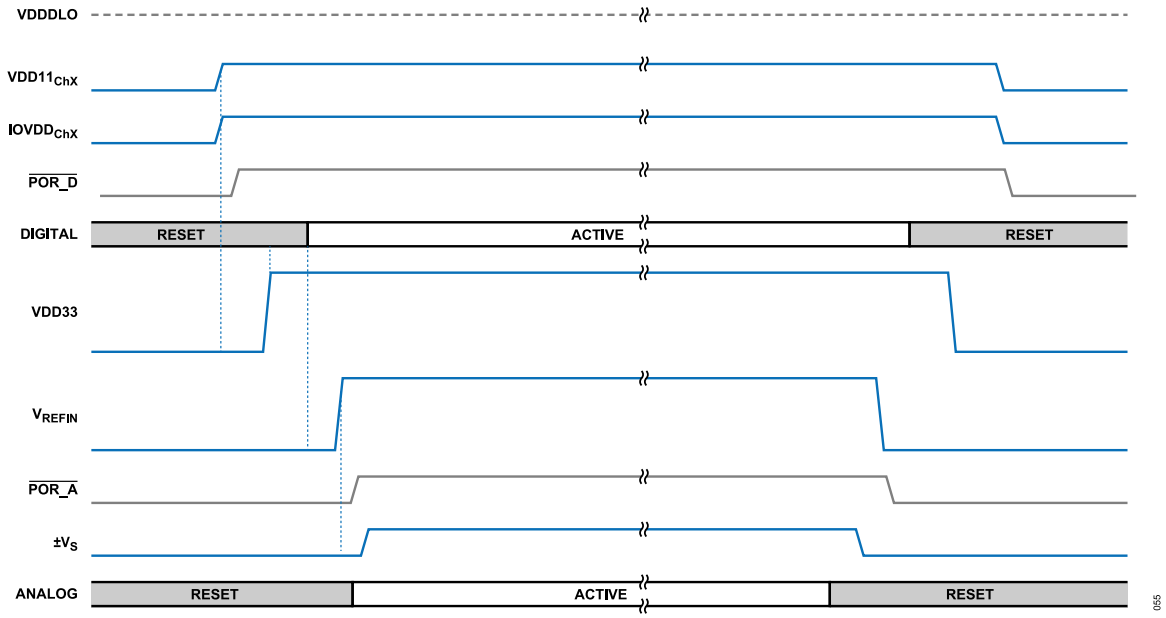

Figure 56. Power Supply Sequence, Externally Generated IOVDD$_{ChX}$ and VDD11$_{ChX}$

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POWER SAVING OPERATING MODES

The operating mode of each AD4885 channel is controlled by the OPERATING_MODES bits in its corresponding Device Configuration Register (Address 0x02). On power up and after reset, the default is normal mode (OPERATING_MODES = 2'b00). Table 10 shows all operating modes, and Figure 57 shows the allowed transitions between these modes. Note that direct transitions between the two power saving modes (standby and sleep mode) are not permitted.

It is important to stop all conversion and data interface clocking to a channel before configuring its power mode.

When both ADC channels have been put in either standby mode or sleep mode, the VDD33 supply can be removed to reduce power consumption. This supply must be reestablished prior to issuing the SPI configuration interface commands to exit either power saving mode.

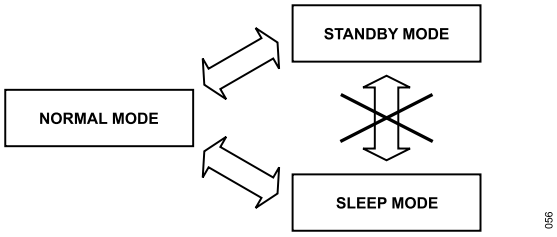

Figure 57. Operating Mode Transitions

Transitioning from normal mode to either of the two power saving modes is achieved by writing the required value to the OPERATING_MODES bits in the Device Configuration Register. Waking up (that is, transitioning back to normal mode) is achieved in a similar way because the SPI configuration interface operation is not affected by any of the power saving modes (see the SPI Configuration Interface section). Standby mode can be selected to save power, in the case where the user wants to quickly return to normal conversions. Sleep mode is a lower power state where returning to normal mode takes longer. Both standby and sleep mode can be particularly useful when used with the result FIFO (see the Result FIFO section), whereby previously stored conversion data can be accessed from the FIFO while it is still in the selected power saving mode.

When using the internally regulated supply configuration, putting a channel into standby or sleep mode powers down the LDO regulator generating its corresponding $IOVDD_{ChX}$ rail. This disables all inputs and outputs under the now unpowered $IOVDD_{ChX}$ domain (all corresponding $GPIOx_{ChX}$, LVDS data interface (see the LVDS Data Interface section), and SPI data interface (see the SPI Data Interface section) signals are disabled). Note that in this condition, it is still possible to write to the AD4885 SPI configuration to issue a command to return to normal mode by writing to the OPERATING_MODES bits in the device configuration register (see the Device Configuration Register section) or to issue a software reset (see the Software Reset section), because $\overline{CS}_{ChX}$, $SCLK_{ChX}$, and SDI_{ChX} are under the $VDD11_{ChX}$ supply domain. As $GPIOx_{ChX}$ is disabled, it is not possible to perform any read activity on the SPI configuration interface bus.

When $IOVDD_{ChX}$ is externally supplied, and the channel is put into standby or sleep mode, its LVDS data interface is disabled, however, all its $GPIOx_{ChX}$, SPI data interface, and SPI configuration interface pins remain enabled and unaffected. While power is supplied externally to $IOVDD_{ChX}$ within its specified range, previously acquired data stored in the channel result FIFO can be access in either standby or sleep mode.

Table 10 also indicates the wake-up times associated with each of the modes. Wake-up time from sleep mode is significantly higher than that of standby mode because time must be allowed for the internal reference and common-mode buffers to reenable and to replenish charge to the internal capacitors. Wake-up time is defined as the interval between writing the SPI command that exits the selected power-saving mode to the device configuration register (see OPERATING_MODES bits in the Device Configuration Register section) and the point at which the first conversion start pulse can be applied. Applying conversion start pulses before the specified wake-up time has elapsed can lead to improper operation or permanent device damage.

For the lowest power consumption of a channel in any of the power saving operating modes, the LVDS_SELF_CLK_MODE must be enabled in its ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section) to power down the LVDS DCO transmitter.

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Table 10. Power Saving Operating Modes

Operating Mode	OPERATING_MODES Bits Value	Description	Effect	Wake-Up Time (Maximum Time to Normal Mode)
Normal	0b00	Normal operating mode.	Normal operation.	N/A[1]
Standby	0b10	Standby operating mode.	The internal $IOVDD_{ChX}$ LDO regulator is disabled. If $IOVDD_{ChX}$ is not externally supplied, all channel $GPIOx_{ChX}$, LVDS data interface and SPI data interface signals are disabled. For the SPI configuration interface, only writes to the device configuration register (see the Device Configuration Register section) and Interface Configuration A register (see the Interface Configuration A Register section) are allowed. If $IOVDD_{ChX}$ is externally supplied, all channel $GPIOx_{ChX}$ and SPI data interface signals are enabled. The SPI configuration interface is fully enabled. Because the SPI data interface remains enabled, the user can access data in the result FIFO (see the Result FIFO section). The ADC core is powered down. The analog circuitry remains in reset ($\overline{ANA_RESET}$ remains asserted), and no ADC conversions can be performed. The VDD33 supply can be removed to reduce power. When in use, the internal $VDD11_{ChX}$ LDO regulator remains on. The internal reference buffer is enabled. Common-mode output buffer is enabled. The LVDS interface is disabled.	100µs
Sleep	0b11	Low power operating mode.	The internal $IOVDD_{ChX}$ LDO regulator is disabled. If $IOVDD_{ChX}$ is not externally supplied, all $GPIOx_{ChX}$, LVDS data interface and SPI data interface signals are disabled. For the SPI configuration interface, only writes to the device configuration register (see the Device Configuration Register section) and Interface Configuration A register (see the Interface Configuration A Register section) are allowed. If $IOVDD_{ChX}$ is externally supplied, all $GPIOx_{ChX}$ and SPI data interface signals are enabled. The SPI configuration interface is fully enabled. Because the SPI data interface remains enabled, the user can access data in the result FIFO (see the Result FIFO section). The ADC core is powered down. The analog circuitry remains in reset ($\overline{ANA_RESET}$ remains asserted), and no ADC conversions can be performed. The VDD33 supply can be removed to reduce power. The internal reference buffer is disabled. When enabled, the internal $VDD11_{ChX}$ LDO regulator remains on. The common-mode output buffer is disabled. The LVDS interface is disabled. The SPI data interface remains enabled to access data in the result FIFO (see the Result FIFO section).	180µs

[1] N/A means not applicable.

THEORY OF OPERATION

SOFTWARE RESET

Each AD4885 channel can be independently reset by software. This reset method must only be used once the channel ADC is in an idle state, where conversions are not being clocked, and any existing conversion is completed.

A software reset is achieved by issuing the following two writes to the Interface Configuration A register of the channel (see the Interface Configuration A Register section, Address 0x00):

1. Set SW_RESET and SW_RESETX bits to 1 by writing 0x81 to the register.
2. Issue another write command that sets either or both of those bits to 0.

This action returns any previously configured registers of the channel to their default settings, except for the ADDR_ASCENSION bit from the Interface Configuration A register, which keeps its previous value. The contents of the channel FIFO, if any, are also not affected by the software reset. The ADDR_ASCENSION bit and FIFO data only return to their default settings after a hardware reset or a full power-up happens.

APPLICATIONS INFORMATION

ANALOG INPUTS DRIVE AND GAIN

Each AD4885 channel has an integrated fully-differential amplifier stage at the input. As shown in Figure 58, the feedback resistors are fixed at 750Ω, whereas a set of three resistors can be arranged in different ways to change the value of the effective series input resistance, and therefore modify the gain of this stage (see Figure 61 to Figure 74). Gains beyond the 5.77 configuration result in a noise contribution from the FDA stage that dominates over that of the ADC itself, so they are generally not recommended.

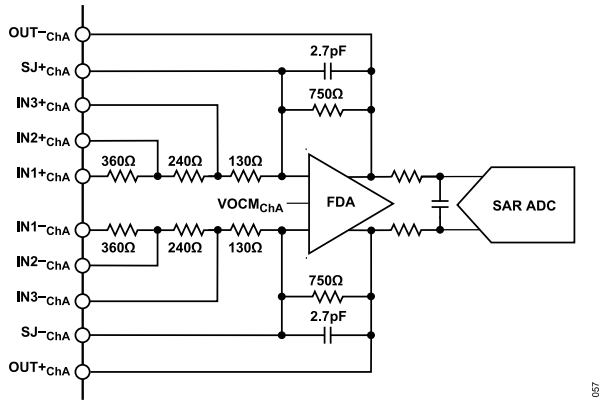
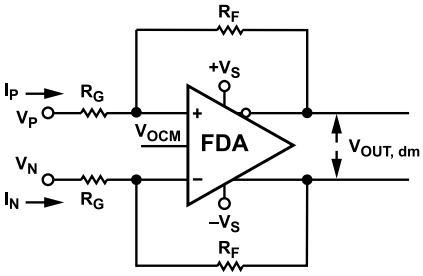


Figure 58. AD4885 Input (Shown for Channel A)

Table 11 shows the gains that can be obtained through different input pin short configurations, along with the resulting input impedance for both differential and single-ended driving. Notation is according to Figure 59 and Figure 60, and the differential gain is calculated as $G = R_F/R_G$.

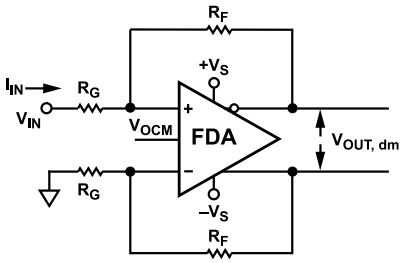
The input of the AD4885 can be driven with either a differential or a single-ended signal. For the single-ended case, note that the input impedance of the circuit is effectively higher than it is for a conventional operation amplifier (op amp) connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the R_G input resistor. As for the common-mode of the input signal, note that absolute voltage limits (Input Common-Mode Voltage Range specification) at the FDA SJ± pins must be respected. In Table 11, the permitted common mode range is worked out for each gain under nominal FDA supply conditions ($+V_S$ = 5V, $-V_S$ = −1V), including some headroom to avoid violating the Input Common-Mode Voltage Range specification even on a transient basis. For more details on the common-mode at the output of the FDA, see the Reference Buffer and Common-Mode Output section.



$$R_{IN,DIFF} = \frac{V_P - V_N}{(I_P - I_N)/2} = 2 \times R_G$$

058

Figure 59. FDA Input Impedance, Differential Drive



$$R_{IN,SE} = \frac{V_{IN}}{I_{IN}} = \frac{R_G}{1 - \left(\frac{R_F}{2 \times (R_G + R_F)}\right)}$$

059

Figure 60. FDA Input Impedance, Single-Ended Drive

Table 11. FDA Gain Options

Gain	Differential Input Voltage Range (V)	Input Signal Common-Mode Range ($+V_S$ = 5V, $-V_S$ = −1V)	Required External Shorting	FDA Stage Input	R_G (Ω)	$R_{IN,DIFF}$ (Ω)	$R_{IN,SE}$ (Ω)
1.03	±2.92	−3.2V to +5.6V	None	IN1±	360 + 240 + 130 = 730	1460	978
1.25	±2.40	−2.8V to +5.2V	IN3↔SJ	IN1±	360 + 240 = 600	1200	831
1.53	±1.96	−2.4V to +4.9V	IN2↔IN3	IN1±	360 + 130 = 490	980	702
2.03	±1.48	−2.0V to +4.6V	IN1↔IN2	IN1± or IN2±	240 + 130 = 370	740	556
2.08	±1.44	−2.0V to +4.6V	IN2↔IN3↔SJ	IN1±	360	720	544
2.74	±1.10	−1.7V to +4.3V	IN1↔IN3	IN2±	(360 || 240) + 130 = 274	548	432
3.13	±0.96	−1.6V to +4.2V	IN1↔IN2, IN3↔SJ	IN1± or IN2±	240	480	386
4.11	±0.73	−1.4V to +4.1V	IN1↔SJ	IN2±	360 || (240 + 130) = 182.5	365	305
5.21	±0.58	−1.3V to +4.0V	IN1↔IN3↔SJ	IN2±	(360 || 240) = 144	288	248
5.77	±0.52	−1.3V to +3.9V	IN1↔IN2↔IN3	IN1± or IN2± or IN3±	130	260	227
7.02	±0.43	−1.2V to +3.8V	IN1↔SJ	IN3±	(360 + 240) || 130 = 106.8	214	190

APPLICATIONS INFORMATION

Table 11. FDA Gain Options (Continued)

Gain	Differential Input Voltage Range (V)	Input Signal Common-Mode Range (+V_S = 5V, −V_S = −1V)	Required External Shorting	FDA Stage Input	R_G (Ω)	$R_{IN,DIFF}$ (Ω)	$R_{IN,SE}$ (Ω)
7.86	±0.38	−1.2V to +3.8V	IN1↔SJ, IN2↔IN3	IN2± or IN3±	(360 || 130) = 96	191	172
8.92	±0.34	−1.1V to +3.8V	IN1↔IN2↔SJ	IN3±	(240 || 130) = 84	169	153
10.98	±0.27	−1.1V to +3.7V	IN1↔IN3, IN2↔SJ	IN1± or IN3±	360 || 240 || 130 = 68.3	137	126

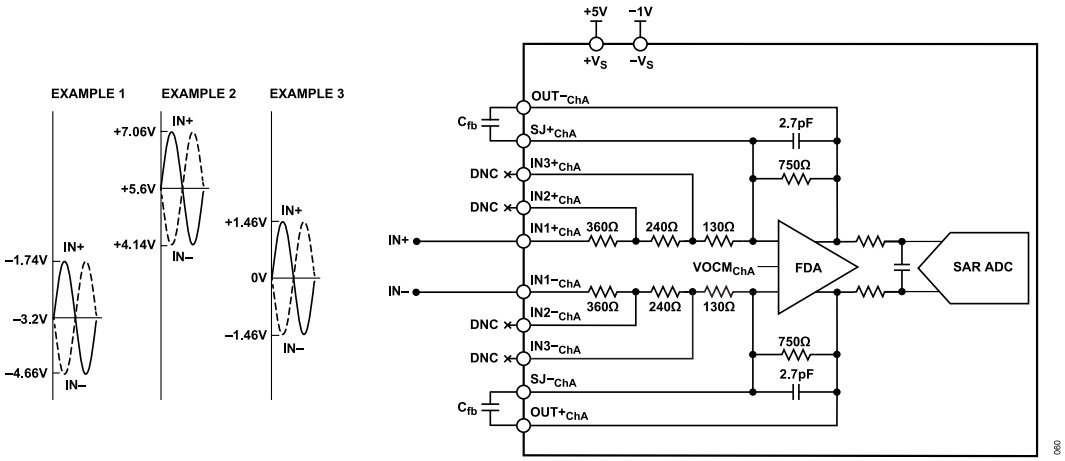


Figure 61. AD4885 Differential Input Configuration with Gain = 1.03, ±2.91V Input Range

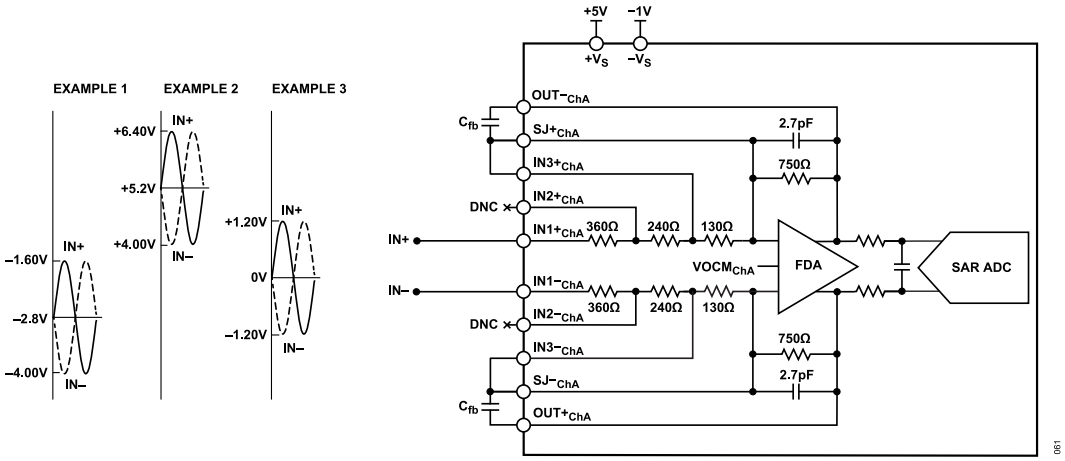


Figure 62. AD4885 Differential Input Configuration with Gain = 1.25, ±2.40V Input Range

APPLICATIONS INFORMATION

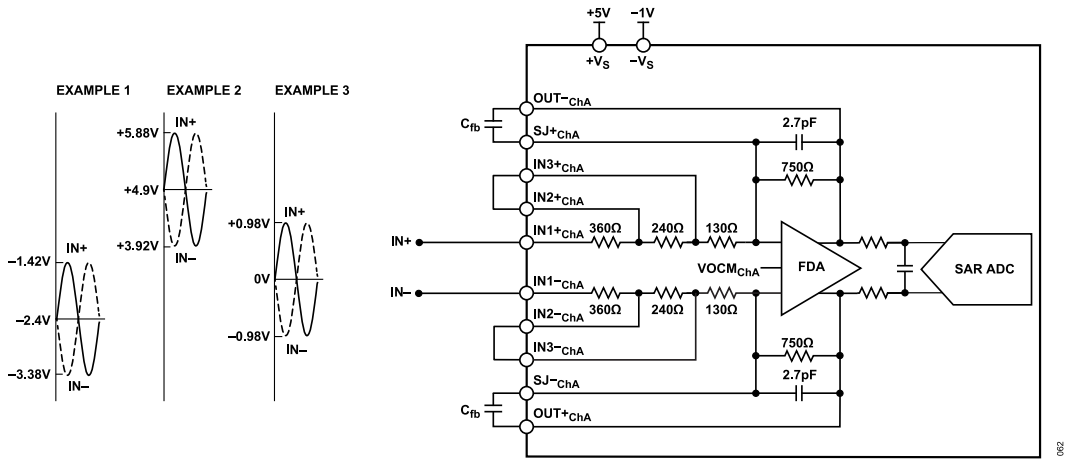


Figure 63. AD4885 Differential Input Configuration with Gain = 1.53, ±1.96V Input Range

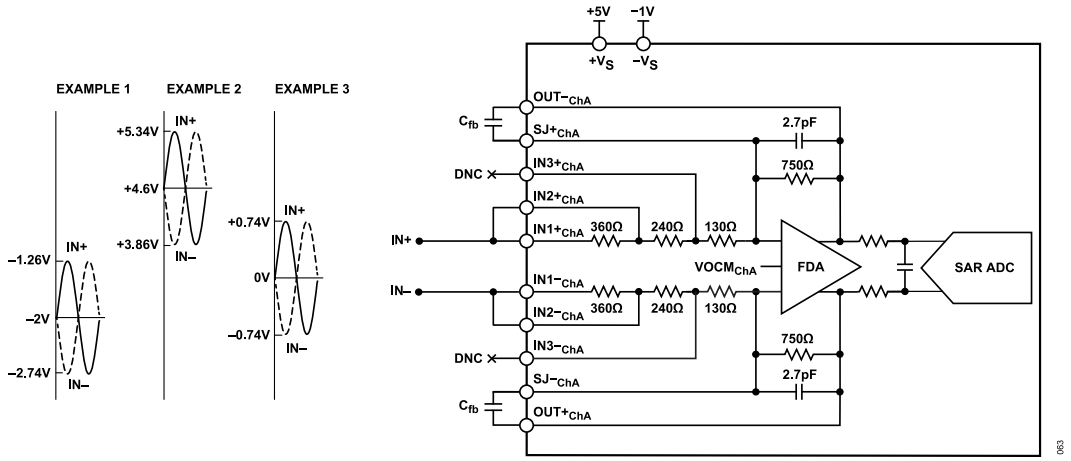


Figure 64. AD4885 Differential Input Configuration with Gain = 2.03, ±1.48V Input Range

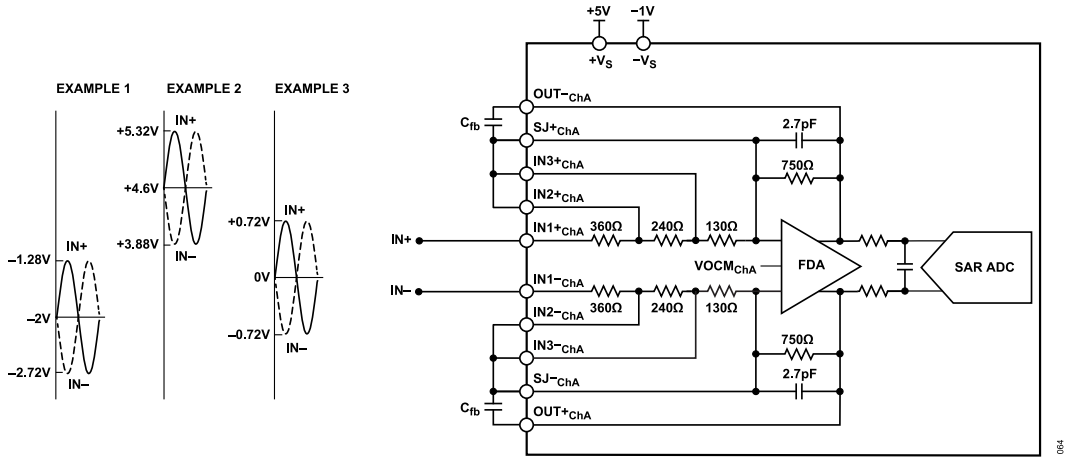


Figure 65. AD4885 Differential Input Configuration with Gain = 2.08, ±1.44V Input Range

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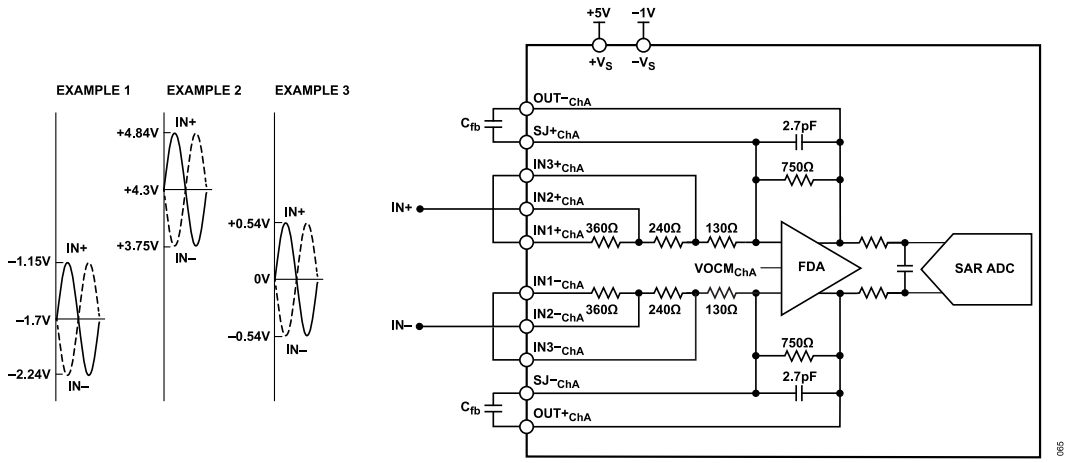

Figure 66. AD4885 Differential Input Configuration with Gain = 2.74, ±1.10V Input Range

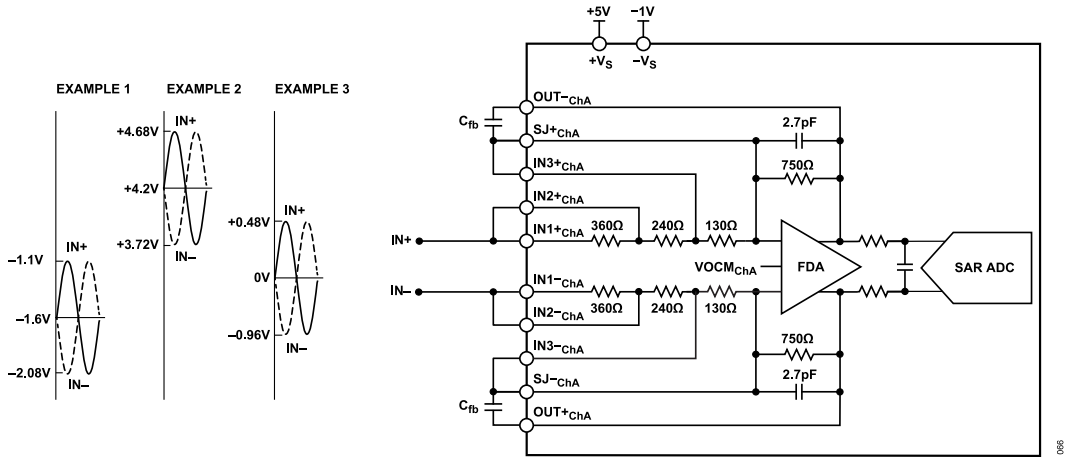

Figure 67. AD4885 Differential Input Configuration with Gain = 3.13, ±0.96V Input Range

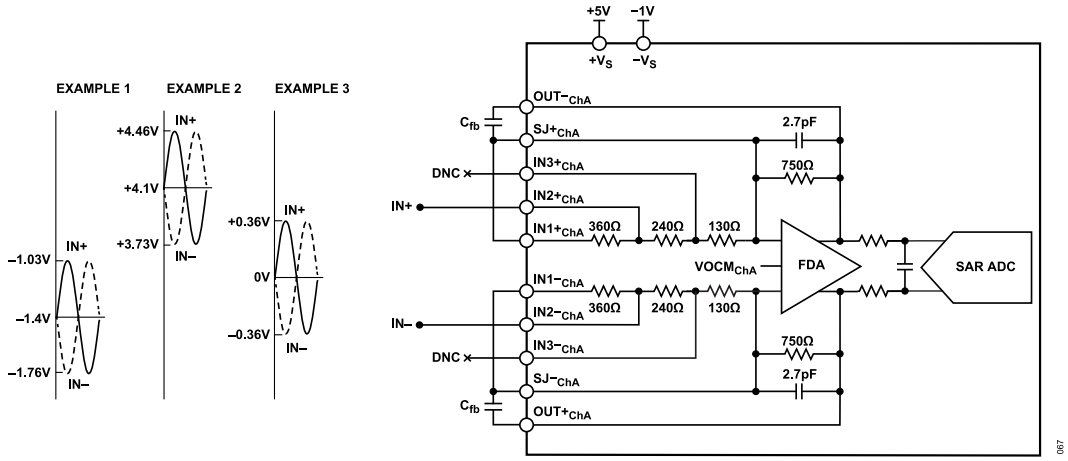

Figure 68. AD4885 Differential Input Configuration with Gain = 4.11, ±0.73V Input Range

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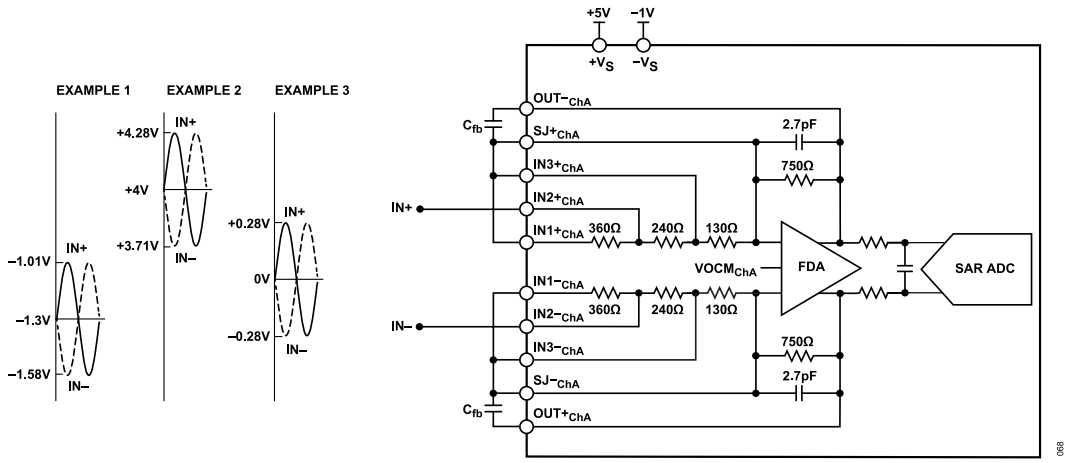

Figure 69. AD4885 Differential Input Configuration with Gain = 5.21, ±0.58V Input Range

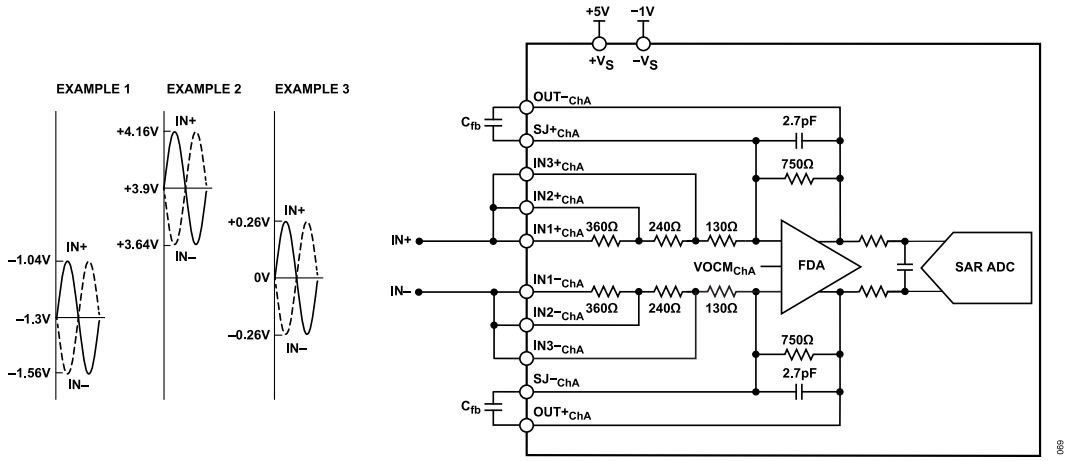

Figure 70. AD4885 Differential Input Configuration with Gain = 5.77, ±0.52V Input Range

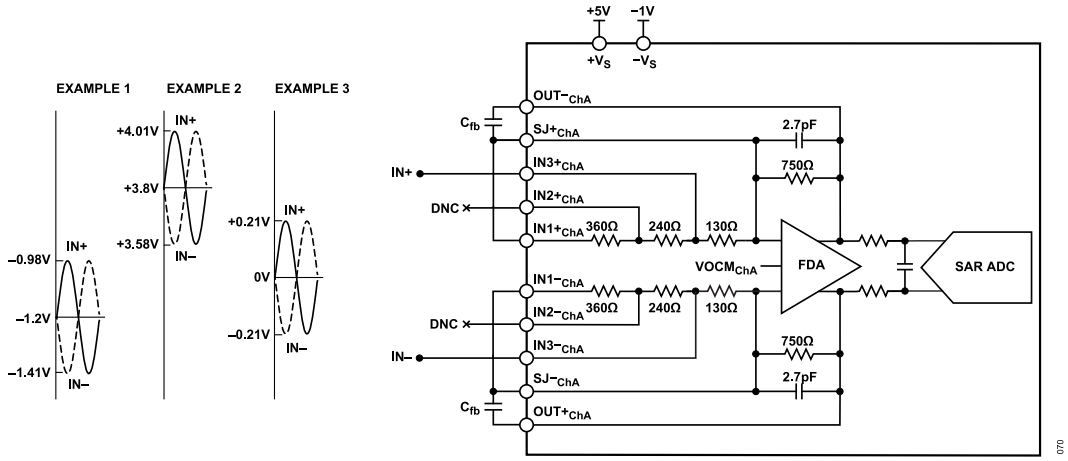

Figure 71. AD4885 Differential Input Configuration with Gain = 7.02, ±0.43V Input Range

APPLICATIONS INFORMATION

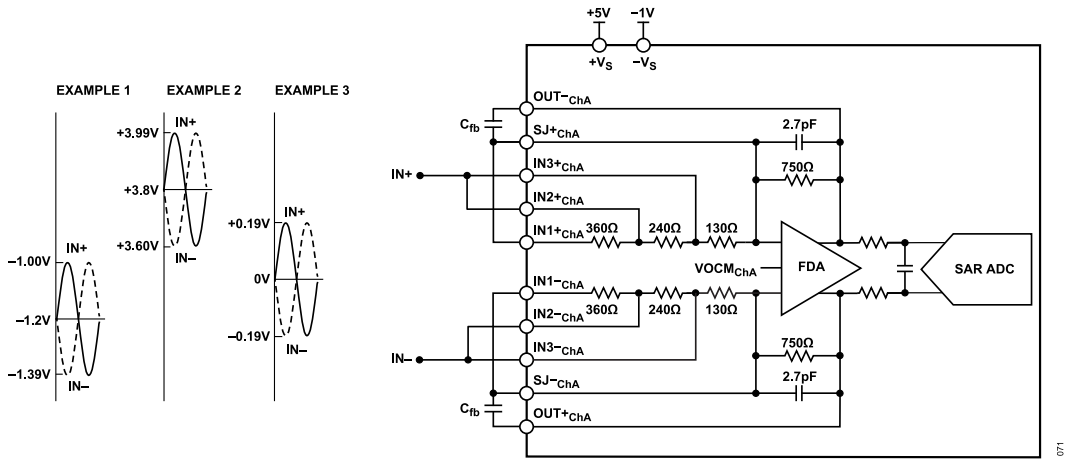

Figure 72. AD4885 Differential Input Configuration with Gain = 7.86, ±0.38V Input Range

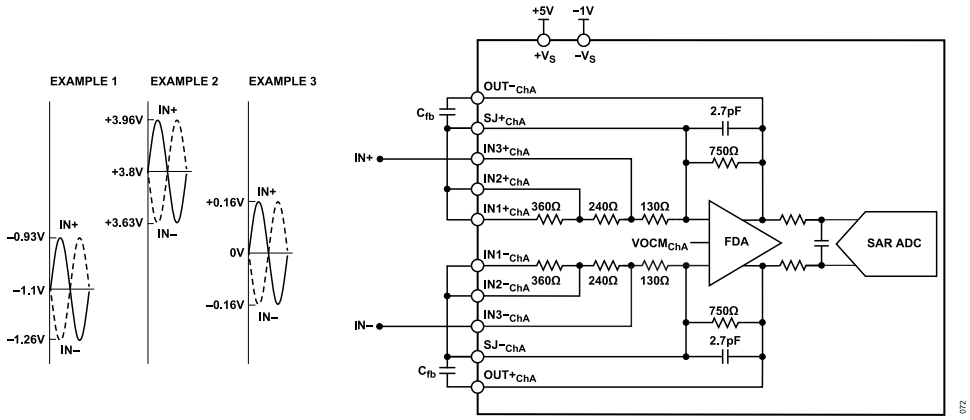

Figure 73. AD4885 Differential Input Configuration with Gain = 8.92, ±0.34V Input Range

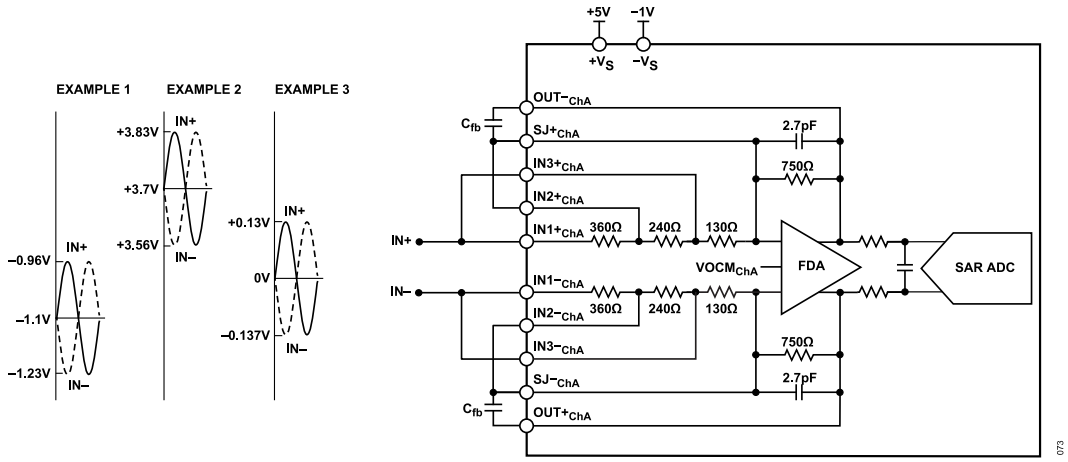

Figure 74. AD4885 Differential Input Configuration with Gain = 10.98, ±0.27V Input Range

APPLICATIONS INFORMATION

ANALOG INPUT FILTERING

The AD4885 is designed for converting signals in the first Nyquist zone ($f < f_S/2$). The highest level of AC performance (SNR, THD) is attainable up to around 1MHz, see Figure 33 and Figure 34. Adequately filtering the noise at the input of the FDA stage and the noise generated by the FDA itself is required for maximizing SNR in an application. Using full FDA bandwidth (or minimal bandwidth restriction) is typically adequate for applications with a multiplexed input that requires fast settling.

FDA bandwidth restriction for noise filtering is done by adding external capacitors to the FDA feedback network, in parallel with the internal 2.7pF ones, that is, across $SJ+_{ChX}$ and $OUT-_{ChX}$ and $SJ-_{ChX}$ and $OUT+_{ChX}$. The use of high-quality, precision NP0 capacitors is recommended. The capacitors must be placed as close as possible to the AD4885 connection points to minimize trace inductance. A value of 220pF provides optimum noise filtering for signals <1MHz. Table 12 shows estimated dynamic range and 3dB bandwidth for different values of the external feedback capacitors.

The FDA configuration for a gain of 1.03 leaves two accessible midpoints in the effective gain setting resistance at the input of the FDA (R_G in Figure 59). This allows increasing the filtering order of the FDA stage with minimal additional components by placing capacitors across these midpoints. Figure 75 and Figure 76 show the arrangement for the creation of an overall 2nd order response in the FDA stage, while Figure 77 depicts a 3rd order response circuit. Gain settings of 1.25, 1.53, 2.03, and 2.74 leave a single accessible midpoint, which allows an increase to the FDA response to 2nd order with just one additional capacitor. Note that this addition of capacitors in the input network of the FDA can result in effective amplification of the noise of the FDA itself, therefore the net effect of increasing filter order at this stage must be carefully analyzed for the specific conditions of the application. A model of the AD4885 is available in LTspice to support simulation-based analysis and refinement of the input filter design.

Table 12. Estimated Effect of External FDA Feedback Capacitors on Bandwidth and Dynamic Range, G = 1.03 Setting

C_{fb} External Capacitor Value (pF)	3dB Bandwidth (MHz)	Dynamic Range (dB)
220	0.95	91.9
180	1.16	91.7
120	1.72	91.7
56	3.55	91.5
22	8.13	91
10	14.67	90.5
0 (no capacitor)	39.33	88.3

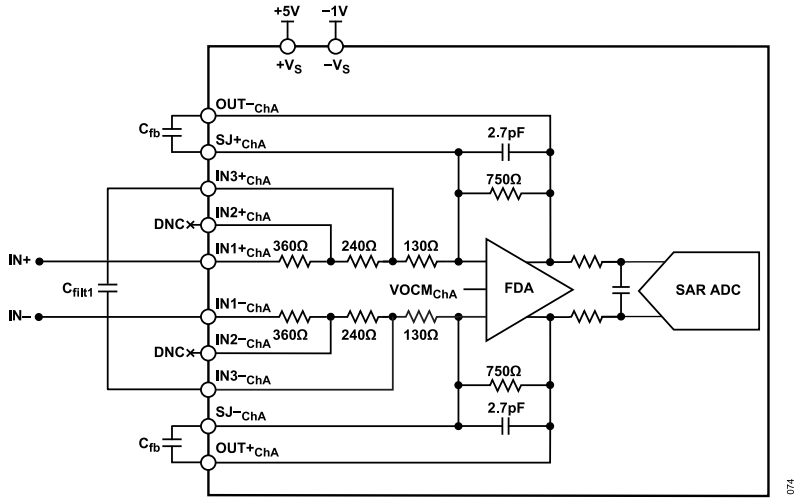

Figure 75. AD4885 FDA Stage, G = 1.03, One Additional Capacitor for 2nd Order Response, Option 1

APPLICATIONS INFORMATION

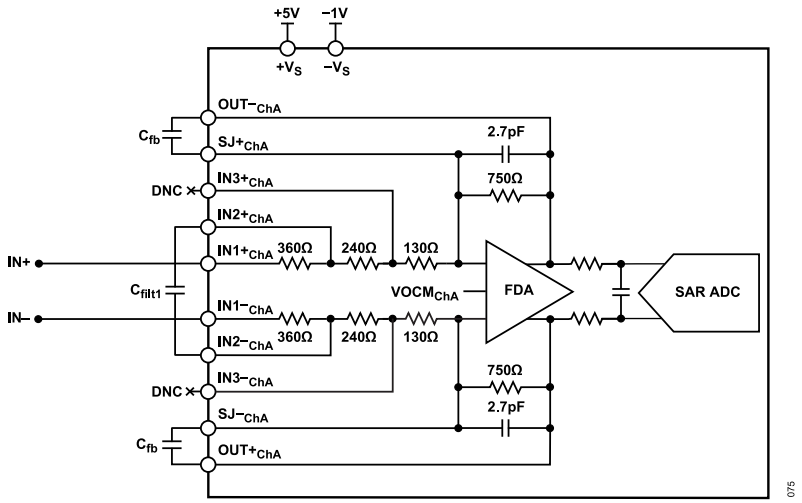

Figure 76. AD4885 FDA Stage, G = 1.03, One Additional Capacitor for 2nd Order Response, Option 2

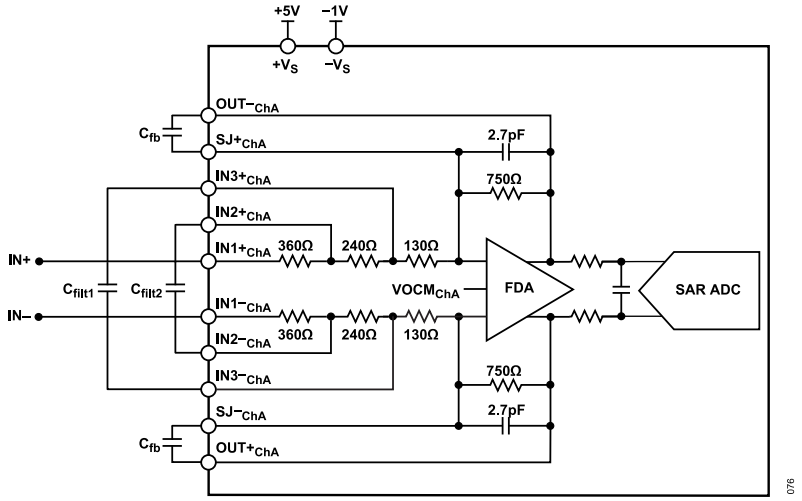

Figure 77. AD4885 FDA Stage, G = 1.03, Two Additional Capacitors for 3rd Order Response

APPLICATIONS INFORMATION

TYPICAL APPLICATIONS DIAGRAMS

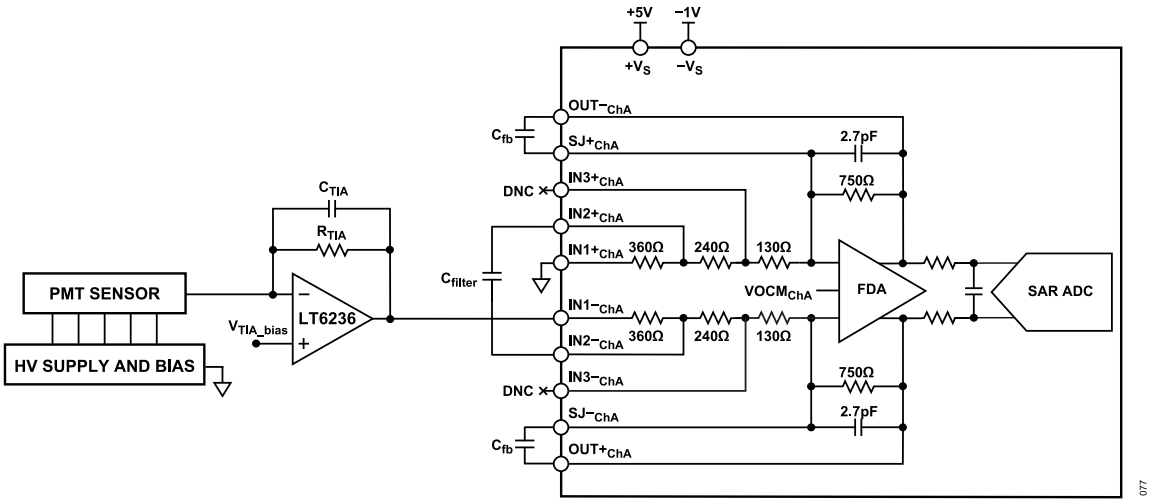

Figure 78. Typical Diagram for Data Acquisition from a Photomultiplier Tube (PMT) Sensor with Low-Gain TIA

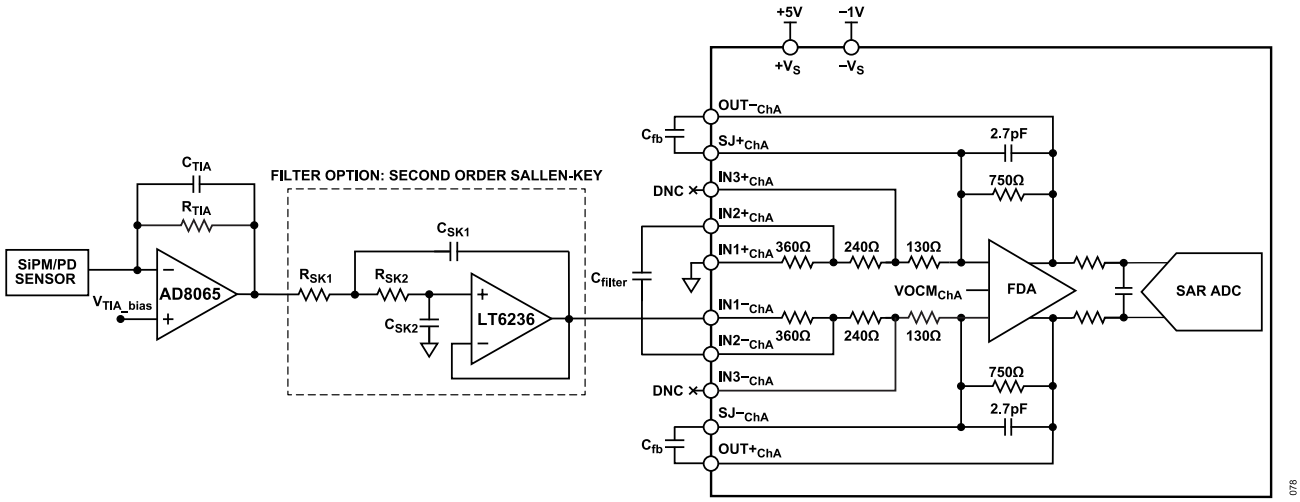

Figure 79. Typical Diagram for Data Acquisition from Photodiode (PD) or Silicon Photomultiplier (SiPM) Sensor with High-Gain TIA

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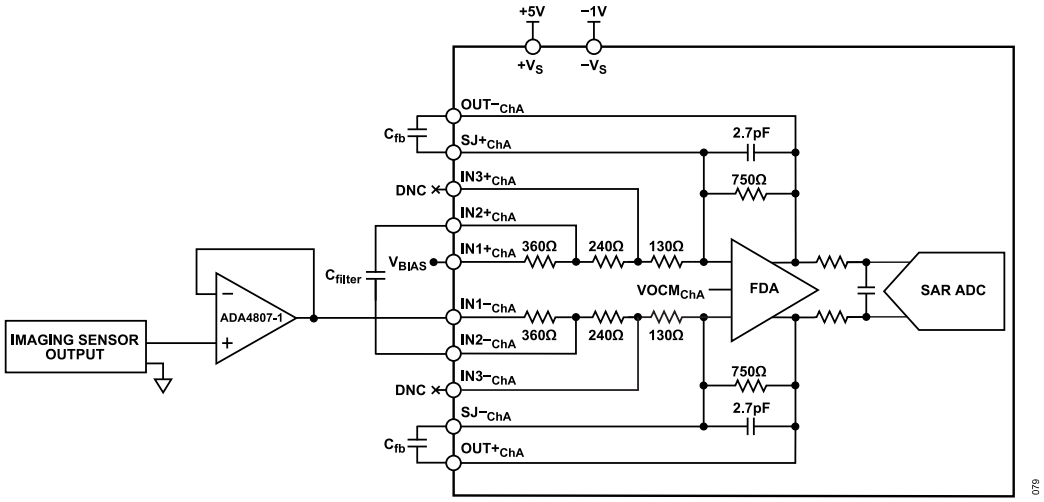

Figure 80. Typical Diagram for Imaging Sensor Readout at Low-Power

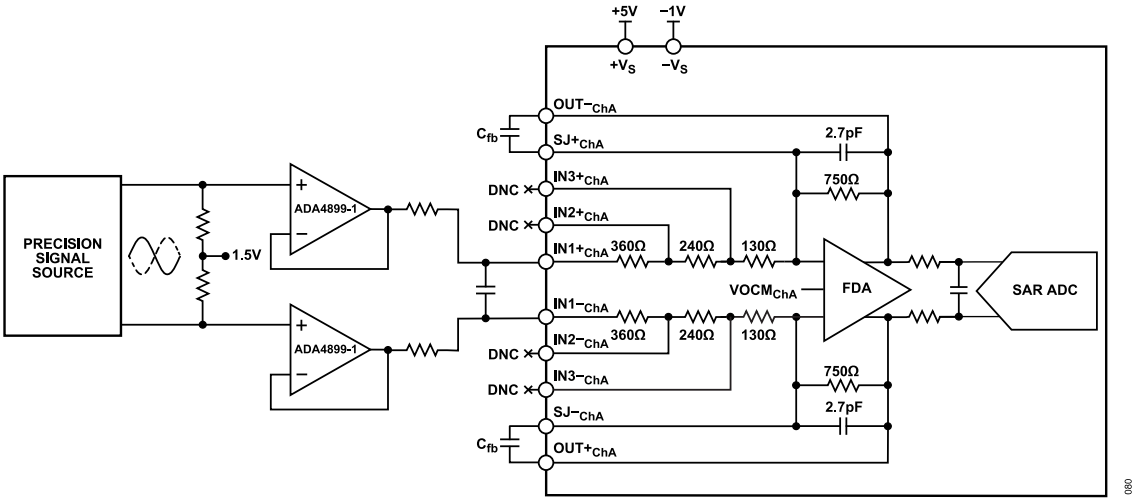

Figure 81. Typical Diagram for Minimum Distortion Laboratory Measurement

APPLICATIONS INFORMATION

REFERENCE CIRCUITRY DESIGN

The AD4885 requires a low noise, high precision and stability, and low temperature drift external reference of 3V. The internal buffers allow the same reference to be used for both channels. This reference defines a differential input range at the input of the SAR ADCs of $\pm V_{REFIN}$. The reference must be within ±5mV of +3V. Recommended references are the LTC6655, LT6657, or ADR4530. For best performance, however, use the LTC6655 external reference. Table 13 details the typical parameters of the previously mentioned references, comparing absolute accuracy, noise, temperature drift, load regulation, and power consumption. For more detailed specifications, refer to the data sheet of the given product.

Table 13. Comparison of the Main Parameters of the LTC6655, LT6657, and ADR4530 References

Parameter	LTC6655	LT6657	ADR4530B
Accuracy	0.025%	0.1%	0.02%
Temperature Coefficient (ppm/°C)	2	1.5	2
0.1Hz to 10Hz Noise (ppm p-p)	0.25	0.5	0.53
Maximum Load (mA)	±5	±10	±10
Load Regulation (ppm/mA)	3	0.7	30
Maximum Supply (V)	13.2	40	15
Shutdown	Yes	Yes	No
Supply Current, I_S (mA)	5	1.2	0.7

There is no need for the external reference capacitor because the AD4885 embeds internally a total of 18.8µF at the REFIN pin (9.4µF per channel, see Figure 82). The REFIN reference input pin is internally buffered, which substantially reduces ADC conversion transients and isolates the external reference from these transients. Therefore, no external amplifier is required to buffer the external reference. For the reference input capacitance (C_{REFIN}) and reference output capacitance (C_{REFOUT}) values, refer to the given external reference IC data sheet recommendations. As a layout recommendation, the external reference chip must be placed as close as possible to the AD4885 and its REFIN pin to minimize the series impedance of the track connecting the REFIN pin to the external reference output. It is recommended to minimize the exposure of this track to noisy signals, especially digital ones.

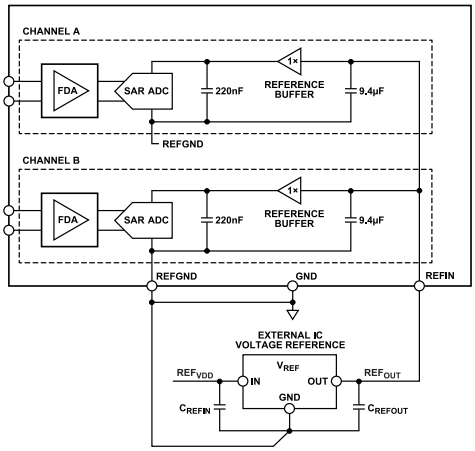

Figure 82. AD4885 General External Reference Design Functional Diagram

DATA INTERFACE CLOCKING SOLUTION

Each AD4885 channel has its own independent LVDS data interface. When designing the LVDS data interfaces (see the LVDS Data Interface section), the user must ensure the clocking solution adheres to the timing specifications of the AD4885 (see Table 2). When configured for LVDS mode data interface, the user must ensure that timing specifications stay within the maximum conversion to clock alignment time of ±535ps (t_{CCA}). In addition, ensure that a low jitter conversion (CNV) clock is provided such that there is no unwanted impact to SNR performance. This jitter is signal frequency dependent, therefore, the level of jitter tolerable in a given system is dependent on the application use case. For more details on this topic, refer to the technical article *Maximum SNR vs Clock Jitter*.

As an example, Figure 83 shows a recommended clocking solution where both AD4885 channels are configured to use the LVDS data interface with a single lane enabled and using echo clock mode. In this solution, a 25MHz oscillator is selected with low phase noise and jitter. The tutorial MT-008 serves as an aid to convert between phase noise and RMS phase jitter, often quoted interchangeably in crystal oscillator product data sheets. The ADF4350 wideband synthesizer with an integrated voltage-controlled oscillator (VCO) serves as versatile means of generating a 80MHz system clock, while maintaining low jitter and offering flexibility and control to reconfigure this frequency depending on the application needs. This clock then feeds the AD9508 clock fanout buffer with output dividers, that can be configured for the desired LVDS level signaling. As shown in Figure 83, two output channels are set to divide by 1 to generate the LVDS clocks ($CLK\pm_{ChA}$, $CLK\pm_{ChB}$), while two other output channels are configured to divide by 8, to generate the AD4885 conversion clocks ($CNV\pm_{ChA}$, $CNV\pm_{ChB}$). This 1:8 ratio of CNV:CLK frequencies ensures 16 bits of data can be read out over the double data rate (DDR), single lane, LVDS data interface. For a dual lane configuration, such as shown in Figure 84, this ratio is adjusted to 1:4.

The example shows echo clock mode being used, which aids in data alignment for the host controller (in the case a field-pro-

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grammable gate array (FPGA)). When both channels are clocked simultaneously, it is also feasible to use a single DCO±$_{ChX}$ pair to synchronize the two data interfaces. In self clock mode, where DCO±$_{ChX}$ are not available for alignment, the ADC Result Latency and LVDS Interface Alignment section describes how the INTF_CHK_EN bit (Address 0x15, Bit 4) can be enabled to help align the host controller to data and to mitigate against any system propagation delays.

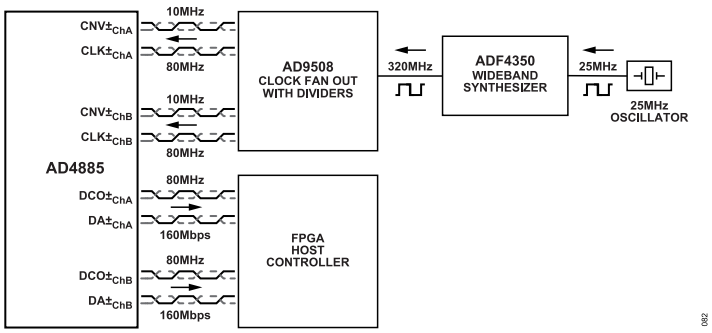

Figure 83. Single Lane, LVDS Data Interface Clocking Example

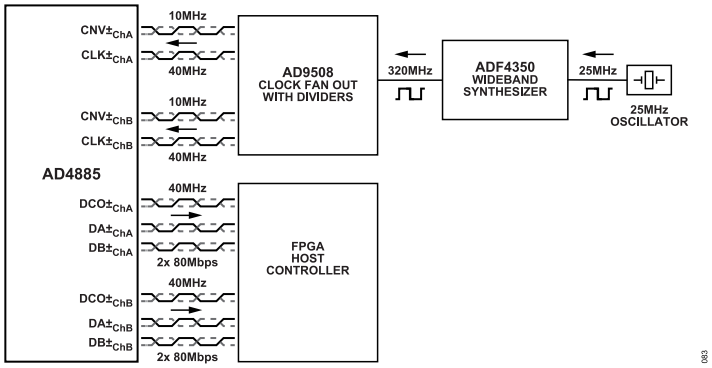

Figure 84. Dual Lane, LVDS Data Interface Clocking Example

When the SPI data interface (see the SPI Data Interface section) is used to access conversion results from the result FIFO (see the Result FIFO section) again, it is important that the CNV±$_{ChX}$ source jitter is carefully considered to achieve the required performance. In the case shown in the SPI data interface clocking example (see Figure 85), an oscillator directly provides the conversion clock to both channels, and the data is asynchronously clocked from the FIFO by a microcontroller unit (MCU). Optionally, as shown in Figure 85, the general-purpose input and output pins can be configured to control the result FIFO operation (see the GPIO Pins section and the Result FIFO section).

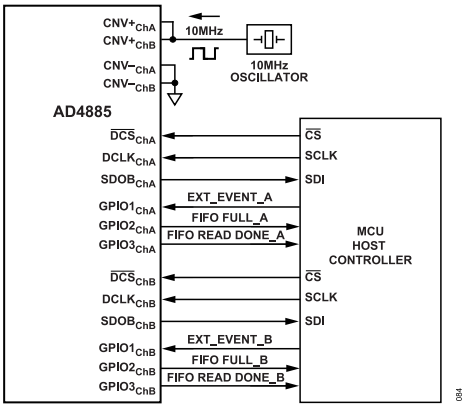

Figure 85. SPI Data Interface Clocking Example, x2 SPI Ports

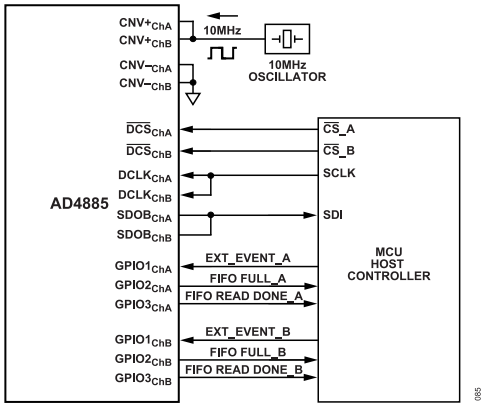

Figure 86. SPI Data Interface Clocking Example, Shared SPI Bus

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POWER SOLUTION

With such low noise and up to a 10MHz sampling rate, it is important that careful consideration is taken for the power solution of applications to ensure that the low noise supplies provided to the AD4885 do not become a source of performance or accuracy degradation. To aid ease of use and to help reduce external required components, four internal LDO regulators are integrated within the AD4885. For more details on these regulators, see the Internally Regulated Supply Configuration section. Also, note that the internal supply decoupling capacitors are included for all supply rails (see Table 8), whether generated internally or externally, reducing external component count, simplifying use, and offering huge benefits to PCB layout, routing, and design density.

For generating the required supplies in the application, excellent choice LDO regulators are the LT3045 or ADP150 for positive rails, while the ADP7182 or ADP7183 can be used to create a negative rail for $-V_S$, all of them offer ultra-low noise and excellent power supply rejection. For high efficiency, step-down switching regulators, the LT8604C is a good choice that can be used for both positive and negative rail generation, however, a user must take care in the design of the switching regulator circuitry because switching frequencies are possibly to be within the application signal bandwidth, and although the AD4885 has high AC power supply rejection on its supplies, appropriate consideration must be given to the supply rails.

The AD4885 is fully specified with the nominal FDA supply voltages of $+V_S$ = +5V and $-V_S$ = −1V, which allow reaching optimum performance at very low-power consumption. The voltage span across $\pm V_S$ can be increased up to the specified maximum of 10V, with a penalty paid in the form of increased power consumption. This enables the reuse of an existing quiet rail in the system (for example, a −5V rail for $-V_S$) if convenient. Conversely, the FDA supply span can be lowered down to a minimum of 3V for the absolute minimum power consumption, but performance degradation must be expected as FDA supply span decreases (see Figure 7) because the full ADC input range cannot be exercised at the specified distortion levels.

DIGITAL INTERFACE

OVERVIEW

The system-in-package construction of AD4885, with two separate ADC die, results in a fully-independent digital interface for each channel. Each digital interface consists of a 4-wire SPI for device configuration, four general-purpose input and output (GPIO) pins, a conversion data access interface with selectable output format (LVDS or SPI data interface), and a conversion start input ($CNV+_{ChX}$ and $CNV-_{ChX}$) that can be configured for LVDS or CMOS level signaling.

Register Interface

Each AD4885 channel has its own separate configuration memory. The configuration registers of each channel are accessed through the corresponding SPI configuration interface (see the SPI Configuration Interface section).

ADC Conversion Control

The ADC conversions of each AD4885 channel can be independently controlled. Each ADC acquires a sample and initiates a conversion operation on the rising edge of a convert start signal, applied at its $CNV+_{ChX}$ and $CNV-_{ChX}$ pins. Due to both channels being identical, AD4885 is also apt for simultaneous sampling applications (see the examples in Data Interface Clocking Solution section).

The input stages of the ADCs inside AD4885 cannot stay indefinitely in acquisition mode. This means that there is a minimum sampling frequency that must be exercised (see Timing Specifications), and that the first two samples acquired after power up or after a sleep or standby period are not guaranteed to be correct, and hence must be discarded.

There are two possible configurations for the electrical signaling at the convert start input pins $CNV\pm_{ChX}$: CMOS or LVDS. CMOS is the default mode on power up and after reset. CMOS requires that the $CNV-_{ChX}$ pin be connected to the digital interface ground (IOGND). In this mode, the convert signal must be a CMOS logic signal referenced to IOGND and applied at $CNV+_{ChX}$, with logic levels according to the digital inputs (CNV_{ChX}, $GPIOx_{ChX}$, $\overline{DCS}_{ChX}$, and $DCLK_{ChX}$) parameters in Table 1.

To switch a channel to LVDS mode, the LVDS_CNV_EN bit of its ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16) must be set to 1. In this mode, an external 100Ω termination resistor must be installed between the $CNV+_{ChX}$ and $CNV-_{ChX}$ pins, as close to the AD4885 as possible. In LVDS mode, the $CNV+_{ChX}$ and $CNV-_{ChX}$ pins must be driven differentially with an LVDS driver conforming to the levels specified in the LVDS I/O (EIA-644) parameters in Table 1. A user must take care to closely match the $CNV+_{ChX}$ and $CNV-_{ChX}$ differential signal pair routing and to use controlled impedance to ensure signal integrity. If the application aims at simultaneous sampling for both channels, proper fanning-out of the common conversion clock must be implemented, along with path length matching also between the $CNV\pm_{ChA}$ and $CNV\pm_{ChB}$ signal pairs.

ADC Conversion Data Interface

The ADC conversion data interface of each channel can be independently configured to one of the following signaling options:

- LVDS level signaling (LVDS data Interface)
- CMOS level signaling (SPI data interface)

The choice of interface is usually determined by the requirements and constraints of the application at hand. For example, if continuous fast data acquisition is required, then the LVDS signaling interface is typically the preferred option. If the application requires only noncontinuous bursts of data acquisitions, then either the LVDS or the SPI data interfaces can be used. The capabilities of the digital interface host can also determine which interface option is chosen.

Common to both the LVDS and SPI data interfaces are the following flexible features, which reduce the burden on the chosen digital host:

- Multilane data transfer: enables sustained data throughput at reduced interface clock speeds.
- Test pattern generation: facilitates interface integrity checks.

Additionally, for the LVDS only, there is the option to set a configurable output drive.

By default, the LVDS interface is selected on power up and after a reset. As shown in Figure 87, for LVDS, the data path of the ADC results is routed though the offset and gain correction block where there is the option to:

- Continuously read, directly, the raw ADC conversion results.
- Continuously read the ADC results processed by a user-selected digital filter (for more details, see the Digital Filter section).
- Read up to 16k unfiltered results from the channel FIFO.
- Read up to 16k digitally filtered results from the channel FIFO.

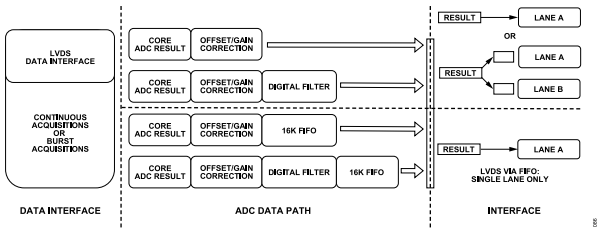

Figure 87. LVDS Data Interface Options (Shown for One Channel)

If configured for the SPI data interface, as shown in Figure 88, the available data paths are as follows:

- Read up to 16k unfiltered results from the channel FIFO.
- Read up to 16k digitally filtered results from the channel FIFO.

DIGITAL INTERFACE

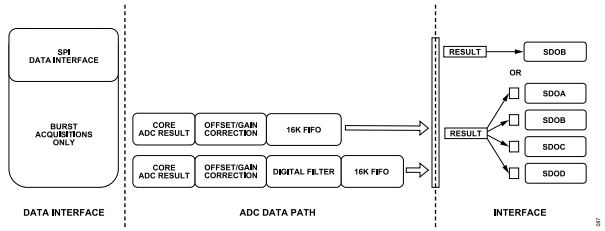

Figure 88. SPI Data Interface Data Path Options (Shown for One Channel)

Additional features specific to the selected interface format are also available and are described in the LVDS Data Interface and the SPI Data Interface sections.

SPI CONFIGURATION INTERFACE

All serial transactions between the system host and each AD4885 channel configuration registers are executed using their respective configuration SPI interfaces. Each serial transaction consists of at least one instruction phase during which the desired memory operation, that is, read or write, and the starting address for the transaction are transmitted to the AD4885 channel. The instruction phase is immediately followed by a data transaction phase during which one or more bytes of information is exchanged between the host and the AD4885 channel. This content is framed by a continuous assertion of the interface chip select ($\overline{CS}_{ChX}$) as shown in the generic timing presented in Figure 89 and Figure 90.

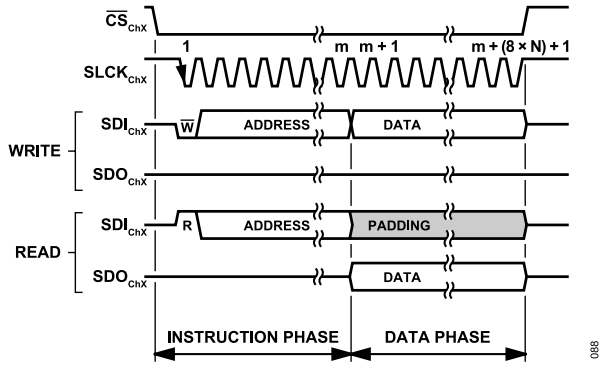

Figure 89. Generic SPI Configuration Frame, CRC Disabled

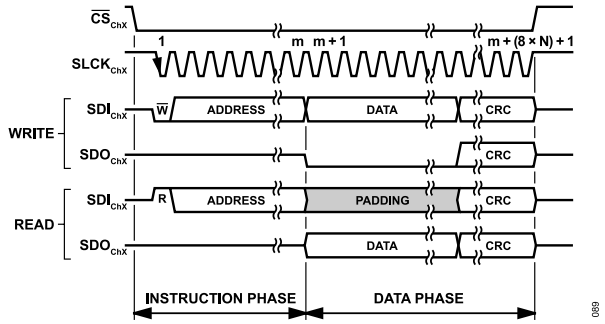

Figure 90. Generic SPI Configuration Write Operation, CRC Enabled

SPI Register Interface

Each AD4885 channel has its own independent configuration register interface in the form of an SPI that enables both configuration and status monitoring. Each interface is configured for 4-wire, full-duplex operation. Dedicated interface pins for the interface chip select ($\overline{CS}_{ChX}$), serial clock ($SCLK_{ChX}$), and serial data input (SDI_{ChX}) are intended for direct connection to the host controller. By default, at power-up or after a software reset, the configuration interface SDO function is enabled and assigned to the $GPIO0_{ChX}$ pin.

The configuration interface timing convention is consistent with SPI Mode 3 (clock polarity CPOL = 1, clock phase CPHA = 1). As such, the serial clock ($SCLK_{ChX}$) is expected to idle high and the state of the data pins, SDI_{ChX} and SDO_{ChX}, are updated on the falling (leading) edge of the clock such that these pins can be sampled on the subsequent rising (trailing) edge. For more details regarding the SPI and SPI modes, refer to the *Introduction to SPI Interface* article.

Each memory access controller associated with the SPI register interfaces supports a number of user-programmable options accessible through its respective interface configuration memory space (Address 0x00 to Address 0x11). The available options are listed and described in Table 14.

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Table 14. Configuration Memory Controller Options Summary

Interface Option	Description
Software Reset (SW_RESET, SW_RESETX)	Resets the internal configuration memory of the channel to the default state (except for ADDR_ASCENSION bit). The channel data FIFO is unaffected. Only use this reset method once the ADC is in an idle state, where conversions are not clocked, and any existing conversion is completed. For more details, see the Software Reset section.
Address Ascension (ADDR_ASCENSION)	Selecting this option changes the behavior of the memory controller address counter from decrementing (default) to incrementing. This change affects multibyte transfers, for example, when accessing a multibyte register as a single entity or when streaming mode is enabled. The selection impacts the starting address for multibyte register accesses in strict register access mode. For more details, see the Address Ascension Selection section.
Short Instruction (SHORT_INSTRUCTION)	Selecting this option reduces the length of the address field in the instruction word from 15 bits to 7 bits.
Single Instruction (SINGLE_INST)	Selecting this option changes from the default streaming mode to single instruction mode, which requires the host controller to transmit an instruction for each register access within a given SPI frame. The size of an entity is dependent on the strict register access setting and whether or not the register is multibyte. This feature allows random access to the memory space during configuration. For more details, see the Instruction Mode Selection section.
Strict Register Access (STRICT_REGISTER_ACCESS)	Selecting this option instructs the memory controller to treat a multibyte register as a single entity, generating a fault when a partial access is attempted. For more details, see the Strict Access Selection and Multibyte Registers section.
CRC Enable (CRC_ENABLE, CRC_ENABLEB)	Selecting this option enables a cyclic redundancy check (CRC) to verify the integrity of data sent to and received from the host. For more details, see the Configuration Cyclical Redundancy Check (CRC) section.
Status Data Transmission (SEND_STATUS)	Selecting this option enables the transmission of status data through the SDO_{ChX} line during the instruction phase of the data frame. For more details, see the Status Data Transmission section.
Loop Count (LOOP_COUNT)	Sets the data byte count before looping to the start address. When streaming data, a nonzero value sets the number of data bytes written before the address loops back to the start address. A maximum of 255 bytes can be written using this approach. A value of 0x00 disables the loop back so that addressing wraps around at the upper and lower limits of the memory. After writing this register, the loop value applies only to the following SPI instruction and auto clears upon the end of that instruction.

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Instruction Phase

An instruction phase immediately follows the assertion of the $\overline{CS}_{ChX}$ pin (Logic 0) and is terminated by transmission of a complete instruction packet or deassertion of $\overline{CS}_{ChX}$. The instruction packet starts with a single command bit indicating the operation type (Logic 1 for read and Logic 0 for write) that is then followed by the start address for the operation. By default, the address is 15-bit long, but the data interface has an optional short instruction mode in which it is reduced to 7 bits. The short instruction mode is enabled by setting the SHORT_INSTRUCTION bit = 1 in the Interface Configuration B register (see the Interface Configuration B Register section, Address 0x01).

Data Phase

Each instruction phase is immediately followed by an associated data phase, during which data is either shifted out of the serial data output (SDO_{ChX}) on the falling edge of $SCLK_{ChX}$ (read access) or is shifted into the device configuration memory through SDI_{ChX} on the rising edge of $SCLK_{ChX}$ (write access). The minimum size of the data payload is defined as a single byte, however, it can include multiple bytes depending on the depth of the register addressed and the interface configuration settings for the SINGLE_INST and STRICT_REGISTER_ACCESS bits (Register 0x01, Bit 7, and Register 0x10, Bit 5, respectively).

Write Access

When $\overline{CS}_{ChX}$ is forced low, a new serial instruction phase begins. The first bit sent in the instruction phase is the command bit, and when it is forced low (Logic 0) this indicates a write operation. The command bit is followed by an address that, for the write operation, indicates where the information received in the subsequent data phase is stored. As previously described in the Instruction Phase section, the address has a default length of 15 bits, but the address can be optionally shortened to 7 bits.

Following the instruction phase, an integer number of bytes containing the data payload for one or more registers in the configuration memory are transmitted to the AD4885 channel. The size of the payload in this data phase is bounded by the selected SINGLE_INST and STRICT_REGISTER_ACCESS interface options as described in the Strict Access Selection and Multibyte Registers section. Each data byte is loaded into the addressed register as it is received, assuming the interface CRC is disabled. If the CRC is enabled, however, the addressed data register is only loaded if the internally computed checksum matches the CRC value received from the host. In the event that the computed CRC and received checksum from the host for a given entity are inconsistent, the register update terminates and all subsequent data in the given frame is treated as invalid as well. The checksum computation for the interface CRC function is described in detail in the Configuration Cyclical Redundancy Check (CRC) section.

Note that during the data phase of a write operation, the SDO_{ChX} output is driven to Logic 0 when the product is not reporting the latest CRC checksum to ensure a valid data state is presented to the host controllers SDI pin.

Read Access

The SPI enables read access to the configuration registers to validate previous configuration writes, read the device identification, or verify the interface status.

When $\overline{CS}_{ChX}$ is forced low, a new serial instruction phase begins. The first bit sent in the instruction phase is the command bit, and when it is forced high (Logic 1) this indicates a read operation. The command bit is followed by an address that, for the read operation, indicates the start address for the register space to be accessed. As previously described in the Instruction Phase section, the address has a default length of 15 bits, but the address can be optionally shortened to 7 bits.

During the subsequent data phase, content from the addressed register space is shifted out, MSB first, on the SDO_{ChX} line on the falling edge of $SCLK_{ChX}$. The number of bytes transmitted in any one data frame is determined by the interface configuration setting selections for the SHORT_INSTRUCTION and STRICT_REGISTER_ACCESS options as demonstrated in the examples shown in the Instruction Mode Selection and the Strict Access Selection and Multibyte Registers sections.

Instruction Mode Selection

The configuration interface memory controller defaults to streaming mode upon power up (SINGLE_INST = 0). In streaming mode, multiple, contiguous registers are accessed in a single SPI frame, starting at the address specified in the instruction phase. In streaming mode, only one instruction phase is permitted per SPI frame, requiring a new SPI frame be initiated for changing access commands or otherwise access a noncontiguous address in the register space. For each byte transferred during the subsequent data phase, the internal address counter is automatically updated according to the setting of the ADDR_ASCENSION bit in the Interface Configuration A register (see the Interface Configuration A Register section), in the way specified by Table 15.

Table 15. Address Ascension Selection

ADDR_ASCENSION Bit Value	Address Controller Behavior (STRICT_REGISTER_ACCESS = 1)
0 (Default)	Decrement Address. Multibyte registers are accessed by addressing the most significant byte address.
1	Increment Address. Multibyte registers are accessed by addressing the least significant byte address.

Figure 91 shows the generic SPI frame formatting for a serial transaction using the default interface configuration. In this example, a portion of the configuration register space consisting of a byte-wide register and a multibyte register is accessed. The address for the byte-wide register resides in the most significant address (ADDRESS) and the most significant byte of the multibyte register resides in the least significant address of the register segment. By default, the ADDR_ASCENSION property is set to descending, indi-

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cating that the address for the most significant register is passed to the host controller during the instruction phase. Depending on the selected operation, the instruction word is followed by either a payload consisting of data for the byte-wide register (DATA), least significant bytes (LSBYTE), and most significant bytes (MSBYTE) of the multibyte register, or, in the case of a read access, padding bits. As a convention, it is recommended to pass Logic 1 to SDI during a read access to avoid accidentally addressing address zero for write access.

In single instruction mode (SINGLE_INST = 1), the memory access controller requires an instruction phase to transmit for each register accessed in a given SPI frame, as shown in Figure 92. This mode is useful when access to nonadjacent sections of the register space is required in a given SPI frame. Note that, the same access flexibility can be achieved in stream mode by initiating a new SPI frame for each unique register access.

The single instruction mode is selected by setting SINGLE_INST = 1 in the Interface Configuration B register (see the Interface Configuration B Register section, Address 0x01).

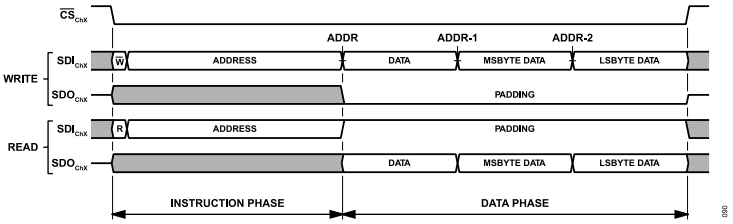

Figure 91. Interface Access Example, Default Interface Configuration, Streaming Mode (ADDR_ASCENSION = 0)

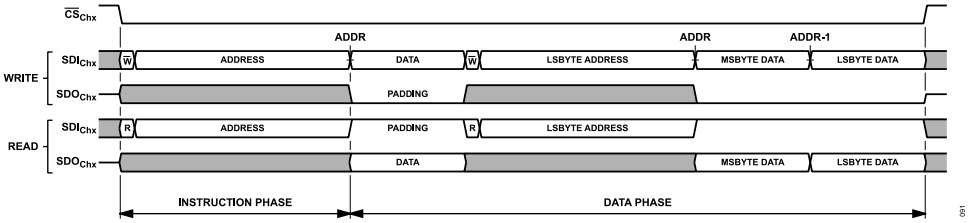

Figure 92. Interface Access Example, Single Instruction Mode (SINGLE_INST = 1), All Other Interface Options Default

DIGITAL INTERFACE

Address Ascension Selection

The address ascension selection (ADDR_ASCENSION) bit, as described in previous sections, determines how the internal interface address pointer is updated for each byte of data transmitted to the AD4885 channel in streaming mode (SINGLE_INST = 0). If using single instruction mode (SINGLE_INST = 1), each register is directly addressed through its own instruction phase, as shown in Figure 92, and thus, the address pointer is not updated. Regardless of the setting for SINGLE_INST, the ADDR_ASCENSION bit directly impacts the formatting of the SPI frame in terms of selection of the instruction phase starting address and byte order of the data phase payload. This impact is described in greater detail in the Strict Access Selection and Multibyte Registers section as much of the data formatting is dependent on this interface configuration selection. The ADDR_ASCENSION selection bit is located in the Interface Configuration A register (see the Interface Configuration A Register section, Address 0x00).

As summarized in Table 15, the ADDR_ASCENSION bit is cleared by default, resulting in the address pointer decrementing by one for each data byte transmitted. In this decrement configuration (ADDR_ASCENSION = 0), the address pointer decrements from the starting address indicated in the instruction phase by one for each data phase byte received until the counter reaches Address 0x0000. If additional bytes are received, the pointer automatically rolls over to the maximum address value, 0x7FFF, the rollover behavior is fixed, and therefore, independent of the SHORT_INSTRUCTION value or the physical address space occupied by the user configurable registers. It is important to understand this behavior to avoid generating interface errors associated with attempting to access one or more invalid register addresses. Limit register access to the register address space associated with the device configuration as described in the Configuration Registers section.

Alternatively, the ADDR_ASCENSION bit can be set (ADDR_ASCENSION = 1), resulting in the address pointer incrementing by one, starting at the address identified in the instruction word, for each data phase byte received at the AD4885 in a given SPI frame. In a manner similar to the descending case, the address counter continues to increment for each data byte received until the maximum address value, 0x7FFFF, is reached, after which the pointer rolls over to 0x0000.

Strict Access Selection and Multibyte Registers

Several locations in the configuration memories of the AD4885 channels have been assigned as multibyte registers to support the storage requirements. For example, the offset correct register (see the Offset Correction Register section, Address 0x25) and gain correction register (see the Gain Correction Register section, Address 0x27) are multibyte registers because the resolution of the correction coefficients they contain exceeds a single byte. For a complete listing of multibyte registers, see the Configuration Registers section. The length of each register, in bytes, is captured in Table 31 in addition to other characteristic information.

The function of the STRICT_REGISTER_ACCESS bit is to indicate to the interface controller that all bytes of a multibyte register must be accessed in the current frame for valid communication to have occurred. In the event a multibyte register is only partially accessed, an interface fault is generated in the Interface Status A register (see the Interface Status A Register section, Address 0x11), and the partial content update is discarded. The intent of this restriction is to ensure that corresponding configuration quantities are updated in a manner that produces the desired device operation. The access restriction function is enabled by default (STRICT_REGISTER_ACCESS = 1) and can be disabled by clearing the access bit (STRICT_REGISTER_ACCESS = 0) in the Interface Configuration C register (see the Interface Configuration C Register section, Address 0x10). With register access restriction disabled, each byte of the configuration memory can be independently addressed, however, it is then incumbent on the software to correctly configure any multibyte registers in the device memory to achieve the required behavior.

The decision to enable or disable the register access restriction has implications with regards to the correct construction of the SPI frames containing one or more multibyte register accesses. When STRICT_REGISTER_ACCESS is disabled, each byte of a multibyte register is treated as a singular element. Furthermore, the interface does not indicate a fault if all bytes of the register are not programmed, or if the bytes are programmed in a random order, and therefore, it is incumbent on the host to ensure that the content of those registers are updated in a manner that produces the required function in the device.

When STRICT_REGISTER_ACCESS is enabled, specific access rules are enforced to ensure consistency between the data and the expected behavior of the device. To understand how these rules apply to multibyte registers in the configuration memory, it is important to understand how the memory is organized. By convention, multibyte registers are arranged in the configuration memory such that the most significant byte of the register is stored in the most significant address of the assigned register space, as shown in Figure 93. As a result, the byte order of the register content transmitted in the data phase is dependent on the ADDR_ASCENSION selection.

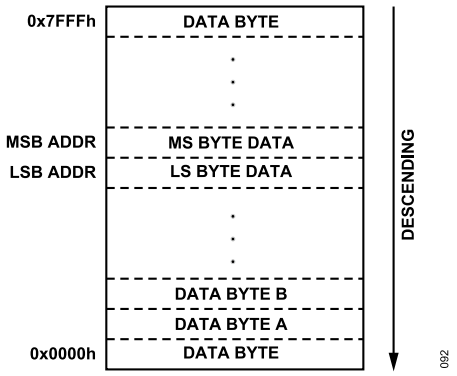

Figure 93. Generic Byte Wide Memory, Multibyte Register Example

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As shown in Figure 94, the address counter, by default, automatically decrements (ADDR_ASCENSION = 0) such that the most significant byte of the multibyte register is accessed first, followed by the remaining byte(s) in that register in ascending order. Conversely, if ADDR_ASCENSION = 1, the least significant byte of the multibyte register is accessed first followed by most significant byte.

As an extension of this concept, when STRICT_REGISTER_ACCESS = 1, any SPI frame that accesses a multibyte register as the first entity in the data transfer must correctly set the starting address in the instruction word to correspond to the ADDR_ASCENSION selection. In the case that the address counter automatically decrements (ADDR_ASCENSION = 0), the starting address is assigned to the register address for the most significant byte of that multibyte register, and conversely, if configured to increment automatically, the starting address must be set to the register address for the least significant byte. As a result of the change to ADDR_ASCENSION from automatic address decrement (0) to automatic increment (1), Figure 91 and Figure 92 change as shown in Figure 94 and Figure 95 to accommodate the changes in data phase byte order and instruction phase multibyte register start address.

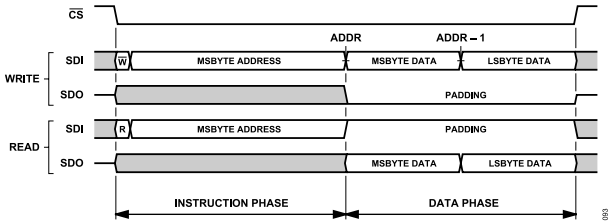

Figure 94. Single Instruction Format, ADDR_ASCENSION = 0 (Descend), STRICT_REGISTER_ACCESS = 1 (Enabled)

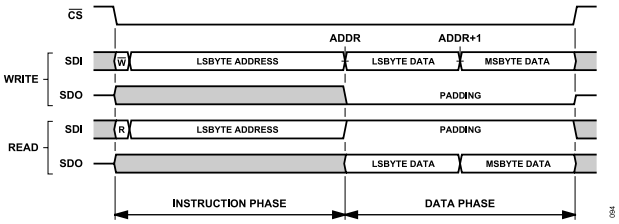

Figure 95. Single Instruction Format, ADDR_ASCENSION = 1 (Increment), STRICT_REGISTER_ACCESS = 1 (Enabled)

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Status Data Transmission

The Interface Status A register (see the Interface Status A Register section, Address 0x11) and device status register (see the Device Status Register section, Address 0x14) of each channel contain status data pertaining to the communications interface and the device itself, respectively. This data enables troubleshooting of device configuration during development and also provides continuous coverage of potential communication issues between the host and the interface once deployed. The SPI controller can access the data through regular register read operations. However, the channel can be configured to autonomously transmit status data through the SDO line every time while the SPI controller is sending the SPI instruction phase data over the SDI. This feature is controlled through the SEND_STATUS bit in the Interface Configuration C register (see the Interface Configuration C Register section, Address 0x10), and it is disabled by default. To enable this bit, set SEND_STATUS = 1. The status data that is sent is taken from the Interface Status A register and from the device status register, but the content is different depending on the setting of the SHORT_INSTRUCTION bit in the Interface Configuration B register (see the Interface Configuration B Register section. Note that the length of the instruction phase also depends on this setting. For a description of the status data sent in each case, where the status data is sent MSB first, see Table 16 and Table 17.

Table 16. Device Status Data Sent Through the SDO_{ChX} in Long Instruction Mode (SHORT_INSTRUCTION = 0)

Bit	Name	Description
15	Not applicable	Bit 15 is always 0.
14	Not applicable	Bit 14 is always 0.
13	FIFO_FULL	Device Status Register Bit 7: FIFO Full Status Flag. 0: FIFO Not Full. 1: FIFO Full.
12	FIFO_READ_DONE	Device Status Register Bit 6: FIFO Read Done Flag. 0: FIFO Read Not Done. 1: FIFO Read Done.
11	HI_STATUS	Device Status Register Bit 5: High Threshold Detection Status Flag. 0: High Threshold Event Not Detected. 1: High Threshold Event Detected.
10	LO_STATUS	Device Status Register Bit 4: Low Threshold Detection Status Flag. 0: Low Threshold Event Not Detected. 1: Low Threshold Event Detected.
9	ADC_CNV_ERR	Device Status Register Bit 2: ADC Conversion Error Flag. 0: ADC Conversion OK. 1: ADC Conversion Error. A. Conversion period is lower than minimum value for speed grade. B. DSP error.
8	ROM_CRC_ERR	Device Status Register Bit 1: Read Only Memory (ROM) CRC and/or Error Correction Code (ECC) Failure Flag. 0: ROM CRC Check OK. 1: ROM CRC and/or ECC Failure.
7	POR_ANA_FLAG	Device Status Register Bit 3: POR Analog Status. Allows user to detect when an analog POR event has occurred. An analog POR is triggered at power-up or when the logic supply drops to less than some threshold value, when the ADC reference drops to less than some threshold value, or when the user issues a software reset. 0: Analog POR Flag Cleared. 1: Analog POR Event Detected.
6	POR_FLAG	Device Status Register Bit 0: POR Status. Allows user to detect when a POR event has occurred. A POR is triggered at power-up or when the logic supply drops to less than some threshold value or when the user issues a software reset. 0: POR Flag Cleared. 1: POR Event Detected.
5	NOT_READY_ERR	Interface Status A Register Bit 7: Device Not Ready for Transaction. This bit is set if the user attempts to execute an SPI transaction before the completion of digital initialization.
4	CLOCK_COUNT_ERR	Interface Status A Register Bit 4: Clock Count Error. This bit is set when an incorrect number of clocks is detected in a transaction.
3	CRC_ERR	Interface Status A Register Bit 3: CRC Error. This bit is set when the SPI controller does not send a CRC value or when the CRC value calculated by the device does not match the value received from the SPI controller.

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Table 16. Device Status Data Sent Through the SDO_{ChX} in Long Instruction Mode (SHORT_INSTRUCTION = 0) (Continued)

Bit	Name	Description
2	WR_TO_RD_ONLY_REG_ERR	Interface Status A Register Bit 2: Write to Read Only Register Error. Write to Read Only Register Attempted. This bit is set when the user attempts a write to a register that is read-only.
1	REGISTER_PARTIAL_ ACCESS_ERR	Interface Status A Register Bit 1: Register Partial Access Error. This bit is set when a fewer than expected number of bytes are read from or written to in a multibyte register access. This bit is only valid when strict register access is enabled.
0	ADDRESS_INVALID_ERR	Interface Status A Register Bit 0: Invalid Address Error. Attempt to read or write nonexistent register address. This bit is set when the user tries to access register addresses outside the allowed memory map space.

Table 17. Device Status Data Sent Through the SDO_{ChX} in Short Instruction Mode (SHORT_INSTRUCTION = 1)

Bit	Name	Description
7	Not applicable	Bit 7 is always 0.
6	POR_FLAG	Device Status Register Bit 0: POR Status. Allows user to detect when a POR event has occurred. A POR is triggered at power-up or when the logic supply drops to less than some threshold value or when the user issues a software reset. 0: POR Flag Cleared. 1: POR Event Detected.
5	NOT_READY_ERR	Interface Status A Register Bit 7: Device Not Ready For Transaction Error. This bit is set if the user attempts to execute an SPI transaction before the completion of digital initialization.
4	CLOCK_COUNT_ERR	Interface Status A Register Bit 4: Clock Count Error. This bit is set when an incorrect number of clocks is detected in a transaction.
3	CRC_ERR	Interface Status A Register Bit 3: CRC Error. This bit is set when the SPI controller does not send a CRC, or when the CRC value calculated by the device does not match the value sent by the SPI controller.
2	WR_TO_RD_ONLY_REG_ERR	Interface Status A Register Bit 2: Write To Read-only Register Error. This bit is set when the user attempts a write to a register that is read only.
1	REGISTER_PARTIAL_ ACCESS_ERR	Interface Status A Register Bit 1: Register Partial Access Error. This bit is set when a fewer than expected number of bytes are read from or written to in a multibyte register access. This bit is only valid when strict register access is enabled.
0	ADDRESS_INVALID_ERR	Interface Status A Register Bit 0: Invalid Address Error. This bit is set when the user tries to read from or write to a register address outside the allowed memory map space.

Configuration Cyclical Redundancy Check (CRC)

The AD4885 includes optional configuration error detection based on an 8-bit cyclical redundancy check algorithm. When enabled, an 8-bit checksum is inserted into the serial data output stream (SDO_{ChX}) during the data phase after each complete register transaction. Depending on the register access type, that is, read or write, the host is expected to conditionally provide a corresponding checksum to the SDI_{ChX} immediately following each register access. The interface controller uses the host supplied checksum to determine if a CRC error has occurred.

A mismatch in the checksum values computed by the host and the AD4885 interface results in setting the CRC_ERR flag (CRC_ERR = 1) in the Interface Status A register (see the Interface Status A Register section, Address 0x11). During a write access, a CRC error invalidates the most recent register data as well as any subsequent register data writes if in streaming mode (SINGLE_INST = 0), which prevents loading any potentially corrupted data into the configuration memory. In response to a CRC event, the host controller is required to initiate a new SPI frame to retry configuration of the affected memory locations. In the event the CRC_ERR is detected during a data read, the host controller must discard the received data and retry the data read in a new SPI frame. Clear the CRC_ERR flag before any attempt to initiate a repeated read or write to the configuration memory to allow detection of any subsequent errors. The error flag is cleared by writing code 0x08 to the Interface Status A register to set the CRC_ERR bit to a Logic 1. It is recommended that an immediate read of the Interface Status A register follows any attempt to clear the fault to validate the attempt is successful.

The configuration CRC function is disabled by default and can be enabled independently for each channel through two complementary bit fields, CRC_ENABLE and CRC_ENABLEB, in their corresponding Interface Configuration C registers (see the Interface Configuration C Register section, Address 0x10). To enable the CRC function, set the CRC_ENABLE bits to 1 and the CRC_ENABLEB bits to 10. Each of the complementary CRC bit fields is 2-bit wide, and any combination other than that specified results in the function remaining disabled. It is important to note that once the CRC function is enabled for an interface, a valid checksum from the host controller is required for all subsequent serial transactions through that interface according to the conditions described in Table 18. If used, enable and validate the CRC function before writing to any of the device configuration registers. To validate the CRC function is enabled, follow the CRC configuration write with a SPI frame

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consisting of a read of both the Interface Configuration C register and the Interface Status A register using a valid checksum for the read transaction. If enabled, the register contents for the CRC_ENABLE and CRC_ENABLEB bits must be 1 and 10, respectively, and the CRC_ERR bit in the Interface Status A register remains cleared (Logic 0). Once confirmed, proceed with programming the remaining configuration registers.

Table 18. Host Controller (SDI_{ChX}) Conditional Checksum Requirement Summary

Command	SINGLE_INST Bit Value	Checksum Requirement
Write	Streaming (0) or single instruction (1)	After each data register payload.
Read	Streaming (0)	After the first register data payload following the instruction phase.
	Single instruction (1)	After each data register payload.

The following CRC-8 polynomial is implemented in the AD4885 to compute the checksum for each register transaction:

$x^8 + x^2 + x + 1$

Each serial transaction is processed through this polynomial to generate the checksum on a per register basis. The data and seed values used for each checksum calculation are a function of the access command (read/write), ADDR_ASCENSION, STRICT_REGISTER_ACCESS, and SINGLE_INST settings, and the location of the register data in the data stream as summarized in Table 19.

All register write access operations, regardless of SINGLE_INST setting, require a valid CRC checksum to be sent from the host following the data payload for each register. For multibyte registers, if STRICT_REGISTER_ACCESS = 1, a valid CRC is appended to the data stream after all bytes of the addressed register are sent.

If STRICT_REGISTER_ACCESS is cleared (0), each byte transmitted must be followed by a valid checksum using the computation rules that are described as follows.

For read access, the computation and transmission of a valid checksum from the host is required to validate the command and starting address only. In streaming mode (SINGLE_INST = 0), a CRC checksum is sent from the host controller after the first register data payload only. Fill all subsequent register accesses in streaming mode with padding data. The AD4885 continues to produce valid checksum values after each register read to allow validation in the host using the preceding data. As a new instruction phase is required for each register accessed in single instruction mode, a valid host CRC checksum is required for each register accessed.

In single instruction mode (SINGLE_INST = 1), the polynomial is computed for each register using the default seed value of 0xA5, the instruction phase data, and depending on the access command, the desired register or padding data. In streaming mode (SINGLE_INST = 0), the checksum computation for the first register in the data stream is computed as if single instruction mode were selected. Each subsequent register access checksum computation is seeded with the starting address for the current register and the corresponding data. Note that the starting address for multibyte registers changes with the ADDR_ASCENSION selection, assuming the register access restriction is enabled (STRICT_REGISTER_ACCESS = 1). As previously described, the memory convention dictates that if ADDR_ASCENSION is set to 0, the address for the least significant byte of the multibyte register serves as the starting address. Conversely, if the ADDR_ASCENSION bit is set to 1, the address of the most significant byte of the multibyte register is used.

Table 19. Configuration CRC Checksum Source Data Summary vs. SINGLE_INST and SPI Command

Command	Checksum Source	Single Instruction Mode (SINGLE_INST = 1) or Streaming Mode First CRC		Streaming Mode (SINGLE_INST = 0) After First CRC	
		Data Source	Seed	Data Source	Seed
Write	Controller	Instruction and data	0xA5	Register data	Current start address
	AD4885	Instruction and data		Register data	Current start address
Read	Controller	Instruction and padding data	0xA5	Not required, send padding data	
	AD4885	Instruction and register content		Register data	Current start address

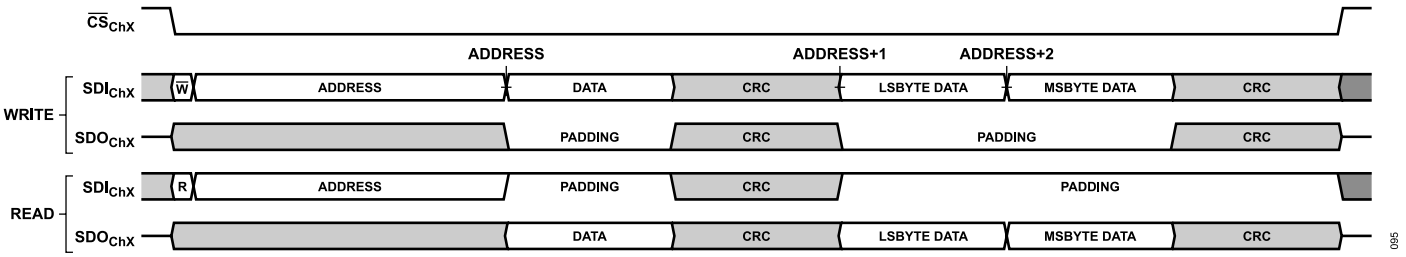

Figure 96. Streaming Mode Configuration with CRC Enabled, ADDR_ASCENSION = 1

DIGITAL INTERFACE

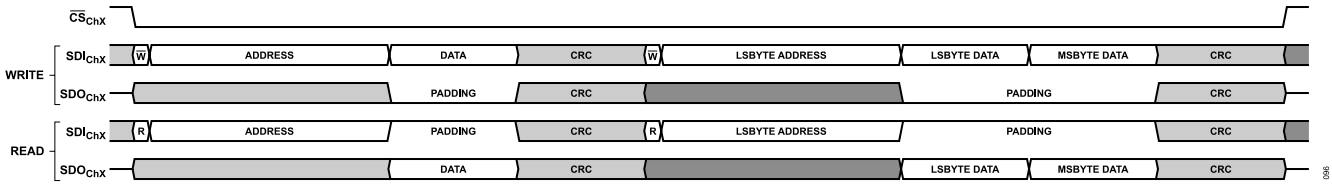

Figure 97. Single Instruction Mode Configuration with CRC Enabled, ADDR_ASCENSION = 1

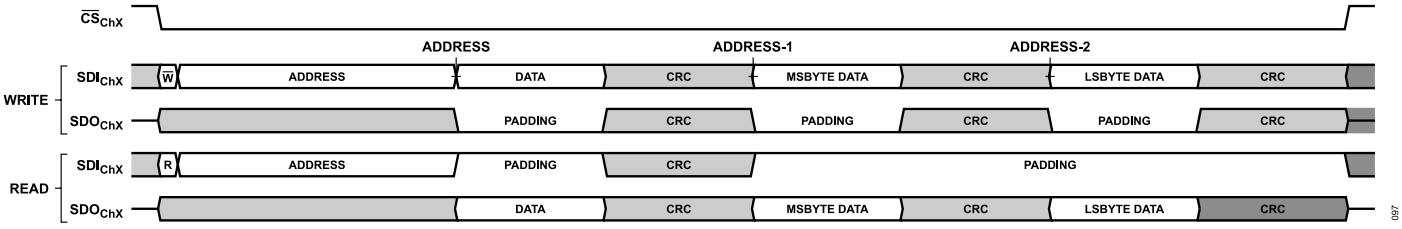

Figure 98. Streaming Mode Configuration with CRC Enabled, STRICT_REGISTER_ACCESS = 0 (Disabled) , ADDR_ASCENSION = 0

DIGITAL INTERFACE

Configuration SPI Frame

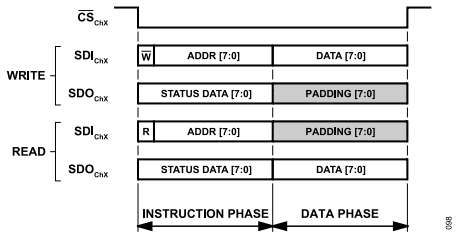

Figure 99. Short Instruction Mode, Data Status Enabled, CRC Not Enabled

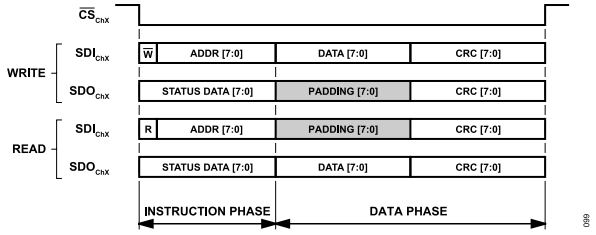

Figure 100. Short Instruction Mode, Data Status Enabled, CRC Enabled

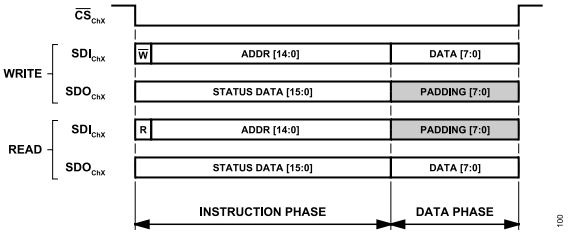

Figure 101. Long Instruction Mode, Data Status Enabled, CRC Not Enabled

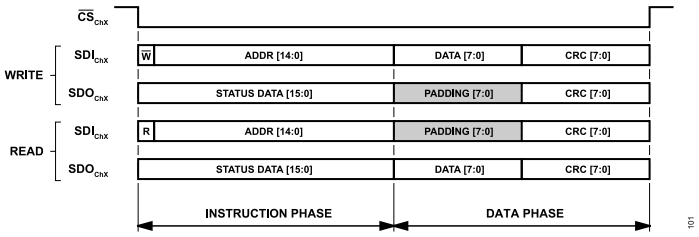

Figure 102. Long Instruction Mode, Data Status Enabled, CRC Enabled

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Configuration SPI Timing

Write Data Frame

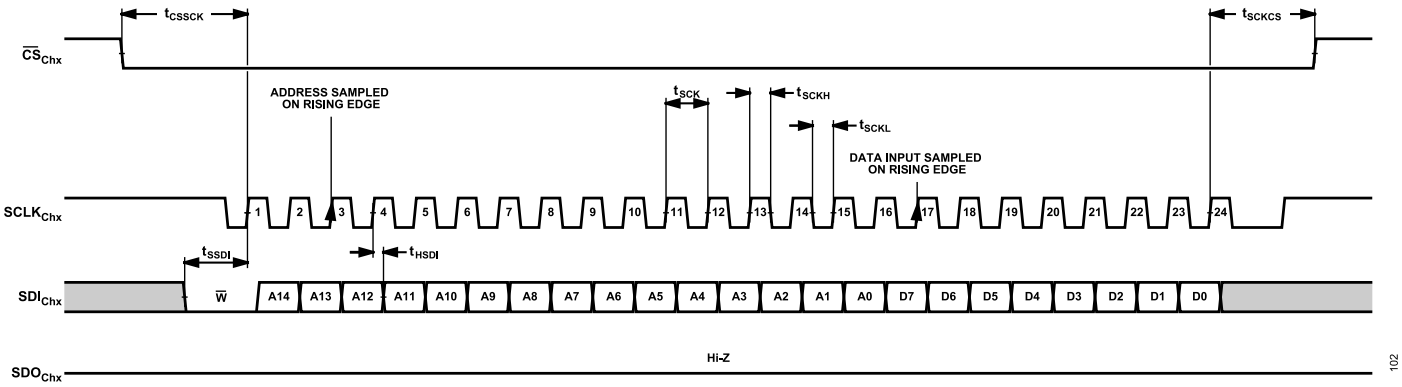

Figure 103. Configuration SPI Timing, Data Write Frame, 16-Bit Instruction Mode (Default)

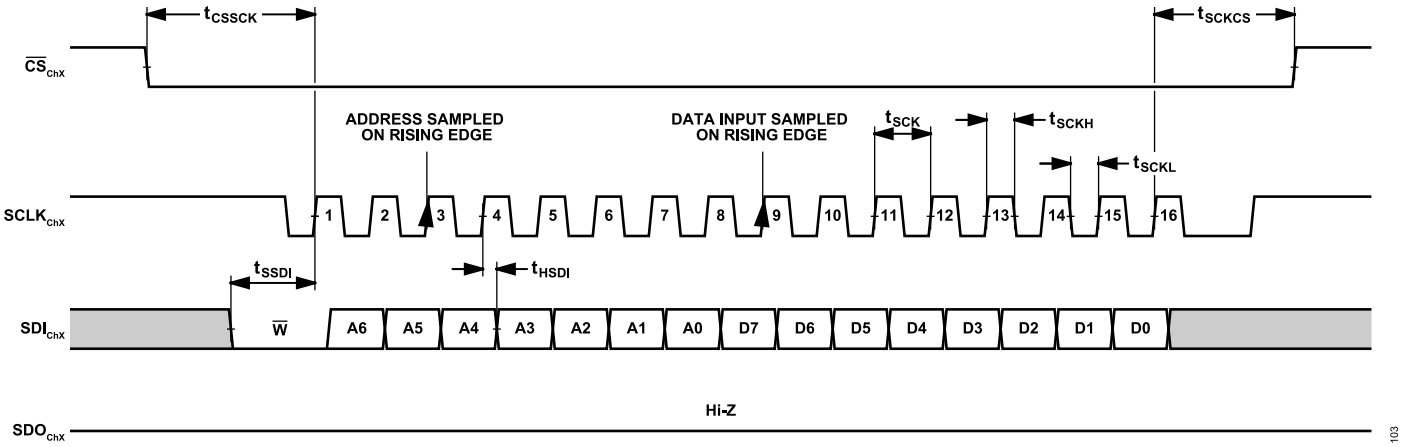

Figure 104. Configuration SPI Timing, Data Write Frame, 8-Bit Instruction Mode, Single 8-Bit Register

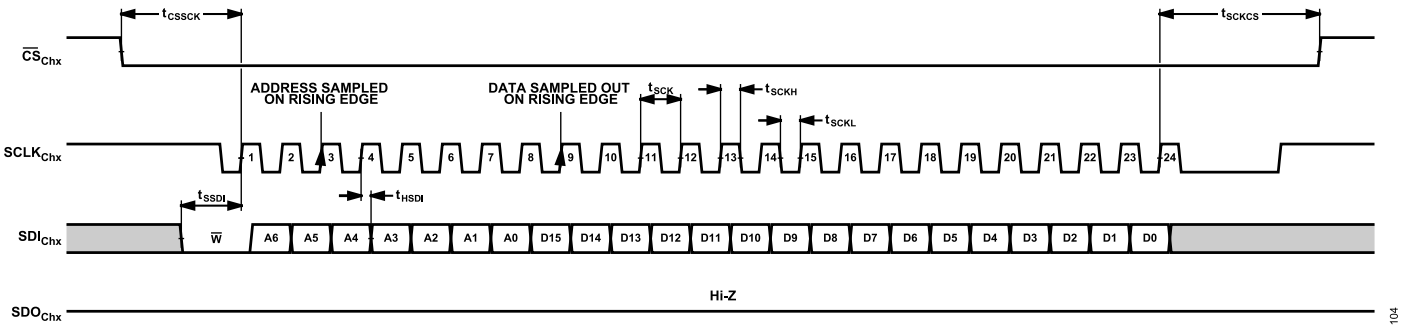

Figure 105. Configuration SPI Timing, Data Write Frame, 8-Bit Instruction Mode, Streaming Mode, Multibyte Register

DIGITAL INTERFACE

Read Data Frame

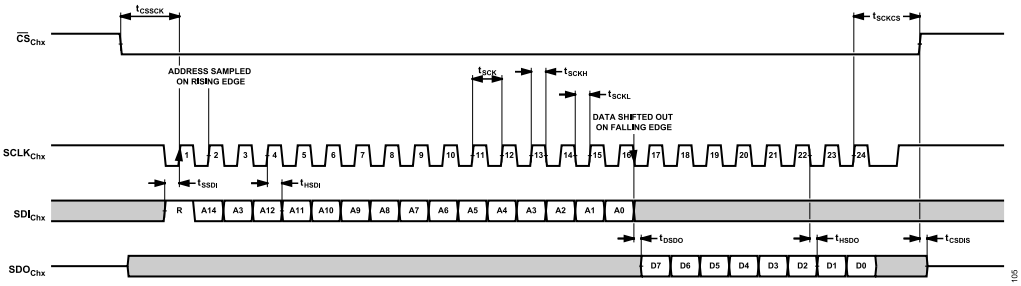

Figure 106. Configuration SPI Timing, Data Read Frame, 16-Bit Instruction Mode (Default)

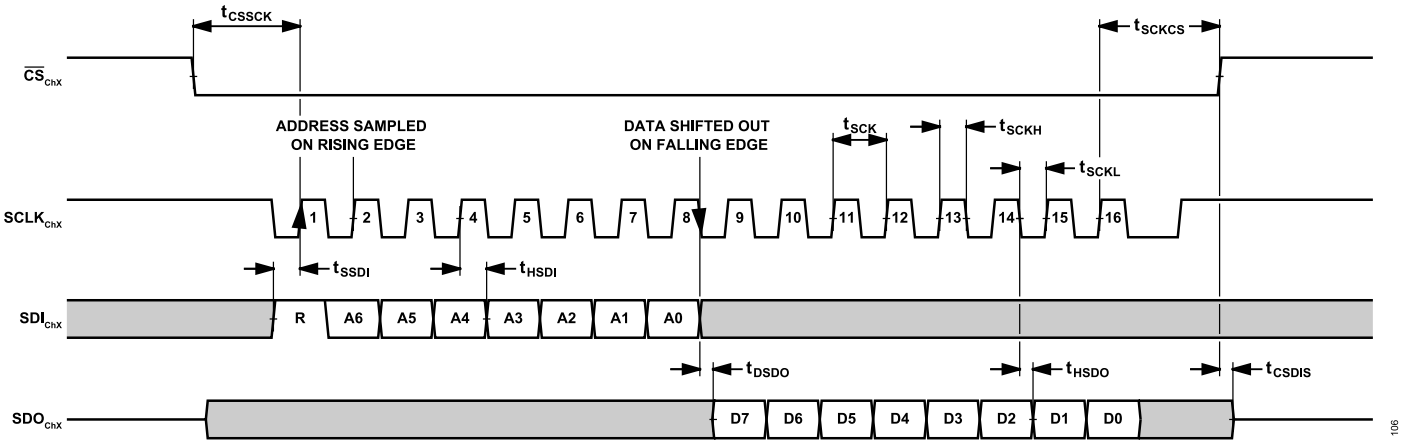

Figure 107. Configuration SPI Timing, Data Read Frame, 8-Bit Instruction Mode

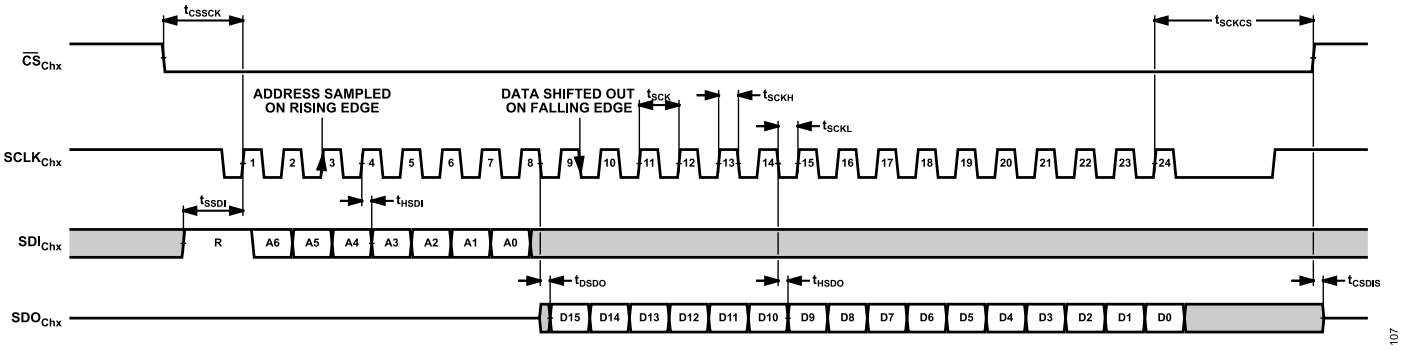

Figure 108. Configuration SPI Timing, Data Read Frame, 8-Bit Instruction Mode, Streaming Mode, Multibyte Register

DIGITAL INTERFACE

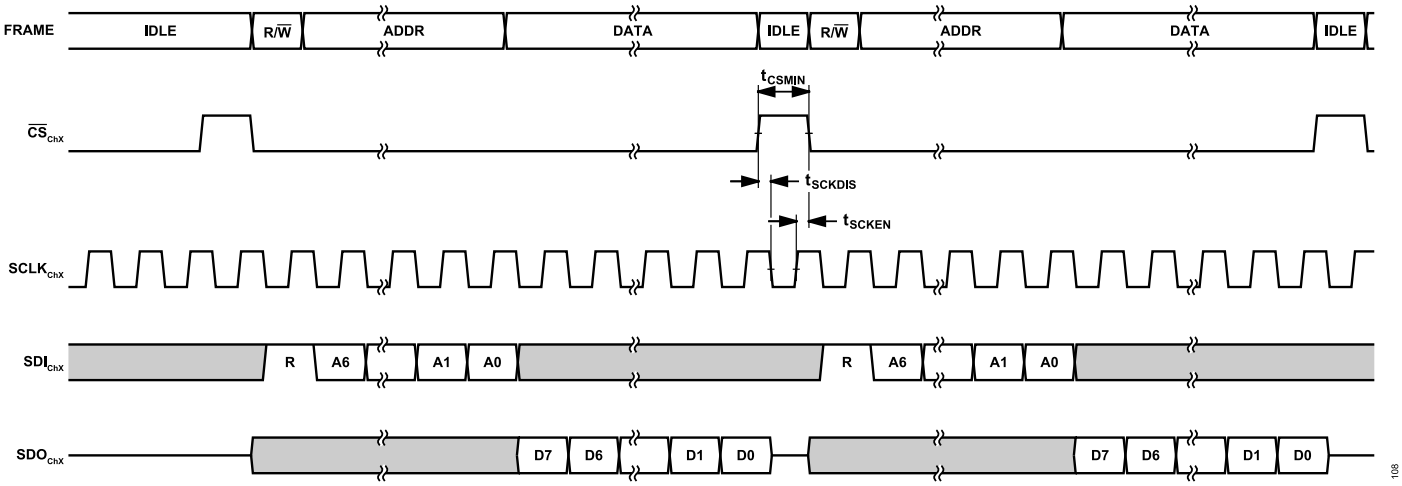

Figure 109. Configuration SPI Timing, Data Read Frame, Continuous $SCLK_{ChX}$

DIGITAL INTERFACE

LVDS DATA INTERFACE

LVDS Data Interface Configuration

The LVDS interface of each channel consists of up to five pairs of differential signals. The data clock input pair ($CLK+_{ChX}$ and $CLK-_{ChX}$), echoed data clock output pair ($DCO+_{ChX}$ and $DCO-_{ChX}$), two data output lanes ($DA+_{ChX}$ and $DA-_{ChX}$, $DB+_{ChX}$ and $DB-_{ChX}$), and optionally, the conversion clock can be configured as either an LVDS pair ($CNV+_{ChX}$ and $CNV-_{ChX}$) or as a CMOS using $CNV+_{ChX}$, where for this case, $CNV-_{ChX}$ is connected to GND. This user selection is configured using the LVDS_CNV_EN bit in the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16). The data lanes use a DDR scheme, which allows a single lane at the maximum interface clock speed of 80MHz to transfer the full maximum throughput of 160Mbps of the channel. Dual lane can be enabled to reduce interface clock speed and ease synchronization (see the ADC Data Interface Configuration A Register section, Address 0x15). By default, LVDS with one active lane is selected as the primary data interface for accessing conversion results.

To achieve maximum channel throughput, it is necessary that while a conversion is performed the result of the previous conversion is read. For this reason, it is critical that both the rising and falling edges of $CNV+_{ChX}$ and $CNV-_{ChX}$ are closely time aligned to the rising edge of $CLK+_{ChX}$ and $CLK-_{ChX}$. To avoid introducing noise into the conversion result, the $CNV+_{ChX}$ and $CNV-_{ChX}$ edge placement must be aligned to within ±535ps (t_{CCA}) of the interface clock ($CLK\pm_{ChX}$), as specified in Table 2.

The data interface is highly configurable allowing the customization of the output stream to meet a wide range of applications. Configuration options include the number of active lanes (1, 2), self clocked and echo clock modes, interface test functions, and data encoding. LVDS interface mode is used in applications where continuous conversion at channel sampling rates exceeding 1MHz is required.

Transmission of the result data occurs MSB first and is output after the amount of time specified in detail in the ADC Result Latency and LVDS Interface Alignment section.

LVDS Active Data Lane Count

The LVDS interface can be configured to output the result data on either one or two data lanes, which is controlled for each channel by the SPI_LVDS_LANES bit in their respective ADC Data Interface Configuration A register (see the ADC Data Interface Configuration A Register section, Address 0x15). By default, this bit is set to 0 (one lane active), and setting SPI_LVDS_LANES = 1 uses two data lanes. Note that this bit is also used to configure the number of active data lanes for the SPI.

In single lane operation, Data Lane A ($DA+_{ChX}$ and $DA-_{ChX}$ signal pair) is enabled as the primary data output, and the conversion result is shifted out serially, MSB first, using 8 interface clocks applied to $CLK+_{ChX}$ and $CLK-_{ChX}$ inputs per conversion. The result data is shifted out of the device on each edge of the echo clock outputs, $DCO+_{ChX}$ and $DCO-_{ChX}$. The result MSB (D15) and all odd numbered data bits are output on the falling edge of the interface clock. Conversely, the even numbered data bits are output on the rising edge of the interface clock.

In dual lane configuration, the result data is shifted out in parallel, 2 bits per clock edge, MSBs first. As a result, only four interface clock cycles are required per conversion. As the data access period is equivalent to the conversion period, the interface clock frequency is reduced by a factor of two relative to the single lane case. For the timing and latency implications of having different clock periods in the single lane and dual lane configurations, see the ADC Result Latency and LVDS Interface Alignment section.

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Echo Clock Mode

In LVDS data interface mode, the DCO+$_{ChX}$ and DCO−$_{ChX}$ pin pair is an echo clock output that provides a buffered and delayed version of CLK+$_{ChX}$ and CLK−$_{ChX}$ pin pair, facilitating data clocking to the host controller. This feature is controlled by the LVDS_SELF_CLK_MODE bit in the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16). By default, echo clock mode is active (LVDS_SELF_CLK_MODE = 0). Setting LVDS_SELF_CLK_MODE = 1 disables the DCO+$_{ChX}$ and DCO−$_{ChX}$ output driver, putting the device in self clock mode (see the Self Clock Mode section).

When echo clock mode is active, the interface requires a minimum of three LVDS pairs (CLK+$_{ChX}$ and CLK−$_{ChX}$, DCO+$_{ChX}$ and DCO−$_{ChX}$, and DA+$_{ChX}$ and DA−$_{ChX}$) to be connected between the host controller and the AD4885. A maximum of five LVDS pairs are required if the CNV+$_{ChX}$ and CNV−$_{ChX}$ pin pair is configured as an LVDS input and the DB+$_{ChX}$ and DB−$_{ChX}$ data lane is enabled. The conversion clock (CNV+$_{ChX}$ and CNV−$_{ChX}$) and data clock (CLK+$_{ChX}$ and CLK−$_{ChX}$) can be shared amongst channels or multiple AD4885 devices as long as care is taken to fanout the clock network, such that the edge placement requirement is satisfied.

In echo clock mode, data from enabled lanes is clocked out in sync to both rising and falling edges of DCO+$_{ChX}$ and DCO−$_{ChX}$ in a DDR scheme. Figure 110 and Figure 111 show the relevant LVDS interface timing with respect to the DCO+$_{ChX}$ and DCO−$_{ChX}$ echo clock for single and dual lane configurations, respectively. Calculation of t_{MSB_READ} is described in the ADC Result Latency and LVDS Interface Alignment section.

Consider matching the data clock (DCO+$_{ChX}$ and DCO−$_{ChX}$) and data lane (DA+$_{ChX}$ and DA−$_{ChX}$, DB+$_{ChX}$ and DB−$_{ChX}$) lane routing from the ADC to the host processor for the physical layout to minimize timing skew, which may affect data recovery in the host. For additional routing suggestions, see the Layout Guidelines section.

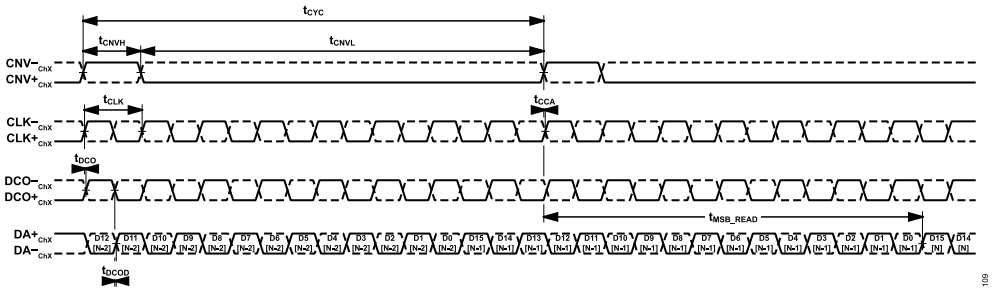

Figure 110. Continuous Conversion Timing, LVDS Data Interface, Single Data Lane, Echo Clock Mode

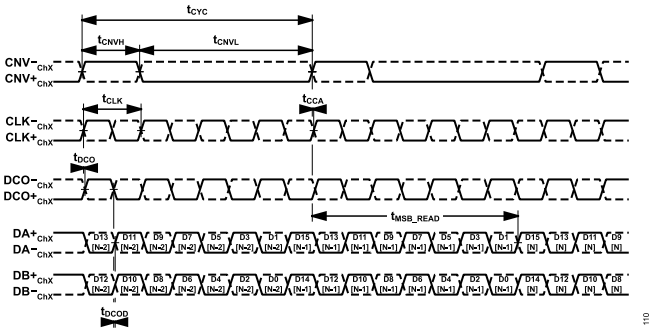

Figure 111. Continuous Conversion Timing, LVDS Data Interface, Dual Data Lane, Echo Clock Mode

DIGITAL INTERFACE

Self Clock Mode

In LVDS data interface mode, it is possible to disable the $DCO+_{ChX}$ and $DCO-_{ChX}$ echo clock output (see the Echo Clock Mode section) by setting LVDS_SELF_CLK_MODE = 1 in the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16). This setting puts the device in self clock mode disabling the $DCO+_{ChX}$ and $DCO-_{ChX}$ output driver, with the benefit of saving interface power as well as reducing the number of LVDS pairs required to interface with the host controller. In this mode, the $DCO+_{ChX}$ and $DCO-_{ChX}$ pins can be left disconnected, therefore, in single-lane configurations, a minimum of two LVDS pairs ($CLK+_{ChX}$ and $CLK-_{ChX}$, $DA+_{ChX}$ and $DA-_{ChX}$) are required to connect to each AD4885 instance. The interface connectivity can further be simplified by sharing the interface clock ($CLK+_{ChX}$ and $CLK-_{ChX}$) between multiple AD4885 instances.

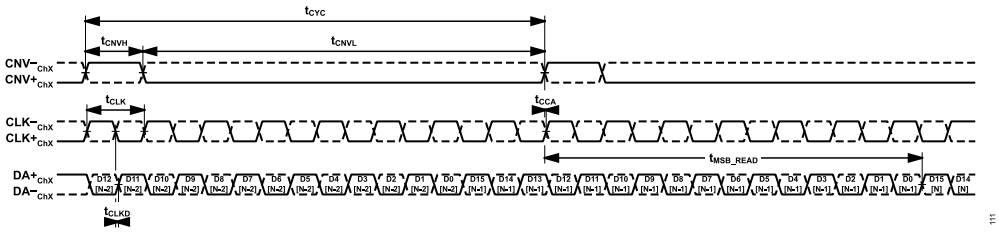

Figure 112. Continuous Conversion Timing, LVDS Data Interface, Single Data Lane, Self Clock Mode

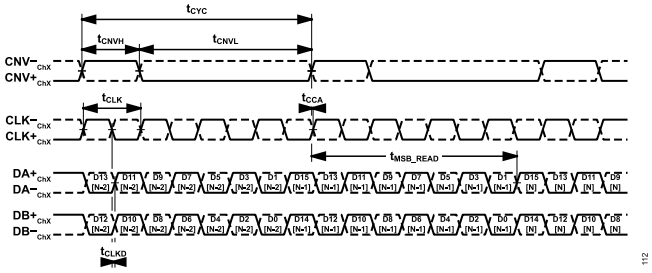

Figure 113. Continuous Conversion Timing, LVDS Data Interface, Dual Data Lane, Self Clock Mode

DIGITAL INTERFACE

LVDS Manchester Encoding Mode

This mode is accessed via the ADC_DATA_INTF_CONFIG_B register (see the ADC Data Interface Configuration B Register section, Address 0x16), which produces Manchester encoding of the result data in compliance with IEEE 802.3. This mode can be used in isolated data applications where the converter supplies can be floated and the data outputs capacitively coupled to the host controller. By ensuring that the mean output of each data lane is 0, the receiver side common-mode voltage is not disturbed by the result pattern.

Manchester encoding is available in dual lane LVDS mode only so that the maximum data throughput is achievable with the maximum 80MHz LVDS clock rate.

Figure 114 shows an example how this isolation can be implemented. Note that the LVDS 100Ω termination resistor prior to the isolation capacitors is required.

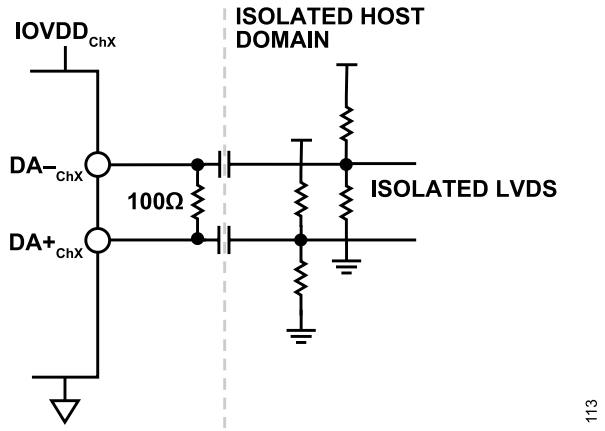

Figure 114. Isolated LVDS

ADC Result Latency and LVDS Interface Alignment

When an AD4885 channel is configured for LVDS interface mode, each conversion result is placed into its LVDS interface output shift register(s). The LVDS_CNV_CLK_CNT bits in the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section, Address 0x16) are used to configure the point in time when the conversion result data is loaded into the LVDS interface output shift register(s), but note that the number of clock counts is not encoded in straight binary, see Table 20. The total time from the rising edge of a convert pulse to when the MSB of that conversion request is internally available to transfer to the output register is defined as (t_{CYC} + t_{MSB}), both specified in Table 2. Because the transfer of this result data is under the control of the LVDS of CLK+ and CLK−, there is an additional (1.5 × t_{CLK}) that must be allowed to guarantee a fully completed result is transferred to the interface for read back. The user must calculate the correct required LVDS_CNV_CLK_CNT value and configure the ADC Data Interface Configuration B register (see the ADC Data Interface Configuration B Register section) according to the conversion rate and t_{CLK} used.

For minimum latency, the correct LVDS_CNV_CLK_CNT value to use for a particular conversion rate is calculated as (t_{MSB}/t_{CLK} + 1.5). This number is rounded down to the nearest integer value.

If gain error correction is enabled (see the Gain Error Correction section), the maximum t_{MSB} time is specified as 22.4ns. For a 10MSPS conversion rate in single lane LVDS with a 80MHz LVDS clock, the minimum LVDS_CNV_CLK_CNT is calculated as 22.4ns/12.5ns + 1.5, yielding a rounded down value of 3. Conversion latency is then determined as time, aligned to the falling edge of the CLK signal, described as t_{MSB_READ} or latency in the timing diagram, which can be calculated as (LVDS_CNV_CLK_CNT + 0.5) × t_{CLK}. For the given example, the resulting single lane latency is then (3 + 0.5) × 12.5ns + t_{CYC} = 143.75ns.

Taking a dual lane example with the LVDS clock running at half the speed (40MHz), again having 10MSPS and gain error correction enabled, the same formula is used and yields (22.4ns/25ns) + 1.5, resulting in an LVDS_CNV_CLK_CNT of 2, and a result for latency of (2 + 0.5) × 25ns + t_{CYC} = 162.5ns.

With gain error correction disabled (see the Gain Error Correction section), the maximum t_{MSB} time is specified as 18ns. For a 10MSPS conversion rate in single lane LVDS with a 80MHz LVDS clock, the calculation becomes (18ns/12.5ns) + 1.5, yielding a setting of 2 for the LVDS_CNV_CLK_CNT. Conversion latency is then determined as time, aligned to the falling edge of the CLK signal, described as t_{MSB_READ} or latency in the timing diagram, which can be calculated as (LVDS_CNV_CLK_CNT + 0.5) × t_{CLK}. Then in this case, the single lane latency is calculated as (2 + 0.5) × 25 + t_{CYC} = 131.25ns latency.

Once again, taking the previous example to a dual lane case with the LVDS clock running at half the speed (40MHz), again having 10MSPS and gain error correction disabled, the formula then becomes (18ns/25ns) + 1.5, resulting in an LVDS_CNV_CLK_CNT of 2, and a result for latency of (2 + 0.5) × 25ns + t_{CYC} = 162.5ns.

The four examples above are calculated to achieve minimum latency, but it is possible to use a higher LVDS_CNV_CLK_CNT value, whereby latency is increased by t_{CLK} for each +1 unit increase in the LVDS_CNV_CLK_CNT value.

Figure 115 and Figure 116 serve as aids to describe the placement of the ADC result data onto the LVDS interface controlled by the LVDS_CNV_CLK_CNT, showing that a new result is internally completed after t_{CYC} + t_{MSB}, signified here also by a notional $t_{MSB_AVAILABLE}$ (introduced only for the purposes of the explanation in Figure 115 and Figure 116). Figure 115 shows an example at 10MSPS conversion rate, with gain error correction, 80MHz LVDS clock, single lane, and shows that the LVDS_CNV_CLK_CNT setting of 3 is the earliest the conversion result can be loaded to the LVDS interface under these conditions. One additional full t_{CLK} cycle is required (a complete cycle being CLK+$_{ChX}$ falling edge to next CLK+$_{ChX}$ falling edge) to make the MSB available at the interface output. This cycle is highlighted within Figure 115 also with a notional t_{MSB_READ} indicator for illustrative purposes only. Figure

DIGITAL INTERFACE

116 similarly displays an example at 10MSPS conversion rate, with gain error correction, 40MHz LVDS clock, dual lane, and the minimal LVDS_CNV_CLK_CNT setting of 2 under these conditions.

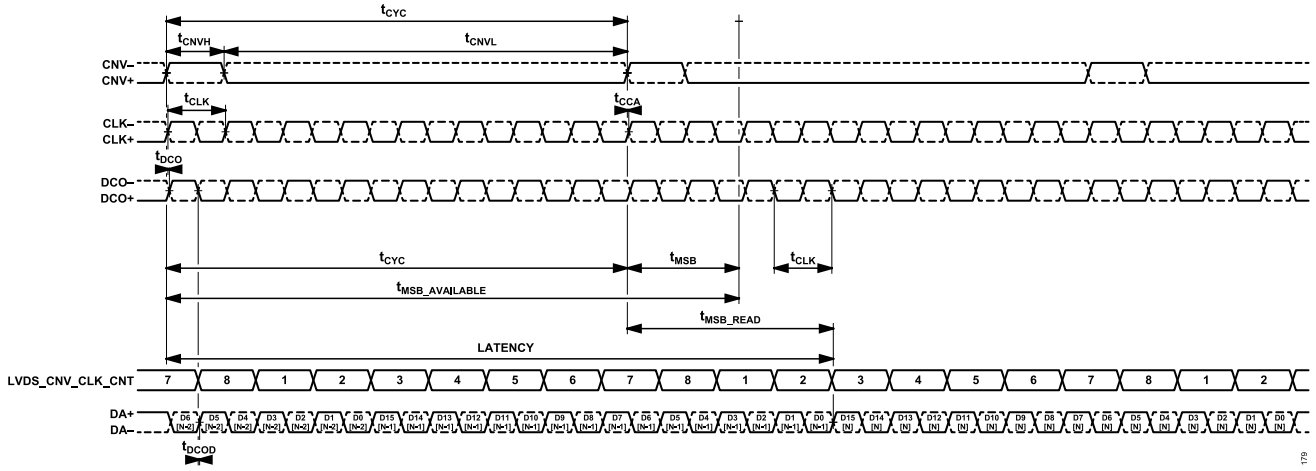

Figure 115. Single Lane LVDS, Echo Clock Mode, Gain Correction Enabled, LVDS_CNV_CLK_CNT Position Example

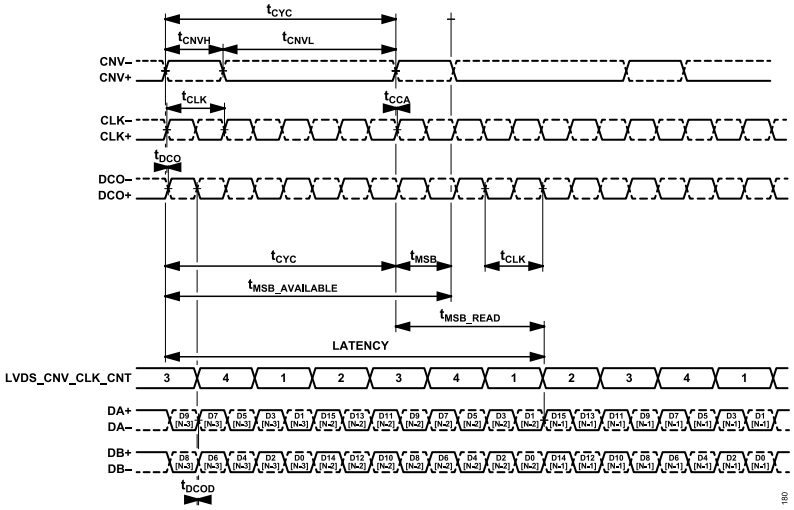

Figure 116. Dual Lane LVDS, Echo Clock Mode, Gain Correction Enabled, LVDS_CNV_CLK_CNT Position Example

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Table 20. LVDS_CNV_CLK_CNT Data Encoding

	Clock Count Number	
LVDS_CNV_CLK_CNT Value	Single Lane Mode	Dual Lane Mode
0b0000	3	3
0b0001	4	4
0b0010	5	1
0b0011	6	2
0b0100	7	Invalid value
0b0101	8	Invalid value
0b0110	1	Invalid value
0b0111	2	Invalid value
0b1000 to 0b1111	Invalid value	Invalid value

For reference, Table 21 indicates the minimum required LVDS_CNV_CLK_CNT settings for various conversion rates, with gain error correction enabled (t_{MSB} = 22.4ns) or disabled (t_{MSB} = 18ns), and the resulting latency. Note that disabling gain error correction, using maximum LVDS data interface clock frequency and single lane configuration results in the minimum achievable latency of 131.25ns.

The AD4885 has an interface check feature that is enabled by setting the INTF_CHK_EN bit in the ADC Data Interface Configuration A register (see the ADC Data Interface Configuration A Register section, Address 0x15). When this bit is set, the ADC results are no longer output on the interface, and the output is replaced by the fixed pattern 16'b1010 1100 0101 1101 (0xAC5D). When the INTF_CHK_EN bit is unset, the normal conversion results are output to the LVDS interface immediately. The interface check feature allows the user to test the correct transfer of data over the interface, and to run alignment procedures, particularly for self clock mode cases where unknown PCB propagation delays may be present between the AD4885 and its digital host controller. Note that this feature was specifically designed to help align the output LVDS data with the LVDS clock of the digital host by using static data, and the feature does not indicate if the correct LVDS_CNV_CLK_CNT setting is used.

Table 21. LVDS_CNV_CLK_CNT Minimum Setting and Latency for Various Sample Rates

Sample Rate (MSPS)	LVDS Lanes	f_{CLK} (MHz)	Gain Error Correction	LVDS_CNV_CLK_CNT Minimum Setting	Latency (ns)
10	1	80	Yes	3	143.75
10	1	80	No	2	131.25
8	1	64	Yes	2	164.06
8	1	64	No	2	164.06
6	1	48	Yes	2	218.75
6	1	48	No	2	218.75
4	1	32	Yes	2	328.13
4	1	32	No	2	328.13
2	1	16	Yes	1	593.75
2	1	16	No	1	593.75
10	2	40	Yes	2	162.5
10	2	40	No	2	162.5

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LVDS Data Transfer Latency

Where the user is concerned in knowing the overall latency from when an individual ADC conversion is initiated to the time when the LSB has reached the host controller, it is important to consider the data transfer latency. The total latency observed is the sum of the ADC latency and the data transfer latency, in this case, the LVDS_CNV_CLK_CNT is set to achieve minimum ADC latency. Additional clock cycles more than the minimum required incur additional LVDS clock cycles of latency to the overall latency, as is shown in Figure 117.

The data transfer latency on the LVDS interface depends on the following parameters:

- LVDS clock period, t_{CLK}
- Number of active LVDS lanes, N_{LANES}
- Number of bits to be read, N_{BITS}

Calculate the latency as follows:

$$Data\ Transfer\ Latency = \frac{N_{BITS}}{N_{LANES}} \times t_{CLK}$$

For applications that require extremely low latencies, note that as the data is transferred MSB to LSB in both single and dual lane modes, and that there is no requirement to fully read a result from the interface, the data transfer latency can be reduced for lower resolution results (that is, N_{BITS} can be chosen to be smaller than the maximum bits available).

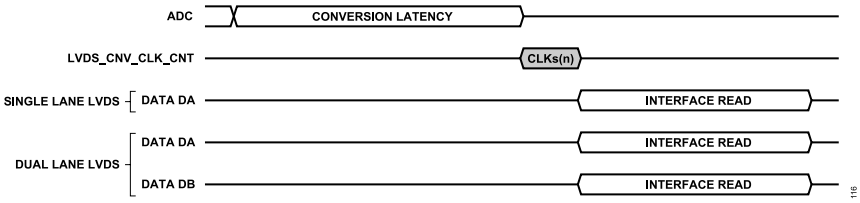

Figure 117. LVDS Data Transfer Latency

DIGITAL INTERFACE

LVDS Output Differential Drive

The AD4885 LVDS interfaces support selection of the differential output voltage from one of three predetermined differential amplitudes of 395mV p-p, 530mV p-p, and 785mV p-p, assuming a termination resistance of 100Ω across the differential pair. The output common-mode voltage of the LVDS driver is adjusted for each selection automatically to ensure that the peak output voltage remains within the $IOVDD_{ChX}$ rail. The default setting is a differential amplitude of 530mV p-p. The output differential voltage can be independently configured for each channel by writing to the LVDS_VOD bits of the corresponding ADC Data Interface Configuration C register (see the ADC Data Interface Configuration C Register section, Address 0x17).

Data Interface Test Function

Regardless of the selected output configuration, the AD4885 is equipped with an interface check function that is enabled by setting the INTF_CHK_EN bit in the Data Interface Configuration A register (see the ADC Data Interface Configuration A Register section, Address 0x15).

The interface check function forces the data interface to output a fixed, 16-bit pattern, which facilitates verification of the integrity of the data interface physical layer, including device pads, PCB interconnect, and the host interface connections. By enabling this built-in test function, access to ADC conversion results is suspended, therefore, only use this function either at power-up or during an idle period when conversion results are not required for normal system function.

For more details, see the ADC Result Latency and LVDS Interface Alignment section.

SPI DATA INTERFACE

SPI Data Interface Configuration

For applications that do not require the interface bandwidth of the LVDS interface, such as when using asynchronous capture into the result FIFO, the data interface of any channel can be reconfigured into a single or quad lane, SPI data interface. In this configuration, the channel outputs its data on either one or four CMOS data lanes simultaneously at serial clock rates up to 50MHz. The result data is shifted out serially on the falling edge of the interface clock ($DCLK_{ChX}$). In SPI configuration, the channel results can be read at an effective interface rate of up to 200Mbps when using four SPI lanes.

The SPI data interface for a channel is activated by setting the DATA_INTF_MODE bit from its Data Interface Configuration A register to 1 (see the ADC Data Interface Configuration A Register section, Address 0x15). Once the data interface is configured for SPI mode, the LVDS drivers are automatically disabled, including the echo clock output ($DCO+_{ChX}$ and $DCO-_{ChX}$), preventing contention between LVDS and CMOS functions. As a result, the LVDS_SELF_CLK_MODE and LVDS_VOD settings no longer affect the operation of the data interface and can be left at their power-on defaults or another convenient value. Because the driver is disabled, the $DCO+_{ChX}$ and $DCO-_{ChX}$ output pins can, therefore, be left disconnected in the hardware design as these pins are unused.

As detailed in Table 22, the following LVDS pins are reconfigured as CMOS input or outputs to realize the SPI data interface.

Table 22. LVDS/SPI Data Interface Pins Crossreference

LVDS Pin	CMOS Pin	Function
$CLK+_{ChX}$	$DCLK_{ChX}$	Data interface clock input
$CLK-_{ChX}$	$\overline{DCS}_{ChX}$	Data interface chip select (active low) input
$DA+_{ChX}$	$SDOA_{ChX}$	Serial Data Output A
$DA-_{ChX}$	$SDOB_{ChX}$	Serial Data Output B
$DB+_{ChX}$	$SDOC_{ChX}$	Serial Data Output C
$DB-_{ChX}$	$SDOD_{ChX}$	Serial Data Output D

As with LVDS configuration mode, SPI configuration selection allows control of the number of active lanes. For SPI data interface configuration, the user has the option to configure single lane SPI or quad lane SPI.

SPI Active Data Lane Count

The SPI data interfaces can be configured to output the result data on either one or four data lanes, which is controlled by the SPI_LVDS_LANES bit in the ADC Interface Configuration A register of each channel (see the ADC Data Interface Configuration A Register section, Address 0x15). By default, this bit is set to 0 (one lane active), and can be set to 1 to use four data lanes. Note that this bit also sets the number of active data lanes for the LVDS interface. The data order and pin assignment to the serial data output ($SDOx_{ChX}$) pins is detailed in Table 23, and shown in Figure 124.

Table 23. SPI Data Lane(s) Data Order and Pin Assignment

	Output Data Order	
Serial Data Output Pin	One Active SPI Lane (SPI_LVDS_LANES = 0)	Four Active SPI Lanes (SPI_LVDS_LANES = 1)
$SDOA_{ChX}$	Not applicable	SDO 3
$SDOB_{ChX}$	SDO 0	SDO 2
$SDOC_{ChX}$	Not applicable	SDO 1
$SDOD_{ChX}$	Not applicable	SDO 0

Data Interface CRC

To ensure the integrity of the result data, a CRC is appended to the FIFO results. This CRC is always enabled and appended. The computation of the result checksum is independent of that of the configuration interface. The result is 24 bits in length and is appended to each data result record acquired from the FIFO.

Sign Extension

When accessing FIFO data through a SPI data interface, the 16-bit data length of AD4885 lends itself to easy data access and storage. Hence, no sign extension is done, as opposed to 20-bit resolution

DIGITAL INTERFACE

devices from the same family of products as AD4880, where sign extension to 24-bits is performed.

GPIO PINS

The AD4885 GPIO pins are intended to simplify the development of synchronous data acquisition applications by facilitating a simplified state control interface between the host processor, the data converter, and other related signal chain components. When configured as an output, these GPIO pins can be assigned as an indicator of device status, a digital control for a related signal chain component, or a serial data lane for device configuration. In input mode, the GPIO pins allow pin programming of converter features such as digital filter synchronization (reset) and an external event trigger. Each channel has its own set of GPIO pins that can be separately configured.

The required function for each GPIO is defined by writing to the GPIO Configuration A through GPIO Configuration C registers (Address 0x19 through Address 0x1B), see the GPIO Configuration A Register through the GPIO Configuration C Register sections. The configuration for each GPIO includes an output enable bit, an output data bit, and a function selection. The output data bit determines the logical state of the output when the GPIO data option is selected, otherwise, the output state is determined by the selected function, assuming the output is enabled. By default, $GPIO0_{ChX}$ is enabled as an output, and the configuration SPI SDO function is selected. All other GPIO outputs are disabled.

Table 25 provides a brief description of the available AD4885 GPIO functions. Each of the GPIO pins can be configured for any of the following functions.

Table 24. GPIO Registers Overview

Register	Bits	Contents
GPIO_CONFIG_A	GPIO_0_EN, GPIO_1_EN, GPIO_2_EN, GPIO_3_EN	Enable bits for each GPIO. 0: Configures the GPIO as an input. 1: Configures the GPIO as an output.
GPIO_CONFIG_A	GPIO_0_DATA, GPIO_1_DATA, GPIO_2_DATA, GPIO_3_DATA	The corresponding GPIO_x_SEL bit for each GPIO can be set to 0111b to read or write data to that GPIO. In this mode, GPIO_x_EN selects whether each of these data bits is read only or write only, depending on whether the GPIO is configured as an input or an output. When configured as an output, these bits are write only, the user can set the bits to a logic level that they need to output on the GPIO. When configured as an input, these bits are read only, the user can read the bits to determine the logic level input to the GPIO. If the corresponding GPIO_x_SEL is not set to 0111b, the GPIO_x_DATA is not valid as the GPIO is overridden with the selected GPIO function.
GPIO_CONFIG_B	GPIO_0_SEL, GPIO_1_SEL	Selection for the function mode of GPIO0 and GPIO1.
GPIO_CONFIG_C	GPIO_2_SEL, GPIO_3_SEL	Selection for the function mode of GPIO2 and GPIO3.

Table 25. GPIO_x_SEL Function Descriptions

GPIO_x_SEL	Function	Description
0000b	Configuration SPI SDO	Configuration Serial Data Output. This configures the selected GPIO to be the SDO for the configuration SPI.
0001b	FIFO full	FIFO Memory Full Indication Output. This configures the selected GPIO to function as an indicator that the channel FIFO is full. The FIFO full indicator is set when the conversion result corresponding to the specified count in the FIFO watermark registers (see the FIFO WATERMARK Register section, Address 0x1D and Address 0x1E) is loaded into the data FIFO. The FIFO full status bit is cleared by reading data from the FIFO, and it is cleared when the first conversion result is moved from the FIFO to the data interface output shift register.
0010b	FIFO read done	FIFO Memory Read Completed Output. This configures the selected GPIO to function as a FIFO read done indicator. The FIFO read done indicator is cleared by default when the channel FIFO is first enabled, and each time the last conversion result is moved from the FIFO into the data interface output shift register. The FIFO read done is cleared when the MSB of the last FIFO result is read on the selected data interface.
0011b	Filter result ready	Filter Result Ready Output. When the digital filter is enabled, this configures the selected GPIO to function as an indicator that new data is available to read on the interface. This active low indication allows synchronization between the host and the AD4885 when utilizing the integrated digital filter to oversample and decimate an incoming signal. The signal is driven low at the end of each filter decimation period and is driven high again before the next decimated output is ready.

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Table 25. GPIO_x_SEL Function Descriptions (Continued)

GPIO_x_SEL	Function	Description
0100b	HI_DTCT	High Threshold Event Output. With threshold detection enabled, this configures the selected GPIO to indicate when the high level threshold is crossed. The output is active high.
0101b	LO_DTCT	Low Threshold Output. With threshold detection enabled, this configures the selected GPIO to indicate when the low level threshold is crossed. The output is active high.
0110b	$\overline{\text{ALERT}}$	Status Alert (Active Low) Output. This configures the selected GPIO to function as the status alert for threshold event detection.
0111b	GPIO data	General-Purpose Output Mode. In this mode, the state of the corresponding GPIO_x_DATA bit in the GPIO Configuration A register (see the GPIO Configuration A Register section, Address 0x19) is applied to the configured output.
1000b	$\overline{\text{FILTER_SYNC}}$	Filter Synchronization Input (Active Low). This configures the selected GPIO to function as a synchronization signal for the digital filter. When held low, this input holds the digital filter in reset.
1001b	EXT_EVENT	External Event Trigger Input. Event triggers when a logic high is detected on the configured GPIO input. This event can be used to trigger the FIFO.

DIGITAL FEATURES

OVERVIEW

The AD4885 includes several useful digital features that offer great solution benefits to many applications. These features are independently configured for each channel and can be individually enabled by the user, when required. A brief overview follows for these features, in depth explanation and definition of these features are found in the following sections.

- Event Detection: This feature allows the detection when the ADC input has crossed user-configured thresholds. Such detections can be flagged in the configuration registers, output to a GPIO, or used to trigger the result FIFO.
- Result FIFO: This feature allows the acquisition of records of up to 16,384 conversion results into the channel FIFO memory. These acquisitions can be read back to the host controller via LVDS or the SPI data interface. The results stored in the FIFO can be either unprocessed ADC results or those that have been processed through the digital filter feature.
- Digital Filter: This feature offers three different digital filter configurations, each with a wide range of decimation rates, allowing oversampling benefits and the close control of the signal bandwidth.
- System Error Correction Coefficients: Although the AD4885 offers excellent factory calibrated precision with minimal offset and gain errors, this feature allows the user to correct for signal chain errors that may be present within their application.

EVENT DETECTION

The AD4885 includes an event detection feature, whereby the user can either indicate when a particular ADC input threshold level is crossed or monitor a GPIO configured as an input. An internally generated event can then be used to set a flag in the configuration memory or routed to a configured GPIO output to be used to alert a host controller that a threshold condition is breached. It is also possible for a user to route an external signal to the AD4885 to be used as an external trigger. An internally or externally generated event can also be used to trigger the corresponding channel FIFO (see the Result FIFO section). The mechanism for this is explained in the Event Detection for FIFO section. The threshold detection compares a converted voltage code to a user-configured code because this is done in a sample by sample basis, and events immediately trigger, level hysteresis setting is also configurable to prevent unwanted triggering.

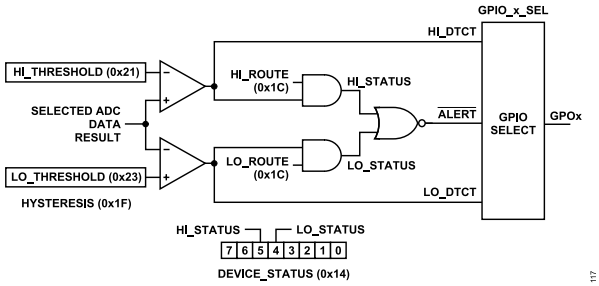

Figure 118. Internally Generated Event Detection Signal Path

The Figure 118 serves as an aid with detailing the configuration and operation of the event detection of the AD4885.

Table 26. Event Detection

INT_EVENT_EN Bit (Address 0x1C)	Mode	Trigger Source	Comment
0	External event	GPIO_x_SEL = 4b1001, that is, configured for EXT_EVENT.	Event triggers when a logic high is detected on the selected GPIO input.
1	Internal event	ADC Results threshold detection is enabled.	HI_THRESHOLD (Address 0x21 and Address 0x22) and LO_THRESHOLD (Address 0x23 and Address 0x24) set the upper and lower ADC result (or the digital filter result) code threshold for the event to be triggered.

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Event Detection Timing

When event detection is enabled for a channel in its general configuration register (see the General Configuration Register section), the HI_DTCT and LO_DTCT signals indicate the occurrence of an internally generated event. These signals can be routed internally through the following paths:

- HI_DTCT and LO_DTCT are directly accessible via an enabled GPIO with GPIO_x_SEL set to 0b100 or 0b101, respectively, a threshold event can be monitored externally by a digital host via the GPIO. Logic 1 on a configured GPIO indicates detection of an event.
- HI_DTCT and LO_DTCT can each be routed by setting the HI_ROUTE and LO_ROUTE bits to 1, respectively, in the general configuration register (Address 0x1C) to allow HI_DTCT and LO_DTCT to propagate to the LO_STATUS and HI_STATUS bits in the device status register (see the Device Status Register section, Address 0x14). These status bits can be monitored by the digital host via the configuration SPI. Logic 1 on a configured GPIO indicates the detection of an event. Each of these two bits are independently cleared when a 1 is written to these bits. Power cycling or device reset also result in the bits clearing.
- HI_DTCT and LO_DTCT can each be routed by setting the HI_ROUTE and LO_ROUTE bits to 1, respectively, in the general configuration register (Address 0x1C) to allow HI_DTCT and LO_DTCT to propagate to the $\overline{\text{ALERT}}$ signal. Any enabled GPIO set to output a status alert, that is, with GPIO_x_SEL set to 0b0110, routes the $\overline{\text{ALERT}}$ signal to the GPIO to indicate when an event occurs. A GPIO configured in this mode is normally high, with a logic low indicating that an event has occurred. As shown in the Figure 120 section, this GPIO remains low only while the threshold level is crossed, and it returns to logic high as soon as the threshold bound is no longer crossed, and the timing in Figure 119 is satisfied.

Event detection is synchronous to the rising edge of the $CNV+_{ChX}$. A latency of two conversion clock cycles exists from the first $CNV+_{ChX}$ edge where the analog input crosses a threshold to a detected event that is flagged in the device status register and to any GPIO configured to route $\overline{\text{ALERT}}$. As is evident in Figure 118, where both the HI_DTCT flag and $\overline{\text{ALERT}}$ routed to a GPIO are shown, the behavior, once the threshold level is no longer crossed, is different. When a $CNV+_{ChX}$ rising edge occurs where the analog input no longer crosses the set threshold, $\overline{\text{ALERT}}$ de-asserts two conversion cycles later, on the rising edge of CNV. Any HI_DTCT or LO_DTCT already set is not cleared at this point. These signals are only cleared by writing 1 to the relevant bits in the device status register (Address 0x14) or where a device reset occurred.

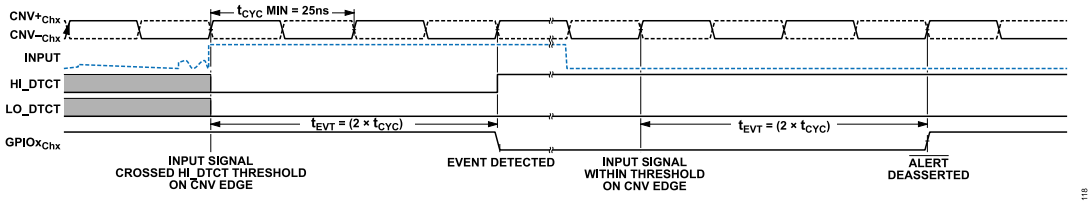

Figure 119. Event Detection Timing

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Threshold Detect Levels

The threshold detection of the AD4885 includes a hysteresis setting. By configuring this setting, the user can ensure that unwanted threshold triggering can be avoided. Figure 120 shows how this can be achieved. A single hysteresis setting is configured, that is then applied to both the HI_THRESHOLD and LO_THRESHOLD bits. The high and low detection flags remain set until the hysteresis thresholds are crossed.

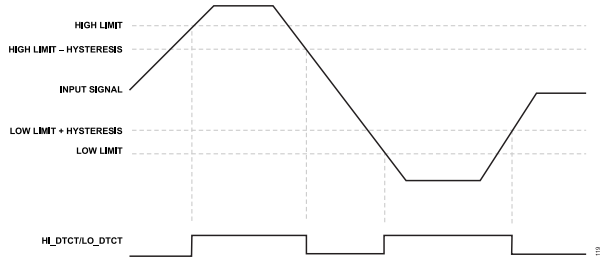

Figure 120. Threshold Detect Levels

Enabling Event Detection

By default, after power on or reset, HI_ROUTE and LO_ROUTE are set to Logic 0, masking the threshold level detection from generating any event alert. When enabled, the gated versions of these signals, HI_DTCT_GATED and LO_DTCT_GATED, are logic NOR'd to generate the $\overline{\text{ALERT}}$ signal. If a user requires the use of the HI_DTCT, LO_DTCT, or $\overline{\text{ALERT}}$ signals to flag an event occurrence externally, back to a digital host, the GPIO_x_SEL registers can be used to route any, or multiple, of these signals to the GPIO pins.

Event Detection for FIFO

Event detection can also be used in a channel to arm its FIFO memory. The event detection for the FIFO can be triggered using either internal or external events as detailed in the Event Detection section.

To use the $\overline{\text{ALERT}}$ signal to trigger the FIFO, the HI_ROUTE and/or the LO_ROUTE bits must be configured as required, and the INT_EVENT_EN bit must be set to 1, to use a combined $\overline{\text{ALERT}}$ output to trigger the FIFO. Alternately, when configured with the INT_EVENT_EN bit set to 0, a GPIO EXT_EVENT input must be configured, and this input triggers the FIFO when a Logic 1 is presented on the GPIO. Because this event was generated externally, there is no $\overline{\text{ALERT}}$ signal generated.

The HI_THRESHOLD (Address 0x21 and Address 0x22) and LO_THRESHOLD (Address 0x23 and Address 0x24) bits can be used to configure the ADC output code thresholds for the internal event detection. These bits can each be masked using the HI_ROUTE and LO_ROUTE bits in the general configuration register (Address 0x1C). Setting these bits logic high, routes the bits to be used for the $\overline{\text{ALERT}}$ flag (that can be monitored using a preconfigured GPIO), it is also enabled as a FIFO event trigger as well as making these available as HI_STATUS and LO_STATUS flags in the device status register (Address 0x14).

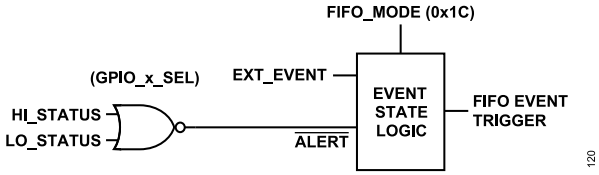

Figure 121. FIFO Event Detection Logic

Event Detection ADC Data Result

The ADC data result, as shown in Figure 118, is dependent of the selected data path. As is evident in Figure 132, where the digital filter (see the Digital Filter section) is enabled, the output of the selected filter refers to the ADC data result that is checked by the threshold detection for event detection.

RESULT FIFO

Each AD4885 channel has an independent single port data FIFO for applications where a reduced data interface transmission load is required and where asynchronous data capture and access is appropriate. This FIFO can serve to reduce the requirements for the digital host controller and can, for example, enable the AD4885 to be deployed in systems using an MCU digital host. Each data FIFO allows for a record of up to 16,384 data results to be captured per acquisition burst without result loss due to data overflow. As a single port memory, simultaneous data interface read and ADC conversion result write operations are not permitted to the FIFO.

To allow synchronization of FIFO access between the host controller and ADC, status flags are included to indicate if the memory is full (FIFO_FULL) or if no new data available in the FIFO (FIFO_READ_DONE), that is, there is no new data since the last trigger is set, or the last FIFO data read back of a result record has already been completed. When N = WATERMARK is reached, that is, when the conversion result corresponding to the specified count in the FIFO_WATERMARK register is loaded into the data FIFO, memory is set as full, and the FIFO_FULL bit gets asserted in device status register (see the Device Status Register section, Address 0x14). The status bits can be accessed by reading directly from the device status register (Address 0x14) via the configuration SPI, appending the status to the data SPI frame, or by assigning the required status flags to a GPIO pin by setting the required GPIO_x_SEL bit. For more details on these GPIOs, see the GPIO Pins section. The user can also select between various modes of initiating the burst acquisition, which is described further in the FIFO Mode Selection and Configuration section.

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FIFO Mode Selection and Configuration

There are four distinct modes in which each channel data FIFO of the AD4885 can be configured. The active mode is selected by setting the FIFO_MODE bits in the general configuration register (see the General Configuration Register section, Address 0x1C). By default, the FIFO is disabled (FIFO_MODE = 00). The modes are designed to fit the use case requirements of different applications. Table 27 provides details about each FIFO mode and their applicable use cases.

Table 27. FIFO Configuration Modes (FIFO_MODE)

FIFO_MODE Bit Value	FIFO Mode	Description	Use Case
00	FIFO disabled	FIFO is not used. This value also resets and rearms the event trigger.	Continuous convert mode, and FIFO is not in use.
01	Immediate trigger mode	In this mode, the data capture is initiated immediately after receipt of the first valid converter result and continues until [N = WATERMARK] results are loaded into the FIFO memory. Upon read back from the FIFO, FIFO_READ_DONE indicates when [N = WATERMARK] results are read from the FIFO.	User is interested in burst acquisition(s) of [N = WATERMARK] results, initiated by setting this FIFO_MODE, Bits[1:0] value.
10	Event trigger capture, read latest WATERMARK	The data capture into the FIFO memory is initiated by the user-selected event method. The result counter initiates by the event, and data captures to the FIFO stop once [N = WATERMARK] results are captured. Upon read back from the FIFO, FIFO_READ_DONE indicates when [N = WATERMARK] results have been read from the FIFO.	User is interested in burst acquisition(s) of [N = WATERMARK] results, initiated by an event. Only result data after the event is of interest.
11	Event trigger capture mode, read all FIFO	The data capture immediately initiates after the receipt of the first valid converter result. The FIFO continuously fills until an event is detected. If no event is detected before the FIFO fills (that is, 16,384 results are written to memory), the memory continues to fill with the oldest results discarded on a first in, first out basis. Upon receipt of the selected event method, a result counter counts up to [N = WATERMARK]. Data capture stops once the WATERMARK is reached. In this mode, once the FIFO is filled, the position in the FIFO memory at which the event occurred gets automatically stored in the FIFO_WATERMARK register. The value read back from FIFO_WATERMARK allows the user to distinguish which of the stored results captured before the event from those that were captured after the event. Further details can be seen in the example given in the Event Trigger Capture Mode, Read All FIFO section. Upon read back from the FIFO, FIFO_READ_DONE indicates when 16,384 results are read from the FIFO. The full memory read back contains [N = WATERMARK] results after the event. If N in this case is less than 16,384, the remaining contents of the FIFO contain the conversion results prior to the event.	User is interested in burst acquisition(s) of [N = WATERMARK] results initiated by an event. The full FIFO contents are read in this mode. In this mode, the user can read [N = WATERMARK] results after the event and (16,384 − [N = WATERMARK]) before the event. Only WATERMARK values that are multiples of four are valid in this mode.

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FIFO Event Detection

The FIFO is configured for capture in event detection mode (FIFO_MODE = 2'b10 or FIFO_MODE = 2'b11), the following event detection options (see the Event Detection section) are available.

The general configuration register of the channel (Address 0x1C) contains the internal event enable bit (INT_EVENT_EN), which determines whether the FIFO is to respond to an external or internal event trigger. The default state of this bit on power on and reset is INT_EVENT_EN = 0, which is configured for an external event.

Asynchronous Data Capture

To use the FIFO for asynchronous capture, first write to the FIFO watermark register (see the FIFO WATERMARK Register section, Address 0x1D) with the number of conversions to be captured in each burst, any integer between 1 and 16,384 can be entered. If using GPIO to pass the FIFO status bits to the host controller, program those selections into the GPIO configuration registers prior to initiating the capture. For more details on GPIO configuration, see the GPIO Pins section.

The final steps in initiating an asynchronous capture into the data FIFO include enabling the FIFO and then starting the conversion clock. To enable the data FIFO in the general configuration register (see the General Configuration Register section, Address 0x1C), the FIFO_MODE bits must be set to immediate trigger mode (01). In this mode, the FIFO stores the results of the most recent FIFO_WATERMARK samples and then automatically disables capture into the memory. The results can then be accessed through the SPI data interface or LVDS interface.

When the FIFO is enabled, each conversion result is loaded on the rising edge of the convert start signal, CNV. Internal timing shows that FIFO_WATERMARK + three conversion clocks are required to write FIFO_WATERMARK sample results into the FIFO memory. For more details, see Figure 123 and Figure 124.

The Figure 122 timing diagram shows an example where FIFO_WATERMARK is set to 1000, and the first ADC result after the event occurred is captured by the FIFO after the third CNV. After N = 1000, that is, it has reached the FIFO_WATERMARK value, FIFO_FULL is asserted, and data stops being loaded into the FIFO.

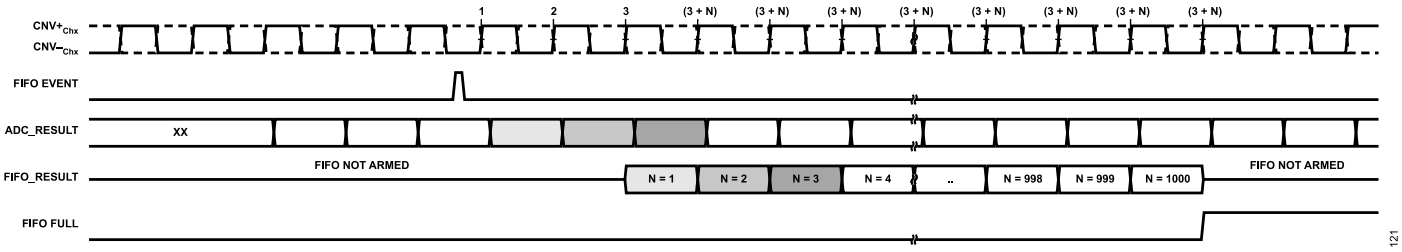

Figure 122. FIFO Data Capture Example, WATERMARK = 1000

DIGITAL FEATURES

Asynchronous Read Access

Access to the FIFO data is made through either a LVDS configuration (single lane only) or the multioutput SPI configuration of the data interface after the capture has completed. As a result, access is asynchronous to the capture process, and there are no specific timing restrictions between the conversion and interface clocks. Synchronization between the data FIFO and the data interface clock domain requires each read access to begin with a header followed by a transfer of M bytes of conversion data, where M equals the product of the total number of results specified in the FIFO_WATERMARK register (Address 0x1D and Address 0x1E) and the integer length in bytes (for SPI data interface) of a single conversion result. Note that the number of active data lanes reduces the access period by a factor of 2 for each doubling of the number of active lanes.

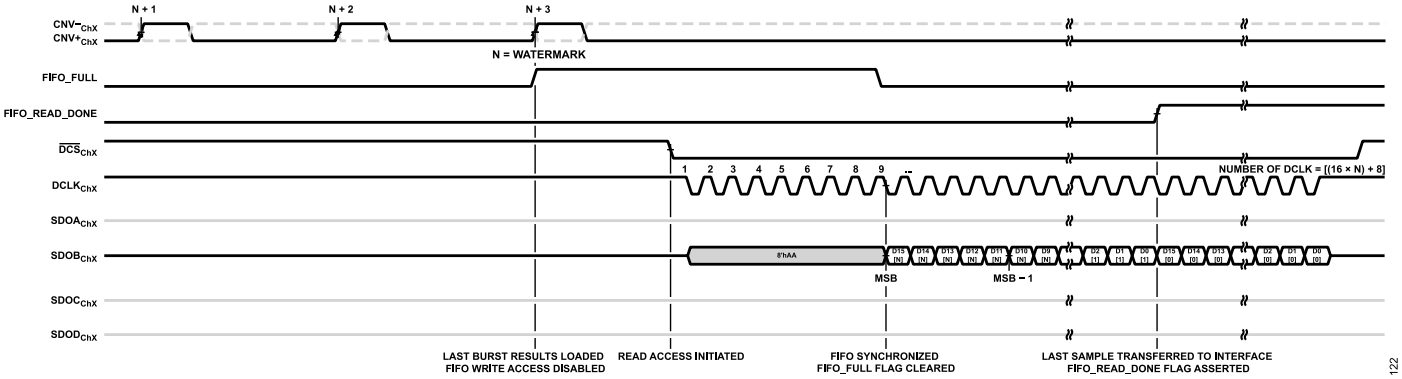

Figure 123. Asynchronous Capture Read Timing, Data FIFO Enabled, Single Data Lane

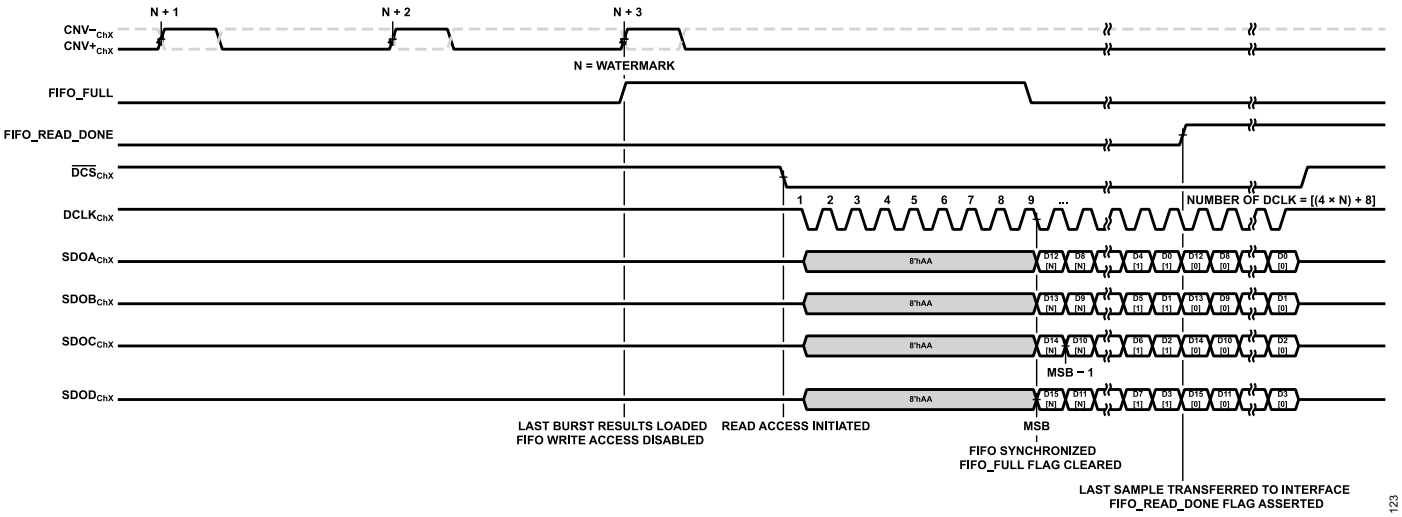

Figure 124. Asynchronous Capture Read Timing, Data FIFO Enabled, Quad Data Lane Configuration

DIGITAL FEATURES

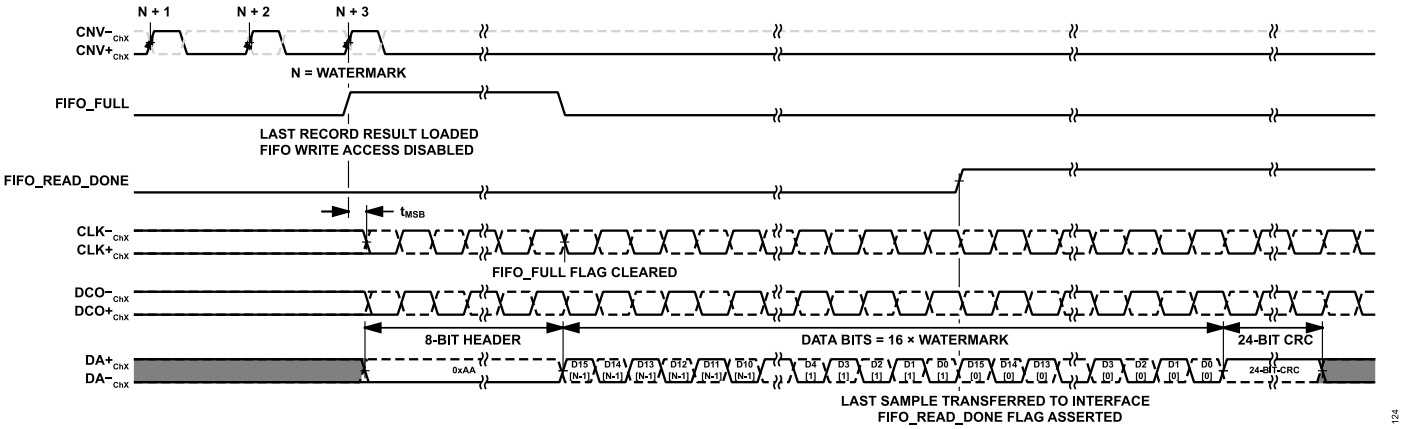

Figure 125. Asynchronous Capture Read Timing, Data FIFO Enabled, LVDS Configuration

DIGITAL FEATURES

FIFO Timing Considerations

Immediate Trigger Mode

Figure 127 shows the timing relationship between the command to arm the channel FIFO for data write access and the point at which the FIFO is armed. Figure 127 shows an example of where single lane SPI data access is configured and FIFO_FULL and FIFO_READ_DONE are output to GPIO. Because a capture has not yet been initiated, FIFO_FULL and FIFO_READ_DONE are driven low. A free running CNV clock is shown in this example. Upon receipt of the update to the general configuration register (Address 0x1C), the FIFO controller advances to an idle state on the next rising edge of CNV. The FIFO then advances to the writing state after two further CNV clock edges and begins filling the FIFO until WATERMARK results are loaded and FIFO_FULL is generated.

Upon completion of reading the FIFO data, a rearming event for immediate mode capture involves disabling the FIFO by writing 2'b00 to FIFO_MODE then re-enabling by writing 2'b01 to FIFO_MODE to arm the FIFO for a new capture. As is the case with the initial arming, the FIFO advances to the idle state upon receipt of the first rising edge of CNV after the configure instruction to arm the FIFO is issued. The sequence and timing is the same as for the initial FIFO arming. See Figure 127.

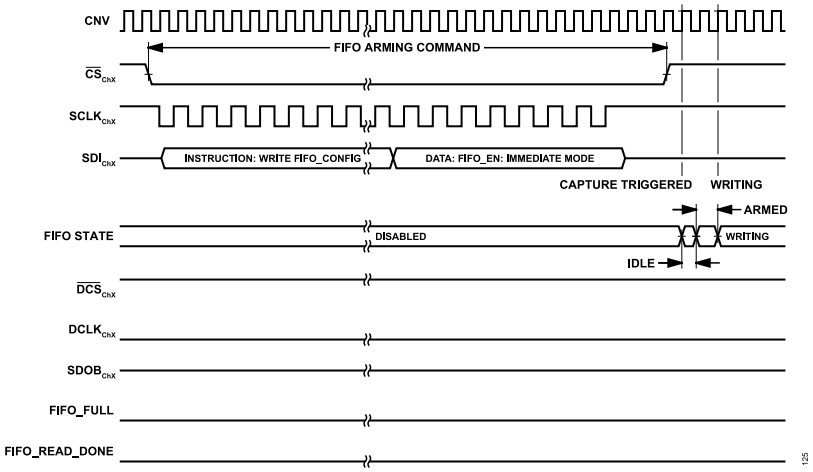

Figure 126. Immediate Trigger Mode Arming

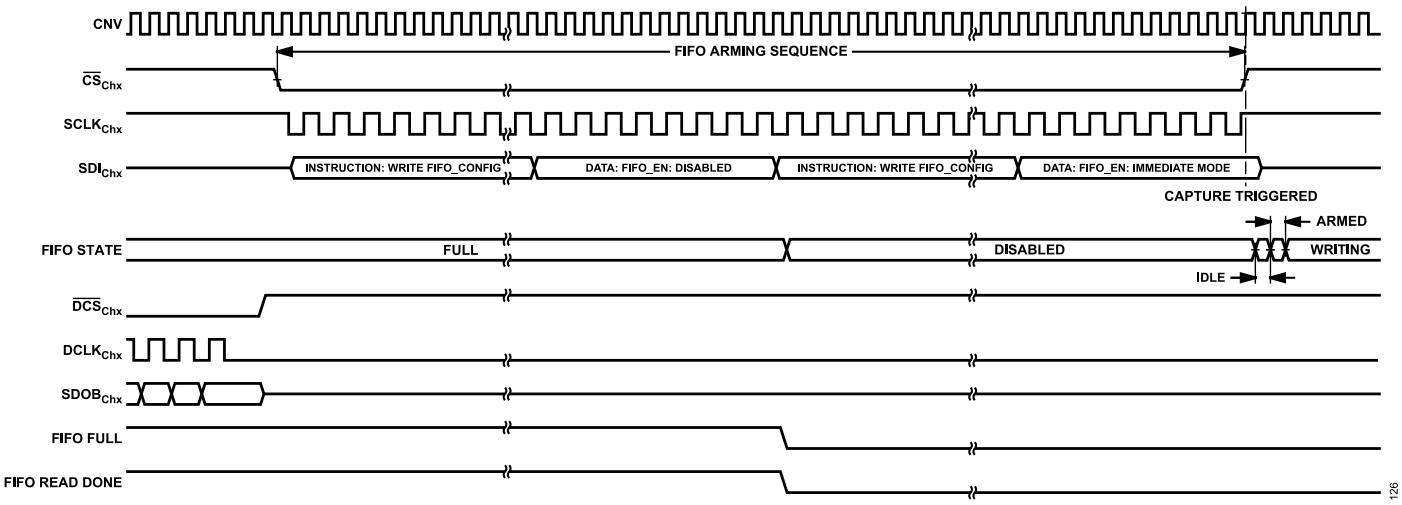

Figure 127. Immediate Trigger Mode Rearming

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Event Triggered Capture, Read Latest WATERMARK

Event triggered (read latest) mode is used where there is interest only in the ADC data after an event occurs. This event can be an internally generated event, where the AD4885 channel is running continuously, and the threshold detection is enabled to trigger an event as soon as an ADC input threshold is crossed. Or, the user can be independently monitoring the system or ADC input for an event, and an external event trigger is user-issued via a configured GPIO. As in all cases of arming the FIFO, the first rising edge after a FIFO_MODE write command arms the FIFO for data capture, however, no data is written to the FIFO until an event of the selected method occurs.

Rearming the trigger involves a similar process to the immediate mode rearming. The FIFO is firstly disabled by writing 2'b00 to the FIFO_MODE bits before, and then rearmed by again enabling the required capture mode.

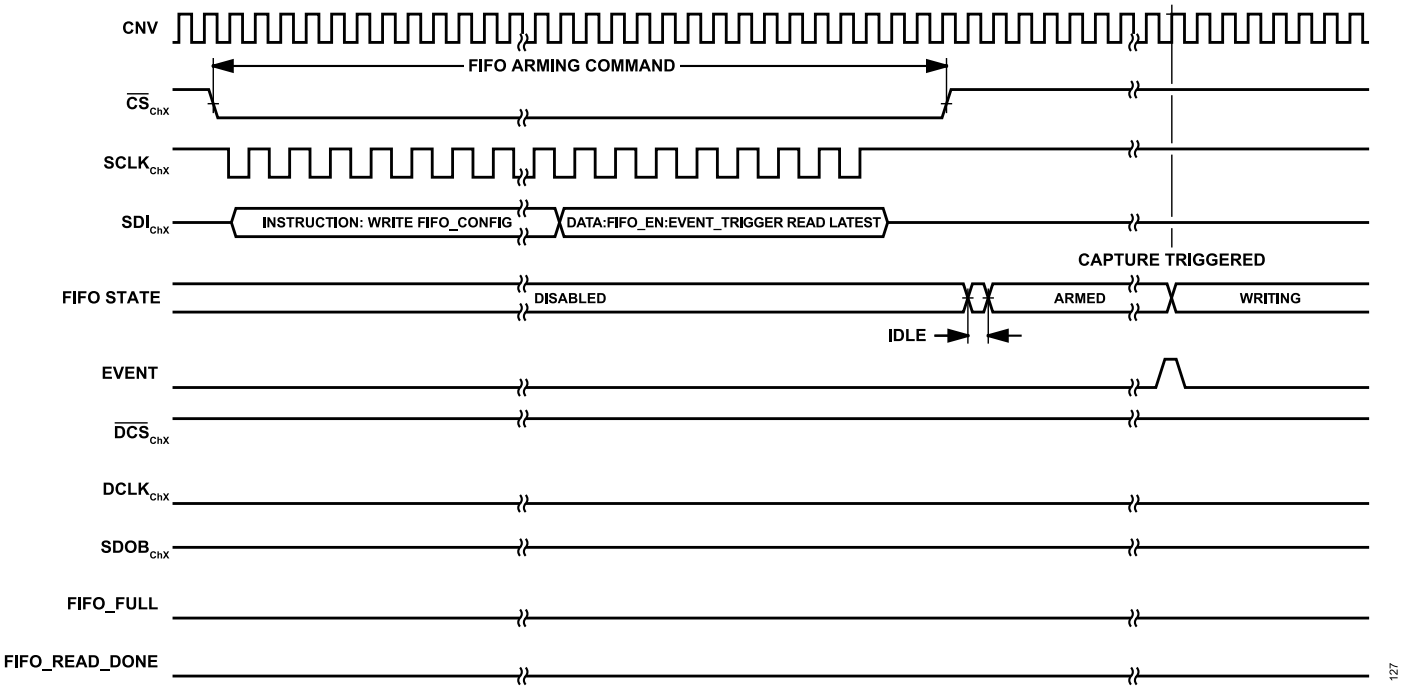

Figure 128. Event Triggered Capture, Read Latest WATERMARK Arming

DIGITAL FEATURES

Event Trigger Capture Mode, Read All FIFO

Event triggered mode can be used where ADC results immediately prior to the event, as well as those after, are of interest to the user. Once armed, the channel FIFO continuously fills with new ADC results, storing up to, at most, 16,384 of the most recent results, wrapping around and overwriting the oldest results in FIFO memory once 16,384 captures are made.

Once a trigger event occurs, the FIFO continues to capture WATERMARK number of results after the event. Only multiples of four are valid values to set the FIFO_WATERMARK register when using this mode. After an event has occurred, and the WATERMARK number of results has been captured in the FIFO, no further new results are captured until the FIFO is rearmed. The user must read back all 16,384 FIFO results, and the value set for FIFO_WATERMARK allows the user to determine where in the FIFO result data that the event occurred and also to distinguish between results that occurred before the event and those which occurred after the event, as shown in Figure 129 and Figure 130. In the full FIFO read back, the first result after the event triggered is located at 16384 − (FIFO_WATERMARK − 1), where FIFO_WATERMARK is the value set prior to arming the capture. If this capture mode is armed and an event occurs before the FIFO wraps around once, the FIFO results before the event contain either results from previous FIFO use or, when used for the first time after power cycling the device, the FIFO contains random data in the FIFO data locations before the event.

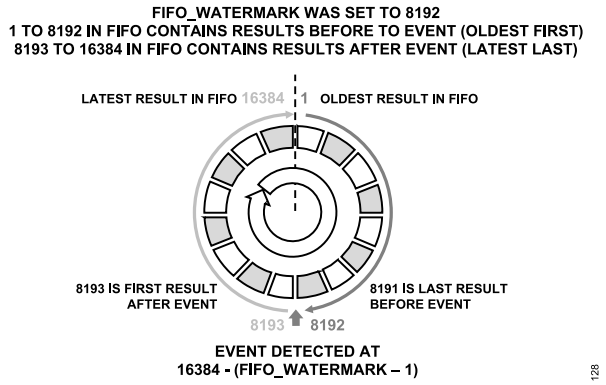

Figure 129. Event Capture Mode Read All FIFO Mode Example, FIFO Filling

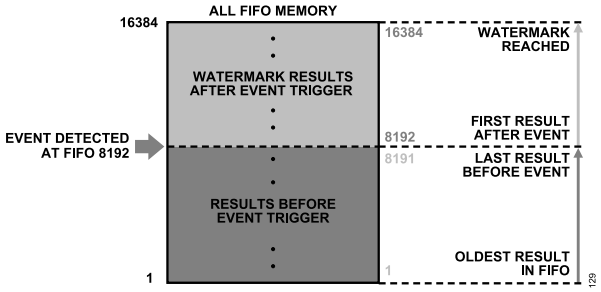

Figure 130. FIFO Event Capture Mode Read All FIFO Mode Example, Locating Event Position in FIFO

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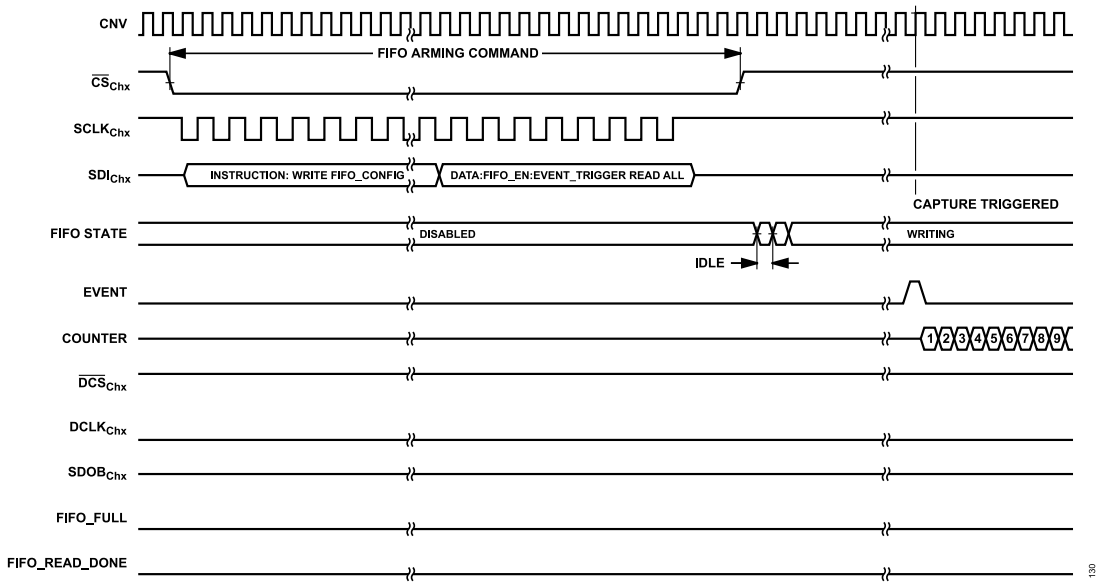

Figure 131. Event Trigger Capture Mode, Read All FIFO Rearming

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DIGITAL FILTER

Each AD4885 channel includes the option of enabling its integrated digital filter for applications where noise rejection by bandwidth limiting is required. As shown in Figure 132 and detailed as follows, there are four paths available by which to route digital data: no digital filtering, a sinc1 filter, a sinc5 filter, or a sinc5 compensated filter.

Further details on each of these filters are described in the following sections. To ensure the first filter result produces the correct data, when a user makes a change to the filter selection, a reset must be issued via the GPIO pin configured for filter synchronization (FILTER_SYNC).

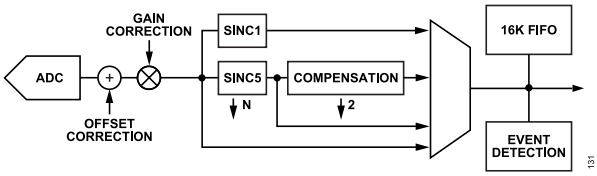

Figure 132. Digital Filter Selection Options

Benefits of Digital Filtering

The ADC result path of each channel can be configured to use the integrated digital filter feature. The filter configuration register (see the Filter Configuration Register section, Address 0x29) contains the FILTER_SEL bits that allow the user to bypass (default register setting) the digital filter or select from one of three filter options. Each filter has unique bandwidth profile properties, which allows high flexibility in allowing selection to be made depending on the end application requirements. Table 28 shows the −3dB bandwidths achievable for each user-selectable filter type. The SINC_DEC_RATE bits controls the bandwidth and the data decimation factor.

These filters allow the user to programmatically control the noise bandwidth of their signal chain and also can offer benefits by reducing the amount of filtering required in the analog front end, while offering dynamic range improvement without the need for additional components. The digital filter response sections have additional details on the different filter profiles that include the following:

- Sinc1 has a wider bandwidth but is not optimized for pass-band flatness.
- Sinc5 has a flatter pass-band response, however, with a reduced bandwidth.
- Sinc5 + compensation is a filter highly optimized to give excellent pass-band flatness with a ripple within ±0.1dB.

Table 28. Filter Bandwidth

Filter Type	SINC_DEC_RATE	Decimation	−3dB Bandwidth
Sinc1	0000	2	0.25 × f_S
Sinc1	0001	4	0.114 × f_S
Sinc1	0010	8	0.056 × f_S
Sinc1	0011	16	0.028 × f_S
Sinc1	0100	32	0.014 × f_S
Sinc1	0101	64	0.007 × f_S
Sinc1	0110	128	0.0035 × f_S
Sinc1	0111	256	0.0017 × f_s
Sinc1	1000	512	0.0009 × f_S
Sinc1	1001	1024	0.0004 × f_S
Sinc5	0000	2	0.117 × f_S
Sinc5	0001	4	0.0525 × f_S
Sinc5	0010	8	0.0256 × f_S
Sinc5	0011	16	0.0127 × f_S
Sinc5	0100	32	0.0064 × f_S
Sinc5	0101	64	0.0032 × f_S
Sinc5	0110	128	0.0016 × f_S
Sinc5	0111	256	0.0008 × f_S
Sinc5 + Compensation	0000	4	0.1015 × f_S
Sinc5 + Compensation	0001	8	0.0506 × f_S
Sinc5 + Compensation	0010	16	0.0253 × f_S
Sinc5 + Compensation	0011	32	0.0127 × f_S

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Table 28. Filter Bandwidth (Continued)

Filter Type	SINC_DEC_RATE	Decimation	−3dB Bandwidth
Sinc5 + Compensation	0100	64	0.0063 × f_S
Sinc5 + Compensation	0101	128	0.0032 × f_S
Sinc5 + Compensation	0110	256	0.0016 × f_S
Sinc5 + Compensation	0111	512	0.0008 × f_S

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Filter Decimation Configuration

Configuration of the digital filter of each channel is done through the corresponding filter configuration register (see the Filter Configuration Register section, Address 0x29). The FILTER_SEL bits select the active filtering path (that is, what filters are active), with each path having different allowed decimation rates (see Table 29).

Table 29. Digital Filters Decimation Options According to FILTER_SEL Bits Value

FILTER_SEL Bits Value	Active Filter	Allowed Decimation Rates
0b00	No filtering (default)	No decimation
0b01	SINC1 filter	2, 4, 8, 16, 32, 64, 128, 256, 512, 1024
0b10	SINC5 filter	2, 4, 8, 16, 32, 64, 128, 256
0b11	SINC5 + compensation filter	4, 8, 16, 32, 64, 128, 256, 512

The decimation factor is set via the SINC_DEC_RATE bits in the filter configuration register (see Table 62 for the encoding).

The readiness of new filter data can be indicated to the host controller via a GPIO pin by setting one of GPIO_x_SEL bits in either GPIO Configuration B register (see the GPIO Configuration B Register section, Address 0x1A) or GPIO Configuration C register (see the GPIO Configuration C Register section, Address 0x1B) to 0011 (filter result ready (active low)). Until new data is available to the interface, the data from the previous result remains in the output shift register. The user must ensure that the same LVDS clock rate is maintained, and the user can either reread or disregard the repeated result data, which is shown in Figure 133, where a decimate by 4 example is used.

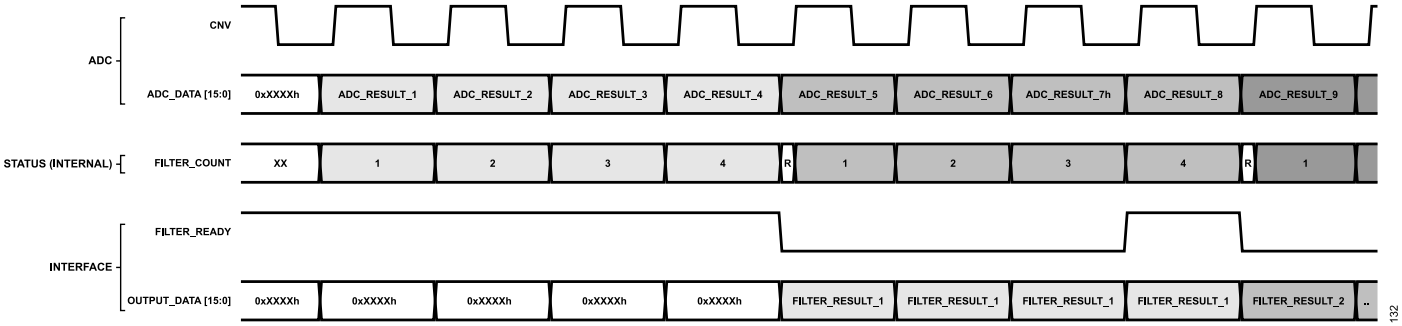

Figure 133. Digital Filter Decimate by 4 Frame Overview

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Filter Reset Conditions

Direct LVDS

When accessing the filtered data directly via the LVDS interface, the AD4885 resets the filter by the following two methods:

- By configuring the filter, by issuing a write to the filter configuration register, Bits[7:0] (see the Filter Configuration Register section, Address 0x29).
- By asserting a GPIO that is configured for $\overline{\text{FILTER_SYNC}}$ operation.

With FIFO

When the channel FIFO is enabled, the user must use a GPIO configured as $\overline{\text{FILTER_SYNC}}$ to reset the filter for each FIFO acquisition.

Filter Synchronization

Set GPIO_x_SEL to $\overline{\text{FILTER_SYNC}}$ to configure this input providing synchronization to the controller of the user, which can be used to synchronize the filters across both channels of AD4885 or across multiple AD4885 devices. The $\overline{\text{FILTER_SYNC}}$ signal timing requirements for a filter reset are shown in Figure 134.

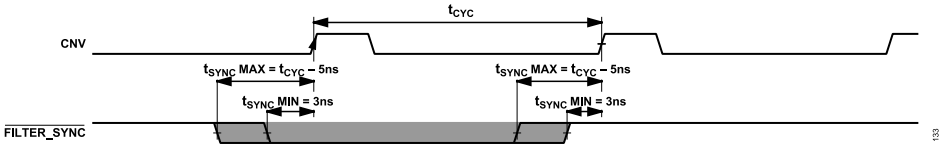

Figure 134. Filter Reset Timing

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Filter Result Ready Indicator

Setting the GPIO_x_SEL bits to 0011 configures the GPIO to output the $\overline{\text{FILTER_RESULT_RDY}}$ signal, which is an active low logic signal that indicates to the host controller when each new filter result from the channel is complete. When LVDS is used to directly read out the filter results, this indicator can alert the user when each new filtered conversion result is available to read via the interface.

Filter Interface Timing Considerations

Continuous access to filtered data results of a channel is available only through its LVDS data interface. SPI data interface access to filtered results is only made via the FIFO. The timing considerations, in this case, are described in the Filter Interface Timing Considerations When Using the FIFO section. For use with the LVDS data interface, it is recommended to use a GPIO, configured with the appropriate GPIO_x_SEL (0011) to output the filter result ready (active low) signal, as shown in the example Figure 133 timing diagram.

Filter Interface Timing Considerations When Using the FIFO

Figure 135 serves as an example to show the sequence of events in this mode of operation. This example shows a sinc1 filter with a decimate by 2 setting, where three results (that is, WATERMARK = 3) are configured to be stored in the FIFO. When using the integrated digital filters with the FIFO, the filter must be reset prior to each FIFO acquisition record. This reset must be given on the first CNV_{ChX} rising edge, where the $\overline{\text{FILTER_SYNC}}$ signal must be brought low at least 15ns prior to the CNV_{ChX} edge and then released at least 5ns before the next rising edge. The first ADC result is ready t_{MSB} after the second CNV_{ChX} rising edge. This first ADC result is latched into the filter on the third CNV_{ChX} rising edge. The fourth CNV_{ChX} rising edge latches the second ADC result into the digital filter. On the fifth rising edge, the first decimate by 2 result is complete, which is indicated by the FILTER_READY signal going active on the fifth rising edge. This first filtered result is loaded into the FIFO on the sixth CNV_{ChX} rising edge. Because this example uses WATERMARK = 3, when three filtered (that is, six core ADC results, decimated by 2) results are loaded to the FIFO, the WATERMARK is reached, and FIFO_FULL is asserted to indicate to the user that a FIFO record is available to read via the configured data interface (that is, the LVDS data lane(s) of the SPI data lane(s)). To initiate a subsequent FIFO record acquisition of the filtered ADC results, the user must start the whole sequence over, beginning again with the reset of the digital filter by bringing the $\overline{\text{FILTER_SYNC}}$ signal low on the first rising edge of CNV_{ChX}.

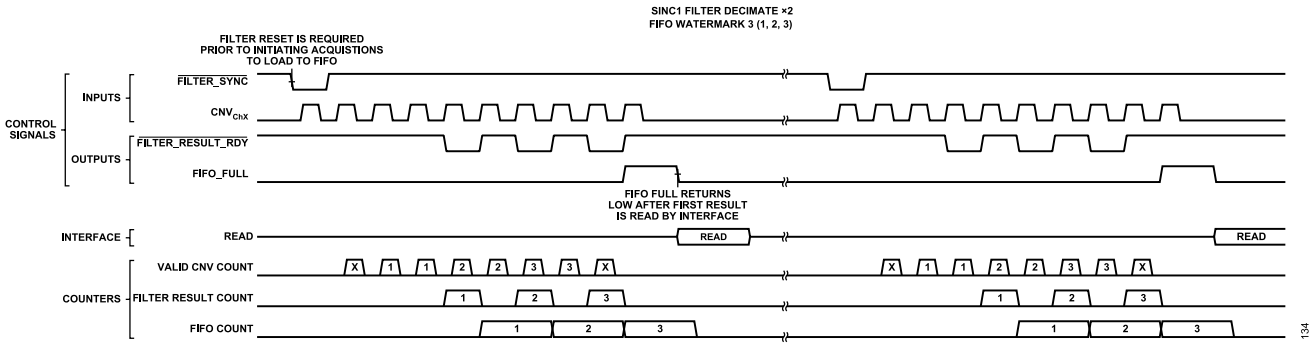

Figure 135. Description of Filter Timing with FIFO

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Digital Filter Conversion Pulses

The total number of CNV_{ChX} pulses required for a single filter decimated result (sinc1 settling clocks) can be calculated using the following formula:

$$Settling\ CNV\ Pulses_{SINC1} = 2 + (D + 1)$$

Note that each of the three filter types has a unique formula to determine the number of clocks required.

For the sinc5 settling clocks, the equation is as follows:

$$Settling\ CNV\ Pulses_{SINC5} = 2 + (5 \times D + 4)$$

For the sinc5 with compensation settling clocks, the equation is as follows:

$$Settling\ CNV\ Pulses_{SINC5+COMP} = 2 + (35 \times D + 10)$$

Where *D* equals the decimation rate 2, 4, 8 …

Digital Filtering Settling Time

The settling time for the selected filter is the number of settling clocks times t_{CONV}, as follows:

$$Filter\ Settling\ Time = (Settling\ CNV\ Pulses_{FILTERTYPE} FILTERTYPE) \times t_{CONV}$$

Digital Filtering Settling Time when Using FIFO

When using the FIFO with filtered data, it is important to note that each new FIFO record of results must begin by issuing a $\overline{\text{FILTER_SYNC}}$ signal on the first CNV_{ChX} to reset and initialize the filter and to prevent unflushed data from being contained in the first FIFO record result.

The minimum total number of conversion pulses required to fill a full FIFO record can be calculated as follows:

$$Total\ Required\ CNVs = (D \times WATERMARK) + Settling\ CNV\ Pulses_{FILTERTYPE}$$

Where *D* equals the decimation rate 2, 4, 8 …

Digital Filter Response

Sinc1 Filter

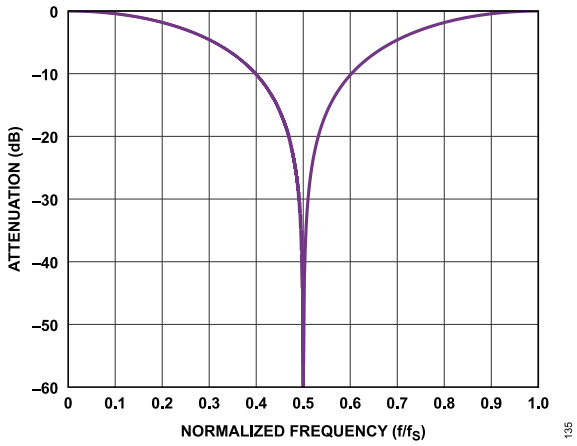

Figure 136. Sinc1 Filter Response, Decimate by 2

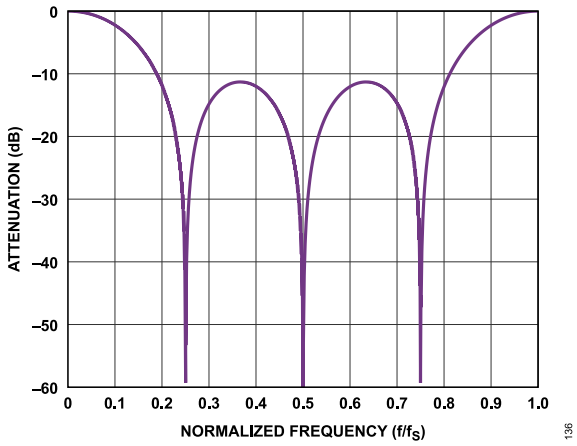

Figure 137. Sinc1 Filter Response, Decimate by 4

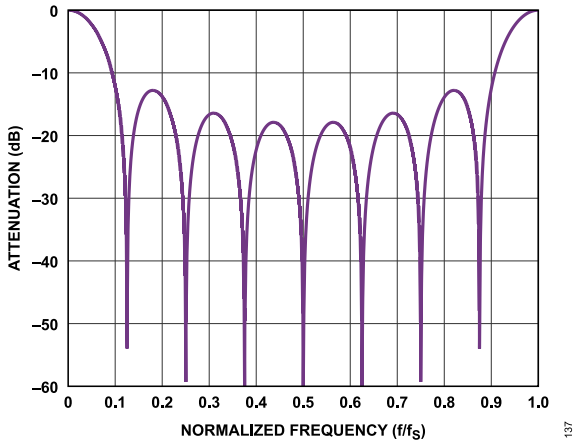

Figure 138. Sinc1 Filter Response, Decimate by 8

DIGITAL FEATURES

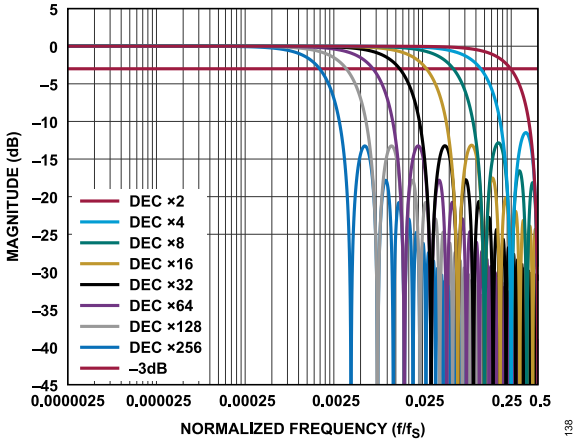

Figure 139. Sinc1 Filter Response, All Decimation Rates

Sinc5 Filter

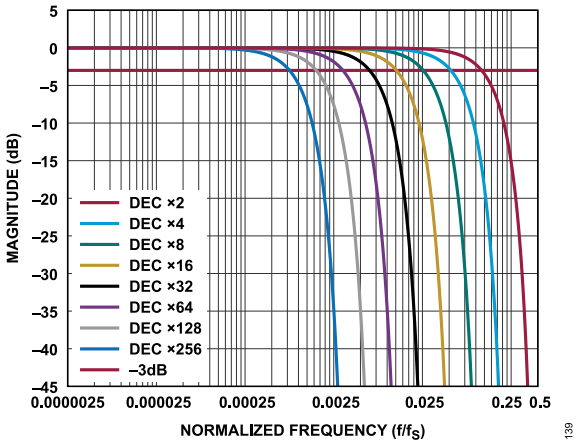

Figure 140. Sinc5 Filter Response, All Decimation Rates

Filter Sinc5 + Compensation Filter

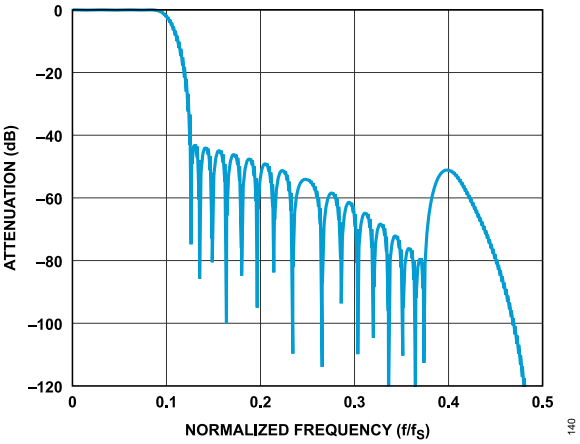

Figure 141. Sinc5 + Compensation Filter Response, Decimate by 2

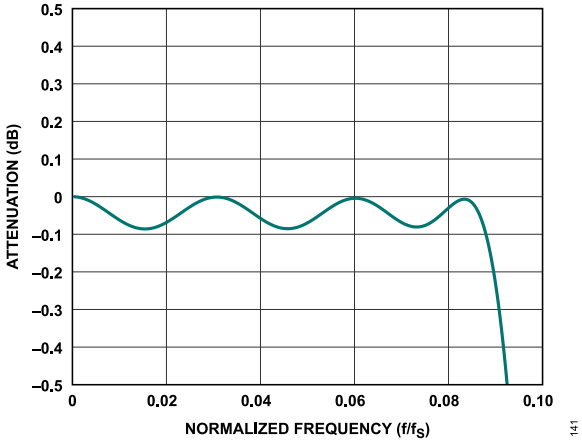

Figure 142. Sinc5 + Compensation Filter Response, Decimate by 2, Pass-Band Ripple

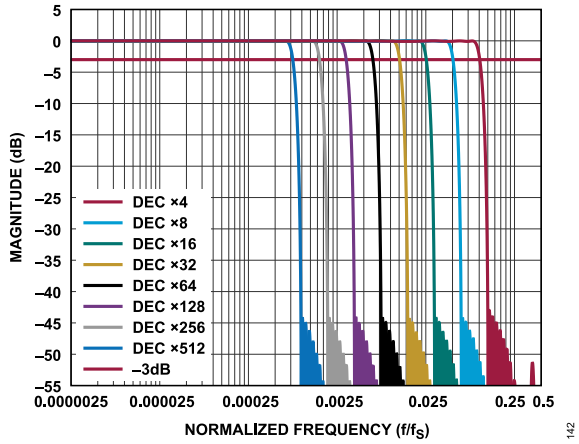

Figure 143. Sinc5 + Compensation Filter Response

DIGITAL FEATURES

SYSTEM ERROR CORRECTION COEFFICIENTS

Systematic gain and offset errors exist in all practical data acquisition circuits, and thus, the need for correction is essential to maximize the precision of the measurement channel. While these quantities can be corrected for in the host processor, implementation can be inefficient and consume more power than if integrated within the data converter. To minimize these challenges for the end user, the AD4885 has integrated both gain and offset correction on a per sample basis.

To describe the available error corrections, consider that the transfer function of an ideal ADC can be described by the straight line equation:

$y = mx + c$

This equation can be applied to the ADC transfer function, where:
y is the corrected ADC result.
m is the gain or slope of the line.
x is the uncorrected ADC result.
c is the offset.

The gain or slope of the line can be described as follows:

$m = (y2 - y1)/(x2 - x1)$

where the following are in volts:
y2 is the input voltage at close to the positive full-scale input.
y1 is the input voltage at close to the negative full-scale input.
x2 is the converted voltage with the y2 voltage applied at the input.
x1 is the converted voltage with the y1 voltage applied at the input.

The ideal slope or gain is m = 1V/V

The system error correction coefficients in the Offset Error Correction and Gain Error Correction sections detail how signal chain errors in offset (c) and gain (m) can be corrected using the configuration registers of each AD4885 channel.

Offset Error Correction

The AD4885 is factory calibrated for low zero error. To account for system offset errors that may be present in the analog signal chain in front of a channel, an offset error correction functionality is provided. The correction value to be applied is written to the OFFSET bit field in the offset correction register of the corresponding channel (see the Offset Correction Register, Address 0x25 and 0x26).

The OFFSET bit field is a 12-bit value in twos complement data format. The LSB size for this field is the same as the ADC conversion LSB (91.55µV). The range for offset error correction is therefore +2047 × LSB (0x7FF) to −2048 × LSB (0x800). This shows an offset correction voltage range between +187.4mV and −187.5mV. The default value for the OFFSET bit field, after power on, or after a software reset, is 0x000, which shows the zero offset correction applied.

Gain Error Correction

The AD4885 is factory calibrated to minimize its intrinsic gain error. To account for system gain errors introduced by the analog signal chain in front of a channel, a gain error correction functionality is provided. The gain correction factor to be applied depends on the value written to the GAIN bit field in the gain correction register of the corresponding channel (see the Gain Correction Register, Address 0x27 and 0x28).

The GAIN bit field is a 10-bit value that allows a nominal gain error correction of ±1.5594% of full scale. The 10-bit register is coded in a straight binary data format, the gain error can be adjusted with a resolution of 1.5594%/512 = 0.00305%. A value of 0x3FF results in a gain correction factor of 1.0 + 0.015594, and a value of 0x001 results in a gain correction factor of 1.0 − 0.015594. The default value after power on, or software reset, is 0x200. This value shows no gain error correction being applied to the ADC results, and allows for lower latency operation (see ADC Result Latency and LVDS Interface Alignment).

To determine the system gain error that must be applied, the user can perform a two-point voltage measurement with gain error correction disabled, preferably close to positive and negative full-scale inputs, and use the slope or gain equation in the System Error Correction Coefficients.

LAYOUT GUIDELINES

The AD4885 includes all critical bypass capacitors within the device package, which along with the integration of the FDAs greatly reduces the layout challenge for a precision, high-speed converter. The integrated capacitors are optimally placed within the device package to ensure that maximum performance is easily obtained. However, as with any precision mixed signal device, a user must take care in system device placement to ensure that there is proper partitioning of the critical analog signal chain component routing and routing of the high-speed digital signals to prevent unwanted coupling effects.

Note the following layout considerations:

- The summing junction pins ($SJ\pm_{ChX}$) and output pins ($OUT\pm_{ChX}$) of the FDA must be treated carefully because of their sensitivity. Most applications benefit from restricting the bandwidth of the FDA by the placement of external capacitors (C_{fb}) across these pins, in parallel to the internal 2.7pF ones. These capacitors must be placed on the bottom layer right below the connection points to minimize trace inductance, as even relatively small parasitics can potentially degrade the characteristics of the FDA. Unnecessary trace stubs must be avoided for these sensitive nodes.
- The AD4885 contains internal decoupling on all power supplies, AVDD33 (0.47µF), $VDD11_{ChA}$ and $VDD11_{ChB}$ (1.88µF each), $IOVDD_{ChA}$ and $IOVDD_{ChB}$ (0.22µF each), VDDLDO (0.22µF), $+V_S$ (0.44µF) and $-V_S$ (0.44µF). Therefore, no external bypass capacitors are required, saving board space and reducing bill of material (BOM) count and sensitivity.
- Ensure good partitioning of analog and digital domain signals within the design by, for example, having all analog signals in from the left-hand side and keeping dynamic digital signals on the right-hand side.
- Have a solid ground plane under the AD4885 and connect all analog ground (GND) pins, reference ground (REFGND), and digital ground (IOGND) pins to this shared plane.
- Recommended connections of ground (GND), reference ground (REFGND), and digital ground (IOGND) connections are shown in Figure 144. It is recommended not to keep the current return path of the reference IC in the same current loop as the current return loop from other circuitry on the PCB. Connect the reference local star point to the ADC star point ground on the top layer of the PCB, as shown in Figure 144.
- For the side view cross-section of the PCB board showing the ground planes distribution, see Figure 145. Note that Figure 145 only shows the ground planes but does not include the signal tracks.

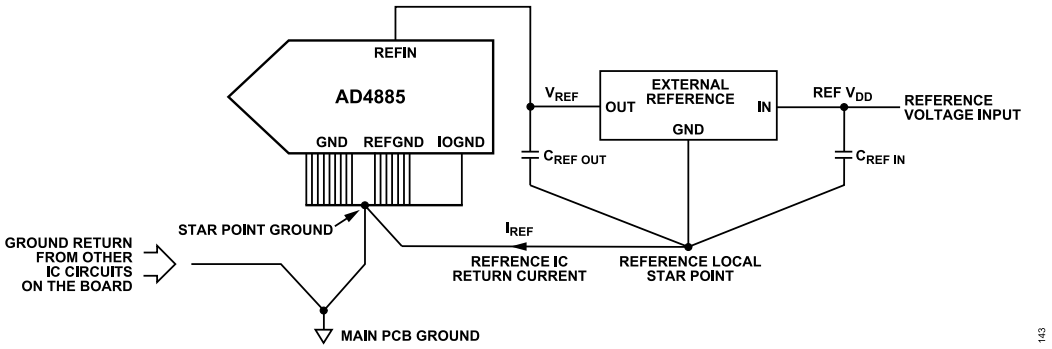

Figure 144. AD4885 External Reference Ground Connections

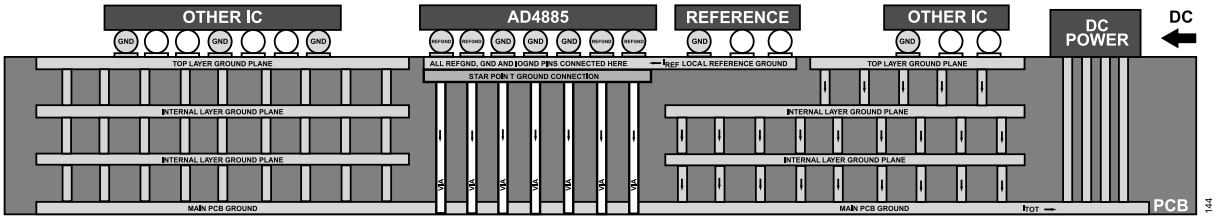

Figure 145. Recommended PCB Ground Planes Layout

CONFIGURATION REGISTERS

The features of the AD4885 family have been designed to simplify the application of low latency data capture to a broad array of measurement applications. This simplification is achieved through customization of the data interface, data path, and data access method for each channel, to satisfy both measurement and the host processor interface requirements via the available configuration registers.

Each channel has its own independent configuration memory, accessible through its separate configuration SPI interface. The register space of each channel is organized in contiguous regions by function to streamline device configuration as described in Table 30. As a result, the interface streaming functions (see Instruction Mode Selection section) can be leveraged to simplify device configuration to a single SPI frame consisting of an instruction word and associated data. For most applications, modifications to the register space address range of Address 0x15 to Address 0x29 are sufficient. Modification of content in the configuration interface and product ID space (Address 0x00 to Address 0x11) is only necessary to initiate a software reset or to change the configuration access method. Note that changes to the configuration access method are outside the scope of this document. For assistance with these options, contact the local Analog Devices, Inc., sales office at www.analog.com/sales, or submit a request for technical assistance through the **Precision ADCs** page on the *ADI Engineer Zone*.

Table 30. Register Map Organization

Address Range	Function
0x00 to 0x11	Configuration interface and Product ID
0x14	Device status
0x15 to 0x17	Interface configuration
0x18 to 0x1B	Power and GPIO configuration
0x1C	General configuration
0x1C to 0x1E	FIFO configuration
0x1F to 0x24	Internal event detection
0x25 to 0x28	System error correction
0x29	Digital filter configuration

This section contains details about the functions of each of the bit fields. The access column in the register tables specifies whether the bit fields are read-only (R), read/write (R/W), or write-1-to-clear (R/W1C) bits.

Table 31. Configuration Register Summary—Configuration Interface Functions (Address 0x00 to Address 0x11)

Addr	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x00	INTERFACE_CONFIG_A	[7:0]	SW_RESET	RE-SERVED	ADDR_ASCENSION	SDO_ENABLE	RESERVED			SW_RESETX	0x10	R/W
0x01	INTERFACE_CONFIG_B	[7:0]	SINGLE_INST	RESERVED			SHORT_INSTRUC-TION	RESERVED			0x00	R/W
0x02	DEVICE_CONFIG	[7:0]	RESERVED						OPERATING_MODES		0x00	R/W
0x03	CHIP_TYPE	[7:0]	RESERVED				CHIP_TYPE				0x07	R
0x04	PRODUCT_ID_L	[7:0]	PRODUCT_ID[7:0]								0x5D	R
0x05	PRODUCT_ID_H	[7:0]	PRODUCT_ID[15:8]								0x00	R
0x06	CHIP_GRADE	[7:0]	GRADE				DEVICE_REVISION				0x02	R
0x0A	SCRATCH_PAD	[7:0]	SCRATCH_VALUE								0x00	R/W
0x0B	SPI_REVISION	[7:0]	SPI_TYPE		VERSION						0x83	R
0x0C	VENDOR_L	[7:0]	VID[7:0]								0x56	R
0x0D	VENDOR_H	[7:0]	VID[15:8]								0x04	R
0x0E	STREAM_MODE	[7:0]	LOOP_COUNT								0x00	R/W
0x0F	TRANSFER_CONFIG	[7:0]	RESERVED					KEEP_STREAM_	RESERVED		0x00	R/W

CONFIGURATION REGISTERS

Table 31. Configuration Register Summary—Configuration Interface Functions (Address 0x00 to Address 0x11) (Continued)

Addr	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
								LENGTH_VAL				
0x10	INTERFACE_CONFIG_C	[7:0]	CRC_ENABLE		STRICT_REGISTER_ACCESS	SEND_STATUS	ACTIVE_INTERFACE_MODE		CRC_ENABLEB		0x23	R/W
0x11	INTERFACE_STATUS_A	[7:0]	NOT_READY_ERR	RESERVED		CLOCK_COUNT_ERR	CRC_ERR	WR_TO_RD_ONLY_REG_ERR	REGISTER_PARTIAL_ACCESS_ERR	ADD-RESS_INVALID_ERR	0x00	R/W
0x14	DEVICE_STATUS	[7:0]	FIFO_FULL	FIFO_READ_DONE	HI_STATUS	LO_STATUS	POR_ANA_FLAG	ADC_CNV_ERR	ROM_CRC_ERR	POR_FLAG	0x09	R/W
0x15	ADC_DATA_INTF_CONFIG_A	[7:0]	RE-SERVED	RE-SERVED	RESERVED	INTF_CHK_EN	RESERVED	SPI_LVDS_LANES	RESERVED	DATA_INTF_MODE	0x40	R/W
0x16	ADC_DATA_INTF_CONFIG_B	[7:0]	LVDS_CNV_CLK_CNT				LVDS_SELF_CLK_MODE	LVDS_MNC_EN	RESERVED	LVDS_CNV_EN	0x00	R/W
0x17	ADC_DATA_INTF_CONFIG_C	[7:0]	LVDS_RX_CURRENT	LVDS_VOD			RESERVED				0x20	R/W
0x18	PWR_CTRL	[7:0]	RESERVED						ANA_DIG_LDO_PD	INTF_LDO_PD	0x00	R/W
0x19	GPIO_CONFIG_A	[7:0]	GPIO_3_DATA	GPIO_2_DATA	GPIO_1_DATA	GPIO_0_DATA	GPO_3_EN	GPO_2_EN	GPO_1_EN	GPO_0_EN	0x01	R/W
0x1A	GPIO_CONFIG_B	[7:0]	GPIO_1_SEL				GPIO_0_SEL				0x00	R/W
0x1B	GPIO_CONFIG_C	[7:0]	GPIO_3_SEL				GPIO_2_SEL				0x00	R/W
0x1C	GENERAL_CONFIG	[7:0]	INT_EVENT_EN	HI_ROUTE	LO_ROUTE	ADC_CNV_ERR_ROUTE	RESERVED		FIFO_MODE		0x00	R/W
0x1D	FIFO_WATERMARK	[7:0]	FIFO_WATERMARK[7:0]								0x00	R/W
0x1E		[15:8]	RE-SERVED	FIFO_WATERMARK[14:8]							0x40	R/W
0x1F	EVENT_HYSTERESIS	[7:0]	HYSTERESIS[7:0]								0x00	R/W
0x20		[15:8]	RESERVED					HYSTERESIS[10:8]			0x00	R/W
0x21	EVENT_DETECTION_HI	[7:0]	HI_THRESHOLD[7:0]								0x00	R/W
0x22		[15:8]	RESERVED				HI_THRESHOLD[11:8]				0x00	R/W
0x23	EVENT_DETECTION_LO	[7:0]	LO_THRESHOLD[7:0]								0x00	R/W
0x24		[15:8]	RESERVED				LO_THRESHOLD[11:8]				0x00	R/W
0x25	OFFSET	[7:0]	OFFSET[7:0]								0x00	R/W
0x26		[15:8]	RESERVED				OFFSET[11:8]				0x00	R/W
0x27	GAIN	[7:0]	GAIN[7:0]								0x00	R/W
0x28		[15:8]	RESERVED						GAIN[9:8]		0x02	R/W
0x29	FILTER_CONFIG	[7:0]	RE-SERVED	SINC_DEC_RATE				RESERVED	FILTER_SEL		0x00	R/W

CONFIGURATION REGISTERS

REGISTER DETAILS
Interface Configuration A Register

Address: 0x00, Reset: 0x10, Name: INTERFACE_CONFIG_A

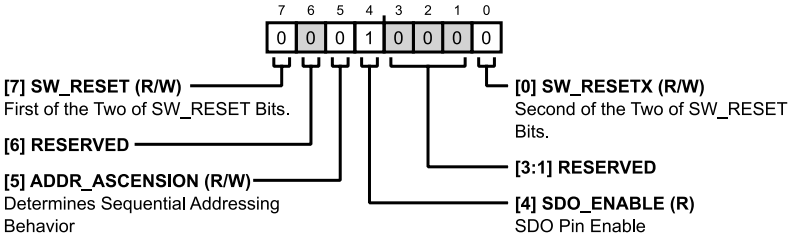

Figure 146. Interface Configuration A Settings

Table 32. Bit Descriptions for INTERFACE_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RESET	First of the Two SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written to at the same time to trigger a software reset of the device. This action returns any previously configured registers to their default settings, except for the ADDR_ASCENSION bit from the Interface Configuration A Register, which keeps its previous value. Only use this reset method once the channel is in an idle state, where conversions are not being clocked, and any existing conversions are completed.	0x0	R/W
6	RESERVED	Reserved. Write 0 to this bit.	0x0	R
5	ADDR_ASCENSION	Determines Sequential Addressing Behavior. 0: Address is decremented by one when streaming. 1: Address is Incremented by one when streaming.	0x0	R/W
4	SDO_ENABLE	SDO Pin Enable.	0x1	R
[3:1]	RESERVED	Reserved. Write 000 to these bits.	0x0	R
0	SW_RESETX	Second of the Two SW_RESET Bits. This bit appears in two locations in this register. Both locations must be written to at the same time to trigger a software reset of the device. This action returns any previously configured registers to their default settings, except for the ADDR_ASCENSION bit from the Interface Configuration A Register, which keeps its previous value. Only use this reset method once the channel is in an idle state, where conversions are not being clocked, and any existing conversion are completed.	0x0	R/W

CONFIGURATION REGISTERS

Interface Configuration B Register

Address: 0x01, Reset: 0x00, Name: INTERFACE_CONFIG_B

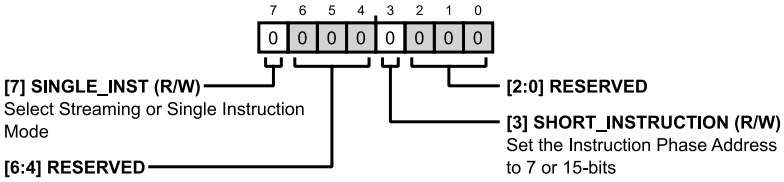

Figure 147. Additional Interface Configuration B Settings

Table 33. Bit Descriptions for INTERFACE_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	SINGLE_INST	Select Streaming or Single Instruction Mode. 0: Streaming mode is enabled. The address increments or decrements as successive data bytes are received. 1: Single instruction mode is enabled.	0x0	R/W
[6:4]	RESERVED	Reserved. Write 0b000 to these bits.	0x0	R
3	SHORT_INSTRUCTION	Set the Instruction Phase Address to 7 or 15 bits. 0: 15-Bit Addressing. 1: 7-Bit Addressing.	0x0	R/W
[2:0]	RESERVED	Reserved. Write 0b000 to these bits.	0x0	R

Device Configuration Register

Address: 0x02, Reset: 0x00, Name: DEVICE_CONFIG

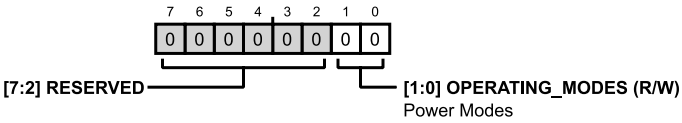

Figure 148. Device Configuration Register

Table 34. Bit Descriptions for DEVICE_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved. Write 0b000000 to these bits.	0x0	R
[1:0]	OPERATING_MODES	Channel Power Mode. 00: Normal Operating Mode. 10: Standby Operating Mode. 11: Sleep Mode.	0x0	R/W

CONFIGURATION REGISTERS

Chip Type Register

Address: 0x03, Reset: 0x07, Name: CHIP_TYPE

The chip type is used to identify the family of Analog Devices devices a given device belongs to. CHIP_TYPE must be used in conjunction with the Product ID to uniquely identify a given product.

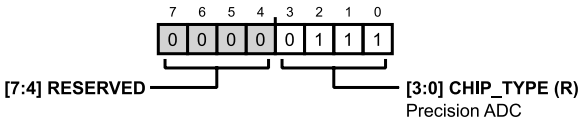

Figure 149. Chip Type Register

Table 35. Bit Descriptions for CHIP_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	CHIP_TYPE	Precision ADC.	0x7	R

Product ID Low Register

Address: 0x04, Reset: 0x5D, Name: PRODUCT_ID_L

This register is the low byte of the Product ID.

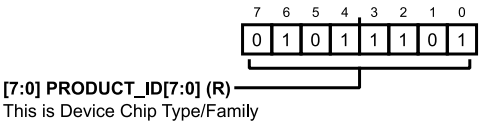

Figure 150. Product ID Low Register

Table 36. Bit Descriptions for PRODUCT_ID_L

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product Identification. These bits are the device chip type/family. The PRODUCT_ID must be used in conjunction with CHIP_TYPE to identify a product.	0x5D	R

Product ID High Register

Address: 0x05, Reset: 0x00, Name: PRODUCT_ID_H

This register is the high byte of the Product ID.

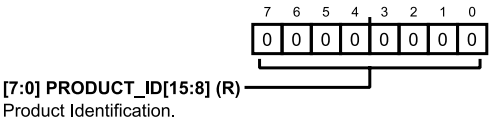

Figure 151. Product ID High Register

Table 37. Bit Descriptions for PRODUCT_ID_H

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product Identification. These bits are the device chip type and family. The PRODUCT_ID must be used in conjunction with CHIP_TYPE to identify a product.	0x0	R

CONFIGURATION REGISTERS

Chip Grade Register

Address: 0x06, Reset: 0x02, Name: CHIP_GRADE

This register identifies product variations and device revisions.

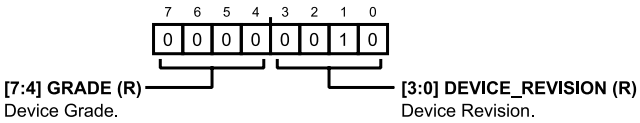

Figure 152. Chip Grade Register

Table 38. Bit Descriptions for CHIP_GRADE

Bits	Bit Name	Description	Reset	Access
[7:4]	GRADE	Device Grade. These bits are the device performance grade.	0x0	R
[3:0]	DEVICE_REVISION	Device Revision. These bits are the device hardware revision.	0x2	R

Scratch Pad Register

Address: 0x0A, Reset: 0x00, Name: SCRATCH_PAD

This register can be used to test writes and reads.

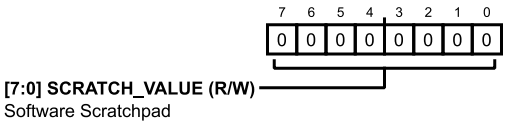

Figure 153. Scratch Pad Register

Table 39. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Software can write to and read from this location without any device side effects.	0x0	R/W

SPI Revision Register

Address: 0x0B, Reset: 0x83, Name: SPI_REVISION

This register indicates the SPI revision.

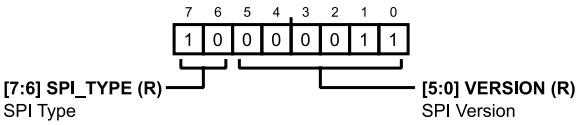

Figure 154. SPI Revision Register

Table 40. Bit Descriptions for SPI_REVISION

Bits	Bit Name	Description	Reset	Access
[7:6]	SPI_TYPE	SPI Type. These bits always read as 0x2.	0x2	R
[5:0]	VERSION	SPI Version. 11: Revision 1.1.	0x3	R

CONFIGURATION REGISTERS

Vendor ID Low Register

Address: 0x0C, Reset: 0x56, Name: VENDOR_L

This register is the low byte of the Vendor ID.

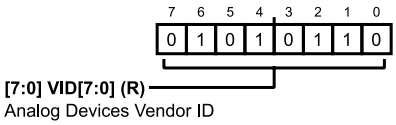

Figure 155. Vendor ID Low Register

Table 41. Bit Descriptions for VENDOR_L

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[7:0]	Analog Devices Vendor ID.	0x56	R

Vendor ID High Register

Address: 0x0D, Reset: 0x04, Name: VENDOR_H

This register is the high byte of the Vendor ID.

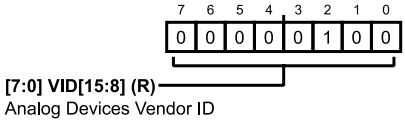

Figure 156. Vendor ID High Register

Table 42. Bit Descriptions for VENDOR_H

Bits	Bit Name	Description	Reset	Access
[7:0]	VID[15:8]	Analog Devices Vendor ID.	0x4	R

Stream Mode Register

Address: 0x0E, Reset: 0x00, Name: STREAM_MODE

This mode is not supported.

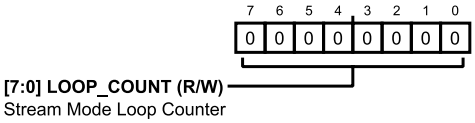

Figure 157. Stream Mode Register

Table 43. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Stream Mode Loop Counter. These bits set the data byte count before looping to the start address. When streaming data, a nonzero value sets the number of data bytes written before the address loops back to the start address. A maximum of 255 bytes can be written using this approach. A value of 0x00 disables the loop back so that addressing wraps around at the upper and lower limits of the memory. After writing to this register, the loop value applies only to the next SPI instruction and auto clears upon the end of that instruction.	0x0	R/W

CONFIGURATION REGISTERS

Transfer Configuration Register

Address: 0x0F, Reset: 0x00, Name: TRANSFER_CONFIG

This register controls how data moves between the controller and the target registers.

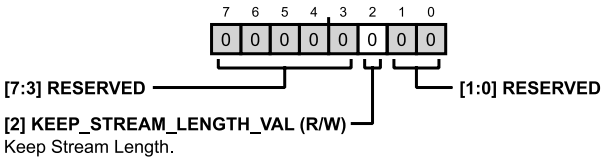

Figure 158. Transfer Configuration Register

Table 44. Bit Descriptions for TRANSFER_CONFIG

Bits	Bit Name	Description	Reset	Access
[7:3]	RESERVED	Reserved. Write 0b00000 to these bits.	0x0	R
2	KEEP_STREAM_LENGTH_VAL	Keep Stream Length. When set, the loop counter does not reset on the $\overline{CS}$ rising edge.	0x0	R/W
[1:0]	RESERVED	Reserved. Write 0b00 to these bits.	0x0	R

Interface Configuration C Register

Address: 0x10, Reset: 0x23, Name: INTERFACE_CONFIG_C

This register contains additional interface configuration settings.

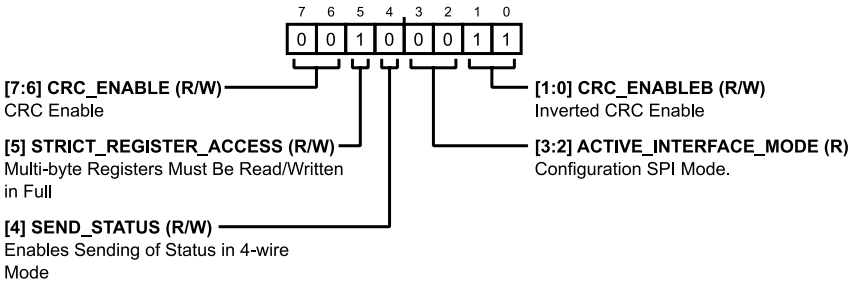

Figure 159. Interface Configuration C Register

Table 45. Bit Descriptions for INTERFACE_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	CRC_ENABLE	CRC Enable. These bits are written to enable or disable the use of CRC on the interface. The $\overline{CRC_ENABLE}$ bits must also be written to with the inverted value of these bits for the CRC to be enabled. 0: CRC Disabled. 1: CRC Enabled.	0x0	R/W
5	STRICT_REGISTER_ACCESS	Multibyte Registers Must Be Read/Written in Full. When this mode is enabled, all bytes of a multibyte register must be read/written in full. 0: Normal Mode. No access restrictions. 1: Strict Mode. Multibyte registers require all bytes accessed.	0x1	R/W
4	SEND_STATUS	Enables Sending of Status in 4-Wire Mode. When set, status information is sent by the device on SDO_{ChX} during the instruction phase. When clear, no status is sent during the instruction phase.	0x0	R/W
[3:2]	ACTIVE_INTERFACE_MODE	Configuration SPI Mode. These bits are the active mode the SPI operates in.	0x0	R
[1:0]	$\overline{CRC_ENABLE}$	Inverted CRC Enable. These bits must be written to with the inverted value of the CRC_ENABLE.	0x3	R/W

CONFIGURATION REGISTERS

Interface Status A Register

Address: 0x11, Reset: 0x00, Name: INTERFACE_STATUS_A

Status bits are set to 1 to indicate an active condition. These bits can be cleared by writing a 1 to the corresponding bit location.

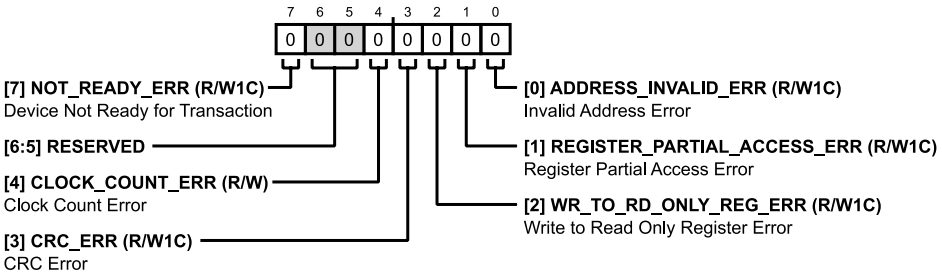

Figure 160. Interface Status A Register

Table 46. Bit Descriptions for INTERFACE_STATUS_A

Bits	Bit Name	Description	Reset	Access
7	NOT_READY_ERR	Channel Not Ready for Transaction. This bit is set if the user attempts to execute an SPI transaction before the completion of digital initialization.	0x0	R/W1C
[6:5]	RESERVED	Reserved. Write 0b00 to these bits.	0x0	R
4	CLOCK_COUNT_ERR	Clock Count Error. This bit is set when an incorrect number of clocks is detected in a transaction.	0x0	R/W1C
3	CRC_ERR	CRC Error. This bit is set when the SPI controller does not send a CRC or when the CRC value calculated by the device does not match the value sent by the SPI controller.	0x0	R/W1C
2	WR_TO_RD_ONLY_REG_ERR	Write to Read Only Register Error. This bit is set when the user attempts a write to a register that is read only.	0x0	R/W1C
1	REGISTER_PARTIAL_ACCESS_ERR	Register Partial Access Error. This bit is set when a fewer than expected number of bytes are read from or written to in a multibyte register access. This bit is only valid when strict register access is enabled.	0x0	R/W1C
0	ADDRESS_INVALID_ERR	Invalid Address Error. This bit is set when the user tries to read from or write to a register address outside of the allowed memory map space.	0x0	R/W1C

CONFIGURATION REGISTERS

Device Status Register

Address: 0x14, Reset: 0x09, Name: DEVICE_STATUS

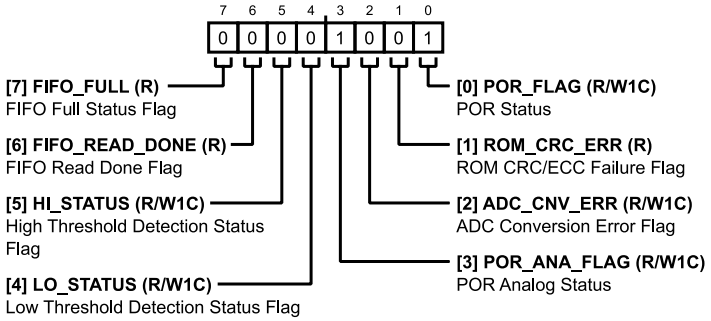

Figure 161. Device Status Register

Table 47. Bit Descriptions for DEVICE_STATUS

Bits	Bit Name	Description	Reset	Access
7	FIFO_FULL	FIFO Full Status Flag. 0: FIFO Not Full. 1: FIFO Full.	0x0	R
6	FIFO_READ_DONE	FIFO Read Done Flag. 0: FIFO Read Not Done. 1: FIFO Read Done.	0x0	R
5	HI_STATUS	High Threshold Detection Status Flag. Writing 1 to this bit clears it. 0: High Threshold Event Not Detected. 1: High Threshold Event Detected.	0x0	R/W1C
4	LO_STATUS	Low Threshold Detection Status Flag. Writing 1 to this bit clears it. 0: Low Threshold Event Not Detected. 1: Low Threshold Event Detected.	0x0	R/W1C
3	POR_ANA_FLAG	POR Analog Status. Allows user to detect when an analog POR event occurs. An analog POR is triggered at power-up or when the 1.1V logic supply or ADC reference drops to less than the 2.7V threshold value or when the user issues a software reset. Writing 1 to this bit clears it. 0: Analog POR Flag Cleared. 1: Analog POR Event Detected.	0x1	R/W1C
2	ADC_CNV_ERR	ADC Conversion Error Flag. Writing 1 to this bit clears it. 0: ADC Conversion Okay. 1: ADC Conversion Error. The user has breached the minimum t_{CONV} specification, and the conversion results are invalid. The user must ensure that the correct clock timing specifications are met.	0x0	R/W1C
1	ROM_CRC_ERR	ROM CRC/ECC Failure Flag. 0: ROM CRC Check Okay. 1: ROM CRC/ECC Failure.	0x0	R
0	POR_FLAG	POR Status. Allows user to detect when a POR event occurs. A POR is triggered at power-up or when the 1.1V logic supply drops to less than the 0.93V threshold value or when the user issues a software reset. Writing 1 to this bit clears it. 0: POR Flag Cleared. 1: POR Event Detected.	0x1	R/W1C

CONFIGURATION REGISTERS

ADC Data Interface Configuration A Register

Address: 0x15, Reset: 0x40, Name: ADC_DATA_INTF_CONFIG_A

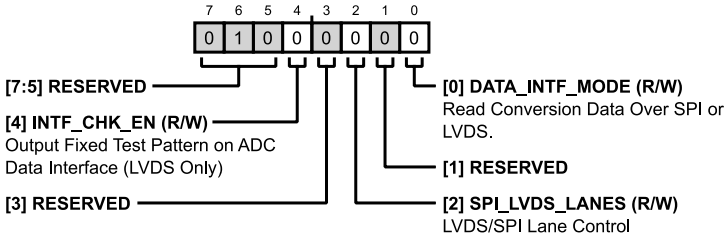

Figure 162. ADC Data Interface Configuration A Register

Table 48. Bit Descriptions for ADC_DATA_INTF_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
6	RESERVED	Reserved. Always set this bit to 1.	0x1	R/W
5	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
4	INTF_CHK_EN	Output Fixed Test Pattern on the Data Interface of the channel (LVDS Only). ADC output is not available when this mode is enabled. Fixed pattern = 16'b1010 1100 0101 1101 (0xAC5D). 0: Test Pattern Disabled. 1: Test Pattern Enabled.	0x0	R/W
3	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
2	SPI_LVDS_LANES	LVDS/SPI Lane Control. Determines the number of lanes that the conversion data of the channel is clocked out on. 0: One Lane Active. 1: Multiple Lanes Active (Two for LVDS and Four for the SPI Data Interface).	0x0	R/W
1	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
0	DATA_INTF_MODE	Read Conversion Data Over SPI or LVDS. Acts as global LVDS enable, setting this bit to 1 powers down the LVDS transmitters/receivers. 0: Data Read Back Over LVDS. 1: Data Read Back Over SPI Data Interface ($\overline{DCS}_{ChX}$/$DCLK_{ChX}$). $CLK+_{ChX}$ is repurposed as the SPI data interface clock ($DCLK_{ChX}$) for reading FIFO data, and $CLK-_{ChX}$ is repurposed as the SPI chip select ($\overline{DCS}_{ChX}$) for reading FIFO data.	0x0	R/W

CONFIGURATION REGISTERS

ADC Data Interface Configuration B Register

Address: 0x16, Reset: 0x00, Name: ADC_DATA_INTF_CONFIG_B

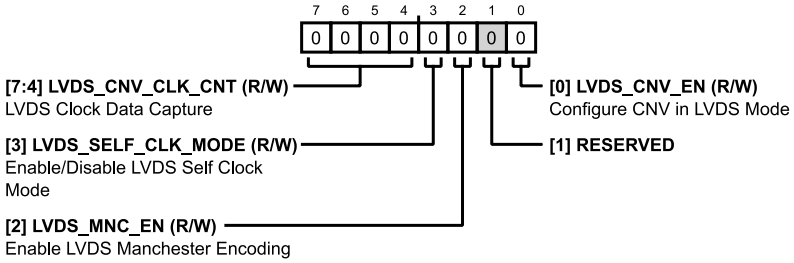

Figure 163. ADC Data Interface Configuration B Register

Table 49. Bit Descriptions for ADC_DATA_INTF_CONFIG_B

Bits	Bit Name	Description	Reset	Access
[7:4]	LVDS_CNV_CLK_CNT	LVDS Clock Data Capture. Determines the negative edge of the LVDS clock that the MSB of the conversion result is available in during conversion mode. For more details on setting this value, see the ADC Result Latency and LVDS Interface Alignment section.	0x0	R/W
3	LVDS_SELF_CLK_MODE	Enable/Disable LVDS Self Clock Mode. 0: Echo Clock Mode Enabled. LVDS DCO transmitter is powered up. 1: Self Clock Mode Enabled. LVDS DCO transmitter is powered down.	0x0	R/W
2	LVDS_MNC_EN	Enable LVDS Manchester Encoding. Manchester encoding is only applied for LVDS read during conversion mode in dual lane mode. This mode only operates with FILTER_SEL = 0, digital filter disabled. 0: Manchester Encoding Disabled. 1: Manchester Encoding Enabled.	0x0	R/W
1	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
0	LVDS_CNV_EN	Configure CNV in LVDS Mode. Only applicable when LVDS interface is selected. 0: CNV Pin Configured in CMOS Mode. 1: CNV Pin Configured in LVDS Mode.	0x0	R/W

ADC Data Interface Configuration C Register

Address: 0x17, Reset: 0x20, Name: ADC_DATA_INTF_CONFIG_C

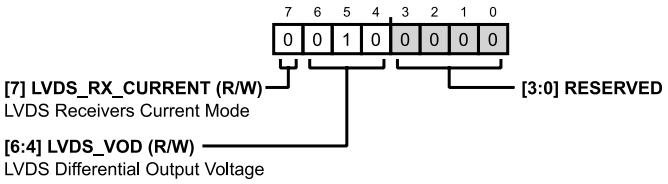

Figure 164. ADC Data Interface Configuration C Register

Table 50. Bit Descriptions for ADC_DATA_INTF_CONFIG_C

Bits	Bit Name	Description	Reset	Access
7	LVDS_RX_CURRENT	LVDS Receivers Current Mode. 1'b0 − 1× current. 1'b1 − 2× current.	0x0	R/W
[6:4]	LVDS_VOD	LVDS Differential Output Voltage. The valid entries are 0b001, 0b010, and 0b100 for the differential voltages of 395mV, 530mV, and 785mV, respectively. Writing an invalid value resets the differential voltage to its default setting of 530mV. However, user can read back the value written to these bits.	0x2	R/W
[3:0]	RESERVED	Reserved. Write 0b0000 to these bits.	0x0	R

CONFIGURATION REGISTERS

Power Control Register

Address: 0x18, Reset: 0x00, Name: PWR_CTRL

It is not recommended to write to this register.

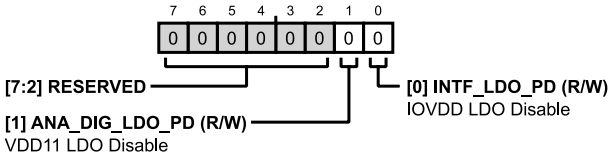

Figure 165. Power Control Register

Table 51. Bit Descriptions for PWR_CTRL

Bits	Bit Name	Description	Reset	Access
[7:2]	RESERVED	Reserved. Write 0b000000 to these bits.	0x0	R
1	ANA_DIG_LDO_PD	VDD11 LDO Disable. Enable or disable the LDO that powers the $VDD11_{ChX}$ rail. It is not recommended to write to this bit. 0: LDO Enabled. 1: LDO Disabled.	0x0	R/W
0	INTF_LDO_PD	IOVDD LDO Disable. Enable or disable the LDO that powers the $IOVDD_{ChX}$ rail. It is not recommended to write to this bit. 0: LDO Enabled. 1: LDO Disabled.	0x0	R/W

CONFIGURATION REGISTERS

GPIO Configuration A Register

Address: 0x19, Reset: 0x01, Name: GPIO_CONFIG_A

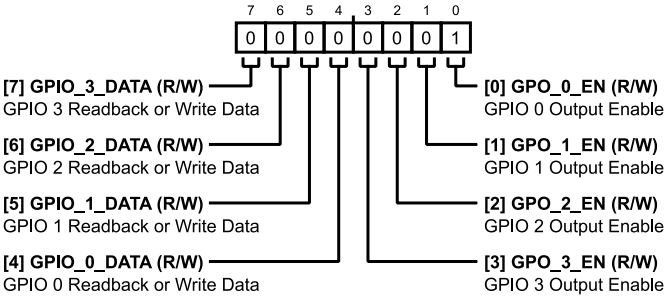

Figure 166. GPIO Configuration A Register

Table 52. Bit Descriptions for GPIO_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	GPIO_3_DATA	GPIO 3 Readback or Write Data. 0: Write 0 to GPIO 3. 1: Write 1 to GPIO 3.	0x0	R/W
6	GPIO_2_DATA	GPIO 2 Readback or Write Data. 0: Write 0 to GPIO 2. 1: Write 1 to GPIO 2.	0x0	R/W
5	GPIO_1_DATA	GPIO 1 Readback or Write Data. 0: Write 0 to GPIO 1. 1: Write 1 to GPIO 1.	0x0	R/W
4	GPIO_0_DATA	GPIO 0 Readback or Write Data. 0: Write 0 to GPIO 0. 1: Write 1 to GPIO 0.	0x0	R/W
3	GPO_3_EN	GPIO 3 Output Enable. 0: GPIO 3 Configured as an Input. 1: GPIO 3 Configured as an Output.	0x0	R/W
2	GPO_2_EN	GPIO 2 Output Enable. 0: GPIO 2 Configured as an Input. 1: GPIO 2 Configured as an Output.	0x0	R/W
1	GPO_1_EN	GPIO 1 Output Enable. 0: GPIO 1 Configured as an Input. 1: GPIO 1 Configured as an Output.	0x0	R/W
0	GPO_0_EN	GPIO 0 Output Enable. 0: GPIO 0 Configured as an Input. 1: GPIO 0 Configured as an Output.	0x1	R/W

CONFIGURATION REGISTERS

GPIO Configuration B Register

Address: 0x1A, Reset: 0x00, Name: GPIO_CONFIG_B

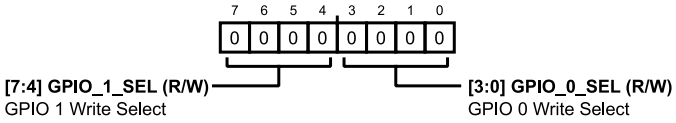

Figure 167. GPIO Configuration B Register

Table 53. Bit Descriptions for GPIO_CONFIG_B

Bits	Bit Name	Description	Reset	Access
[7:4]	GPIO_1_SEL	GPIO 1 Write Select. 0000: Configuration SPI SDO Data. 0001: FIFO Full Flag. 0010: FIFO Read Done Flag. 0011: Filter Result Ready (Active Low). 0100: High Threshold Detect. 0101: Low Threshold Detect. 0110: Status Alert (Active Low). 0111: GPIO Data. 1000: Filter Synchronization Input (Active Low). 1001: External Event Trigger Input for FIFO. 1010: Do not use this setting.	0x0	R/W
[3:0]	GPIO_0_SEL	GPIO 0 Write Select. 0000: Configuration SPI SDO Data. 0001: FIFO Full Flag. 0010: FIFO Read Done Flag. 0011: Filter Result Ready (Active Low). 0100: High Threshold Detect. 0101: Low Threshold Detect. 0110: Status Alert (Active Low). 0111: GPIO Data. 1000: Filter Synchronization Input (Active Low). 1001: External Event Trigger Input for FIFO. 1010: Do not use this setting.	0x0	R/W

CONFIGURATION REGISTERS

GPIO Configuration C Register

Address: 0x1B, Reset: 0x00, Name: GPIO_CONFIG_C

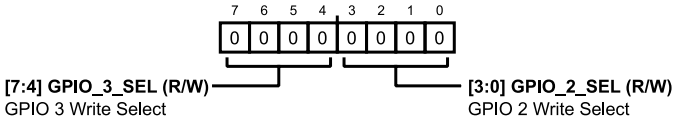

Figure 168. GPIO Configuration C Register

Table 54. Bit Descriptions for GPIO_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:4]	GPIO_3_SEL	GPIO 3 Write Select. 0000: Configuration SPI SDO Data. 0001: FIFO Full Flag. 0010: FIFO Read Done Flag. 0011: Filter Result Ready (Active Low). 0100: High Threshold Detect. 0101: Low Threshold Detect. 0110: Status Alert (Active Low). 0111: GPIO Data. 1000: Filter Synchronization Input (Active Low). 1001: External Event Trigger Input for FIFO. 1010: Do not use this setting.	0x0	R/W
[3:0]	GPIO_2_SEL	GPIO 2 Write Select. 0000: Configuration SPI SDO Data. 0001: FIFO Full Flag. 0010: FIFO Read Done Flag. 0011: Filter Result Ready (Active Low). 0100: High Threshold Detect. 0101: Low Threshold Detect. 0110: Status Alert (Active Low). 0111: GPIO Data. 1000: Filter Synchronization Input (Active Low). 1001: External Event Trigger Input for FIFO. 1010: Do not use this setting.	0x0	R/W

CONFIGURATION REGISTERS

General Configuration Register

Address: 0x1C, Reset: 0x00, Name: GENERAL_CONFIG

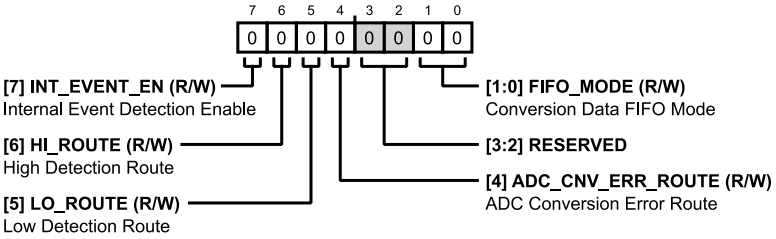

Figure 169. General Configuration Register

Table 55. Bit Descriptions for GENERAL_CONFIG

Bits	Bit Name	Description	Reset	Access
7	INT_EVENT_EN	Internal Event Detection Enable. ADC result or filtered data is only used for internal event detection after this bit is set to 1. 0: Internal event detection is disabled. 1: Internal event detection is enabled.	0x0	R/W
6	HI_ROUTE	High Detection Route. Allows high detection status to be used for FIFO event detection, status register, and alert function (via the GPIO). 0: Mask High Detection. 1: Route High Detection to Alert Pin, Status Register, and FIFO.	0x0	R/W
5	LO_ROUTE	Low Detection Route. Allows low detection status to be used for FIFO event detection, status register, and alert function (via the GPIO). 0: Mask Low Detection. 1: Route Low Detection to Alert Pin, Status Register, and FIFO.	0x0	R/W
4	ADC_CNV_ERR_ROUTE	ADC Conversion Error Route. Allows ADC conversion error status to be routed to the status register and alert function (via the GPIO). 0: Mask ADC Conversion Error. 1: Route ADC Conversion Error to Alert Pin and Status Register.	0x0	R/W
[3:2]	RESERVED	Reserved. Write 0b0 to these bits.	0x0	R
[1:0]	FIFO_MODE	Conversion Data FIFO Mode. 00: FIFO Disabled. 01: Immediate Trigger Mode. 10: Event Trigger Capture, Read Latest WATERMARK. 11: Event Trigger Capture Mode, Read All FIFO.	0x0	R/W

CONFIGURATION REGISTERS

FIFO WATERMARK Register

Address: 0x1D and Address: 0x1E, Reset: 0x4000, Name: FIFO_WATERMARK

In event trigger capture mode, read all FIFO, the FIFO event address can be read. Otherwise, it is the WATERMARK value. If the user writes a value <1, it is clipped at 1. If >16,384, clipped at 16,384.

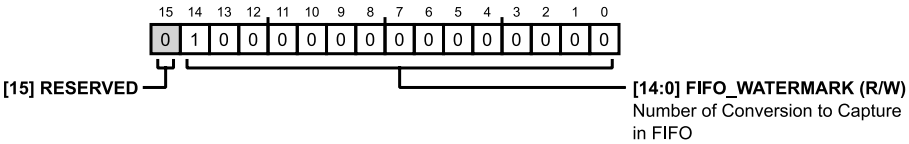

Figure 170. FIFO WATERMARK Register

Table 56. Bit Descriptions for FIFO_WATERMARK

Bits	Bit Name	Description	Reset	Access
15	RESERVED	Reserved. Write 0b0 to this bit.	0x0	R
[14:0]	FIFO_WATERMARK	Number of Conversion to Capture in FIFO. In event trigger capture mode, read all FIFO, this value must be set as a multiple of four only. In this mode, once a WATERMARK number of results have been written to the FIFO, these bits contain the location in the FIFO where the event occurred.	0x4000	R/W

Event Detection Hysteresis Configuration Register

Address: 0x20 and Address: 0x1F, Reset: 0x0000, Name: EVENT_HYSTERESIS

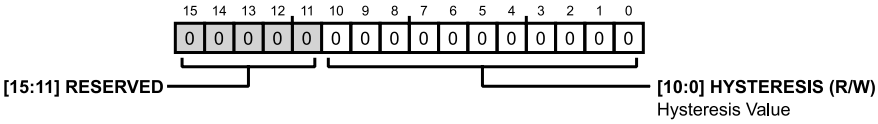

Figure 171. Event Detection Hysteresis Configuration Register

Table 57. Bit Descriptions for EVENT_HYSTERESIS

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved. Write 0b00000 to these bits.	0x0	R
[10:0]	HYSTERESIS	Hysteresis Value. Unsigned data format where LSB = 1.46484mV. 0x000 shows 0 × LSB, and 0x7FF shows 2047 × LSB.	0x0	R/W

Event Detection High Threshold Configuration Register

Address: 0x21 and Address: 0x22, Reset: 0x0000, Name: EVENT_DETECTION_HI

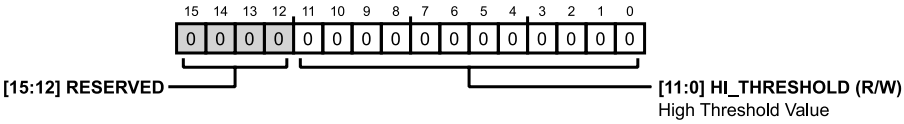

Figure 172. Event Detection High Threshold Configuration Register

Table 58. Bit Descriptions for EVENT_DETECTION_HI

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved. Write 0b0000 to these bits.	0x0	R
[11:0]	HI_THRESHOLD	High Threshold Value. Twos complement data format where LSB = 1.46484mV. 0x800 shows −2048 × LSB, and 0x7FF shows +2047 × LSB.	0x0	R/W

CONFIGURATION REGISTERS

Event Detection Low Threshold Configuration Register

Address: 0x23 and Address: 0x24, Reset: 0x0000, Name: EVENT_DETECTION_LO

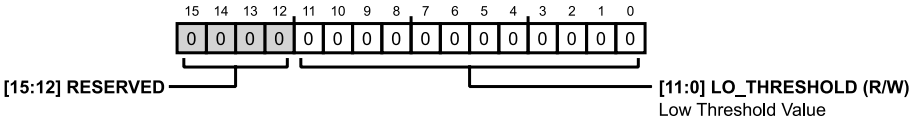

Figure 173. Event Detection Low Threshold Configuration Register

Table 59. Bit Descriptions for EVENT_DETECTION_LO

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved. Write 0b0000 to these bits.	0x0	R
[11:0]	LO_THRESHOLD	Low Threshold Value. Twos complement data format where LSB = 1.46484mV. 0x800 shows −2048 × LSB, and 0x7FF shows +2047 × LSB.	0x0	R/W

Offset Correction Register

Address: 0x25 and Address: 0x26, Reset: 0x0000, Name: OFFSET

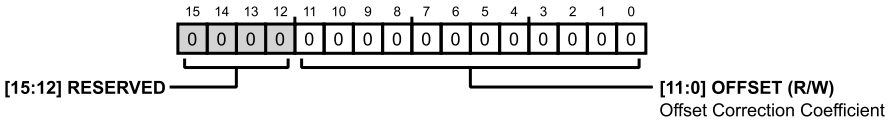

Figure 174. Offset Correction Register

Table 60. Bit Descriptions for OFFSET

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved. Write 0b0000 to this bit field.	0x0	R
[11:0]	OFFSET	Offset Correction Coefficient. Twos complement data format where LSB = 91.55µV. 0x800 shows −2048 × LSB, and 0x7FF shows +2047 × LSB.	0x0	R/W

Gain Correction Register

Address: 0x27 and Address: 0x28, Reset: 0x0200, Name: GAIN

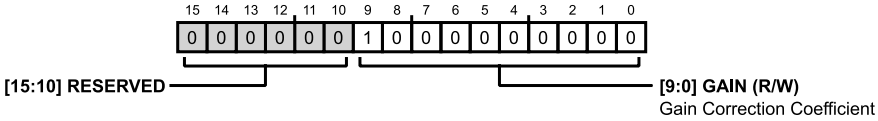

Figure 175. Gain Correction Register

Table 61. Bit Descriptions for GAIN

Bits	Bit Name	Description	Reset	Access
[15:10]	RESERVED	Reserved. Write 0b000000 to these bits.	0x0	R
[9:0]	GAIN	Gain Correction Coefficient. GAIN = 0x3FF results in an overall system gain of 1.0 + 0.015594. GAIN = 0x200 disables the gain correction function and allows for lower latency operation. GAIN = 0x001 results in an overall system gain of 1.0 − 0.015594.	0x200	R/W

CONFIGURATION REGISTERS

Filter Configuration Register

Address: 0x29, Reset: 0x00, Name: FILTER_CONFIG

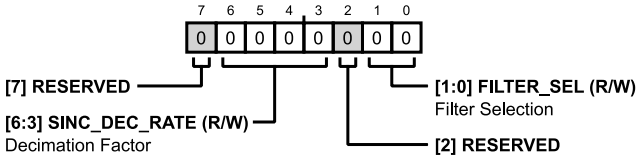

Figure 176. Filter Configuration Register

Table 62. Bit Descriptions for FILTER_CONFIG

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved. Write 0b0 to this bit field.	0x0	R
[6:3]	SINC_DEC_RATE	Decimation Factor. These bits set the Sinc Decimation Factor N. The filter compensation block incurs an additional 2× decimation. The total decimation for a selected filter is sinc1 = N, sinc5 = N, or sinc5 + compensation = N × 2. For a selected filter, setting invalid values, outside of those specified here, set the filter at the maximum decimation rate. 0000: N = 2. 0001: N = 4. 0010: N = 8. 0011: N = 16. 0100: N = 32. 0101: N = 64. 0110: N = 128. 0111: N = 256. 1000: N = 512 (sinc1 only). 1001: N = 1024 (sinc1 only).	0x0	R/W
2	RESERVED	Reserved.	0x0	R
[1:0]	FILTER_SEL	Filter Selection. To ensure the first filter result produces the correct data, when a user makes a change to the filter selection, a reset must be issued via the GPIO pin configured for filter synchronization ($\overline{\text{FILTER_SYNC}}$). 00: Filter Disabled. 01: Sinc1 Filter Selected. 10: Sinc5 Filter Selected. 11: Sinc5 + Compensation Filter Selected.	0x0	R/W

OUTLINE DIMENSIONS

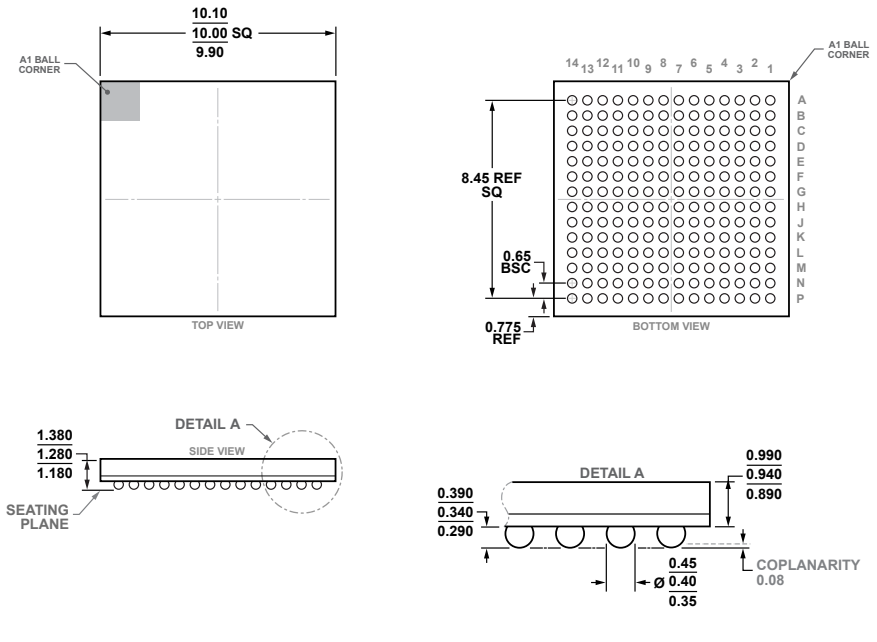

Figure 177. 196-Ball Chip-Scale Package Ball Grid Array [CSP_BGA] (BC-196-20)
Dimensions shown in millimeters

OUTLINE DIMENSIONS

Updated: October 30, 2026

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4885BBCZ	−40°C to +85°C	196-Ball CSP_BGA (10mm x 10mm x 1.28mm)	TRAY, 168	BC-196-20
AD4885BBCZ-RL	−40°C to +85°C	196-Ball CSP_BGA (10mm x 10mm x 1.28mm)	REEL, 1500	BC-196-20
AD4885BBCZ-RL7	−40°C to +85°C	196-Ball CSP_BGA (10mm x 10mm x 1.28mm)	REEL, 400	BC-196-20

[1] Z = RoHS Compliant Part.

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