16-Channel, Easy Drive Multiplexed SAR ADC with Averaging Filters Per Channel

FEATURES

- Easy Drive features enable compact system designs
  - Precharge buffers reduce analog input and reference circuit drive requirements
  - On-chip reference buffer (WLCSP only)
- Small footprint, big performance
  - Sample rate: 500kSPS (AD4691) and 1MSPS (AD4692)
  - INL: ±0.85 LSB maximum
  - Guaranteed 16-bit, no missing codes
  - First conversion accurate
  - SINAD: 93dB typical, f_{IN} = 1kHz
  - 14.6mW at f_S = 1MSPS and 7.3mW at f_S = 500kSPS
  - 32-lead 5mm × 5mm LFCSP or 36-ball 2.96mm × 2.96mm WLCSP
- Enhanced digital functionality
  - Averaging filters per channel
  - Customizable channel sequencer
  - Interleaved channel sampling
  - Autonomous and burst sampling modes
  - 4-wire SPI compatible with 1.2V and 1.8V logic
- Wide operating temperature range: −40°C to +125°C

APPLICATIONS

- Optical power monitoring
- Medical instrumentation
- Electronic test and measurement
- Automated test equipment
- Battery-powered equipment

GENERAL DESCRIPTION

The AD4691/AD4692 are compact, high accuracy, 16-channel, 16-bit successive approximation register (SAR) analog-to-digital converters (ADCs) optimized for high-density multichannel precision data acquisition solutions. The AD4691/AD4692 combine precision performance with Easy Drive features and flexible digital processing to ensure compatibility with space-constrained analog front-end (AFE) designs and low-power digital hosts.

The AD4691/AD4692 Easy Drive features broaden the selection of compatible amplifiers and voltage references. The precharge buffers enable smaller and lower power AFE designs by significantly reducing input voltage and current transients that typically force AFEs to include high-bandwidth ADC driver amplifiers per channel. The WLCSP model also includes an integrated reference buffer which provides a true, buffered reference input.

The AD4691/AD4692 digital features and serial interface are optimized for use with low-power or power-cycled microcontrollers. The AD4691/AD4692 include averaging filters per channel and a customizable channel sequencer, which combined enable on-chip noise filtering with channel-independent averaging ratios. An integrated burst sampling timer enables autonomous and burst sampling schemes to perform conversions with minimal digital resources. Device configuration and ADC data readback are supported via a robust, 4-wire serial peripheral interface (SPI) with optional cyclic redundancy check (CRC).

The AD4691/AD4692 are available in a 5mm × 5mm, 32-lead lead frame chip scale package (LFCSP) and a 2.96mm × 2.96mm, 36-ball wafer level chip scale package (WLCSP) with operation specified from −40°C to +125°C.

One Analog Way, Wilmington, MA 01887-2356, U.S.A.

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REVISION HISTORY

2/2026—Revision 0: Initial Version

FUNCTIONAL BLOCK DIAGRAM

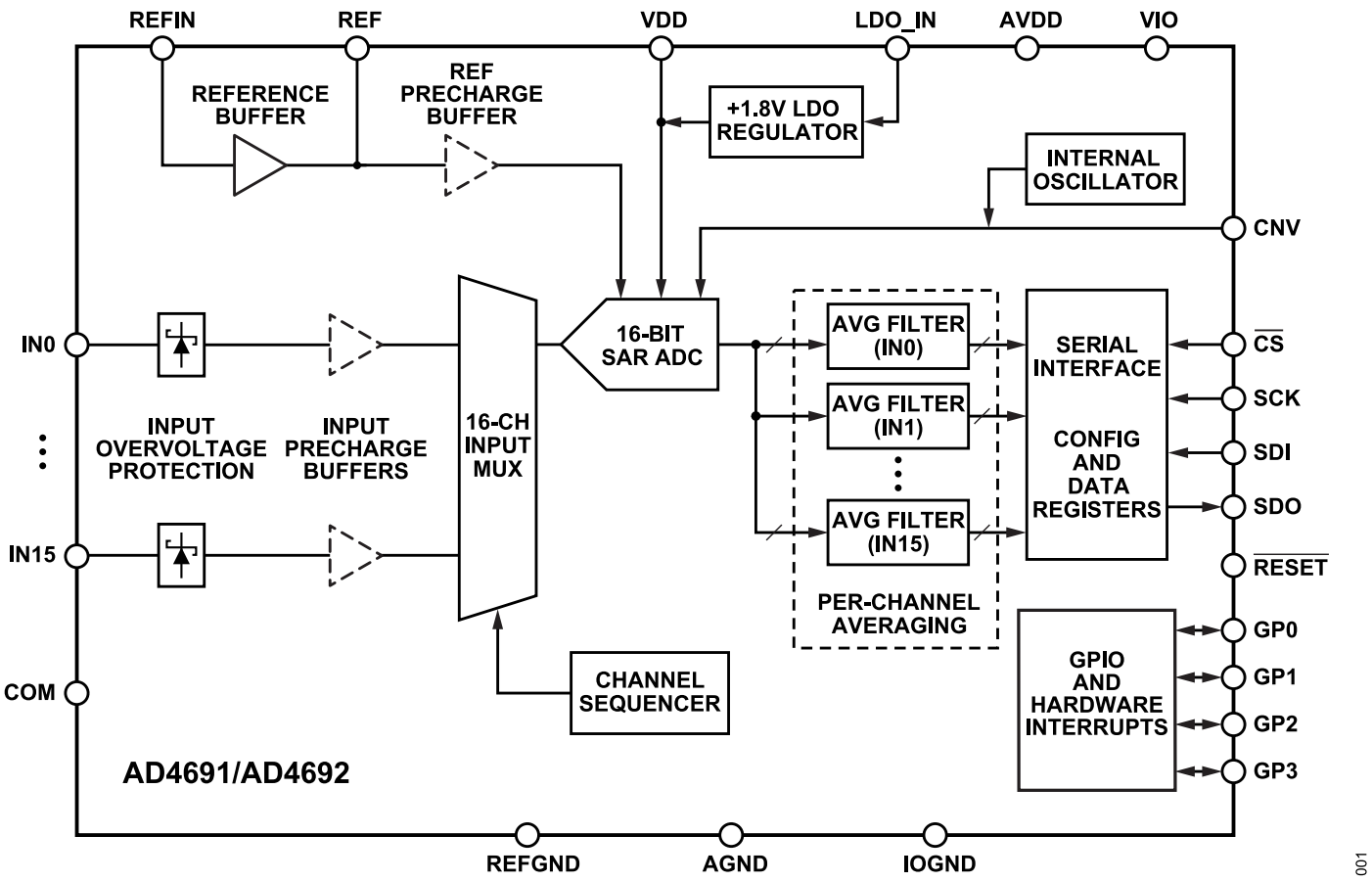

Figure 1. AD4691/AD4692 Functional Block Diagram

SPECIFICATIONS

AVDD = LDO_IN = 5V, REF = 5V, VIO = 1.8V, internal reference buffer disabled, internal LDO regulator enabled, REF decoupling capacitor (C_{REF}) = 1µF, operating at maximum sampling frequency (f_S), and all other features in their default configuration. Minimum and maximum values at T_A = −40°C to +125°C and typical values at T_A = +25°C, unless otherwise specified.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RESOLUTION					
ADC Resolution	No missing codes	16			Bits
Averaging Filter Resolution		16		22	Bits
SAMPLING DYNAMICS					
ADC Sampling Rate (f_S)	AD4691			500	kSPS
	AD4692			1	MSPS
Aperture Delay			2		ns
ANALOG INPUTS					
Input Voltage (V_{IN}) Range					
Unipolar Mode	INx − REFGND	0		$+V_{REF}$	V
Pseudo differential Mode	INx − COM	0		$+V_{REF}$	V
Absolute Input Voltage	INx − REFGND	−0.1		V_{REF} + 0.1	V
	COM − REFGND	−0.1		+0.1	V
Common-Mode Rejection Ratio (CMRR)	f_{IN} = 250kHz		69.5		dB
Analog Input Leakage Current	V_{IN} = 5V		2		nA
Sampling Capacitance (C_{SH})			60		pF
REFERENCE INPUT	Internal reference buffer disabled				
Reference Voltage (V_{REF}) Range	REF − REFGND	2.4		5.1	V
	REF − AVDD			+0.25	V
REF Leakage Current	ADC idle (f_S = 0SPS)				
LFCSP	All clamps deactivated		165		nA
	All clamps activated		8		µA
WLCSP			165		nA
REF Input Current	f_S = 500kSPS		4.75		µA
	f_S = 1MSPS		9.5		µA
INTERNAL REFERENCE BUFFER	Internal reference buffer enabled (WLCSP only)				
V_{REF} Range	REFIN − REFGND	2.4		5.1	V
	AVDD − REFIN			+0.3	V
REFIN Leakage Current	ADC idle (f_S = 0SPS)				
	All clamps deactivated		16		nA
	All clamps activated		4.5		µA
REFIN Input Capacitance			50		pF
Turn-On Time (t_{REFBUF})[1]	C_{REF} = 1µF		1.2		ms
	C_{REF} = 10µF		10		ms
OVERVOLTAGE (OV) CLAMPS					
Clamp Active Input Current (I_{CLAMP})				5	mA
Clamp Activation Voltage				V_{REF} + 0.55	V
Clamping Voltage	I_{CLAMP} = 5mA		V_{REF} + 0.2		V
Clamp Deactivation Voltage		V_{REF} + 0.1			V
DC ACCURACY	VIO = 1.14 V				
Integral Nonlinearity Error (INL)		−1.0	±0.4	+1.0	LSB
Differential Nonlinearity Error (DNL)		−0.65	±0.3	+0.65	LSB
Transition Noise			0.5		LSB rms
Offset Error	LFCSP	−360	±30	+360	µV
	WLCSP	−500	±115	+500	µV

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
Offset Error Drift[2]			±1.1		µV/°C
Offset Error Match	LFCSP	−200	±25	+200	µV
	WLCSP	−240	±80	+240	µV
Gain Error		−0.018	±0.001	+0.018	%FS[3]
Gain Error Drift[2]			±0.08		ppm/°C
Gain Error Match		−0.01	±0.002	+0.01	%FS
Full-Scale Error	LFCSP	−8.5	±1.0	+8.5	LSB
	WLCSP	−14	±1.5	+14	LSB
Full-Scale Error Drift			±0.25		ppm/°C
Total Unadjusted Error (TUE)	LFCSP	−8.5	±1.0	+8.5	LSB
	WLCSP	−14	±2.2	+14	LSB
Low Frequency Noise	Bandwidth = 0.1Hz to 10Hz		5		µV p-p
AC PERFORMANCE					
Total RMS Noise			37.8		µV rms
Dynamic Range			93.4		dB
Signal-to-Noise Ratio (SNR)	f_{IN} = 1kHz, −0.5dBFS				
	LFCSP	90.9	93		dB
	WLCSP	90.5	92.6		dB
Total Harmonic Distortion (THD)	f_{IN} = 1kHz, −0.5dBFS		−117		dB
Signal-to-Noise-and-Distortion (SINAD)	f_{IN} = 1kHz, −0.5dBFS				
	LFCSP	90.8	93		dB
	WLCSP	90.4	92.5		dB
Spurious-Free Dynamic Range (SFDR)	V_{REF} = 5V		121		dB
−3dB Input Bandwidth			11.7		MHz
Channel-to-Channel Crosstalk	f_{IN} = 100kHz				
	LFCSP option		−123		dB
	WLCSP option		−120		dB
Channel-to-Channel Memory	f_{IN} = 100kHz, f_S = 1MSPS		−100		dB
	f_{IN} = 100kHz, f_S = 500kSPS		−110		dB
DIGITAL INPUTS					
Logic Levels					
Input Low Voltage (V_{IL})		−0.3		+0.3 × VIO	V
Input High Voltage (V_{IH})		0.7 × VIO		VIO + 0.3	V
Input Current (I_L)		−1		+1	µA
Input Pin Capacitance			5		pF
DIGITAL OUTPUTS					
Logic Levels					
Output Low Voltage (V_{OL})	Digital output current = +500µA			0.4	V
Output High Voltage (V_{OH})	Digital output current = −500µA	VIO − 0.3			V
POWER REQUIREMENTS					
AVDD to AGND		2.7		5.5	V
LDO_IN to AGND[4]	Internal LDO enabled	2.4		5.5	V
VDD to AGND	Internal LDO disabled	1.71	1.8	1.89	V
VIO to IOGND		1.14		1.98	V
POWER SUPPLY CURRENT					
Standby Current	ADC idle (f_S = 0SPS)				
AVDD	Internal reference buffer disabled		190		nA
	Internal reference buffer enabled		470		µA

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LDO_IN	Internal LDO regulator enabled				
	Internal reference buffer disabled		9		µA
	Internal reference buffer enabled		18		µA
VDD	Internal LDO regulator disabled				
	Internal reference buffer disabled		3.7		µA
	Internal reference buffer enabled		9		µA
VIO	VIO = 1.8V		250		nA
AVDD Current					
Internal reference buffer disabled	f_S = 500kSPS		0.6	0.73	mA
	f_S = 1MSPS		1.2	1.45	mA
Internal reference buffer enabled	f_S = 500kSPS		1.0	1.4	mA
	f_S = 1MSPS		1.65	2.2	mA
LDO_IN Current	Internal LDO regulator enabled				
	f_S = 500kSPS		2.5	3.4	mA
	f_S = 1MSPS		5	6.8	mA
VDD Current	Internal LDO regulator disabled				
	f_S = 500kSPS		2.4	3.3	mA
	f_S = 1MSPS		4.8	6.6	mA
POWER DISSIPATION					
Standby Power Dissipation					
Internal LDO regulator disabled	Internal reference buffer disabled		7.6		µW
	Internal reference buffer enabled		2.4		mW
Internal LDO regulator enabled	Internal reference buffer disabled		46		µW
	Internal reference buffer enabled		2.5		mW
Power Dissipation, Internal LDO Regulator Disabled	LDO_IN = AGND, VDD = 1.8V				
Internal reference buffer disabled	f_S = 500kSPS		7.3	9.6	mW
	f_S = 1MSPS		14.6	19.1	mW
Internal reference buffer enabled	f_S = 500kSPS		9.3	12.9	mW
	f_S = 1MSPS		16.9	22.9	mW
Power Dissipation, Internal LDO Regulator Enabled	LDO_IN = 5V				
Internal reference buffer disabled	f_S = 500kSPS		15.5	20.7	mW
	f_S = 1MSPS		31	41.4	mW
Internal reference buffer enabled	f_S = 500kSPS		17.5	24	mW
	f_S = 1MSPS		33.3	45	mW
TEMPERATURE RANGE					
Specified Performance	T_{MIN} to T_{MAX}	−40		+125	°C

[1] The reference buffer turn-on time specification is the time needed for the reference buffer to drive the REF voltage from 0V to V_{REF} to 0.01% accuracy. See Figure 41.

[2] Offset error, gain error, and full-scale error drift utilizes the box method across the full operating temperature range of −40°C to +125°C.

[3] %FS is the percentage of the ADC full scale (see the Transfer Function section for a definition of full scale).

[4] See the Internal LDO Regulator section for more information.

SPECIFICATIONS

TIMING SPECIFICATIONS

AVDD = LDO_IN = 5V, REF = 5V, VIO = 1.14V to 1.98V, digital output load capacitance (C_{LOAD}) = 20pF, and all other features in their default configuration. Minimum and maximum values at T_A = −40°C to +125°C and typical values at T_A = +25°C, unless otherwise specified.

Table 2. ADC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit
Conversion Time	t_{CONV}		380	430	ns
Acquisition Time[1]	t_{ACQ}				
f_S = 1MSPS		485			ns
f_S = 500kSPS		1485			ns
Sample Period	t_{CYC}				
f_S = 1MSPS		1000			ns
f_S = 500kSPS		2000			ns
CNV High Time	t_{CNVH}	10			ns
CNV Low Time	t_{CNVL}	80			ns
Quiet Time					
Lst SCK Edge to CNV Rising Edge Delay	t_{SCKCNV}	80			ns
$\overline{CS}$ Rising Edge to CNV Rising Edge Delay	t_{CSBCNV}	10			ns
Internal Oscillator Frequency[2]	f_{OSC}	−15%		+15%	MHz

[1] The t_{ACQ} specification is the length of time that the ADC sampling capacitor is connected to the input pin via the input MUX (see Figure 47). The minimum t_{ACQ} is equal to t_{CYC} − 515ns, and therefore increases with slower sampling rates.

[2] See the nominal oscillator frequency settings in Table 42.

Table 3. SPI Timing (All Modes Except Manual Mode)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ High Time	t_{CSBH}	10			ns
$\overline{CS}$ Falling Edge to Interface Ready	t_{EN}			15	ns
SCK Period	t_{SCK}	32			ns
SCK Low Time	t_{SCKL}	10			ns
SCK High Time	t_{SCKH}	10			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	2			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}			8	ns
SDI Valid Setup Time to SCK Rising Edge	t_{SSDI}	2			ns
SDI Valid Hold Time After SCK Rising Edge	t_{HSDI}	2			ns
SCK Rising Edge to $\overline{CS}$ Rising Edge	t_{SCKCSB}	2			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{DIS}			15	ns

Table 4. SPI Timing (Manual Mode)

Parameter	Symbol	Min	Typ	Max	Unit
$\overline{CS}$ High Time	t_{CSBH}	10			ns
$\overline{CS}$ Falling Edge to Interface Ready	t_{EN}			15	ns
SCK Period	t_{SCK}	12.5			ns
SCK Low Time	t_{SCKL}	5			ns
SCK High Time	t_{SCKH}	5			ns
SCK Falling Edge to Data Remains Valid	t_{HSDO}	2			ns
SCK Falling Edge to Data Valid Delay	t_{DSDO}			8	ns
SDI Valid Setup Time to SCK Rising Edge	t_{SSDI}	2			ns
SDI Valid Hold Time After SCK Rising Edge	t_{HSDI}	2			ns
SCK Rising Edge to $\overline{CS}$ Rising Edge	t_{SCKCSB}	2			ns
$\overline{CS}$ Rising Edge to SDO High Impedance	t_{DIS}			15	ns

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Table 5. GPIO and Reset

Parameter	Symbol	Min	Typ	Max	Unit
Convert-Start to BUSY Falling Edge	t_{BUSY}			t_{CONV}	ns
Convert-Start to $\overline{EOS}$ Falling Edge	t_{EOSB}			t_{CONV}	ns
Convert-Start to $\overline{DRDY}$ Falling Edge	t_{DRDYB}			t_{CONV}	ns
$\overline{RESET}$ Low Time	t_{RESETL}	10			ns
Hardware Reset Delay	t_{HWR}		300		µs
Software Reset Delay	t_{SWR}		300		µs
Power-On Reset Delay	t_{POR}		3		ms

TIMING DIAGRAMS

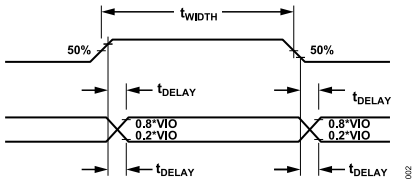

Figure 2. Voltage Levels for Timing Specifications

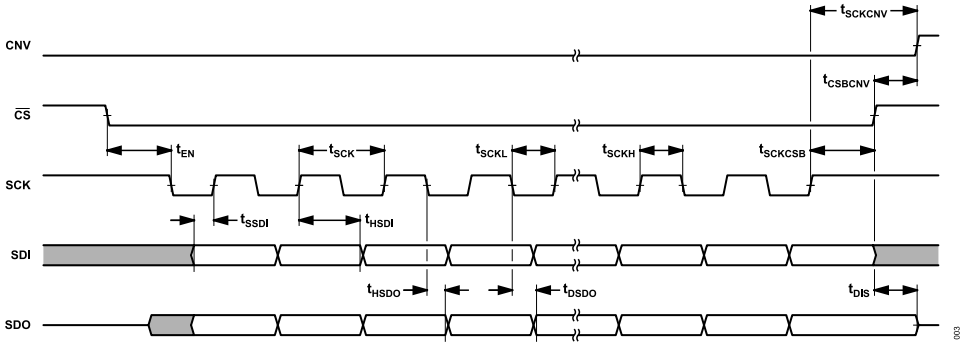

Figure 3. SPI Timing Specifications Definition Diagram

ABSOLUTE MAXIMUM RATINGS

Table 6. Absolute Maximum Ratings

Parameter	Rating
Analog Inputs	
INn,[1] COM to REFGND	−0.3V to REF + 0.3V
Reference Inputs	
REF, REFIN to AGND, REFGND, IOGND	−0.3V to +6V
REF to REFIN	−6.3V to +6.3V
Supply Inputs	
AVDD, LDO_IN to AGND, REFGND, IOGND	−0.3V to +6V
VDD, VIO to AGND, REFGND, IOGND	−0.3V to +2.1V
AVDD to LDO_IN	−6.3V to +6.3V
AVDD, LDO_IN to REF	−6.3V to +6.3V
VDD, VIO to AVDD, LDO_IN, REF	−6.3V to +2.4V
VDD to VIO	−2.4V to +2.4V
Ground	
AGND, IOGND to REFGND	−0.3V to +0.3V
AGND to IOGND	−0.3V to +0.3V
Digital Inputs	
CNV, $\overline{CS}$, SDI, SCK, $\overline{RESET}$ to IOGND	−0.3V to +6V
Digital Outputs	
SDO, GP0, GP1, GP2, GP3 to IOGND	−0.3V to VIO + 0.3V
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature Soldering	260°C reflow, as per JEDEC J-STD-020

[1] INn refers to the analog inputs, Pin IN0 through Pin IN15.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is specified for worst case conditions and is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction to case thermal resistance.

Thermal resistance values specified in Table 7 were calculated based on JEDEC specifications and must be used in compliance with JESD51-12. The worst case junction temperature is reported.

θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The θ_{JA} value can vary depending on PCB material, layout, and environmental conditions.

Table 7. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
CP-32-39	40.2	17.5	°C/W
CP-36-5	41.8	0.1	°C/W

[1] Simulated values are based on the JEDEC 2S2P thermal test board with nine thermal vias in a JEDEC natural convection environment. See JEDEC JESD51.

[2] Simulated values are measured to the package top surface with a cold plate attached directly to the package top surface.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD-protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Field induced charged device model (FICDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4691/AD4692

Table 8. AD4691/AD4692 32-Lead LFCSP

ESD Model	Withstand Threshold (kV)	Class
HBM	2.5	2
FICDM	1	C3

Table 9. AD4691/AD4692 36-Lead WLCSP

ESD Model	Withstand Threshold (kV)	Class
HBM	3	2
FICDM	1	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

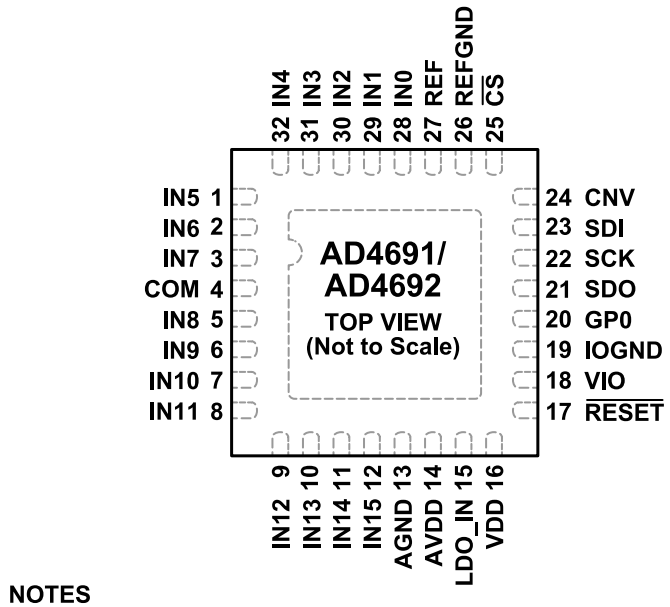

Figure 4. AD4691/AD4692 LFCSP Pin Configuration

Table 10. AD4691/AD4692 LFCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	IN5	AI	Analog Input Channel 5.
2	IN6	AI	Analog Input Channel 6.
3	IN7	AI	Analog Input Channel 7.
4	COM	AI	Common Channel Input. COM can optionally be sampled by the ADC core negative input to function as a sense ground (see the Multiplexer Configuration Options section). COM is nominally tied to signal ground.
5	IN8	AI	Analog Input Channel 8.
6	IN9	AI	Analog Input Channel 9.
7	IN10	AI	Analog Input Channel 10.
8	IN11	AI	Analog Input Channel 11.
9	IN12	AI	Analog Input Channel 12.
10	IN13	AI	Analog Input Channel 13.
11	IN14	AI	Analog Input Channel 14.
12	IN15	AI	Analog Input Channel 15.
13	AGND	P	Analog Supply Ground. AVDD, LDO_IN, and VDD are referenced to AGND.
14	AVDD	P	Analog Power Supply. The range of AVDD is 2.7V to 5.5V. Decouple AVDD to AGND with a local 100nF capacitor.
15	LDO_IN	P	Internal LDO Regulator Input. Nominally tied to AVDD when using the internal LDO regulator to supply the 1.8V VDD rail. When powering VDD with an external 1.8V supply, tie LDO_IN to AGND. See the Internal LDO Regulator section for more information.
16	VDD	P	ADC Core Power Supply. VDD is nominally 1.8V. VDD must be decoupled to AGND with a local 100nF capacitor. When the internal LDO regulator is enabled, VDD is internally generated. Disable the internal LDO regulator when supplying VDD with an external 1.8V supply.
17	$\overline{\text{RESET}}$	DI	Hardware Reset Input (Active Low). Drive $\overline{\text{RESET}}$ low to perform a hardware reset of the device (see the Device Reset section).
18	VIO	P	Logic Input and Output Power Supply. Sets the logic voltage levels for digital inputs and digital outputs (see Table 1). VIO is nominally supplied by the host interface logic supply (1.2V or 1.8V). Decouple VIO to IOGND with a local 100nF capacitor.
19	IOGND	P	Logic Input and Output Ground. VIO is referenced to IOGND.
20	GP0	DI/DO	General-Purpose Pin 0. The GP0 pin can be configured to function as a general-purpose input/output (GPIO) or a variety of device status and hardware interrupt signals (see the General Purpose Pin Functions section).

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 10. AD4691/AD4692 LFCSP Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
21	SDO	DO	Serial Data Output. Data are shifted out of the SDO output on the falling edge of SCK.
22	SCK	DI	Serial Data Clock Input. SCK is used to clock out data on SDO and clock in data on SDI during SPI transactions.
23	SDI	DI	Serial Data Input. Data are shifted into the SDI input on the rising edge of SCK.
24	CNV	DI	Convert Input. A rising edge on CNV initiates one or multiple conversions based on the selected operating mode (as described in the Modes of Operation section).
25	$\overline{CS}$	DI	Chip Select Input (Active Low). The $\overline{CS}$ input frames all SPI transactions (see the Digital Interface section).
26	REFGND	P/AI	Reference Ground. REF is referenced to REFGND. By default, REFGND is sampled by the ADC core negative input (see the Multiplexer Configuration Options section).
27	REF	AI	Reference Input. Sets the ADC core full-scale range (see the Voltage Reference Input section). The range of REF is 2.4V to 5.1V. REF must be decoupled with a minimum 1µF capacitor for optimal operation.
28	IN0	AI	Analog Input Channel 0.
29	IN1	AI	Analog Input Channel 1.
30	IN2	AI	Analog Input Channel 2.
31	IN3	AI	Analog Input Channel 3.
32	IN4	AI	Analog Input Channel 4.
33	EPAD	NC	Exposed Pad. The exposed pad is not connected internally. For increased reliability of the solder joints, it is recommended that the pad be soldered to the system ground plane.

[1] AI is analog input, P is power, DI is digital input, DO is digital output, and NC is no internal connection.

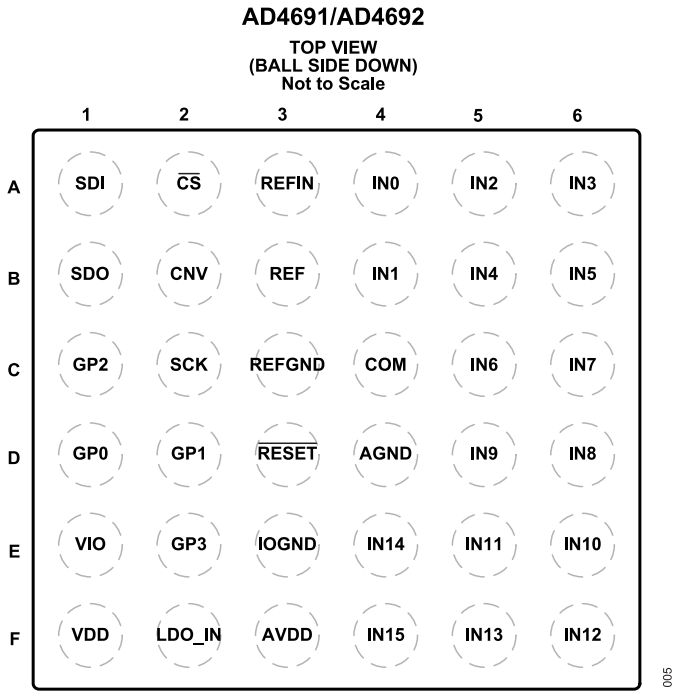

Figure 5. AD4691/AD4692 WLCSP Pin Configuration

Table 11. AD4691/AD4692 WLCSP Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
A1	SDI	DI	Serial Data Input. Data are shifted into the SDI input on the rising edge of SCK.
A2	$\overline{CS}$	DI	Chip Select Input (Active Low). The $\overline{CS}$ input frames all SPI transactions (see the Digital Interface section).
A3	REFIN	AI	Internal Reference Buffer Input. The internal reference buffer provides a high impedance input for the ADC V_{REF} voltage. When the internal reference buffer is disabled, REFIN must be tied to REF. See the Internal Reference Buffer section for more information.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 11. AD4691/AD4692 WLCSP Pin Function Descriptions (Continued)

Pin No.	Mnemonic	Type[1]	Description
A4	IN0	AI	Analog Input Channel 0.
A5	IN2	AI	Analog Input Channel 2.
A6	IN3	AI	Analog Input Channel 3.
B1	SDO	DO	Serial Data Output. Data are shifted out of the SDO output on the falling edge of SCK.
B2	CNV	DI	Convert Input. A rising edge on CNV initiates one or multiple conversions based on the selected operating mode (as described in the Modes of Operation section).
B3	REF	AI	Reference Input. Sets the ADC core full-scale range (see the Voltage Reference Input section). The range of REF is 2.4V to 5.1V. REF must be decoupled with a minimum 1µF capacitor for optimal operation.
B4	IN1	AI	Analog Input Channel 1.
B5	IN4	AI	Analog Input Channel 4.
B6	IN5	AI	Analog Input Channel 5.
C1	GP2	DI/DO	General-Purpose Pin 2. The GPx pins can be configured to function as a general-purpose input/output (GPIO) or a variety of device status and hardware interrupt signals (see the General Purpose Pin Functions section).
C2	SCK	DI	Serial Data Clock Input. SCK is used to clock out data on SDO and clock in data on SDI during SPI transactions.
C3	REFGND	P/AI	Reference Ground. REF is referenced to REFGND. By default, REFGND is sampled by the ADC core negative input (see the Multiplexer Configuration Options section).
C4	COM	AI	Common Channel Input. COM can optionally be sampled by the ADC core negative input to function as a sense ground (see the Multiplexer Configuration Options section). COM is nominally tied to signal ground.
C5	IN6	AI	Analog Input Channel 6.
C6	IN7	AI	Analog Input Channel 7.
D1	GP0	DI/DO	General-Purpose Pin 0. The GPx pins can be configured to function as a general-purpose input/output (GPIO) or a variety of device status and hardware interrupt signals (see the General Purpose Pin Functions section).
D2	GP1	DI/DO	General-Purpose Pin 1. The GPx pins can be configured to function as a general-purpose input/output (GPIO) or a variety of device status and hardware interrupt signals (see the General Purpose Pin Functions section).
D3	$\overline{\text{RESET}}$	DI	Hardware Reset Input (Active Low). Drive $\overline{\text{RESET}}$ low to perform a hardware reset of the device (see the Device Reset section).
D4	AGND	P	Analog Supply Ground. AVDD, LDO_IN, and VDD are referenced to AGND.
D5	IN9	AI	Analog Input Channel 9.
D6	IN8	AI	Analog Input Channel 8.
E1	VIO	P	Logic Input and Output Power Supply. Sets the logic voltage levels for digital inputs and digital outputs (see Table 1). VIO is nominally supplied by the host interface logic supply (1.2V or 1.8V). Decouple VIO to IOGND with a local 100nF capacitor.
E2	GP3	DI/DO	General-Purpose Pin 3. The GPx pins can be configured to function as a general-purpose input/output (GPIO) or a variety of device status and hardware interrupt signals (see the General Purpose Pin Functions section).
E3	IOGND	P	Logic Input and Output Ground. VIO is referenced to IOGND.
E4	IN14	AI	Analog Input Channel 14.
E5	IN11	AI	Analog Input Channel 11.
E6	IN10	AI	Analog Input Channel 10.
F1	VDD	P	ADC Core Power Supply. VDD is nominally 1.8V. VDD must be decoupled to AGND with a local 100nF capacitor. When the internal LDO regulator is enabled, VDD is internally generated. Disable the internal LDO regulator when supplying VDD with an external 1.8V supply.
F2	LDO_IN	P	Internal LDO Regulator Input. Nominally tied to AVDD when using the internal LDO regulator to supply the 1.8V VDD rail. When powering VDD with an external 1.8V supply, tie LDO_IN to AGND. See the Internal LDO Regulator section for more information.
F3	AVDD	P	Analog Power Supply. The range of AVDD is 2.7V to 5.5V. Decouple AVDD to AGND with a local 100nF capacitor.
F4	IN15	AI	Analog Input Channel 15.
F5	IN13	AI	Analog Input Channel 13.
F6	IN12	AI	Analog Input Channel 12.

[1] AI is analog input, P is power, DI is digital input, DO is digital output, and NC is no internal connection.

TYPICAL PERFORMANCE CHARACTERISTICS

AVDD = LDO_IN = 5V, REF = 5V, VIO = 1.8V, internal reference buffer disabled, internal LDO regulator enabled, REF decoupling capacitor (C_{REF}) = 1µF, operating at maximum sampling frequency (f_S), T_A = +25°C, and all other features in their default configuration.

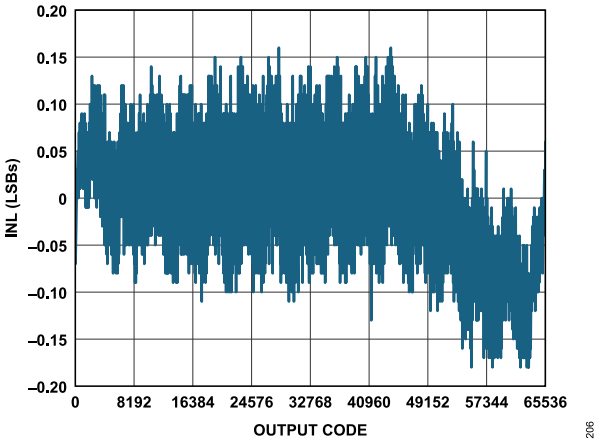

Figure 6. INL vs. Output Code

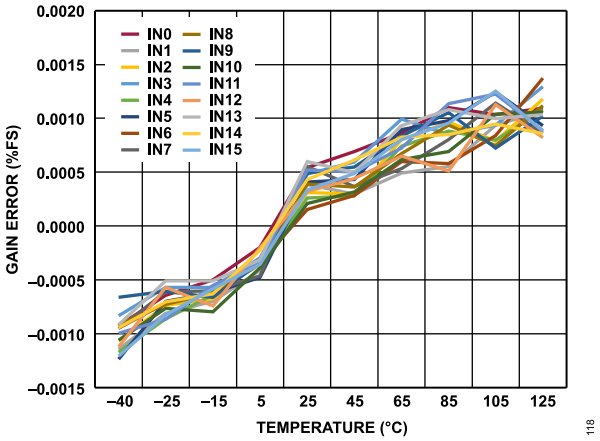

Figure 9. Gain Error vs. Temperature

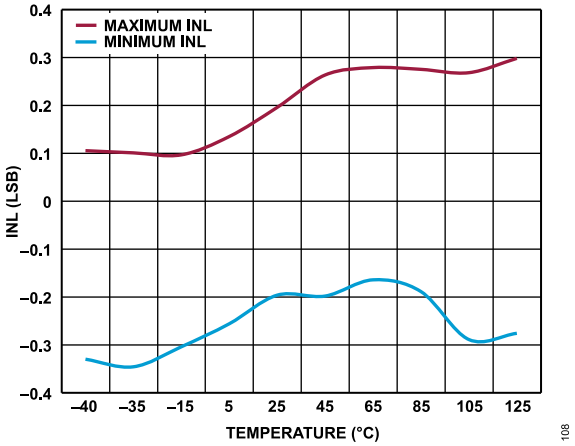

Figure 7. INL vs. Temperature

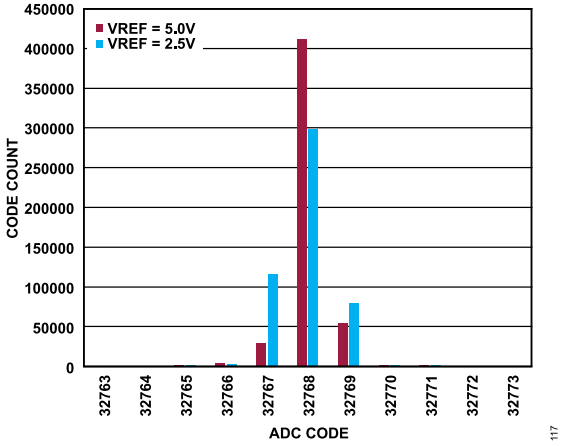

Figure 10. Histogram, Accumulator Depth = 1

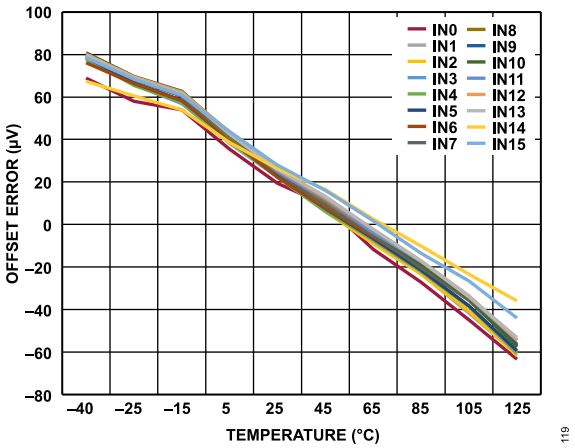

Figure 8. Offset Error vs. Temperature

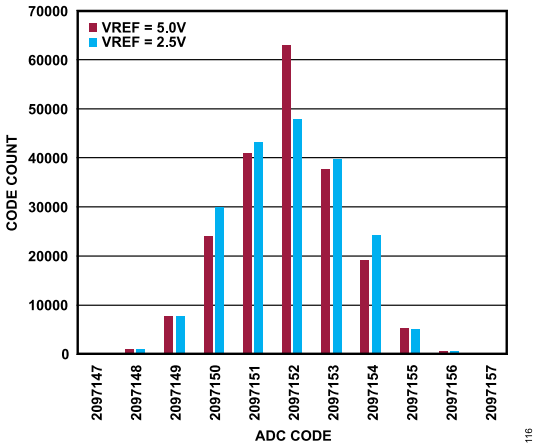

Figure 11. Histogram, Accumulator Depth = 64

TYPICAL PERFORMANCE CHARACTERISTICS

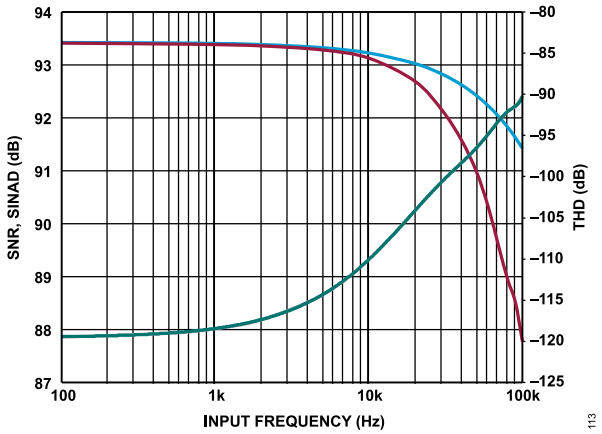

Figure 12. SNR, SINAD, and THD vs. Input Frequency

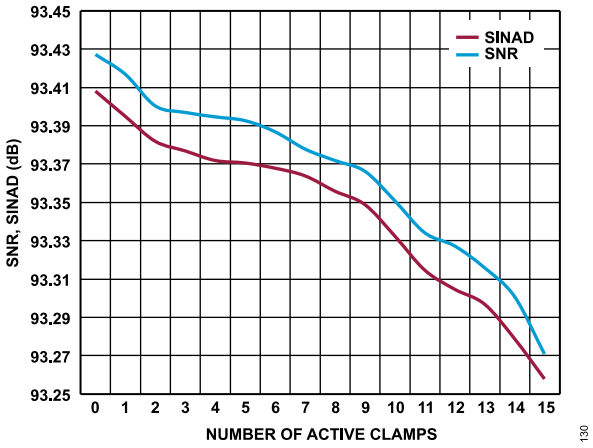

Figure 15. SNR and SINAD vs. Number of Active Clamps

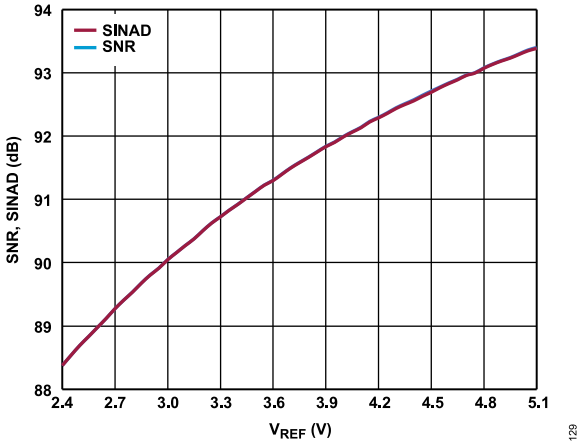

Figure 13. SNR and SINAD vs. V_{REF}

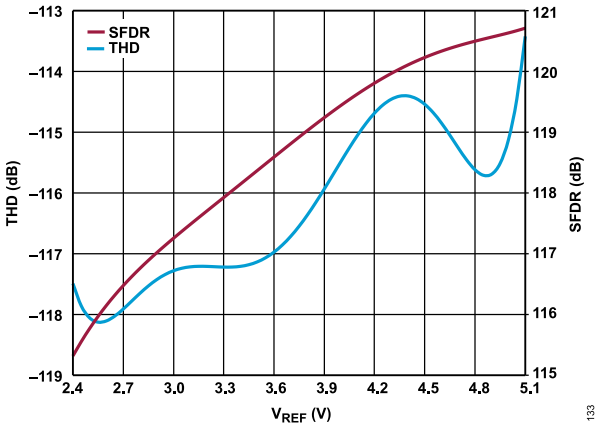

Figure 16. THD and SFDR vs. V_{REF}

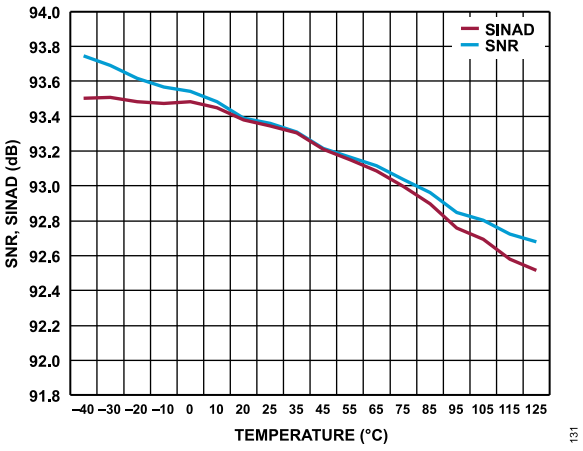

Figure 14. SNR and SINAD vs. Temperature

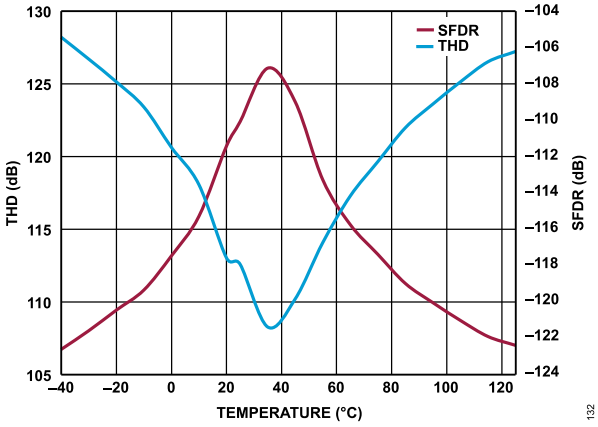

Figure 17. THD and SFDR vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

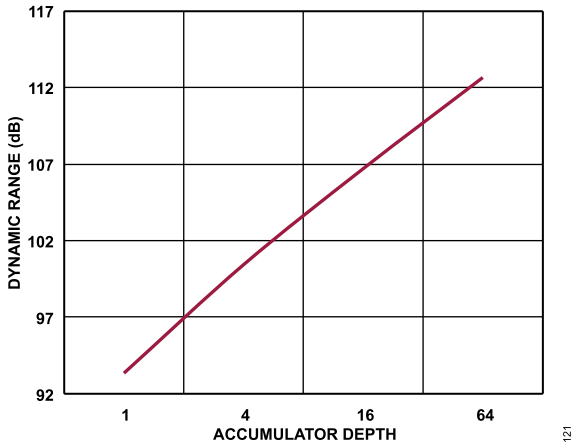

Figure 18. Dynamic Range vs. Accumulator Depth

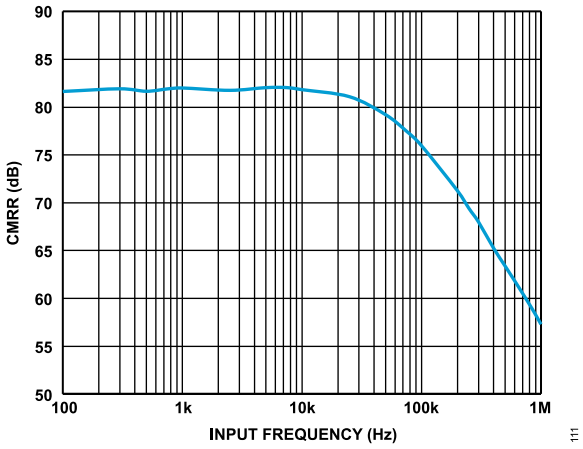

Figure 19. CMRR vs. Input Frequency

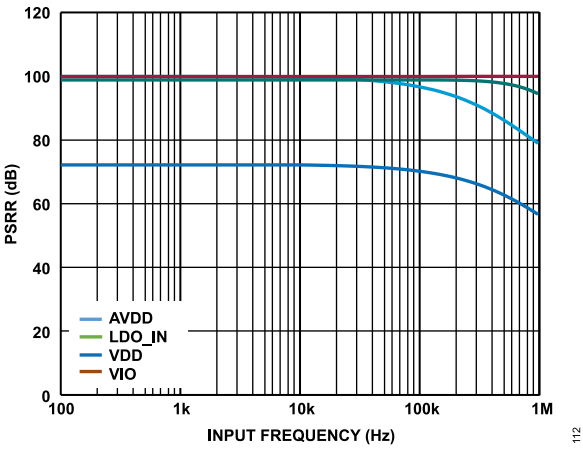

Figure 20. Power Supply Rejection Ratio (PSRR) vs. Input Frequency

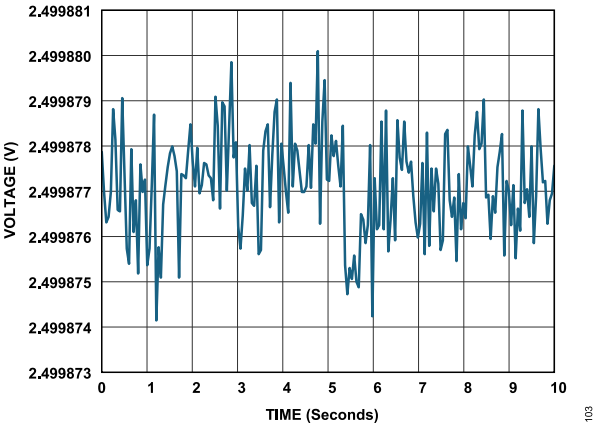

Figure 21. 1/f Noise (0.1Hz to 10Hz Bandwidth), 50kSPS

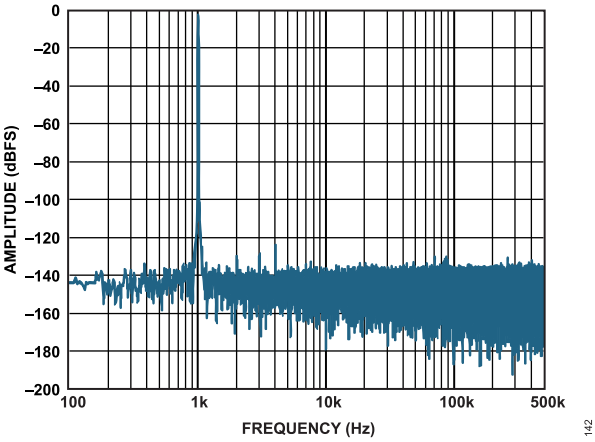

Figure 22. Fast Fourier Transform (FFT), fIN = 1kHz, V_{REF} = 5V

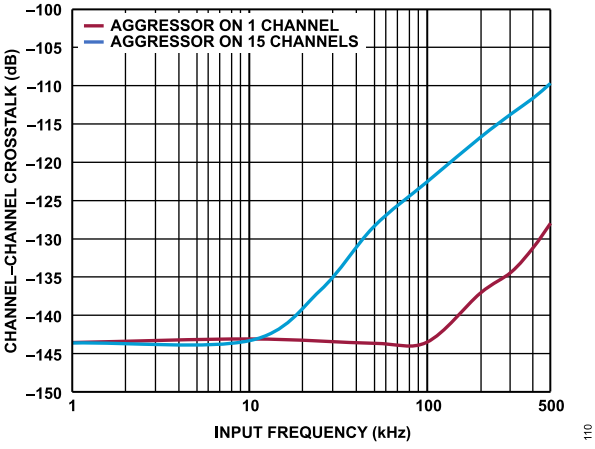

Figure 23. Channel-to-Channel Crosstalk vs. Input Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

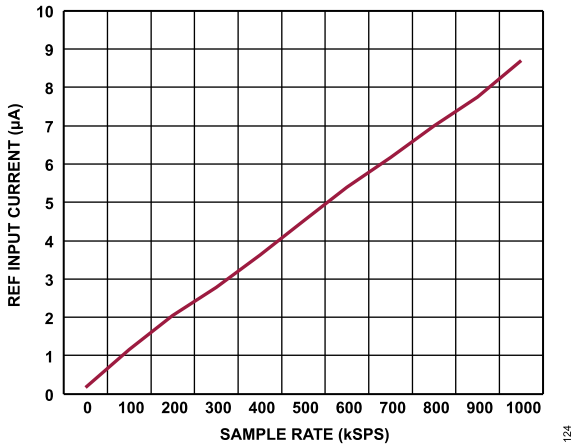

Figure 24. REF Input Current vs. Sample Rate

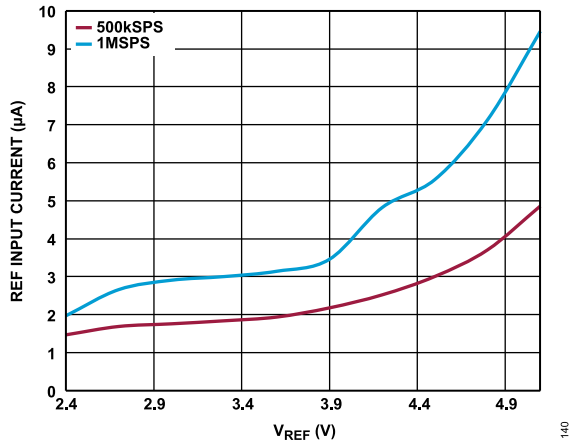

Figure 25. REF Input Current vs. V_{REF}

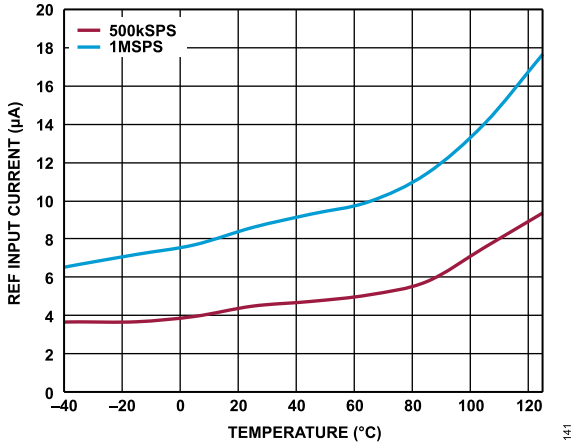

Figure 26. REF Input Current vs. Temperature

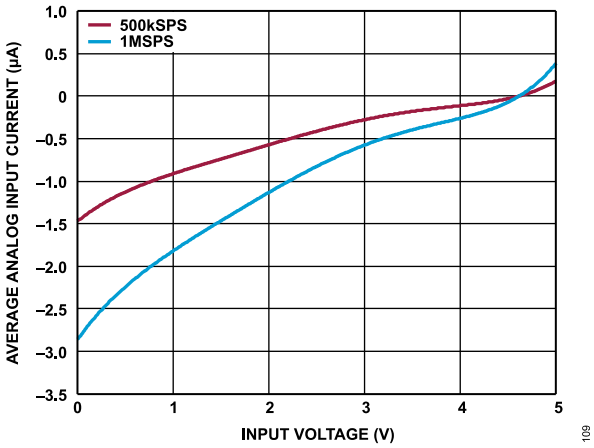

Figure 27. Average Analog Input Current vs. Input Voltage, f_S = 1MSPS and 500kSPS

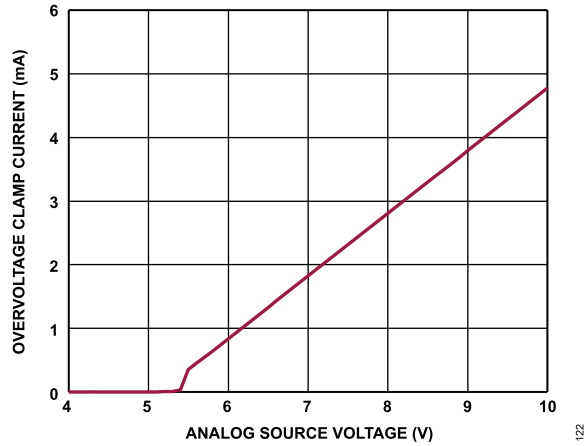

Figure 28. Overvoltage Protection Clamp Current vs. Analog Source Voltage

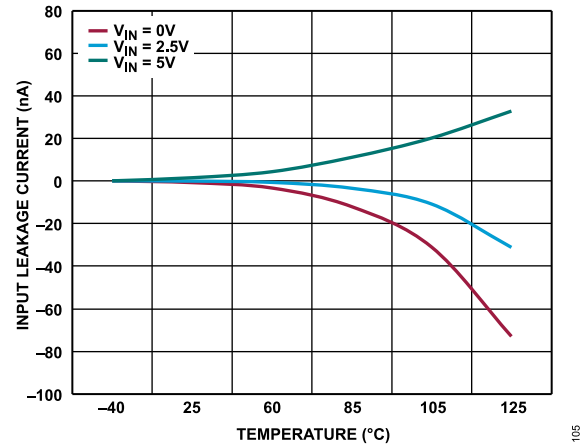

Figure 29. Analog Input Leakage Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

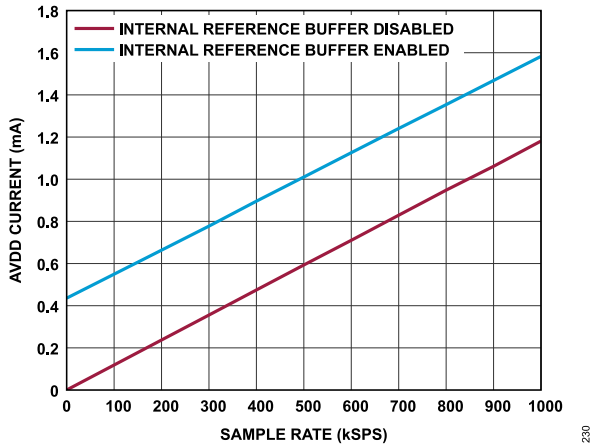

Figure 30. AVDD Current vs. Sample Rate

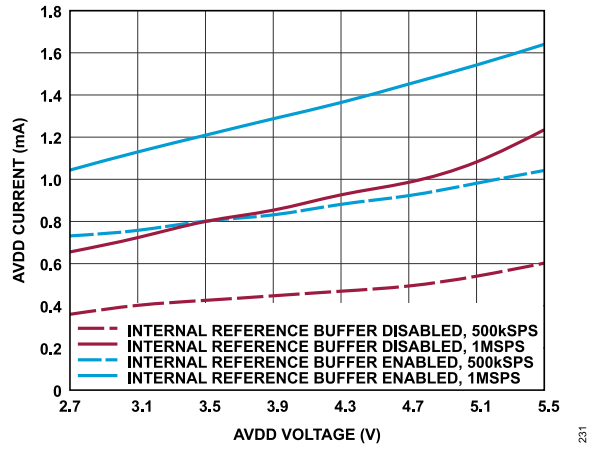

Figure 31. AVDD Current vs. AVDD Voltage

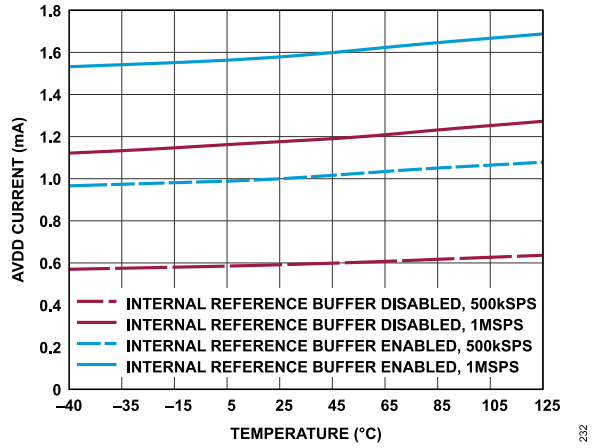

Figure 32. AVDD Current vs. Temperature

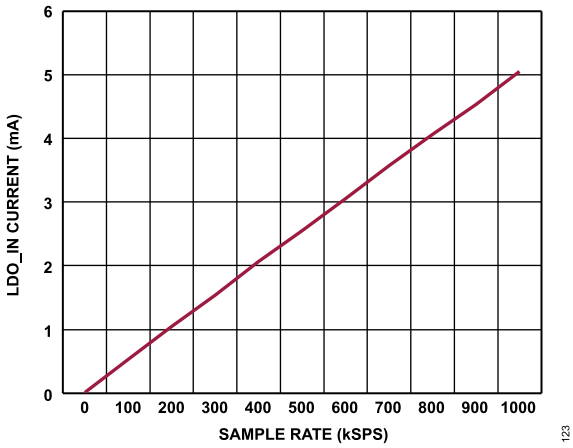

Figure 33. LDO_IN Current vs. Sample Rate

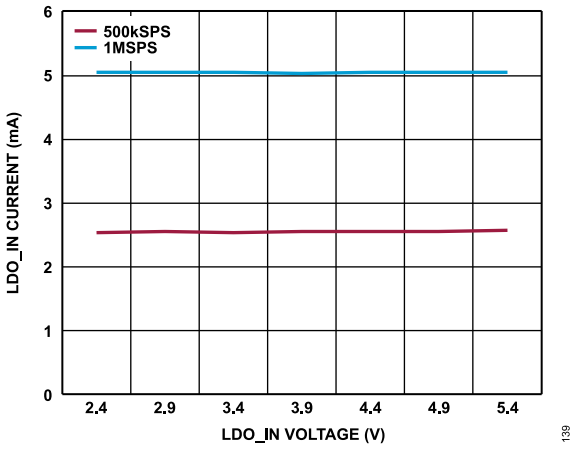

Figure 34. LDO_IN Current vs. LDO_IN Voltage

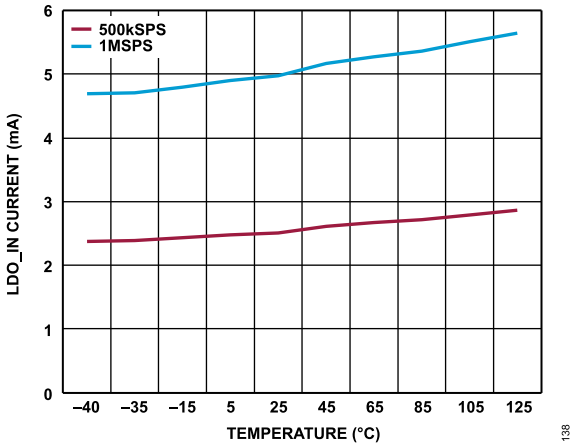

Figure 35. LDO_IN Current vs. Temperature

TYPICAL PERFORMANCE CHARACTERISTICS

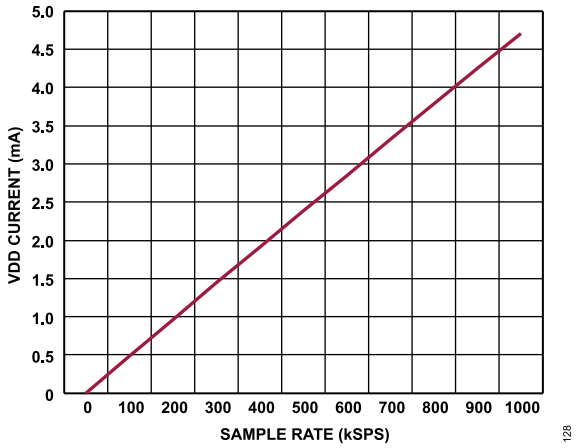

Figure 36. VDD Current vs. Sample Rate

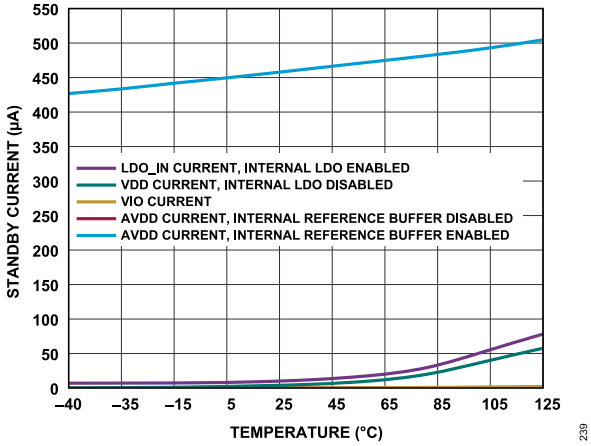

Figure 39. Standby Current vs. Temperature

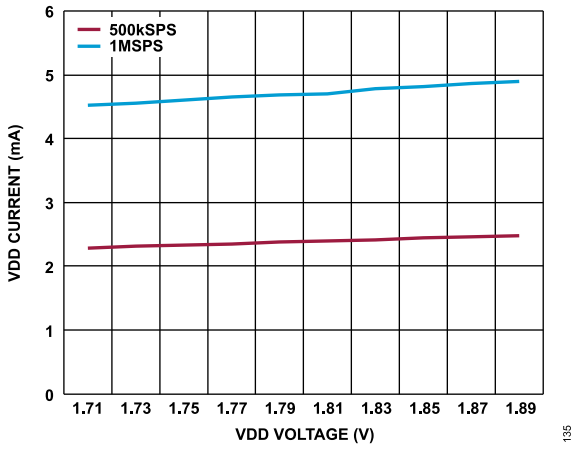

Figure 37. VDD Current vs. VDD Voltage

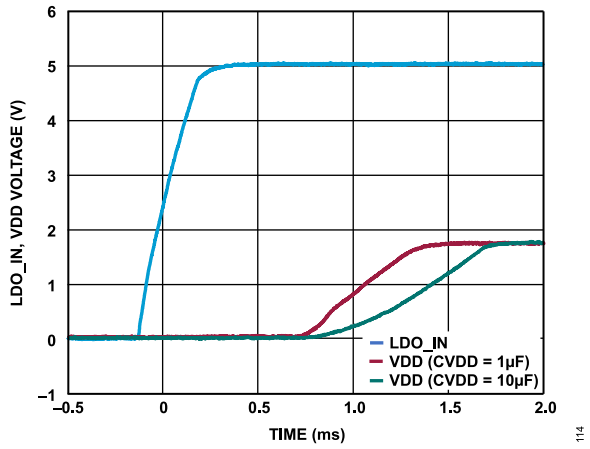

Figure 40. LDO_IN and VDD Voltage vs. Time

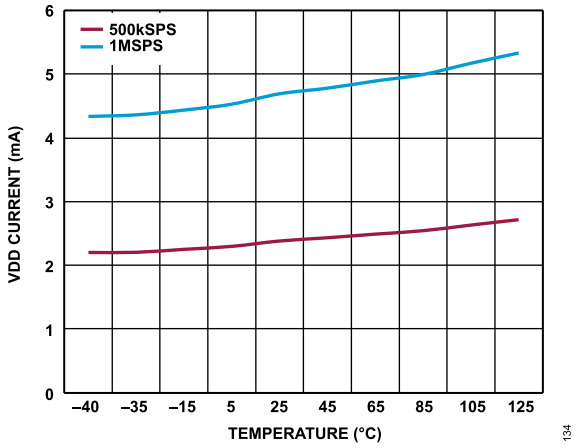

Figure 38. VDD Current vs. Temperature

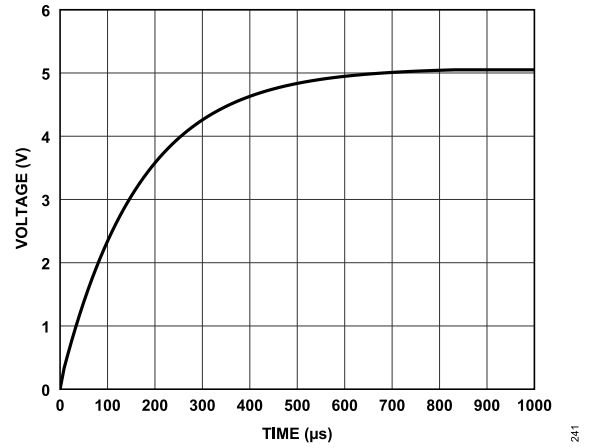

Figure 41. V_{REF} vs. Time (Internal Reference Buffer Enabled), C_{REF} = 1µF

TYPICAL PERFORMANCE CHARACTERISTICS

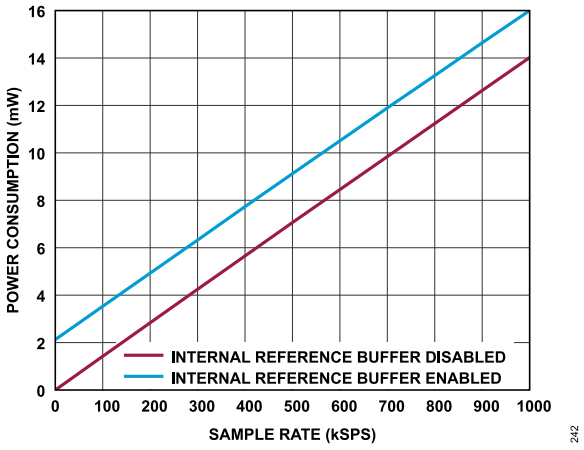

Figure 42. Power Consumption vs. Sample Rate (Internal LDO Disabled)

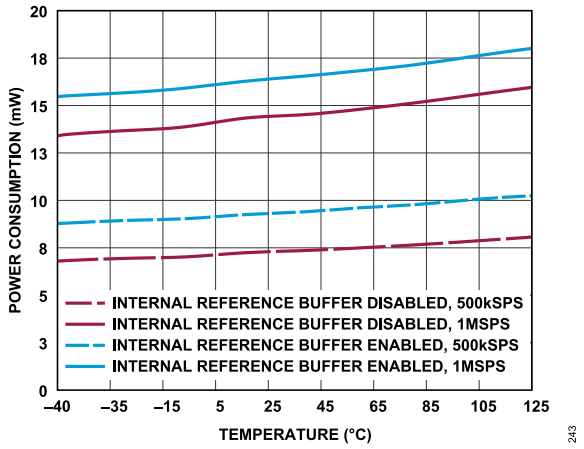

Figure 43. Power Consumption vs. Temperature (Internal LDO Disabled)

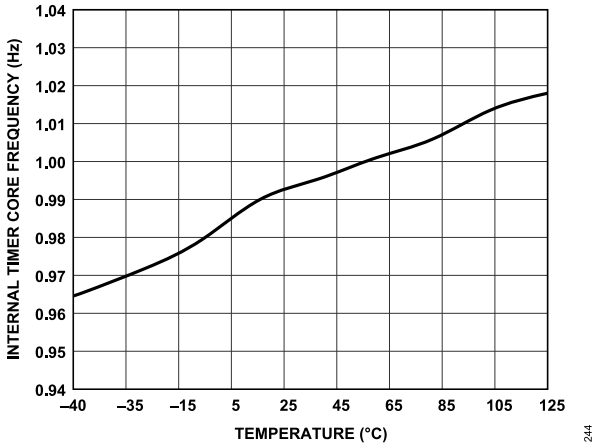

Figure 44. Internal Timer Core Frequency vs. Temperature

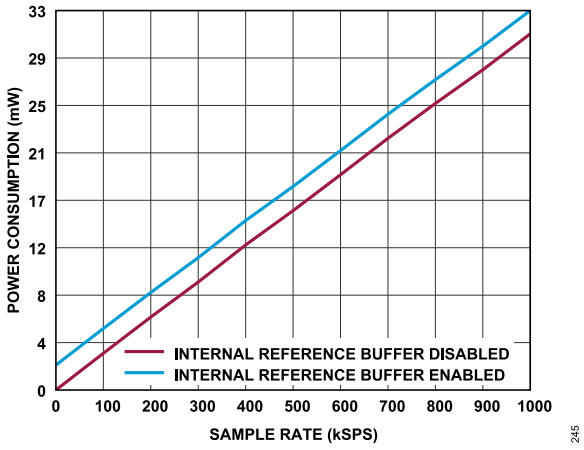

Figure 45. Power Consumption vs. Sample Rate (Internal LDO Enabled)

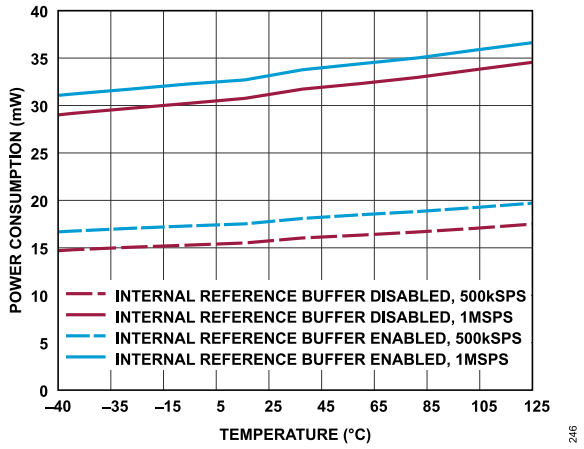

Figure 46. Power Consumption vs. Temperature (Internal LDO Enabled)

TERMINOLOGY

Integral Nonlinearity Error (INL)

INL is the deviation of each individual code from a line drawn through the two endpoints of the ADC transfer function. The two endpoints of the transfer function are ½ LSB before the first code transition and 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line.

Differential Nonlinearity Error (DNL)

In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. DNL is often specified in terms of resolution for which no missing codes are guaranteed.

Offset Error

The offset error is the deviation of the measured transition between −FSR and −FSR + 1 from the ideal transition. The ideal transition between −FSR and −FSR + 1 occurs at an analog input level ½ LSB above 0V (see the Transfer Function section).

Offset error drift is the typical change in offset error vs. temperature, expressed in µV/°C. Offset error match is the largest difference in offset error between any two input channels for a given device.

Gain Error

Gain error is the deviation of the slope of the measured transfer function and the ideal transfer function. The ideal slope is $V_{REF}/2^{16}$.

Gain error drift is the typical change in gain error vs. temperature, expressed in ppm/°C. Gain error match is the largest difference in gain error between any two input channels for a given device.

Full-Scale Error

The full-scale error is the deviation of the measured transition between +FSR – 1 and +FSR from the ideal transition, measured in LSBs. The ideal transition between +FSR − 1 and +FSR occurs for an analog input level 1½ LSB below the nominal full scale (see the Transfer Function section). Full-scale error is combination of the offset and gain errors for each device.

Full-scale error drift is the typical change in full-scale error vs. temperature, expressed in ppm/°C.

Dynamic Range

Dynamic range is the ratio of the RMS value of the full scale to the total RMS noise measured with the inputs shorted together. The value for dynamic range is expressed in dB and is measured with a signal at −60dBFS to include all noise sources and DNL artifacts.

Signal-to-Noise Ratio (SNR)

SNR is the ratio of the RMS value of the actual input signal to the RMS sum of all other spectral components below the Nyquist frequency, excluding harmonics and DC. The value for SNR is expressed in dB.

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of harmonics to the fundamental and is defined as

$$THD(\text{dB}) = 20\log\frac{\sqrt{{V_2}^2 + {V_3}^2 + {V_4}^2 + {V_5}^2 + {V_6}^2}}{V_1} \quad (1)$$

where:
V_1 is the RMS amplitude of the fundamental.
V_2, V_3, V_4, V_5, and V_6 are the RMS amplitudes of the second through the sixth harmonic.

Signal-to-Noise-and-Distortion Ratio (SINAD)

SINAD is the ratio of the RMS voltage of a full-scale sine wave to the RMS sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding DC. The value of SINAD is expressed in decibels.

Effective Number of Bits (ENOB)

ENOB is a measurement of the resolution with a sine wave input and is related to SINAD by the following formula:

$$ENOB = (SINAD - 1.76)/6.02$$

ENOB is expressed in bits.

Spurious-Free Dynamic Range (SFDR)

SFDR is the difference, in decibels (dB), between the RMS amplitude of the input signal and the peak spurious signal.

Channel-to-Channel Crosstalk

Channel-to-channel crosstalk is a measure of the level of crosstalk from a signal on an inactive channel to an active channel. Channel-to-channel crosstalk is measured by applying a full-scale interferer sine wave on one or more channels and a DC mid-scale signal on the active channel. The channel-to-channel crosstalk is the ratio of the amplitude of the interferer sine wave and the amplitude of the spectrum of the active channel at the same frequency.

Channel-to-Channel Memory

Channel-to-channel memory is a measure of the level of crosstalk that occurs when switching between channels in a channel sequence. It is measured by applying a full-scale interferer sine wave to one analog input channel and a DC voltage on another analog input channel, and repeatedly alternating sampling between the two channels on each conversion. The channel-to-channel memory is the ratio of the amplitude of the interferer sine wave and the amplitude of the spectrum of the DC-driven channel at the same frequency.

Aperture Delay

Aperture delay is the measure of the acquisition performance. Aperture delay is the time between the rising edge of the CNV

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input (or other convert-start trigger based on the selected operating mode) and when the input signal is held for a conversion.

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OVERVIEW

The AD4691/AD4692 are compact, 16-channel, 16-bit, 500kSPS/1MSPS, Easy Drive precision SAR ADCs with flexible digital processing and control features to enable a diverse range of space-constrained precision measurement applications (see Figure 1). The AD4691/AD4692 include features that reduce dependence on high-bandwidth ADC driver amplifiers and reference buffers and high-speed, low-latency digital hosts. These features include the following:

- 16-bit SAR ADC core with no missing codes and first conversion accuracy
- 16-channel, low-crosstalk multiplexer
- Precharge buffers that minimize analog input and reference input transients
- Internal reference buffer
- Overvoltage protection clamps on each analog input
- Flexible, programmable channel sequencer
- Averaging filters per channel
- Internal oscillator for autonomous and burst sampling modes
- Hardware interrupt signals for synchronization to external SPI peripherals

The AD4691/AD4692 channel sequencer and per-channel averaging filters provide flexible control of each channel's sample rate and averaging ratio to optimize for signal bandwidth and measurement resolution while offloading computations and SPI data transfers from the host processor. Including a filter per channel enables interleaved channel sequencing to minimize sampling blind spots and maximize repeatability of channel measurements (see Figure 86).

The autonomous and burst sampling modes allow the firmware to preconfigure a channel sampling sequence to execute with minimal digital overhead. The burst sampling modes also enable fast scanning of the input channels to maximize the time for the host SPI to offload the results, thereby reducing the overhead to operate the ADC and allowing power-conscious digital hosts to spend more time in sleep modes.

The AD4691/AD4692 include a novel precharge buffer feature that minimizes dependence on high-bandwidth, power-hungry ADC drivers. The analog input precharge buffers reduce the aggressive voltage transients typical of multiplexed SAR ADCs by orders of magnitude by precharging the ADC sampling capacitor to the channel's input voltage prior to acquisition. The precharge buffers thereby allow the AD4691/AD4692 to interface directly with higher impedance and lower bandwidth sensors or amplifiers than traditional precision multiplexed ADCs, and allow for drastic reductions in solution size and power consumption by removing an ADC driver amplifier per channel.

The AD4691/AD4692 are available in a 32-lead, 5mm × 5mm LFCSP or in a 36-lead 2.96 mm × 2.96 mm WLCSP.

CONVERTER OPERATION

The AD4691/AD4692 conversion process consists of three phases: the acquisition phase, the conversion phase, and the precharge phase. Figure 47 shows the timing of the ADC phases relative to convert-start. During the acquisition phase, the multiplexer connects the active channel to the ADC sampling capacitor (C_{SH}) to track the input signal. The device remains in the acquisition phase until the convert start trigger occurs to initiate a conversion. At the start of the conversion phase, the multiplexer switch opens, sampling the input signal on C_{SH}. At the end of the conversion phase (after t_{CONV} elapses), the SAR ADC core generates a corresponding 16-bit digital output.

The precharge phase occurs after the conversion phase and before the next acquisition phase. During the precharge phase, C_{SH} is driven to the voltage on the next channel to be acquired, drastically reducing the charge and voltage transients at the start of acquisition. The precharge phase ends 515ns after the start of conversion. See the Analog Input Precharge section for a detailed description of the precharge buffers and precharge phase.

The next acquisition phase starts at the end of the precharge phase. At the start of the acquisition phase, the multiplexer selects the next channel specified by the channel sequencing logic and connects it to C_{SH} to acquire the next signal until the next convert-start initiates another conversion phase.

The minimum acquisition time specification (t_{ACQ}) in Table 2 indicates the minimum amount of time that the AD4691/AD4692 are in the acquisition phase when running at their respective maximum sample rates. The t_{ACQ} is equal to the sample period (t_{CYC}) minus the combination of t_{CONV} and t_{PREQ}. Therefore, t_{ACQ} increases with longer sample periods and is equal to t_{CYC} − 515ns.

The ADC core outputs a signal called ADC_BUSY, which goes high during the conversion phase and goes low when a new sample is ready.). ADC_BUSY can be routed to the GP0 pin to the GP3 pin and used as a hardware interrupt via the GPx_MODE bit fields (see Table 52 and Table 53).

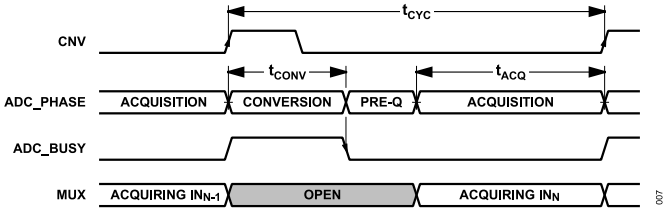

Figure 47. ADC Phase Timing Diagram

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TRANSFER FUNCTION

Figure 48 shows the ideal transfer function of the AD4691/AD4692 SAR ADC core. The ADC core encodes the sampled voltage as a fraction of the full-scale range (FSR) into a 16-bit digital code. The transfer function consists of 2^{16} LSBs, where 1 LSB is the smallest discrete voltage step that can be resolved by the ADC and is equal to ($V_{REF}/2^{16}$)V. The AD4691/AD4692 input range is unipolar (0 to V_{REF}), and its output codes are in straight binary format ranging from 0 to 65,535. Table 12 shows the ideal transfer function mapping from input voltage to output code for each LSB using V_{REF} = 5V as an example.

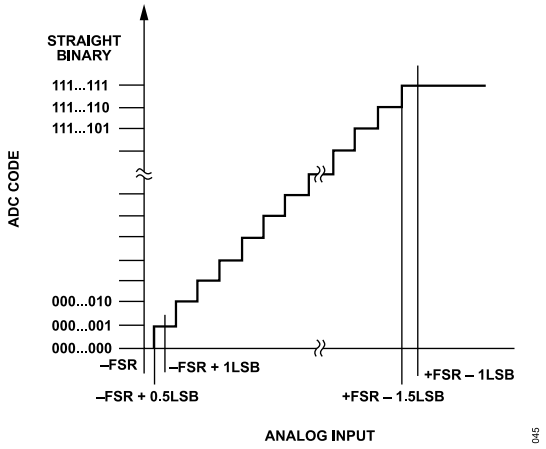

Figure 48. ADC Ideal Transfer Function (FSR Is Full-Scale Range)

Table 12. ADC Input Voltage to Output Code Mapping

Description	Input Voltage	Digital Output Code
FSR − 1 LSB	(65535/65536) × V_{REF}	0xFFFF
...	...	...
Midscale + 1 LSB	(32769/65536) × V_{REF}	0x8001
Midscale	(½) × V_{REF}	0x8000
Midscale − 1 LSB	(32767/65536) × V_{REF}	0x7FFF
...	...	...
−FSR + 1 LSB	(1/65536) × V_{REF}	0x0001
−FSR	0 V	0x0000

EASY DRIVE FEATURES

Traditional multiplexed SAR ADCs typically exhibit aggressive charge and voltage transients on their analog inputs that require the addition of high-speed, low-noise, and power-hungry ADC driver amplifiers per channel. The need for dedicated ADC drivers per channel drastically increases the system size and power dissipation, compromising the goal for small and power-efficient multichannel precision measurements. The AD4691/AD4692 are equipped with several Easy Drive features which ease the signal chain design challenges associated with multiplexed SAR ADCs and enable power- and space-efficient multichannel precision measurement solutions.

The AD4691/AD4692 include analog input precharge buffers that dramatically reduce the input transients typical of multiplexed SAR ADCs. The smaller transients allow the AD4691/AD4692 to tolerate higher impedance signal sources without compromised sampling accuracy, thereby enabling direct interfacing with precision-focused amplifiers without high-speed ADC drivers. The reduced transient also allows for lower capacitance and higher resistance in the RC input filters, reducing instability concerns and power dissipation for the front-end amplifiers. See the Analog Input Precharge section for more information.

The AD4691/AD4692 also include a precharge buffer on the REF input to reduce transients on the V_{REF} signal. The reference input precharge buffer reduces the voltage reference transient response requirements for directly driving the ADC REF input without a dedicated reference buffer. The reduced average REF current reduces also allows the ADC to tolerate larger series resistance between the reference source and the REF input without compromising accuracy.

The WLCSP package option for AD4691/AD4692 features a true buffered reference input (REFIN). The internal reference buffer is useful in applications using unbuffered, low power reference sources, for references that require external noise filtering, or where multiple devices share a common reference source. See the Internal Reference Buffer section for more information.

The AD4691/AD4692 include overvoltage protection clamps on IN0 to IN15 and COM to reduce the risk of device damage from sustained DC overvoltage events. These clamps eliminate the need for external clamping diodes in systems where the input driving circuitry positive supply rail is greater than V_{REF}. See the Input Overvoltage Protection Clamps section for more information.

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ANALOG INPUTS

Figure 49 shows an equivalent circuit of the AD4691/AD4692 analog inputs, which include IN0 through IN15 and COM.

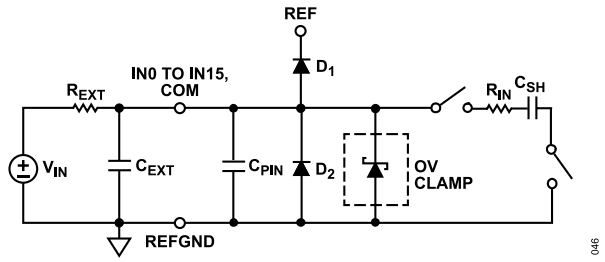

Figure 49. Equivalent Analog Input Circuit

A low crosstalk analog multiplexer routes the signals from the analog input pins to the ADC core inputs. The impedance of the analog inputs is modeled as the parallel combination of the pin capacitance (C_{PIN}) and the network formed by the series connection of R_{IN} and C_{SH}. R_{IN} represents the ADC input series resistance and the multiplexer switch resistance and is typically 240Ω. C_{SH} represents the ADC sampling capacitor and is typically 60pF.

Each analog input has a dedicated overvoltage protection clamp circuit, represented by OV CLAMP in Figure 49. The clamps protect the analog inputs from DC overvoltage conditions and eliminate the need for additional external protection diodes. See the Input Overvoltage Protection Clamps section for a detailed description of the overvoltage protection clamps.

R_{EXT} and C_{EXT} in Figure 49 represent an external, RC low-pass filter, which is used to provide immediate charge for C_{SH} at the start of acquisition. As described in the Easy Drive Features section and the Analog Input Precharge section, C_{SH} is precharged to the next channel's voltage before the start of acquisition, allowing for smaller values of C_{EXT} and higher values of R_{EXT} than traditional multiplexed SAR ADCs.

Multiplexer Configuration Options

The AD4691/AD4692 contain a flexible, low crosstalk analog multiplexer for selecting from the 16 analog inputs and routing them to the inputs of the 16-bit SAR ADC core. Figure 50 shows a simplified schematic of the internal multiplexer. SW_{MUX+} and SW_{MUX-} represent the multiplexer switches that route the selected channel to the ADC inputs. SW_{MUX+} and SW_{MUX-} are break-before-make and are controlled by the internal channel sequencing logic (see the Channel Sequencer section).

Each of the AD4691/AD4692 input channels can be configured in single-ended mode or pseudo differential mode, as shown in Figure 50. In single-ended mode, SW_{MUX-} connects the ADCIN− input to REFGND to sample the input signal with respect to the device ground. In pseudo differential mode, SW_{MUX-} connects the ADCIN- input to COM to sample the input signal with respect to signal ground.

Pseudo differential mode can be used in systems with a dedicated signal ground to attenuate common-mode noise from the sampled signal. Figure 19 shows the typical CMRR of the AD4691/AD4692, which represents the attenuation factor for a common-mode signal between the ADCIN+ and ADCIN− inputs to the ADC across frequency. Note that the input voltage range for COM is REFGND ± 0.1V, so the signal ground connected to COM must also be common to the device ground.

The channel configuration settings for each channel are determined by the active channel sequencer mode and the IN_MODE bits in the CONFIG_INn registers. In standard sequencer mode, the IN_MODE bit in the CONFIG_IN0 register sets the channel configuration mode for all 16 channels. In advanced sequencer mode, each channel's configuration mode is set independently via the IN_MODE bits in their corresponding CONFIG_INn register. Figure 98 shows a flowchart for configuring the analog input modes for each sequencer mode.

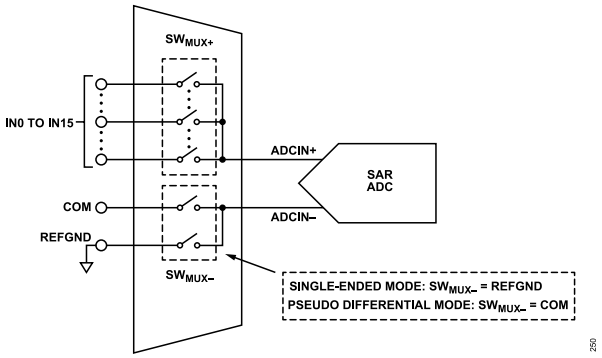

Figure 50. Multiplexer Simplified Connection Diagram

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ANALOG INPUT PRECHARGE

The AD4691/AD4692 analog input precharge buffers enable efficient multichannel data acquisition designs by reducing the need for high-speed ADC driver amplifiers for each channel. Traditional multiplexed SAR ADCs exhibit large input transients caused by voltage mismatches between channels. These transients must be settled to within ½ LSB of the ADC, forcing strict requirements on the analog front-end circuit that increase power, area, and noise.

In traditional multiplexed ADCs, the C_{SH} sampling capacitor holds the sampled voltage from the previous channel. When the multiplexer progresses to the next channel, the voltages on the input pin and sampling capacitor can be as large as V_{REF}, resulting in a spike of current through the channel as charge is rapidly redistributed to equalize the voltage. The magnitude of the resulting glitch is a related to the magnitude of the voltage mismatch and the size of the external capacitor (C_{EXT} in Figure 49).

The AD4691/AD4692 input precharge buffers drive C_{SH} to the voltage on the next channel prior to acquisition, thus reducing the input glitches by orders of magnitude. The precharge buffers are power efficient alternatives to integrated buffers because they power down between conversions and their power consumption scales with sampling rate (see Figure 42 and Figure 45).

Figure 51 and Figure 52 illustrate the precharging action with an example channel sequence of IN0 and IN1. Each precharge buffer includes a parallel sampling path to track and hold the next channel's signal while the ADC core samples the previous channel. The precharge buffer phases are aligned to the ADC conversion and acquisition phases and the channel sequencing logic.

Prior to the first conversion, the ADC core tracks IN0 through the multiplexer (through IN0_SH) while the precharge sampling circuit tracks IN1 (through PQ1_SH). The first convert-start triggers the ADC and IN1 precharge sampling switches to open, sampling the voltages on IN0 and IN1. At the end of the conversion the ADC has finished converting the IN0 voltage and the IN1 precharge phase begins. The IN1 precharge buffer powers up and sources or sinks current from sampling capacitor to drive it to IN1 voltage. When the precharge phase ends, the IN1 pin is connected to the sampling capacitor through the multiplexer. At the next convert-start, the process repeats with the ADC sampling IN1 and the IN0 precharge buffer sampling IN0 (through PQ0_SH).

The time delay between convert-start and the end of the precharge phase is 515ns. The precharge buffers drive the sampling capacitor to within 5mV accuracy during the precharge phase, equivalent to 0.1% full-scale for a 5V V_{REF}. This effectively reduces the charge loss per sample to 300fC, 1000 times lower than an equivalent multiplexed ADC without precharge.

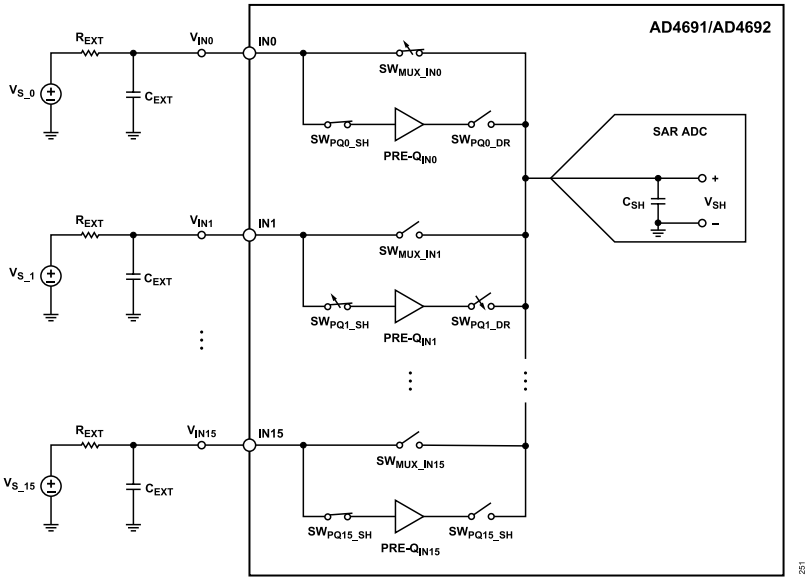

Figure 51. Precharge Buffer Simplified Circuit Diagram

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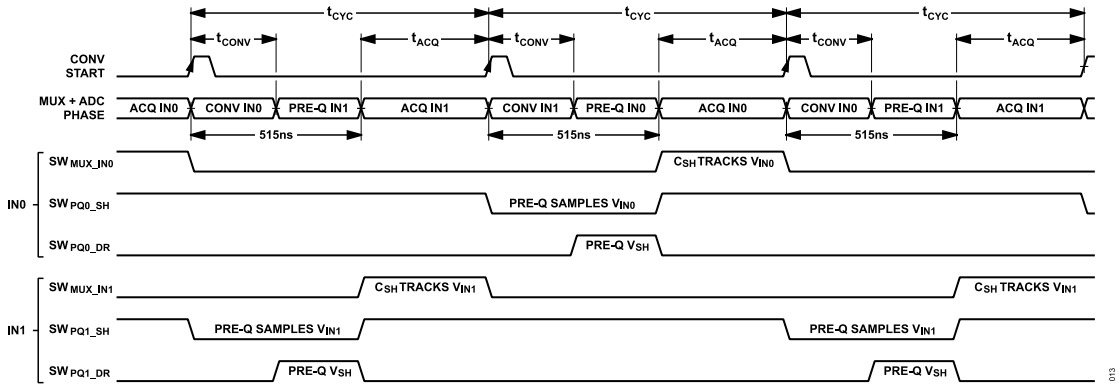

Figure 52. Precharge Example Timing Diagram

INPUT OVERVOLTAGE PROTECTION CLAMPS

The AD4691/AD4692 include overvoltage protection clamps on IN0 to IN15 and COM to reduce the risk of device damage from sustained DC overvoltage events. These clamps reduce the need for external clamping diodes in systems where the input driving circuitry positive supply rail is greater than V_{REF}.

The overvoltage protection clamps limit the extent to which input overvoltage events disturb the reference source. When active, the clamps limit the voltage on the analog inputs to the specified clamping voltage and conduct the input current to ground rather than through the ESD diode connecting the analog input to the REF input (D1 in Figure 49), which prevents overvoltage conditions on one analog input from degrading performance on other analog inputs or other devices sharing the reference.

Table 1 shows the activation, deactivation, and clamping voltages of the overvoltage protection clamps. Figure 28 show typical behavior of the clamps during overvoltage conditions. The clamp circuits activate when the analog input voltage exceeds the activation voltage. The clamps deactivate when the input voltage drops below the deactivation voltage. While a clamp is active, a flag is set in the status registers that can be read by the digital host (see the Overvoltage Clamp Flags section).

Each overvoltage protection clamp circuit supports a maximum sustained current of 5mA. All 17 clamp circuits can sink 5mA simultaneously without damaging the device. The clamp current is a function of V_{REF}, the external series resistance (such as R_{EXT} in Figure 49), and the output voltage of the AFE circuitry.

Overvoltage Clamp Flags

The AD4691/AD4692 provide several means to check the status of the overvoltage protection clamps.

The INX_CLAMP_FLAG bits in the CLAMP_STATUS1 and CLAMP_STATUS2 registers indicate the status of the overvoltage protection clamps for IN0 to IN15. Each INX_CLAMP_FLAG bit is asserted when the corresponding input clamp circuit is active and is deasserted when the corresponding input clamp circuit is inactive. The CLAMP_FLAG bit in the DEVICE_STATUS register is asserted when any combination of the overvoltage clamps on IN0 to IN15 are activated (when any of the INX_CLAMP_FLAG bits are asserted). This bit is sticky and is only cleared when it is read while all clamps are inactive.

The COM_CLAMP_FLAG bit in the status register is asserted when the COM input overvoltage protection clamp activates and is deasserted when the COM input overvoltage protection clamp deactivates.

VOLTAGE REFERENCE INPUT

V_{REF} sets the ADC full-scale voltage (see the Transfer Function section). The ADC core samples the voltage on the reference input (REF) during the bit trials in the conversion process to determine the output code result. The AD4691/AD4692 are compatible with reference voltages from 2.4V to 5.1V.

A common challenge presented by traditional SAR ADCs is in designing reference circuitry with sufficient drive capability to maintain a precise V_{REF} while the REF input dynamically draws input current during the SAR bit trials. The reference input precharge buffer reduces the REF input transient current spikes and allows a broader selection of voltage reference and amplifiers to drive the AD4691/AD4692 REF input without degrading accuracy. The REF precharge buffer allows the reference decoupling capacitor (C_{REF}) to be as small as 1µF, an order of magnitude smaller than traditional SAR ADCs.

The WLCSP models of the AD4691/AD4692 also include an internal reference buffer for a true buffered reference input (see the Internal Reference Buffer section).

The AD4691/AD4692 must be configured for optimal performance with the selected reference voltage. The VREF_SET bit field in the REF_CTRL register provides five V_{REF} range options, as shown in Table 40. This value must be programmed to match the V_{REF} voltage applied to the REF pin. Figure 99 shows a flowchart for configuring the reference input and reference buffer.

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Internal Reference Buffer

The internal reference buffer (available only in the WLCSP option of the AD4691/AD4692) provides a true buffered reference input (REFIN). The internal reference buffer is useful in applications using unbuffered, low power voltage references, or where multiple devices share a common reference source with the AD4691/AD4692. The internal reference buffer's true high impedance input allows for more aggressive low pass filtering between the voltage reference and the ADC input.

When the internal reference buffer is enabled, the maximum allowable V_{REF} is AVDD – 0.3V (see Table 1), the AVDD supply consumes 470µA additional standby current. Table 1, Figure 42 through Figure 46 show the power consumption with the internal reference buffer disabled and enabled.

Figure 53 shows a simplified diagram of the AD4691/AD4692 internal reference buffer. The internal reference buffer is enabled by setting the REFBUF_EN bit in the REF_CTRL register to 1. The internal reference buffer is disabled by default.

The internal reference buffer turn-on time specification (t_{REFBUF} in Table 1) is the delay between enabling the internal reference buffer and the REF pin voltage transitioning from 0V to V_{REF} within 0.01%. t_{REFBUF} is proportional to the REF decoupling capacitor (C_{REF}).

When not using the internal reference buffer, REFIN must be shorted to REF, and the REFBUF_EN bit must remain set to 0 to ensure the internal reference buffer is disabled.

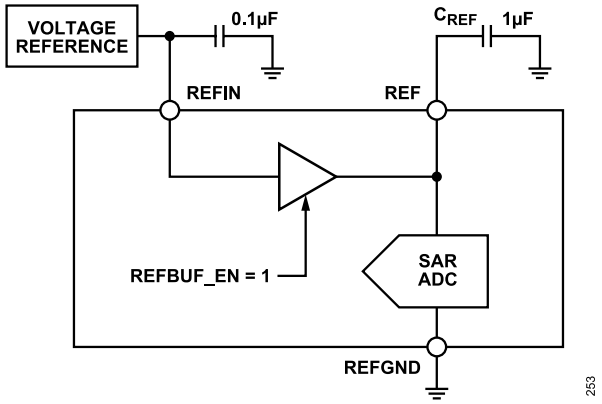

Figure 53. Internal Reference Buffer Simplified Schematic

POWER SUPPLIES

The AD4691/AD4692 have the following four power domains:

- AVDD is the analog supply rail
- VDD is the ADC core supply rail
- VIO is the digital interface logic supply rail
- LDO_IN is the input to the internal LDO regulator that can optionally supply the VDD rail internally

See Table 1 for the voltage ranges for each power supply input.

The AD4691/AD4692 are independent of the power supply sequencing between VIO, VDD, and AVDD (and LDO_IN when the internal LDO is enabled). When VIO and VDD are first supplied, a power-on reset (POR) initiates (see the Device Reset section). Additionally, the AD4691/AD4692 are insensitive to power supply ripple over a wide frequency range, as shown in Figure 20.

VDD powers both the ADC core and the device register memory. When VDD is powered down (for example, when disabling the internal LDO regulator to go into a low-power state), the configuration registers are cleared.

Decouple AVDD, LDO_IN, VDD to AGND, and VIO to IOGND with at least 100nF. When shorting AVDD and LDO_IN, a single decoupling capacitor can be used for both pins. When not using the internal LDO, LDO_IN does not require decoupling. As described in the Internal LDO Regulator section, the internal LDO regulator requires a decoupling capacitor of at least 100nF on the VDD pin for proper device operation.

Internal LDO Regulator

The AD4691/AD4692 include an optional internal LDO regulator to power the +1.8V VDD rail internally and minimize the number of required system supplies. LDO_IN can be tied to AVDD to enable a single source to supply AVDD and VDD.

The output of the internal LDO regulator is internally connected to the VDD pin. When the internal LDO is enabled, its output drives VDD internally (see Figure 54). To enable the internal LDO regulator, LDO_IN must be driven to at least 2.4V, VIO must already be powered, and the LDO_EN bit in the DEVICE_SETUP register must be set to 1. The internal LDO regulator is enabled by default on device power-up and after device resets. It is not possible to power the VIO supply with the internal LDO regulator output. VIO must be supplied by the digital host or other system supply rail.

The internal LDO regulator requires an output decoupling capacitor for stable operation. When using the internal LDO, include a 100nF to 10µF decoupling capacitor between the VDD and AGND pins.

When the internal LDO regulator is disabled, its output is disabled and high impedance. When not using the internal LDO, LDO_IN must be tied to AGND and VDD must be supplied externally (see Figure 55). Clear the LDO_EN bit of the DEVICE_SETUP register when powering VDD externally, even if the LDO_IN input is shorted to AGND. Figure 99 shows a flowchart for enabling or disabling the internal LDO regulator.

The internal LDO regulator output is designed to withstand being powered up with VDD either driven by a separate 1.8V supply or inadvertently shorted to AGND. Ensure that the VDD pin is disconnected from any other rails or loads. The internal LDO is not intended to power additional devices.

The internal LDO regulator can be temporarily disabled to put the AD4691/AD4692 in a low power state without disabling the AVDD, LDO_IN, or VIO rails. When the internal LDO regulator is disabled

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(while VDD is not powered by an external supply), the ADC core shuts down, and the configuration register contents are erased. The internal LDO regulator can be enabled again either with a wake-up command over the SPI or with a hardware reset. The wake-up command is 0x000081 and is identical to performing a software reset (see the Device Reset section for detailed descriptions of hardware and software resets). The digital interface requires that VIO still be supplied to accept the wake-up command, and the internal LDO regulator is not enabled if VIO is not within the specified range (see Table 1).

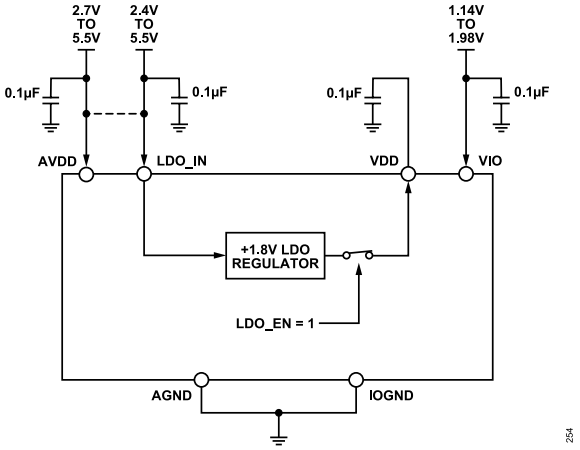

Figure 54. Powering VDD with the Internal LDO Regulator

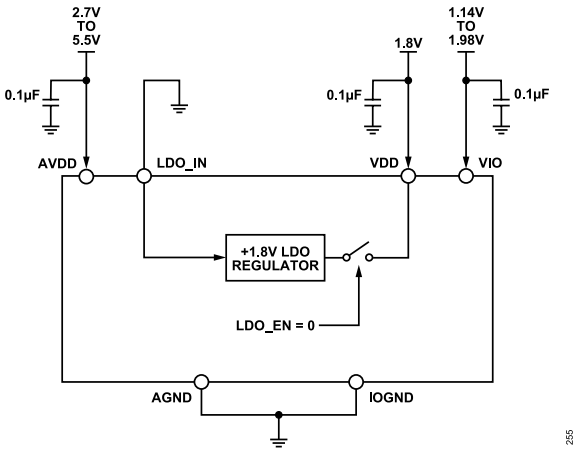

Figure 55. Powering VDD Externally

CHANNEL SEQUENCER

The AD4691/AD4692 include a channel sequencer which automates scanning through a user programmed sequence of channels in sync with ADC sampling. The channel sequencer controls the multiplexer switches to update the active channel once per ADC conversion.

The channel sequencer includes two sequencing modes. Standard sequencer mode supports simple channel sequences where all channels have the same sampling rates and averaging ratios (see the Standard Sequencer Mode section). Advanced sequencer mode supports fully custom channel sequences and enables different sampling rates and averaging ratios per channel (see the Advanced Sequencer Mode section). The channel sequencer mode is set by the SEQ_MODE bit in the SEQ_CTRL register.

The channel sequencer generates an active low end of sequence ($\overline{EOS}$) status signal which indicates when the sequencer has reached the end of the programmed sequence. $\overline{EOS}$ can optionally be driven out on the GP0 pin to theGP3 pin to act as an interrupt signal and can be assigned as the stop trigger in burst sampling modes. See the End of Sequence (EOS) Signal section for more information.

All channels included in the channel sequence must be unmasked prior to performing conversions to ensure proper functionality of the $\overline{DRDY}$ signal and prevent lockout conditions (see the Data Ready (DRDY) Signal section for more information).

The channel sequencer is enabled in all operating modes except manual mode, where the digital host sends the channel sequence in real time over the SPI (see the Manual Mode section for more information).

End of Sequence ($\overline{EOS}$) Signal

The AD4691/AD4692 channel sequencer includes an ($\overline{EOS}$) signal that goes low at the end of the channel sequence. $\overline{EOS}$ is asserted after the ADC core completes a conversion on the last channel in the sequence, causing the sequencer to roll over to the first channel in the sequence. The $\overline{EOS}$ signal de-asserts after the next conversion or following a state reset. $\overline{EOS}$ is supported in both standard sequencer mode and advanced sequencer mode, and it is pictured in Figure 57 and Figure 59.

$\overline{EOS}$ can be routed to the general purpose pins to function as a hardware interrupt (see Table 18).

$\overline{EOS}$ can also be assigned as the internal oscillator stop trigger for automatically stopping burst sampling in CNV burst mode and SPI burst mode. In these modes, the AD4691/AD4692 autonomously execute a burst of samples through a single iteration of the channel sequence (see the CNV Burst Mode and SPI Burst Mode sections).

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Standard Sequencer Mode

Standard sequencer mode is the simpler of the two sequencer modes and is recommended when every channel needs the same output data rate and when arbitrary channel orders are not required.

In standard sequencer mode, the channel sequencer scans through a preprogrammed set of enabled channels in ascending order. Each channel is enabled or disabled through their corresponding INx_EN bits in the STD_SEQ_CONFIG register. The sequencer scans through each enabled channel in ascending order and skips each disabled channel. Each enabled channel is therefore sampled once per sequence iteration. Figure 56 and Figure 57 show examples where the standard sequencer and four analog inputs (IN0, IN2, IN5, and IN7) are enabled in the sequence.

Standard sequencer mode is selected by setting the SEQ_MODE bit to 1 in the SEQ_CTRL register. The INx_EN bits in the STD_SEQ_CONFIG register configure each INx channel as enabled (INx_EN = 1) or disabled (INx_EN = 0). The STD_SEQ_CONFIG register is a 16-bit wide register and must be written to in its entirety in one SPI frame (see the Register Length section). By default, the channel sequencer is in standard sequencer mode with IN0 enabled and all other channels disabled.

A state reset is required to update the internal state of the channel sequencer after updating the SEQ_MODE bit or the INx_EN bits (see the State Reset section). In standard sequencer mode, the multiplexer channel is set to the lowest-numbered enabled channel in the sequence following a state reset.

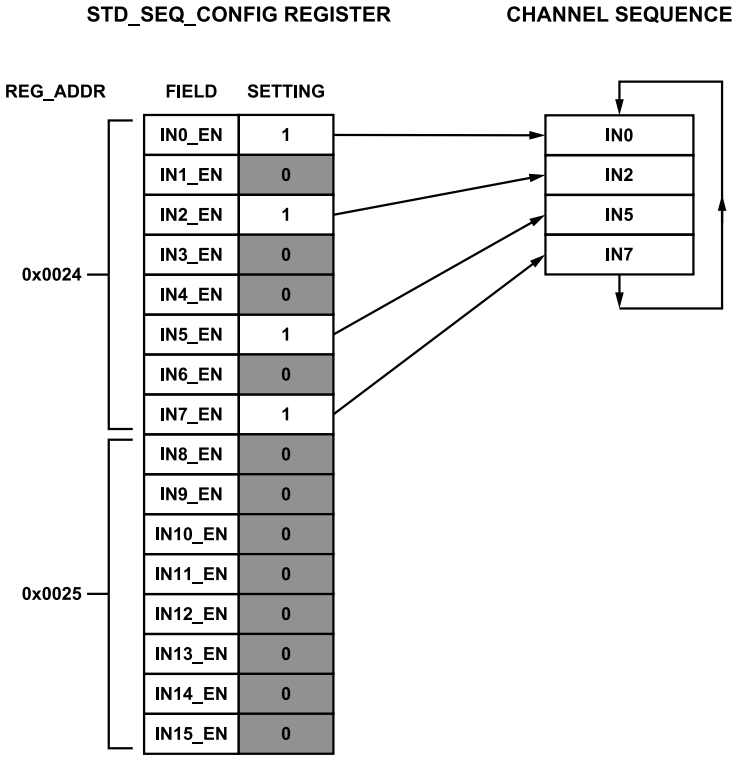

Figure 56. Standard Sequencer Simplified Diagram

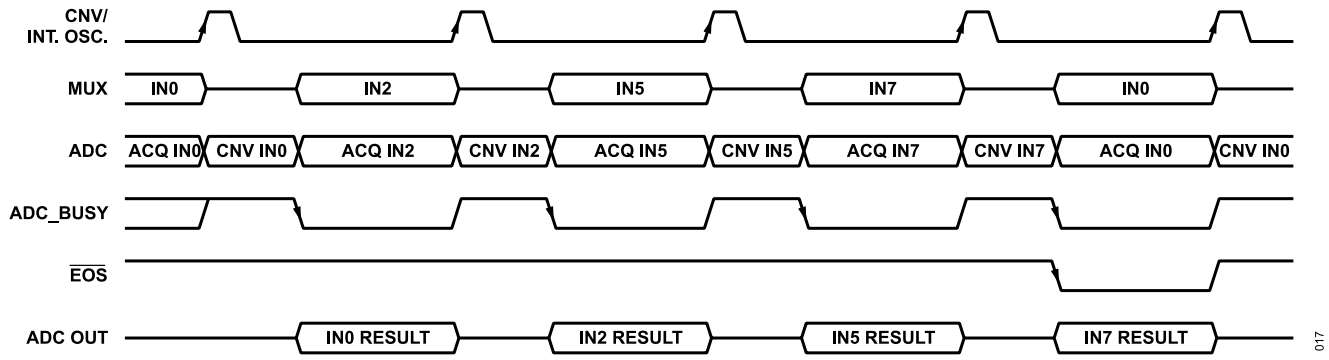

Figure 57. Standard Sequencer Example Timing Diagram

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Advanced Sequencer Mode

Advanced sequencer mode scans through a preprogrammed channel sequence where the order of channels is completely customizable. Advanced sequencer mode enables flexible sample rates and decimation rates per channel, as described in the Effective Channel Sample Rate section.

In advanced sequencer mode, the channel sequence is defined as a series of slots, where each slot can be assigned to any of the 16 channels. The sequence length is programmable between one and 128 slots. The sequencer progresses through the slots in ascending order starting from Slot 0. Figure 59 shows an example where the advanced sequencer is enabled with a sequence length of four slots assigned to Channel IN4, Channel IN6, Channel IN4, and Channel IN2.

Advanced sequencer mode is selected by setting the SEQ_MODE bit in the SEQ_CTRL register to 0. The sequence length is set with the NUM_SLOTS_AS bit field in the SEQ_CTRL register. The sequence length is equal to NUM_SLOTS_AS + 1. In the example shown in Figure 58, the NUM_SLOTS_AS bit field is set to 3 to implement a sequence that is four slots long.

The channel assignment of each Slot is set with the SLOT_INX bit fields in the AS_SLOT0 through AS_SLOT127 registers, where AS_SLOT0 corresponds to Slot 0, AS_SLOT1 corresponds to Slot 1 and so on. Table 45 shows the corresponding values of SLOT_INX for each of the 16 analog inputs.

A state reset is required to update the internal state of the channel sequencer after updating the SEQ_MODE bit, NUM_SLOTS_AS bit field, or the AS_SLOTX registers (see the State Reset section). In advanced sequencer mode, the multiplexer channel is set to the channel assigned to Slot 0 (set by the AS_SLOT0 register).

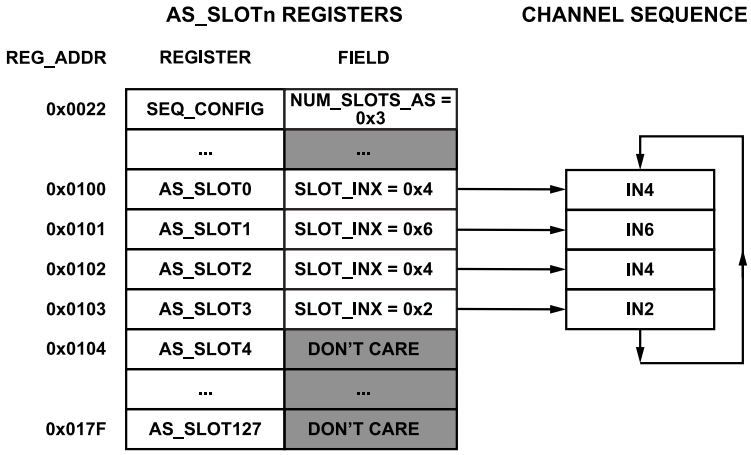

Figure 58. Advanced Sequencer Simplified Diagram

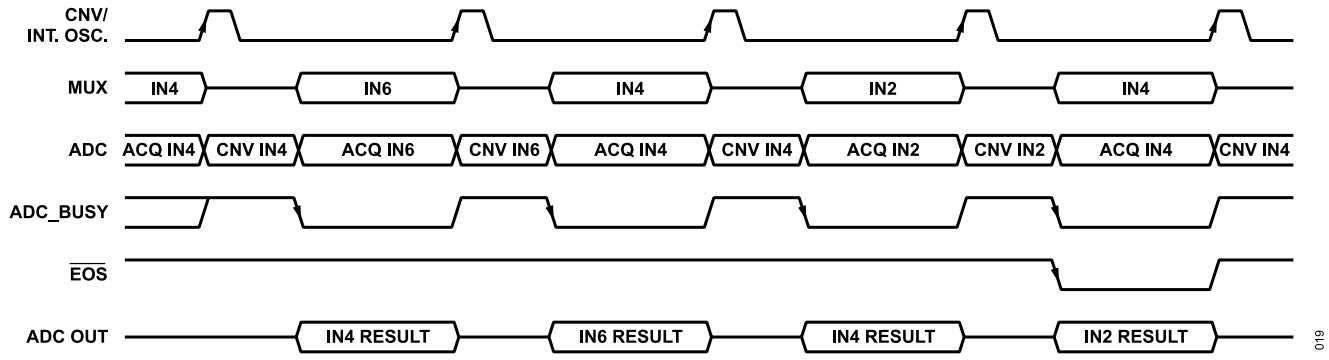

Figure 59. Advanced Sequencer Example Timing Diagram

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AVERAGING FILTERS

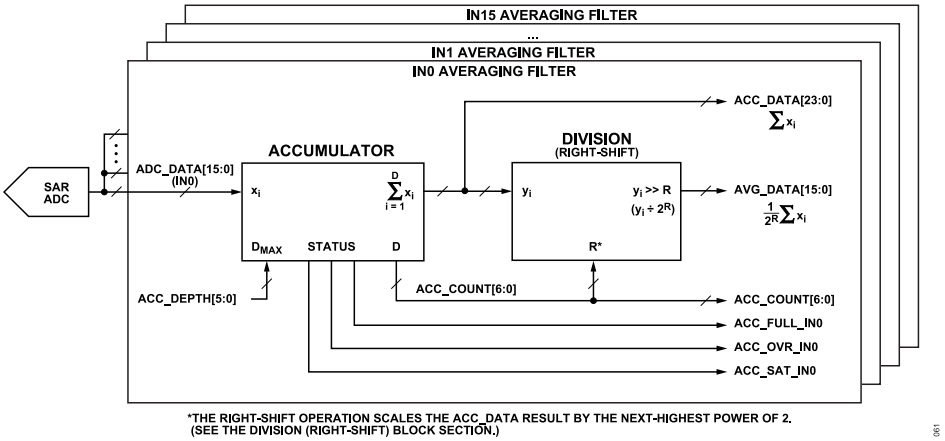

Figure 60. Averaging Filter Simplified Diagram

The AD4691/AD4692 feature averaging filters for each of their 16 channels. The averaging filters provide on-chip noise filtering to improve measurement resolution and dynamic range. The inclusion of a dedicated averaging filter for each channel prevents one channel's data from overwriting another, effectively decoupling channel sequencing from the averaging filter and enabling interleaved channel sampling for more accurate multichannel measurements.

Figure 60 shows a simplified diagram of the averaging filters. Each filter includes an accumulator block and a division (right-shift) block to perform the addition and division of the averaging function, respectively. The accumulators calculate the running sum of ADC samples from their corresponding input channel, and the division block right-shifts the 24-bit sum to scale it to a 16-bit averaged value. The AD4691/AD4692 support SPI readback of the raw 24-bit accumulator output or the 16-bit averaged output (see the Averaging Filter Readback section).

The averaging filters are enabled in all modes except manual mode. If averaging is not required, set the accumulator depth settings for each channel to 1 and read from the 16-bit AVG_INx registers to effectively set the averaging ratio to 1. See the Accumulators section for more information.

Accumulators

The accumulator block of each averaging filter performs the running sum portion of the averaging calculation. Each accumulator outputs the sum of conversion results taken from its corresponding channel. Each accumulator has a data output (ACC_DATA) and a sample counter (ACC_COUNT) that outputs the current sum of samples and number of samples in the sum, respectively. ACC_COUNT is incremented each time the accumulator receives a new sample from its channel.

Each accumulator accepts new samples until it reaches its programmed depth setting, after which it is considered full and ignores new samples until it is reset. The depth settings therefore set the effective accumulation (and averaging) ratio for each channel.

The accumulator depth can be set between 1 and 64 via the ACC_DEPTH bit fields in the ACC_DEPTH_IN0 through ACC_DEPTH_IN15 registers. The depth setting is equal to ACC_DEPTH + 1, where ACC_DEPTH is an integer value between 0 and 63. By default, all channels are configured with a depth of 64 samples.

In standard sequencer mode, the ACC_DEPTH_IN0 register sets the depth for all 16 channels, ensuring all channels have the same effective averaging ratio. In advanced sequencer mode, the depth of each channel is independently set by their corresponding ACC_DEPTH_INx register, allowing each channel to have a different averaging ratio.

The ACC_DATA data are formatted as a right-justified 24-bit code that can be read directly via the ACC_IN0 through ACC_IN15 or ACC_STS_IN0 through ACC_STS_IN15 registers, as described in the Averaging Filter Readback section). ACC_DATA and ACC_COUNT maintain their states after being read. A state reset is required to clear the ACC_DATA and ACC_COUNT to prepare the accumulators for new samples (see the State Reset section).

Division (Right-Shift) Block

Each averaging filter contains a division block to scale the accumulator's running sum output (ACC_DATA) to a 16-bit averaged value (AVG_DATA). The division block performs right-shift operations on the ACC_DATA data to divide it by powers-of-2. The division block monitors the ACC_COUNT counter value of the accumulator to determine the number of right-shift operations needed to divide ACC_DATA by the next-highest power-of-2. Table 13 summarizes the relationship the ACC_COUNT counter value and the corresponding number of right-shift operations.

The outputs of the division block feed the outputs of the averaging filter, as shown in Figure 60. Each averaging filter's AVG_DA-

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TA output can be read via the AVG_IN0 through AVG_IN15 or AVG_STS_IN0 through AVG_STS_IN15 registers (see the Averaging Filter Readback section).

Note that because the division block performs right-shift operations instead of arithmetic division, the averaging filter only divides by powers-of-2. When ACC_COUNT is a power-of-2, the LSB size of the 16-bit AVG_DATA data is equal to the LSB size of the 16-bit ADC core (as described in the Transfer Function section). When ACC_COUNT is not a power-of-2, the running sum is divided by a larger divisor than a true mean calculation would use, resulting in a smaller effective LSB size and a loss in resolution. When reading from AVG_DATA, it is therefore recommended to set the accumulator depth to a power-of-2. Otherwise, it is recommended to read the ACC_DATA value instead (and optionally perform divide-by-depth in the digital host).

Table 13. Averaging Filter Right-Shift Operations vs. ACC_COUNT

ACC_COUNT	Right-Shifts	Effective Divisor
1	0	1
2	1	2
3, 4	2	4
5 to 8	3	8
9 to 16	4	16
17 to 32	5	32
33 to 64	6	64

Averaging Filter Readback

The AD4691/AD4692 include the following four sets of registers for reading data (and optional status) from the averaging filters:

- AVG_IN0 through AVG_IN15 contain the 16-bit averaged data from each channel
- AVG_STS_IN0 through AVG_STS_IN15 contain the 16-bit averaged data plus eight bits of status from each channel
- ACC_IN0 through ACC_IN15 contain the 24-bit accumulator output from each channel
- ACC_STS_IN0 through ACC_STS_IN15 contain the 24-bit accumulator output plus eight bits of status from each channel

Table 14 through Table 17 summarize the names, addresses, and contents of the four readback register sets. The Bulk Reading ADC Data Registers section provides recommendations for reading multiple (or all) channels' registers in a single SPI frame for efficient data transfer to the digital host.

Figure 101 shows a flowchart for selecting between the different readback register sets.

Table 14. Averaging Filter Data Registers (AVG_INx)

Register Name	Register Address	Register Contents
AVG_IN0	0x0200	AVG_DATA[7:0]
	0x0201	AVG_DATA[15:8]
AVG_IN1	0x0202	AVG_DATA[7:0]
	0x0203	AVG_DATA[15:8]
...	...	...
AVG_IN15	0x021E	AVG_DATA[7:0]
	0x021F	AVG_DATA[15:8]

Table 15. Averaging Filter Data Plus Status Registers (AVG_STS_INx)

Register Name	Register Address	Register Contents
AVG_STS_IN0	0x0220	ACC_ERR, ACC_COUNT[6:0]
	0x0221	AVG_DATA[7:0]
	0x0222	AVG_DATA[15:8]
...	...	...
AVG_STS_IN15	0x024D	ACC_ERR, ACC_COUNT[6:0]
	0x024E	AVG_DATA[7:0]
	0x024F	AVG_DATA[15:8]

Table 16. Accumulator Data Registers (ACC_INx)

Register Name	Register Address	Register Contents
ACC_IN0	0x0250	ACC_DATA[7:0]
	0x0251	ACC_DATA[15:8]
	0x0252	ACC_DATA[23:16]
...	...	...
ACC_IN15	0x027D	ACC_DATA[7:0]
	0x027E	ACC_DATA[15:8]
	0x027F	ACC_DATA[23:16]

Table 17. Accumulator Data Plus Status Registers (ACC_STS_INx)

Register Name	Register Address	Register Contents
ACC_STS_IN0	0x0280	ACC_ERR, ACC_COUNT[6:0]
	0x0281	ACC_DATA[7:0]
	0x0282	ACC_DATA[15:8]
	0x0283	ACC_DATA[23:16]
...	...	...
ACC_STS_IN15	0x02BC	ACC_ERR, ACC_COUNT[6:0]
	0x02BD	ACC_DATA[7:0]
	0x02BE	ACC_DATA[15:8]
	0x02BF	ACC_DATA[23:16]

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Averaging Filter Status Indicators

The averaging filters generate several status flags that indicate their current states and certain error conditions.

As described in the Accumulators section, an accumulator is considered full when its ACC_COUNT value is equal to its programmed depth setting (ACC_DEPTH + 1). The ACC_FULL_INx bits assert when their corresponding accumulators are full and their data are ready for readback via the register map (as described in the Averaging Filter Readback section). The ACC_FULL_INx bits can be read via the ACC_STS_FULL_1 and ACC_STS_FULL_2 registers.

The ACC_FULL_INx bits are also used to generate the $\overline{\text{DRDY}}$ signal as described in the Data Ready ($\overline{\text{DRDY}}$) Signal section.

The ACC_OVR_INx bits assert following an accumulator overflow error. Accumulator overflows occur when the ADC attempts to write a new sample to an accumulator when it is already full. The new sample is ignored and effectively discarded during the overflow event. The ACC_OVR_INx bits can be read via the ACC_STS_OVR_1 and ACC_STS_OVR_2 registers.

The ACC_SAT_INx bits assert following an accumulator saturation error. Accumulator saturation is defined as any instance where the accumulator receives a positive FSR output code (0xFFFF) or negative FSR output code (0x0000) from the ADC, indicating possible saturation at the ADC input corrupting the accumulator and averaged result. Accumulator saturation errors do not prevent data from being written to the accumulator, and are included for detection purposes only.

The ACC_ERR bit in each of the AVG_STS_INx and ACC_STS_INx registers is the logical OR of their respective channel's ACC_OVR_INx and ACC_SAT_INx bits (see Table 63 and Table 65).

The ACC_OVR_SIG and ACC_SAT_SIG signals are the logical OR of all 16 ACC_OVR_INx bits and ACC_SAT_INx bits, respectively. ACC_OVR_SIG and ACC_SAT_SIG can be driven out on the GP0 pin to the GP3 pin to function as a hardware interrupt or alert to the host processor (see the General Purpose Pin Functions section).

Data Ready ($\overline{\text{DRDY}}$) Signal

The AD4691/AD4692 include an active low data ready ($\overline{\text{DRDY}}$) signal that indicates when all averaging filters are full and have new data to read. $\overline{\text{DRDY}}$ can be routed to the general purpose pins (GP0 to GP3) to function as a hardware interrupt for the digital host. $\overline{\text{DRDY}}$ can also be assigned as the internal oscillator stop trigger for automatically stopping burst sampling when all data are ready in CNV burst mode and SPI burst mode (see the CNV Burst Mode and SPI Burst Mode sections).

Figure 61 shows a simplified logic diagram for the $\overline{\text{DRDY}}$ signal generation. The ACC_MASK_INx bits (in the ACC_MASK_1 and ACC_MASK_2 registers) act to mask or unmask the ACC_FULL_INx signal of each channel. The $\overline{\text{DRDY}}$ signal goes low only after all unmasked channels' accumulators are full. When a channel is masked, its ACC_FULL_INx signal is ignored and never triggers a $\overline{\text{DRDY}}$ assertion. By default, all channels are masked except IN0 to match the default configuration of the channel sequencer (standard sequencer mode with only IN0 enabled).

The ACC_MASK_INx bits must be configured prior to using the $\overline{\text{DRDY}}$ signal. Channels are masked or unmasked when their corresponding ACC_MASK_INx bit is set to 1 or 0, respectively. To avoid lockout conditions, channels must be masked when they are not included in the channel sequence and unmasked when they are included. Setting all ACC_MASK_INx bits to 1 simultaneously is invalid and prevents the $\overline{\text{DRDY}}$ signal from asserting. See the Masking Channels to Avoid Lockout Conditions section for more information.

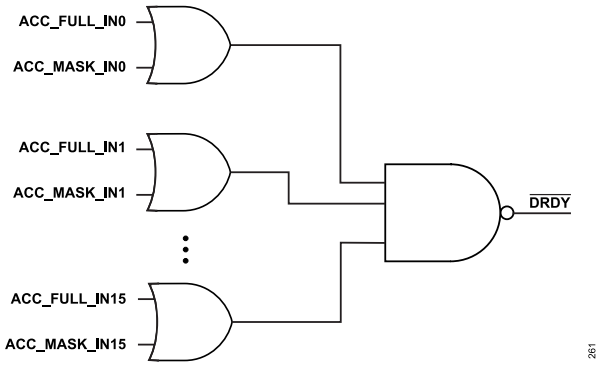

Figure 61. $\overline{\text{DRDY}}$ Masking Logic Diagram (Simplified)

INTERNAL OSCILLATOR

The AD4691/AD4692 include an internal oscillator to autonomously generate the ADC sampling clock in CNV burst mode, SPI burst mode, and autonomous mode. The internal oscillator core frequency is 2MHz and is divided down to generate the sampling clock by setting the OSC_FREQ bit field in the INTERNAL_OSCILLATOR register. The sampling frequency options range from 1.25kHz to 1MHz (see Table 42). The OSC_FREQ bit field must not be modified while the internal oscillator is active. See the Modes of Operation sections for details on the activation and deactivation of the internal oscillator in each of the relevant operating modes.

Note that the 1MHz setting is not supported by the AD4691, and setting OSC_FREQ to 0x0 will set the oscillator frequency to 500kHz.

TEMPERATURE SENSOR

The AD4691/AD4692 include temperature sensors that convert the die temperature to a voltage that can be sampled and converted to an output code by the SAR ADC core. The temperature sensor is only accessible while the AD4691/AD4692 are in manual mode (see the Manual Mode section).

The temperature sensor sensitivity is a measure of the change in output voltage in relation to a change in device temperature, and

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it is typically −1.8mV/°C. At 0°C, the temperature sensor output is typically 725mV. The typical range for V_{TEMP} is therefore 797mV to 500mV across a −40°C to 125°C temperature range.

The relationship between the measured die temperature (T) and the temperature sensor output voltage (V_{TEMP}) is nominally:

$$V_{TEMP} = \left(-1.8\frac{mV}{°C} \times T\right) + 725mV \quad (2)$$

V_{TEMP} is converted to a 16-bit output code (D_{TEMP}) by the ADC with the same transfer function as the analog inputs. V_{TEMP} is calculated from D_{TEMP} with the following equation:

$$V_{TEMP} = D_{TEMP} \times \frac{V_{REF}}{2^{16}} \quad (3)$$

Conversely, measured die temperature (T) is calculated from V_{TEMP} with the following equation:

$$T = \frac{V_{TEMP} - 725mV}{-1.8mV/°C} \quad (4)$$

GENERAL PURPOSE PIN FUNCTIONS

The AD4691/AD4692 general purpose pins support multiple digital functions for timing synchronization, hardware interrupts, and basic logic signals. The LFCSP model includes one general purpose pin (GP0) and the WLCSP model includes four general purpose pins (GP0 to GP3). The function for each general purpose pin is selected by its corresponding GPx_MODE bit field in the GP_CONFIG_1 and GP_CONFIG_2 registers.

Table 18 shows the GPx_MODE bit field configuration settings for selecting the signals for each of the general purpose pins. Note that GP1_MODE, GP2_MODE and GP3_MODE are don't care on the LFCSP. The general purpose pins are disabled (high-impedance) by default.

Table 18. General Purpose Pin Configuration

GPx_MODE	GPx Pin Function Assignment
0x0	Disabled/high-Z (default)
0x1	Logic low output
0x2	Logic high output
0x3	Logic input
0x4	ADC_BUSY signal
0x5	$\overline{EOS}$ signal
0x6	$\overline{DRDY}$ signal
0x7	ACC_OVR_SIG
0x8	ACC_SAT_SIG

Logic Outputs

Each general-purpose pin can be configured to output a static logic low or logic high signal. This allows the host to control the logic inputs of the external devices (such as switch positions or PGIA gain settings, for example) through the AD4691/AD4692 SPI and registers instead of using additional digital host resources. The logic output functionality is especially useful in isolated applications by reducing the number of digital isolation channels.

The logic level is selected by the GPx_MODE bit field as shown in Table 18. The logic output thresholds for the GP0 pin to the GP3 pin are specified in Table 1 as V_{OL} and V_{OH}.

Logic Inputs

Each general-purpose pin can be configured as a logic input to monitor the state of an external logic signal through the AD4691/AD4692 SPI and registers instead of using an additional digital host resource. The logic input functionality is especially useful in isolated applications by reducing the number of digital isolation channels.

The GPx_MODE bit fields are used to configure the corresponding GPx pin as a logic input (see Table 18). While configured as a logic input, the state of the GP0 to GP3 input signals are reflected in the GP0_READ through GP3_READ bits in the GPIO_READ register, respectively. The logic input thresholds for the general purpose pins are specified in Table 1 as V_{IL} and V_{IH}.

MODES OF OPERATION

The AD4691/AD4692 include several ADC operating modes, each optimized for automation or throughput. Each mode differs in their ADC sampling control and timing.

Table 19 summarizes each of the AD4691/AD4692 operating modes. In CNV clock mode, the CNV input acts as the ADC sampling clock for direct control over each sampling instant. CNV burst mode and SPI burst mode use the internal oscillator to perform a configurable burst of samples using $\overline{EOS}$ or $\overline{DRDY}$ to end the burst. In autonomous mode, the internal oscillator acts as a free-running sampling clock that is enabled and disabled with an SPI write. Manual mode bypasses the channel sequencer, averaging filters, and register map for the fastest possible ADC sampling and throughput at the expense of more direct digital host intervention.

Table 20 lists the configuration bits used to select from the AD4691/AD4692 operating modes. CNV clock mode is selected by default. Each mode's functionality and SPI protocol are detailed in the following sections.

Table 19. Operating Mode Feature Summary

Mode Name	Channel Sequencing	Averaging Filters	ADC Convert Start
CNV Clock Mode	Channel Sequencer	Enabled	CNV Input
CNV Burst Mode	Channel Sequencer	Enabled	Internal oscillator, burst sampling triggered by CNV rising edge
SPI Burst Mode	Channel Sequencer	Enabled	Internal oscillator, burst sampling triggered by SPI write to OSC_EN
Autonomous Mode	Channel Sequencer	Enabled	Internal oscillator, autonomous sampling toggled by SPI write to OSC_EN
Manual Mode	SPI Commands	Disabled/Bypassed	CNV input

Table 20. Operating Mode Configuration Bits

Mode Name	MANUAL_MODE	ADC_MODE[1]	OSC_EN[2]	STOP_STATE[1]
CNV Clock Mode	0	0x0	Don't care	Don't care
CNV Burst Mode	0	0x1	Don't care	0 = $\overline{EOS}$, 1 = $\overline{DRDY}$
SPI Burst Mode	0	0x3	1 = Initiates burst sampling	
Autonomous Mode	0	0x2	1 = Initiates sampling, 0 = stops sampling	Don't care
Manual Mode	1	Don't care	Don't care	Don't care

[1] A state reset is required after changing the state of ADC_MODE or STOP_STATE.

[2] OSC_EN must be set to 0 before updating ADC_MODE.

MODES OF OPERATION

CNV CLOCK MODE

In CNV clock mode, the CNV input functions as the ADC sampling clock source. Each rising edge of the CNV signal triggers a single conversion. After each conversion, the ADC result is pushed to the averaging filter of the corresponding channel, and the channel sequencer updates the multiplexer to the next channel in the sequence. ADC results are read back via the averaging filter or accumulator output registers as described in the Averaging Filter Readback section. Table 20 shows the configuration bit settings for selecting CNV clock mode.

Figure 62 shows a typical connection diagram for the digital host and AD4691/AD4692 digital interface in CNV clock mode. Figure 63 shows a timing diagram of the CNV signal, SPI transactions, and ADC_BUSY signal in CNV clock mode.

Prior to performing conversions in CNV clock mode, the channel sequencer and averaging filter settings must be configured as described in the Theory of Operation section, followed by a state reset.

Figure 93 illustrates the step-by-step configuration flow for AD4691/AD4692 in CNV clock mode.

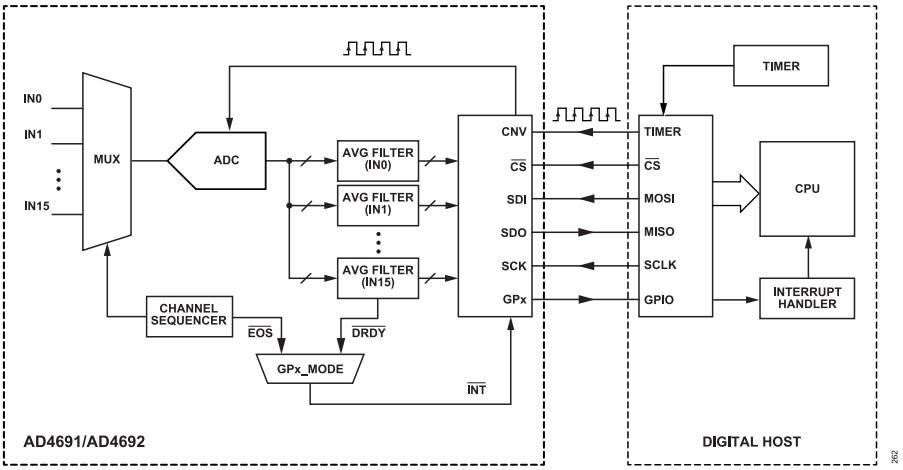


Figure 62. CNV Clock Mode Example Connection Diagram

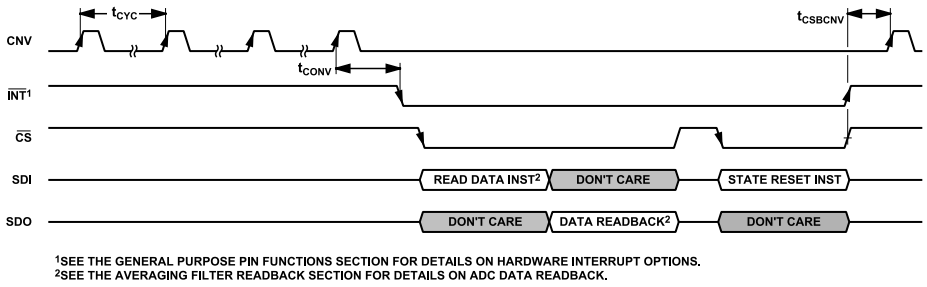


Figure 63. CNV Clock Mode Timing Diagram

MODES OF OPERATION

CNV BURST MODE

In CNV burst mode, each CNV rising edge triggers a burst of samples. The internal oscillator functions as the ADC sampling clock and runs until selected stop state occurs. The stop state can be triggered by the $\overline{EOS}$ signal or the $\overline{DRDY}$ signal, as set by the STOP_STATE bit in the ADC_SETUP register. After each conversion (within the burst), ADC results are pushed to the averaging filter of the corresponding channel, and the channel sequencer updates the multiplexer to the next channel in the sequence. At the end of the sample burst, the ADC results are read back via the averaging filter or accumulator output registers as described in the Averaging Filter Readback section. Table 20 shows the configuration bit settings for selecting CNV burst mode and the desired stop state source.

Figure 64 shows a typical connection diagram for the digital host and AD4691/AD4692 digital interface in CNV burst mode. Figure 65 shows a timing diagram of the CNV signal, the internal oscillator, the stop state signal ($\overline{EOS}$ or $\overline{DRDY}$), and SPI readback timing in CNV burst mode.

Prior to performing conversions in CNV burst mode, the internal oscillator frequency, stop state source, channel sequencer, and averaging filter settings must be configured as described in the Theory of Operation section, followed by a state reset. As mentioned in the Data Ready (DRDY) Signal, the accumulator mask bits must be set to avoid lock out conditions where the $\overline{DRDY}$ never asserts and the stop state never triggers, preventing the burst sampling from stopping automatically.

Figure 94 illustrates the step-by-step configuration flow for AD4691/AD4692 in CNV burst mode.

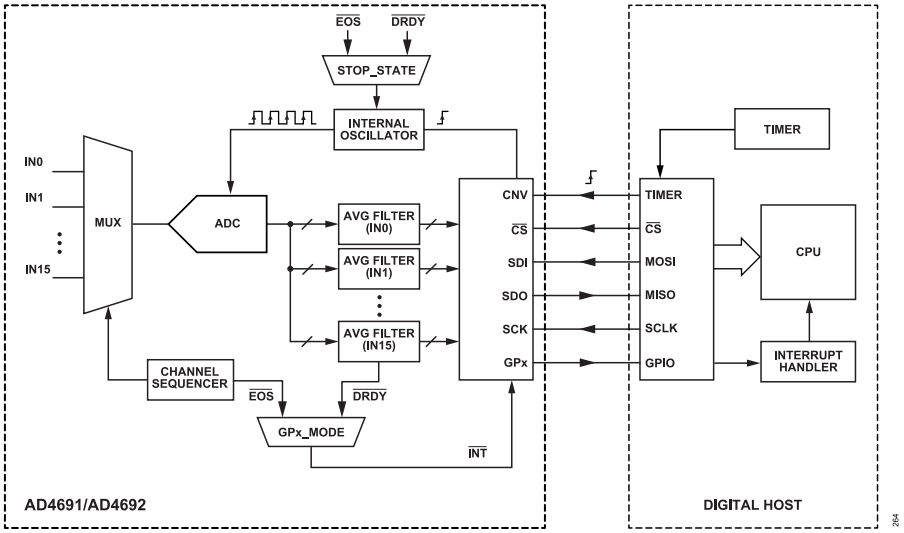


Figure 64. CNV Burst Mode Example Connection Diagram

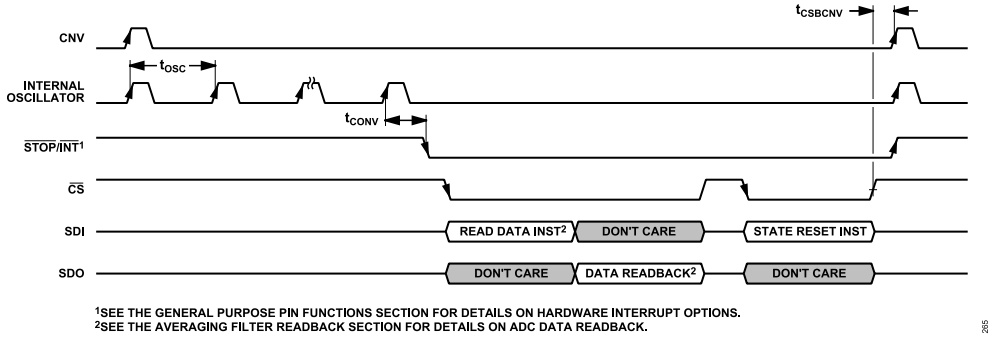


Figure 65. CNV Burst Mode Timing Diagram

MODES OF OPERATION

SPI BURST MODE

In SPI burst mode, bursts of samples are triggered by an SPI write to the OSC_EN bit in the OSC_EN_REG register. The internal oscillator functions as the ADC sampling clock and runs until selected stop state occurs. The stop state can be triggered by the $\overline{EOS}$ signal or the $\overline{DRDY}$ signal, as set by the STOP_STATE bit in the ADC_SETUP register. After each conversion (within the burst), ADC results are pushed to the averaging filter of the corresponding channel, and the channel sequencer updates the multiplexer to the next channel in the sequence. At the end of the sample burst, the ADC results are read back via the averaging filter or accumulator output registers as described in the Averaging Filter Readback section. Table 20 shows the configuration bit settings for selecting SPI burst mode and the desired stop state source.

Burst sampling is initiated by writing the OSC_EN bit to 1. When the stop state trigger occurs and the sample burst stops, the OSC_EN bit is internally reset to 0.

Figure 66 shows a typical connection diagram for the digital host and AD4691/AD4692 digital interface in SPI burst mode. The CNV input state is don't care in SPI burst mode. Figure 67 shows a timing diagram of the OSC_EN SPI write, the internal oscillator, the stop state signal ($\overline{EOS}$ or $\overline{DRDY}$), and SPI readback timing in SPI burst mode.

Prior to performing conversions in SPI burst mode, the internal oscillator frequency, stop state source, channel sequencer, and averaging filter settings must be configured as described in the Theory of Operation section, followed by a state reset. As mentioned in the Data Ready (DRDY) Signal, the accumulator mask bits must be set to avoid lock out conditions where the $\overline{DRDY}$ never asserts and the stop state never triggers, preventing the burst sampling from stopping automatically.

Figure 95 illustrates the step-by-step configuration flow for AD4691/AD4692 in SPI burst mode.

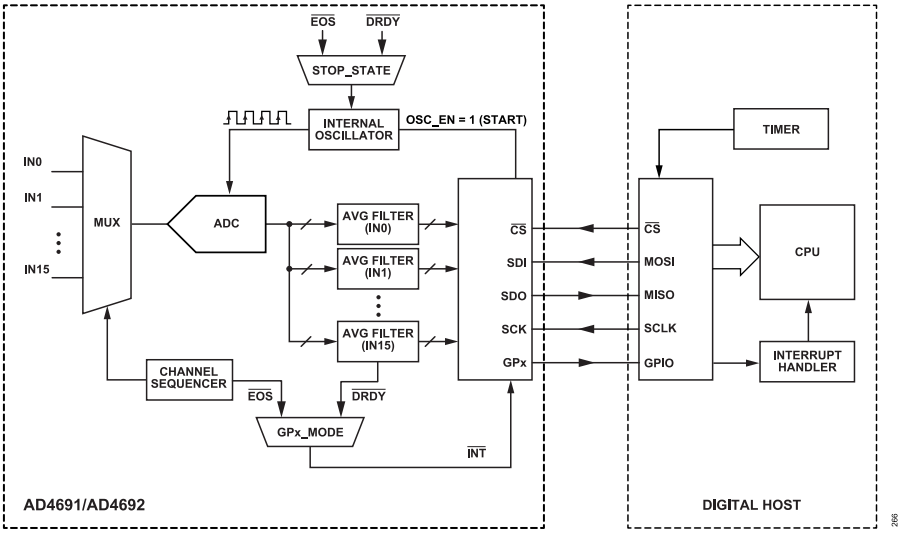


Figure 66. SPI Burst Mode Example Connection Diagram

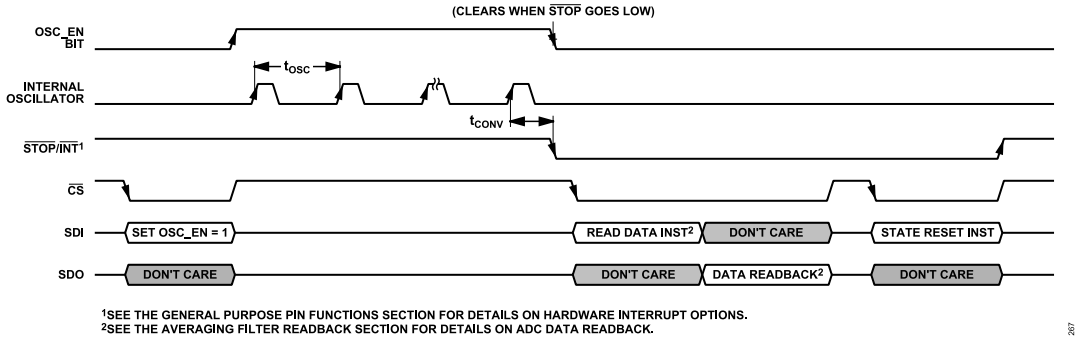


Figure 67. SPI Burst Mode Timing Diagram

MODES OF OPERATION

AUTONOMOUS MODE

In autonomous mode, SPI commands are used to start and stop autonomous ADC sampling. The internal oscillator functions as the ADC sampling clock, and is enabled and disabled by writing to the OSC_EN bit in the OSC_EN_REG register. Setting OSC_EN to 1 enables the internal oscillator to run and trigger conversions until OSC_EN is set back to 0. After each conversion, ADC results are pushed to the averaging filter of the corresponding channel, and the channel sequencer updates the multiplexer to the next channel in the sequence. After disabling the internal oscillator, the ADC results are read back via the averaging filter or accumulator output registers as described in the Averaging Filter Readback section. Table 20 shows the configuration bit settings for selecting autonomous mode and the desired stop state source.

Figure 68 shows a typical connection diagram for the digital host and AD4691/AD4692 digital interface in autonomous mode. The CNV input state is don't care in autonomous mode. Figure 69 shows a timing diagram of the OSC_EN SPI writes, the internal oscillator, and SPI readback timing in autonomous mode.

Prior to performing conversions in autonomous mode, the internal oscillator frequency, channel sequencer, and averaging filter settings must be configured as described in the Theory of Operation section, followed by a state reset.

Figure 96 illustrates the step-by-step configuration flow for AD4691/AD4692 in autonomous mode.

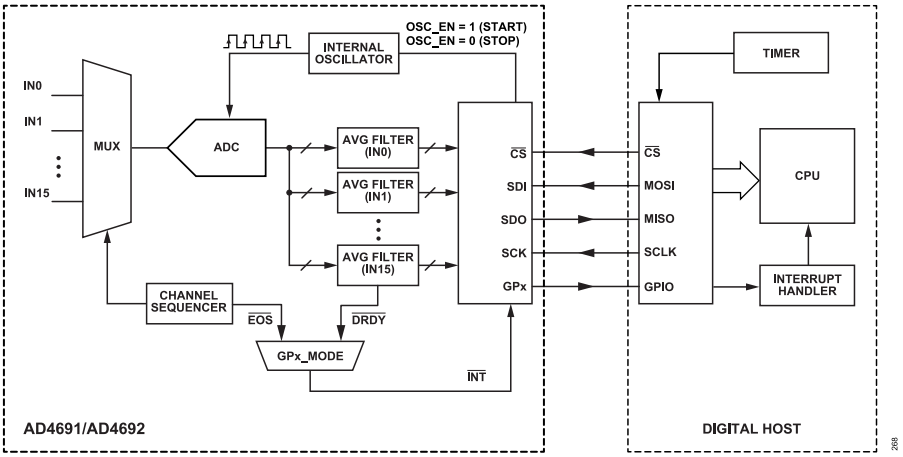


Figure 68. Autonomous Mode Example Connection Diagram

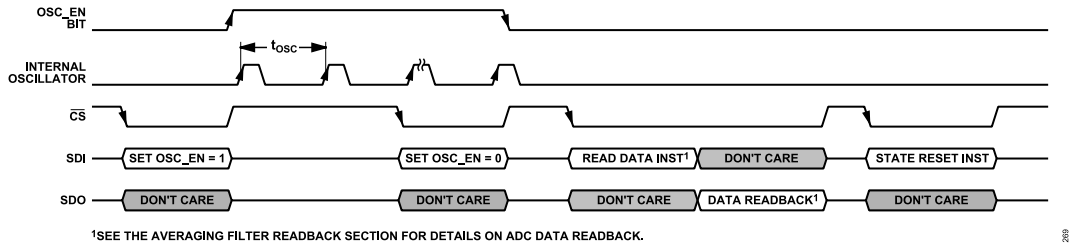


Figure 69. Autonomous Mode Timing Diagram

MODES OF OPERATION

MANUAL MODE

Manual mode differs from the other operating modes by bypassing the configuration registers, channel sequencer, and averaging filters to enable faster data readback and direct SPI control over the multiplexer channel sequencing. The manual mode SPI protocol does not follow the register access format described in the Register Access section. ADC results are read out on SDO without a register access instruction phase on SDI. The SDI data instead consist of a 5-bit command code (CMD) used for selecting the next multiplexer channel.

Table 21 lists the valid manual mode CMD codes. CMD codes are sent in the first five bits of SDI input data. The code values written in the CMD[4:0] column represent the 5-bit CMD values, while the SDI[15:0] column translates these 5-bit values to a 16-bit equivalent value (with padded zeros) to align with the 16-bit ADC data on SDO. All other 5-bit values of CMD are treated as no operation, where the multiplexer remains on the current channel for the next conversion.

Setting the MANUAL_MODE bit to 1 puts the AD4691/AD4692 into manual mode. The device remains in manual mode until the exit command is sent on SDI. Upon receiving the exit command, the MANUAL_MODE bit is cleared and the device exits manual mode. Figure 73 shows a timing diagram of exiting manual mode with the exit command.

In manual mode, the CNV input functions as the ADC sampling clock source. Each rising edge of the CNV signal triggers a single conversion. The digital host reads the conversion result via the SPI before sending the next CNV rising edge.

Figure 70 shows a typical connection diagram for the digital host, and Figure 71 shows a timing diagram of the CNV signal and SPI frames containing the CMD codes on SDI and the ADC data on SDO. Manual mode is backwards compatible with the AD4696 two cycle command mode. There is a two cycle delay between sending an SDI CMD and when the resulting ADC sample is read on SDO.

Manual mode includes optional status bits which contain the channel identification for the ADC data, and an OV_ERR bit which indicates if any of the overvoltage protection clamps are active. The status bits are enabled by setting the STATUS_EN bit in the DEVICE_SETUP bit to 1. When the status bits are enabled, the 16-bit SDO data packets are extended to 24-bits. Figure 72 shows the SDO data packet format in manual mode with status bits disabled and enabled.

Figure 97 illustrates the step-by-step configuration flow for AD4691/AD4692 in manual mode.

Table 21. Manual Mode CMD Code Functions

CMD[4:0]	SDI[15:0]	Function
0x0A	0x5000	Exit command
0x0F	0x7000	Temperature sensor
0x10 to 0x1F	0x8000 to 0xF800	IN0 to IN15 channel selection

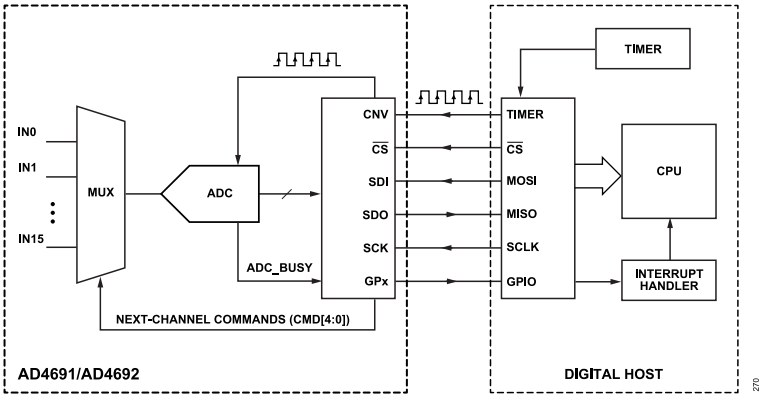


Figure 70. Manual Mode Example Connection Diagram

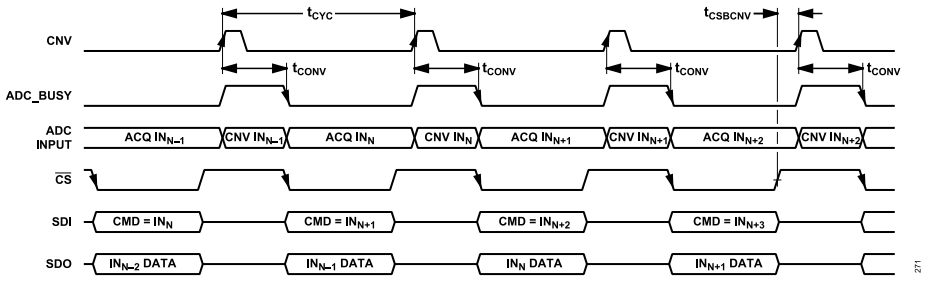


Figure 71. Manual Mode Timing Diagram

MODES OF OPERATION

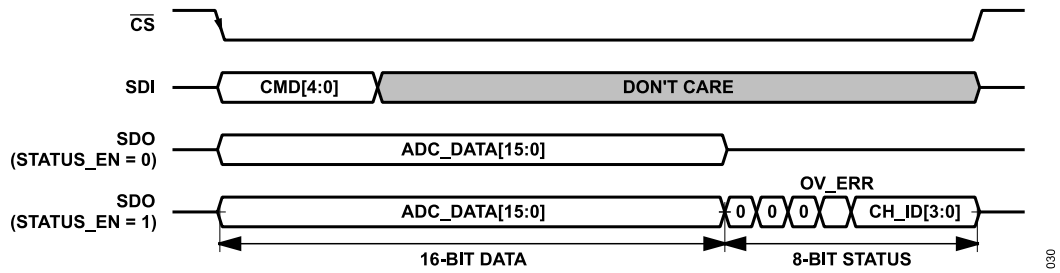


Figure 72. Manual Mode SPI Data Format

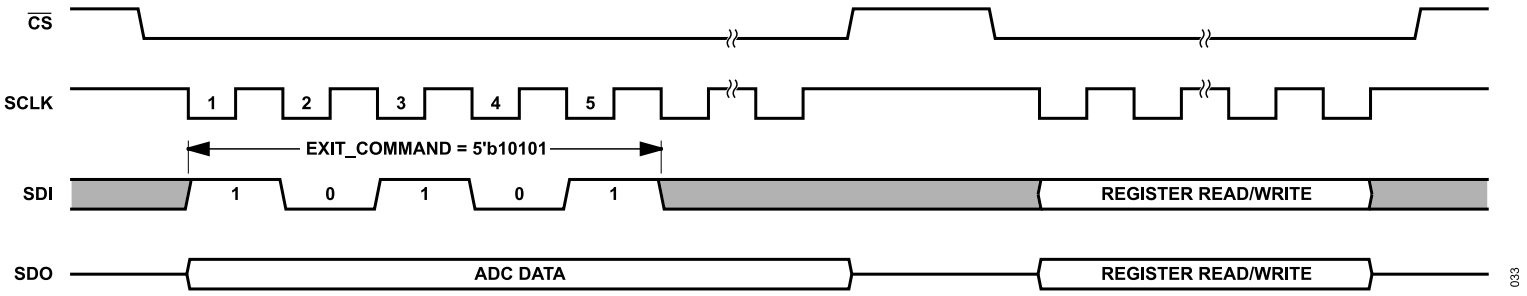


Figure 73. Exit Command Timing Diagram

DIGITAL INTERFACE

The AD4691/AD4692 digital interface includes a 4-wire SPI, a convert start input (CNV), an active low reset input ($\overline{\text{RESET}}$), and general purpose digital pin(s) with multiple configurable signal options.

The SPI is primarily used for reading and writing the device configuration registers and reading the ADC or averaging filter conversion results. The Register Access section describes the SPI protocol for accessing the configuration registers. The Modes of Operation sections describe the ADC sampling control and data readback protocol for each operating mode.

The Device Reset section defines the reset options on the AD4691/AD4692. Full device resets can be initiated by the $\overline{\text{RESET}}$ input or by writing to the software reset bits over the SPI. The AD4691/AD4692 also include a state reset option which resets the current state of the multiplexer channels and averaging filters without resetting the configuration registers.

The interface logic level is set by the VIO voltage, and it supports 1.2V to 1.8V logic systems. The AD4691/AD4692 use SPI Mode 3 (clock phase (CPHA) = clock polarity (CPOL) = 1).

REGISTER ACCESS

The AD4691/AD4692 configuration registers are read and written via the SPI. All configuration registers are mapped to a set of register addresses, with each address value corresponding to one byte of register data. Each register access transaction consists of an instruction phase (to specify which register is to be accessed) and a data phase (which contains the register read or write data). Figure 74 illustrates the basic SPI transaction format for writing to and reading from the configuration registers.

The instruction phase includes the R/$\overline{\text{W}}$ bit, followed by the address of the register being accessed (REG_ADDR). The R/$\overline{\text{W}}$ bit specifies whether the transaction is a write (R/$\overline{\text{W}}$ = 0) or a read (R/$\overline{\text{W}}$ = 1). REG_ADDR is a 15-bit value that specifies which address is being written to or read from. Table 24 lists all of the AD4691/AD4692 configuration registers and their corresponding address values.

The data phase follows the instruction phase. The data phase includes read or write data (REG_DATA) for one or more registers, plus optional cyclic redundancy check (CRC) bytes for SPI error detection. Each register must be read from or written to in its entirety in the same data phase for the read or write to be considered valid. Partial register writes are considered invalid and will be ignored by the device. The length of each REG_DATA packet depends on the length of the register being accessed which ranges from eight bits to 32 bits (as described in the Register Length section).

The CRC Error Detection section provides information on the 8-bit CRC checksum calculations for detecting SPI transmission errors.

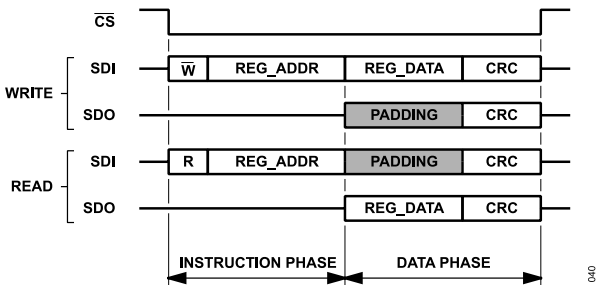


Figure 74. SPI Format for Register Access

Register Length

Each of the AD4691/AD4692 configuration registers is an integer multiple of eight bits long. Most registers are eight bits long, but some are 16 bits, 24 bits, and 32 bits long, as noted in Table 24.

As mentioned in the Register Access section, registers must be read from or written to in their entirety within one SPI frame to be considered valid. Partial writes to a register are invalid and are ignored. The SPI_STATUS register contains multiple error flags which assert when the AD4691/AD4692 SPI detects partial reads or writes.

Registers that are more than eight bits long (multibyte registers) always exist across adjacent register addresses, with the most significant byte (MSByte) stored at the highest-valued address and the least significant byte (LSByte) stored at the lowest-value address. For example, the AVG_IN0 register is a 16-bit long register with its MSByte at address 0x0201 and LSByte at address 0x0200. (The Bulk Reading ADC Data Registers section provides more specific guidance on reading the multibyte data readback registers for all 16 channels.)

As mentioned in the Bulk Register Reads and Writes section, the active register address is decremented after each byte of data is read. This means the REG_DATA packets for each register are read or written MSByte first. For example, to read from the AVG_IN0 register, send REG_ADDR = 0x0201 in the instruction phase, and clock out all 16 bits of REG_DATA to read the MSByte and LSByte of the AVG_IN0 register.

The only writable multibyte register is the STD_SEQ_CONFIG register, which is 16 bits long and exists in Address 0x0025 and Address 0x0024 (see the Standard Sequencer Mode section). All 16 bits of the STD_SEQ_CONFIG register must be written in one SPI frame to update them.

When CRC is enabled, the CRC checksum byte is appended to the end of REG_DATA of each register. For example, if the register is eight bits long, the CRC byte will occur after the 8-bit REG_DATA. If the register is 16 bits long, the CRC byte will occur after the 16-bit REG_DATA, and so on.

DIGITAL INTERFACE

Bulk Register Reads and Writes

The AD4691/AD4692 SPI supports two modes for bulk register reads and writes for efficient access to multiple registers within a single SPI frame.

Autodecrement mode is optimized for reading from contiguous sections of the register map, such as reading all 16 channels of ADC readback registers in one SPI read frame or configuring all enabled advanced sequencer slots in one SPI write frame. The REG_ADDR specified in the instruction phase is decremented by 1 following each byte of REG_DATA, allowing efficient access to registers that are next to each other in the memory map without starting another SPI frame. Figure 75 shows a generalized SPI protocol for bulk register reads and writes in autodecrement mode.

Direct-address mode is optimized for reading from noncontiguous sections of the register map, such as reading from a subset of the 16 channels of ADC readback registers without needing to stream through all of them. The digital host sends a new REG_ADDR value after each REG_DATA transfer, allowing efficient access to multiple registers that are not next to each other in the memory map in a single SPI frame. For registers that are multiple bytes long, REG_ADDR must be the MSByte address to ensure REG_DATA contains all of that register's data (see the Register Length section for more details). Figure 76 shows a generalized SPI protocol for bulk register reads and writes in direct-address mode.

The INST_MODE bit in the SPI_CONFIG_B register selects between autodecrement mode and direct-address mode (see SPI Configuration B Register). Autodecrement mode is enabled by default.

In both modes, register writes are applied at different times depending on whether CRC is disabled or enabled. When CRC is disabled, the CRC byte is omitted, and the register is updated on the last bit of its REG_DATA byte. When CRC is enabled, each REG_DATA byte must be immediately followed by its corresponding CRC byte, and the register contents are updated only after the CRC byte is received and validated. See the CRC Error Detection section for more information on CRC byte validation.

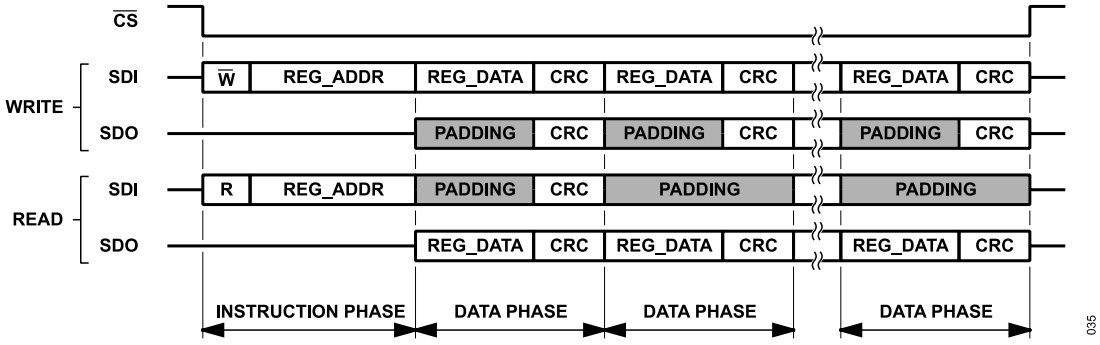


Figure 75. Bulk Register Access in Autodecrement Mode

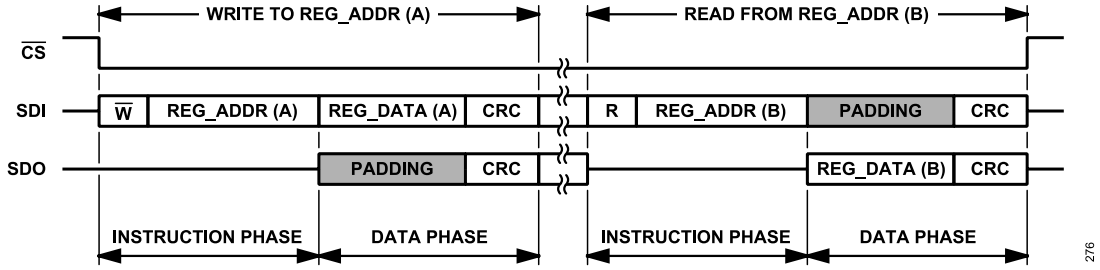


Figure 76. Bulk Register Access in Direct-Address Mode

DIGITAL INTERFACE

CRC Error Detection

The AD4691/AD4692 include SPI transmission error detection for register reads and writes based on the following CRC-8 polynomial:

$$x^8 + x^2 + x + 1 \quad (5)$$

The CRC is enabled by setting the CRC_EN_A and CRC_EN_B bit fields to 0x1 and 0x2 in the same SPI frame, respectively. Both bit fields must be written in the same SPI frame to prevent SPI transaction errors from inadvertently enabling or disabling CRC. When the CRC is enabled an 8-bit checksum code is appended to each REG_DATA packet in the data phase, as shown in Figure 74. The checksum calculator applies the CRC-8 polynomial to the incoming and outgoing REG_DATA packets, allowing the AD4691/AD4692 to detect transmission errors from the host and vice versa.

Figure 74 and Figure 75 shows the expected CRC checksum code format for single or multiple register writes and reads per SPI frame. When CRC is enabled, the AD4691/AD4692 send checksum codes to the digital host via SDO and validate checksum codes sent by the digital host via SDI. If the incoming checksum does not match the expected value, the AD4691/AD4692 assume the transmission was corrupted; therefore, the internal registers do not update their values, and the CRC_ERROR bit in the SPI_STATUS register is asserted. The host software should periodically check the CRC_ERROR bit to detect the occurrence of corrupted data transmissions and resulting unexpected device configuration settings.

Table 22 summarizes the data and seed values for the checksum calculation for all possible register write and read transactions. The checksum calculation is seeded by a nonzero value to detect if the SDI input is stuck low. The seed value is 0xA5 for the first register write or read in the SPI frame. For bulk transactions, the checksum for each subsequent register is seeded with the MSByte of the address of that register (for example, 0x0025 for STD_SEQ_CONFIG, and so on).

Table 22. CRC Calculator Seed and Data Values

Command	CRC Source	First CRC		Subsequent CRCs	
		Seed Input	Data Input	Seed	Data Source
Write	SDI (from host)	0xA5	R/$\overline{W}$, REG_ADDR, REG_DATA	Current start address	REG_DATA
	SDO (to host)		R/$\overline{W}$, REG_ADDR, REG_DATA	Current start address	REG_DATA
Read	SDI (from host)	0xA5	R/$\overline{W}$, REG_ADDR, PADDING	Not required, send padding data	
	SDO (to host)		R/$\overline{W}$, REG_ADDR, REG_DATA	Current start address	REG_DATA

DIGITAL INTERFACE

DEVICE RESET

The AD4691/AD4692 provide the following device reset options:

- Power-on reset (POR)
- Hardware reset via the $\overline{\text{RESET}}$ input
- Software reset via the SPI_CONFIG_A register

A device reset reinitializes the configuration registers to their default settings and puts the AD4691/AD4692 into CNV clock mode. Hardware resets, software resets, and PORs all assert the RESET_FLAG bit in the DEVICE_STATUS register. The RESET_FLAG bit is a read to clear bit and is automatically set to 0 after a valid read from the DEVICE_STATUS register. The RESET_FLAG bit can be used by the digital host to confirm that the device has executed a device reset, or if a reset was performed unintentionally.

The reset delay specifications in Table 5 indicate the typical delay between a device reset and when the device is ready for SPI communications and operation. When the digital host attempts to perform an SPI read or write transaction before the device is ready, the transaction is considered invalid, and the NOT_RDY_ERROR bit in the SPI_STATUS register is set to 1. The NOT_RDY_ERROR bit is a R/W1C bit and is only reset when set to 1 with a valid register write transaction.

In addition to the full device resets, the AD4691/AD4692 include a state reset option that resets the current state of the multiplexer channels and averaging filters without resetting the configuration registers. The state reset delay (t_{STATE}) is the minimum delay needed between writing the STATE_RESET bit to 1 and when the ADC is ready to perform more conversions. See the State Reset for more information.

Hardware Reset

A hardware reset is initiated by the $\overline{\text{RESET}}$ falling edge. Figure 77 shows a timing diagram for performing a hardware reset. The minimum amount of time that $\overline{\text{RESET}}$ must be driven low is the t_{RESETL}, and t_{HWR} is the time that the digital host must wait between a $\overline{\text{RESET}}$ falling edge and starting an SPI frame (see Table 5).

If the internal LDO regulator supplies VDD, and the internal LDO regulator is disabled before a hardware reset, the internal LDO regulator is enabled by the hardware reset and an additional delay is required to account for the internal LDO output reaching the VDD minimum required voltage (see the Power-On Resets (PORs) section).

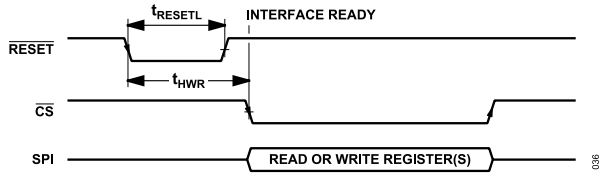


Figure 77. Hardware Reset Timing Diagram

Software Reset

To initiate a software reset, set the SW_RST_MSB bit and SW_RST_LSB bit in the SPI_CONFIG_A register to 1. A software reset reinitializes the state of all configuration registers listed in the Register Information section to the default values, except for the SPI_CONFIG_A register. When the software reset is complete, the SW_RST_MSB bit and SW_RST_LSB bit automatically clear. Figure 78 shows the timing requirements for performing a software reset. The time that the digital host must wait between the software reset and starting a new SPI frame is t_{SWR} (see Table 5).

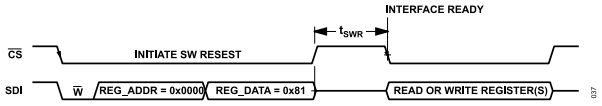


Figure 78. Software Reset Timing Diagram

Power-On Resets (PORs)

A POR is initiated when VDD or VIO is first supplied. When a POR event is detected, the AD4691/AD4692 configuration registers are initialized to the default values, but it is still recommended to perform either a hardware reset or a software reset after a POR.

Figure 79 shows a timing diagram of a VDD POR where VIO is already supplied. Figure 80 shows a timing diagram of a VIO POR where VDD is already supplied by an external +1.8V source. Note that the internal LDO regulator does not turn on until VIO is supplied; if using the internal LDO regulator to power VDD internally, the VDD POR will occur after the VIO POR, as shown in Figure 81.

Figure 82 shows a timing diagram of a VDD POR following the LDO regulator wake-up command. When the internal LDO regulator wakes up, it drives VDD to +1.8V and triggers a VDD POR. The combined delay between the wake-up command and device ready is the LDO regulator start-up delay plus the POR delay.

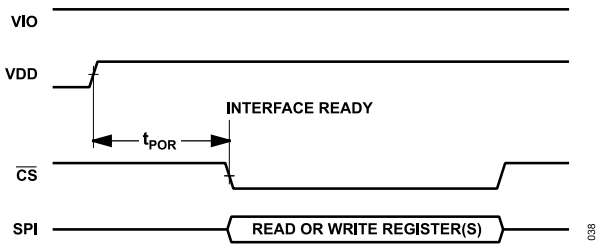


Figure 79. VDD POR Timing Diagram

DIGITAL INTERFACE

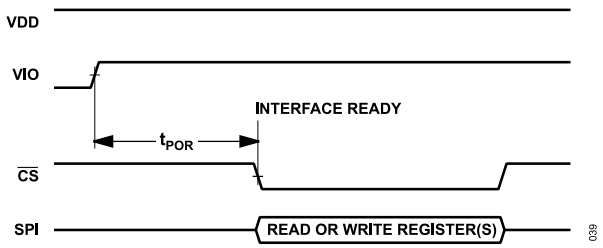


Figure 80. VIO POR Timing Diagram (VDD Supplied Externally)

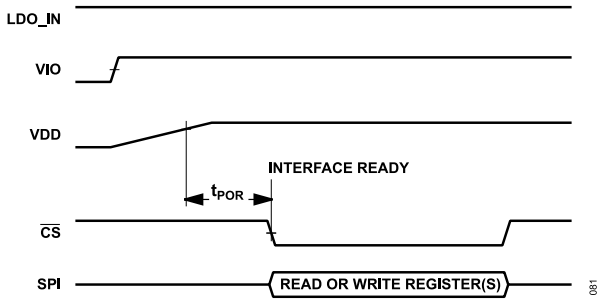


Figure 81. VIO POR Timing Diagram (VDD Supplied Internally)

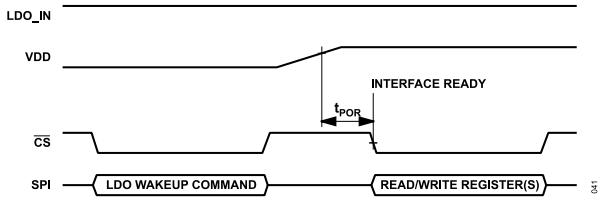


Figure 82. LDO Regulator Wake-Up Command POR Timing Diagram

STATE RESET

The state reset resets the state of the following functional blocks without resetting the state of any of the R/W bits in the configuration registers:

- Channel sequencer position and active multiplexer channel
- Averaging filter data and sample counter

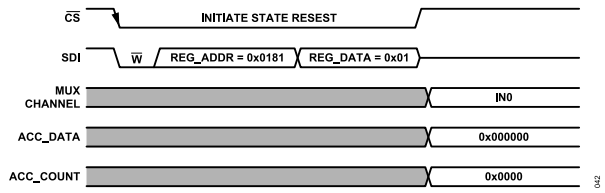
To initiate a state reset, set the STATE_RESET bit in the STATE_RESET_REG register to 1. The STATE_RESET bit is automatically cleared after the state reset is finished.

The digital host must perform a state reset after the averaging filters are full to empty them and prepare them for new ADC samples. The Modes of Operation sections provides guidance on performing the state reset in each operating mode.

The digital host must also perform a state reset after updating any of the configuration registers related to the channel sequencer or averaging filters. In general, it is recommended to perform a state reset after updating any of the configuration registers to ensure proper device operation.

Figure 83 illustrates a state reset with several relevant internal device states and read-only bits.

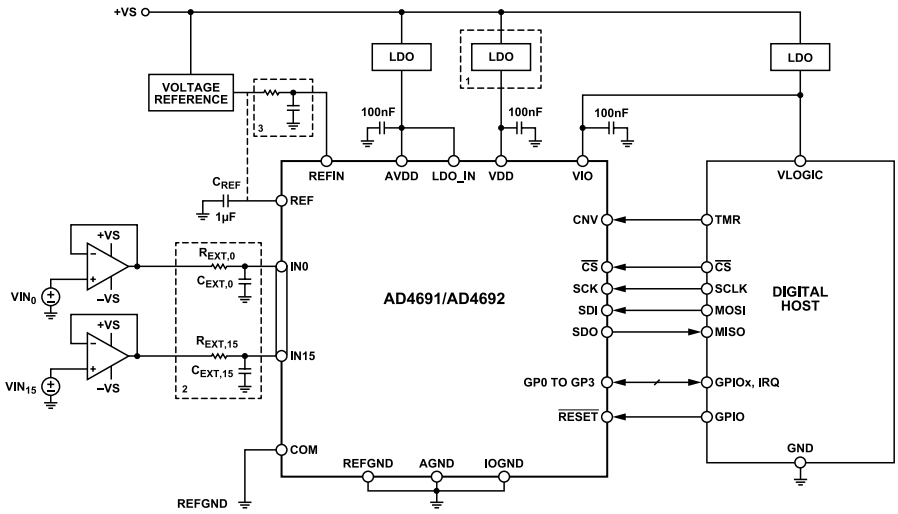
Figure 83. State Reset Timing Diagram



APPLICATIONS INFORMATION

Figure 84 shows an example of a recommended connection diagram for the AD4691/AD4692 companion circuitry.

The AD4691/AD4692 companion circuitry typically includes power supplies, a voltage reference, AFE signal conditioning circuits per channel, and an SPI-compatible digital host.



[1]DEDICATED +1.8V SUPPLY FOR VDD NOT REQUIRED WHEN USING INTERNAL LDO REGULATOR. (SEE THE INTERNAL LDO REGULATOR SECTION.)
[2]$R_{EXT,X}$ AND $C_{EXT,X}$ REPRESENT EXTERNAL INPUT RC FILTERS FOR ANALOG INPUT INx.
[3]OPTIONAL LOW PASS FILTER BETWEEN VOLTAGE REFERENCE AND REFIN INPUT (REFERENCE BUFFER ENABLED ONLY).

Figure 84. AD4691/AD4692 Typical Connection Diagram

APPLICATIONS INFORMATION

INTERLEAVED CHANNEL SEQUENCING

The AD4691/AD4692 combines a flexible channel sequencer with averaging filters per channel to enable interleaved channel sequencing schemes for more consistent acquisition of multiple ADC channels. Traditional multiplexed ADCs that include average filters typically include a single filter shared by all channels, which forces the filter to wait until the averaged result of one channel is ready before sampling the next channel. This results in blind spots where some channels may not be sampled for extended periods of time and leads to decreased measurement repeatability. The inclusion of an averaging filter per channel provides each channel a memory location for its data, preventing channels from overwriting each other and allowing the sequencer to scan through the channels without blind spots.

Figure 85 and Figure 86 show the difference between traditional channel sequencing and interleaved channel sequencing. The interleaved sequencing approach significantly reduces blind spots in the acquisition window of each channel .

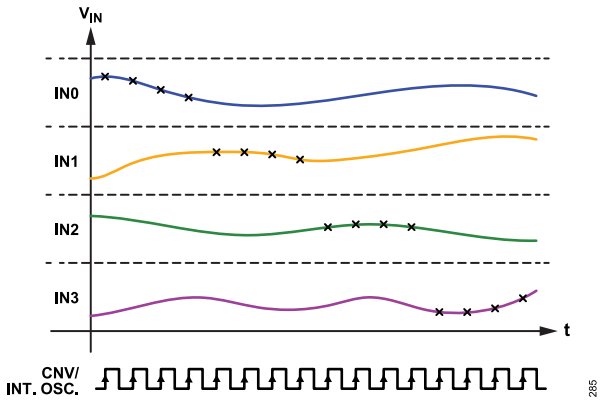


Figure 85. Traditional Sequencing (Averaging by 4)

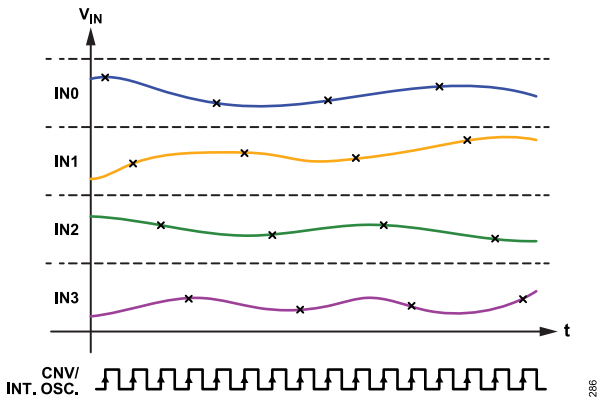


Figure 86. Interleaved Sequencing with AD4691/AD4692 (Averaging by 4)

EFFECTIVE CHANNEL SAMPLE RATE

The AD4691/AD4692 analog inputs are multiplexed to a single ADC core, and the state of the multiplexer is updated at the end of the conversion phase. Therefore, the effective sample rate for each individual channel (f_{S_INx}) depends on the ADC sampling rate (f_S) and the channel sequence configuration.

The effective sample rate equations below assume f_S is constant. This is true in CNV clock mode and autonomous mode. In CNV burst mode and SPI burst mode, the equations only apply within each sample burst window.

In standard sequencer mode, each enabled channel is sampled once per sequence, so all enabled channels have the same effective sample rate, and is given by the following equation:

$$f_{S\_INx} = \frac{f_S}{N_{CH}}$$

where:
N_{CH} is the number of enabled channels.
f_{S_INx} is equal to the input data rate of each channel's averaging filter.

The output data rate for each channel (f_{ODR_INx}) is the rate at which new accumulator or averaging data are ready, and is calculated in the following equation:

$$f_{ODR\_INx} = \frac{f_{S\_INx}}{ACC\_DEPTH}$$

where ACC_DEPTH is the number of samples per averaged (or accumulated) result, as described in the Averaging Filters section.

In advanced sequencer mode, the channel sequence is more flexible and customizable, so f_{S_INx} can vary between channels and is impractical to generalize. The Priority Sequence Scheme section details a type of sequence supported by the advanced sequencer which enables multiple sample rates per channel.

APPLICATIONS INFORMATION

PRIORITY SEQUENCE SCHEME

The priority sequence scheme is a method for programming the advanced sequencer to achieve a set of high priority channels (higher sampling rates and higher averaging ratios) and low priority channels (lower sampling rates and lower averaging ratios). The following describes how to implement a priority sequencing scheme using the AD4691/AD4692 advanced sequencer mode.

Figure 87 shows a generalized channel sequence with two priority levels. Channels are grouped into high priority (HP) and low priority (LP) channels. The LP channels are sampled once per sequence, while the HP channels are sampled multiple times per sequence. Alternatively, the channel sequence can be thought of as a grouping of subsequences, where all of the HP channels are sampled once per subsequence, but only one LP channel is sampled per subsequence.

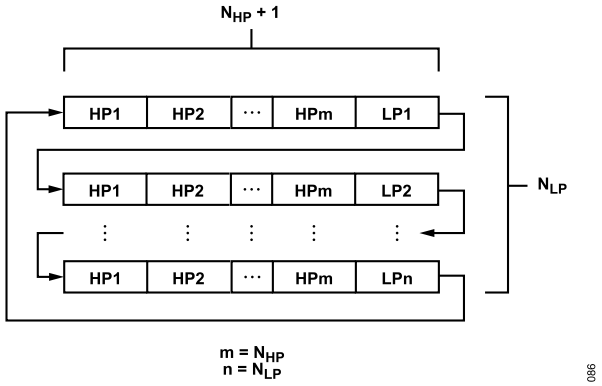


Figure 87. Sequence of HP and LP Channels in Two-Priority Channel Sequence

The number of LP and HP channels dictate the length of the entire channel sequence and their effective sample rates. The number of advanced sequencer slots needed to implement the two priority sequence scheme (N_{SLOTS}) is defined by the following equation:

$$N_{SLOTS} = N_{LP} \times (N_{HP} + 1) \quad (6)$$

where:
N_{LP} is the number of LP channels.
N_{HP} is the number of HP channels.

The maximum value of N_{SLOTS} needed to implement a two priority sequence scheme is when $N_{LP} = N_{HP} = 8$ channels, where $N_{SLOTS} = 72$ slots.

Because the LP channels are only sampled once per N_{SLOTS} channels, their effective sampling frequency (f_{S_LP}) is as follows:

$$f_{S\_LP} = {}^{f_S}/_{N_{SLOTS}} \quad (7)$$

Because the HP channels are sampled once for each LP channel, their effective sampling frequency (f_{H_LP}) is as follows:

$$f_{S\_HP} = f_S \times \frac{N_{LP}}{N_{SLOTS}} \quad (8)$$

Table 23 and Figure 88 show an example two-priority sequence with IN0, IN1, and IN2 as HP channels and IN3 and IN4 as LP channels. N_{SLOTS} is 8 in this example, so the NUM_SLOTS_AS bit field is set to 0x7. The sequence slot channel assignments are set via the AS_SLOTx registers, as described in the Advanced Sequencer Mode section. In this example, configuring the HP channels accumulator depths to twice the LP channels accumulator depths ensures all channels have the same output data rate. Figure 88 shows an example where the HP channels depth is 4 and the LP channels depth is 2, and each channel therefore has an output data rate of $f_S/16$.

Table 23. Two-Priority Example with Sampling Rates and Output Data Rates

Slot Number	Slot Channel	Channel Effective Sampling Rate	Accumulator Depth (i.e. Averaging Ratio)	Output Data Rate
0	IN0	$f_S/4$	4	$f_S/16$
1	IN1	$f_S/4$	4	$f_S/16$
2	IN2	$f_S/4$	4	$f_S/16$
3	IN3	$f_S/8$	2	$f_S/16$
4	IN0	$f_S/4$	4	$f_S/16$
5	IN1	$f_S/4$	4	$f_S/16$
6	IN2	$f_S/4$	4	$f_S/16$
7	IN4	$f_S/8$	2	$f_S/16$

APPLICATIONS INFORMATION

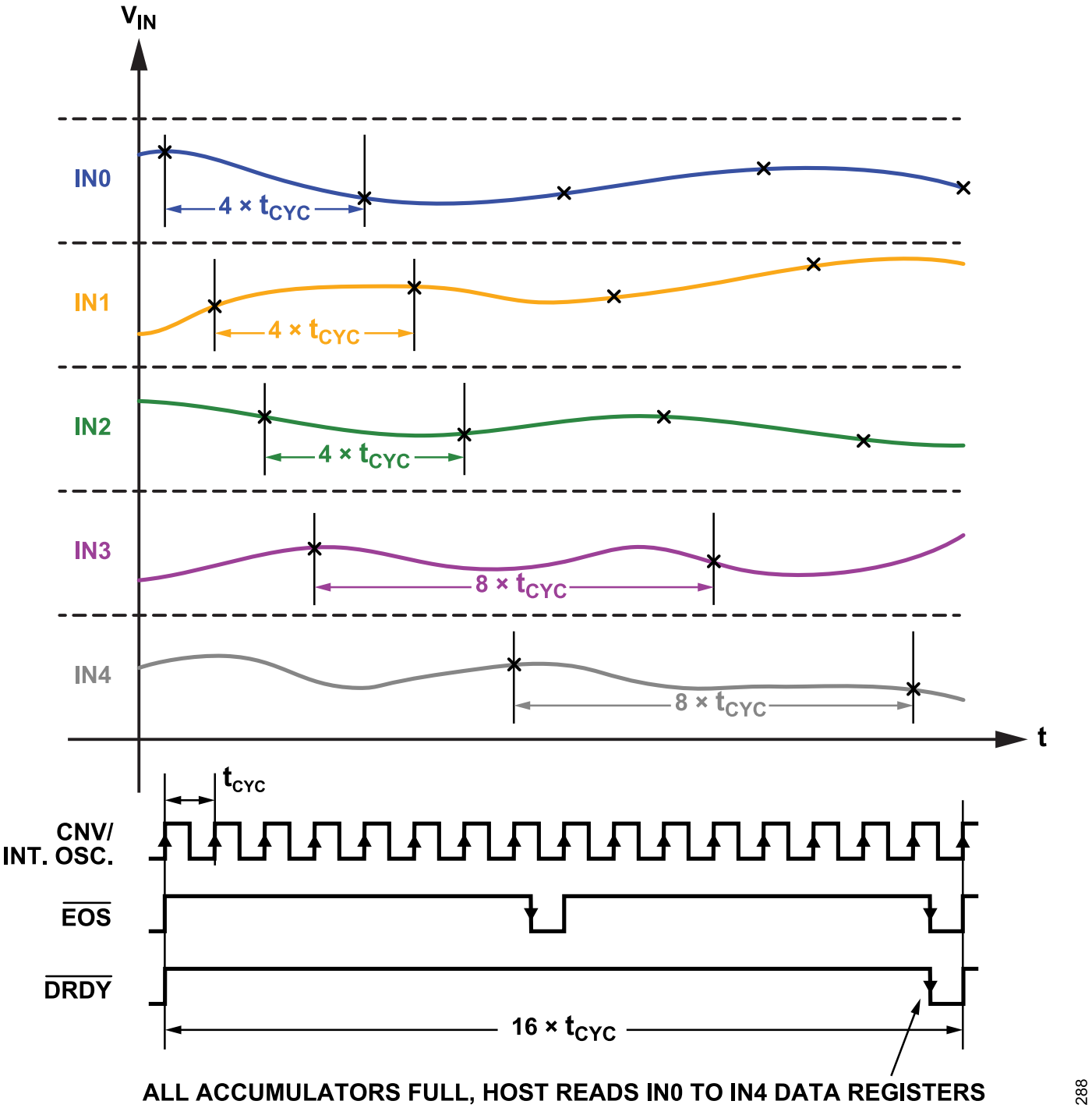


Figure 88. Two-Priority Example Timing Diagram

APPLICATIONS INFORMATION

SELECTING RC KICKBACK FILTER COMPONENTS

This section provides recommendations for selecting the RC kickback filter components at the inputs of the AD4691/AD4692 (see R_{EXT} and C_{EXT} in Figure 84). The analysis shows the relationship between the precharge buffers, the sampling capacitor (C_{SH}) and RC filter component values for achieving accurate settling.

As described in the Analog Input Precharge section, a voltage glitch (V_{GLITCH}) occurs when the MUX switch toggles to start acquiring an input channel. V_{GLITCH} is caused when the voltages on C_{EXT} and C_{SH} are different when the MUX switch shorts them together. The magnitude of V_{GLITCH} is proportional to the capacitances and voltage difference between C_{EXT} and C_{SH} (ΔV) as follows:

$$V_{GLITCH} = \left(\frac{C_{SH}}{C_{SH} + C_{EXT}}\right) \times \Delta V \quad (9)$$

The values of R_{EXT} and C_{EXT} must be chosen to ensure V_{GLITCH} settles to within ½ LSB before the next convert-start to prevent the ADC from sampling a settling error. The following is the settling time of the kickback filter (t_{SETTLE}):

$$t_{ACQ} > t_{SETTLE} = \tau \times N_{\tau} \quad (10)$$

where:
τ is the RC time constant
N_{τ} is the number of time constants required to settle V_{GLITCH} to within ½ LSB.

N_{τ} is determined as follows by the RC exponential settling relationship:

$$N_{\tau} = \ln\left(\frac{V_{GLITCH}}{V_{REF}/2^{17}}\right) \quad (11)$$

t_{ACQ} is the acquisition time which is a function of the sampling period (t_{CYC}) and the precharge delay is calculated as follows:

$$t_{ACQ} = t_{CYC} - \quad 515ns = \quad \frac{1}{f_S} - 515ns \quad (12)$$

For traditional MUX SAR ADCs, ΔV can be as large as V_{REF}, which requires a large C_{EXT} to attenuate V_{GLITCH} and a small R_{EXT} to achieve a small enough τ, which also requires a high-speed, low-noise amplifier to maintain stability and SNR. The AD4691/AD4692 precharge buffers remove the need for these high-speed amplifiers by minimizing ΔV and V_{GLITCH} by extension. The precharge buffers ensure ΔV is 5mV, a 1000 times reduction compared to a traditional MUX SAR ADC with a V_{REF} of 5V.

Figure 89 shows the maximum recommended R_{EXT} values for different C_{EXT} values and sampling rates, using the preceding equations. The analysis given previously and in Figure 89 assumes the settling time is dominated by the kickback filter time constant and ignores any overshoot or ringing caused by interaction of the kickback filter and the output impedance of the front-end amplifier.

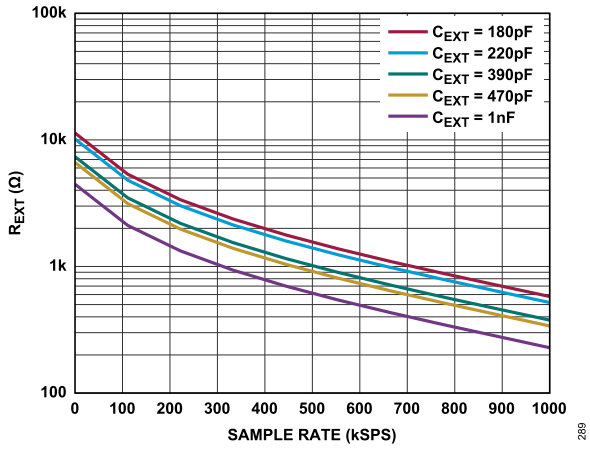


Figure 89. R_{EXT} and C_{EXT} Values vs. Sampling Rate

MASKING CHANNELS TO AVOID LOCKOUT CONDITIONS

A lockout condition is when the $\overline{DRDY}$ signal cannot assert while being used as the stop trigger in CNV burst mode or SPI burst mode. This causes the internal oscillator to run without stopping, even if all accumulators are full. Lockout conditions are caused by improper configuration of the accumulator mask bits (ACC_MASK_INx) relative to the active channel sequence, preventing the ACC_FULL_INx signals from toggling the $\overline{DRDY}$ signal and holding it high indefinitely.

To avoid lockout conditions, all channels that are included in the sequence must be unmasked, while all channels that are excluded are masked. These masking requirements apply to both the standard sequencer mode and advanced sequencer mode. Figure 90 shows an example channel sequence with the corresponding ACC_MASK_INx bits set to 0 (to unmask the included channels) or 1 (to mask the excluded channels).

Setting all ACC_MASK_INx bits to 1 simultaneously also causes lockout conditions because it guarantees all included channels are masked.

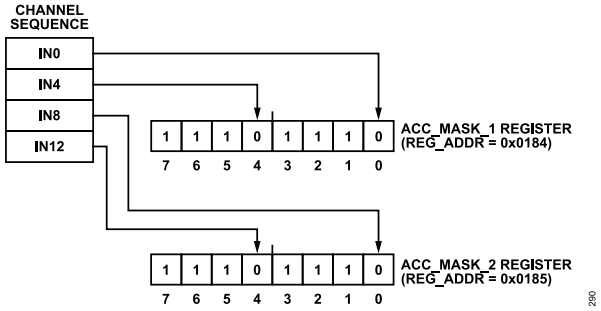


Figure 90. Mask Bit Setting vs. Channel Sequence Example

APPLICATIONS INFORMATION

BULK READING ADC DATA REGISTERS

As described in the Averaging Filter Readback section, the AD4691/AD4692 include multiple registers for reading ADC results for each of the 16 channels. This section provides recommendations for efficiently reading data from these registers using the autodecrement mode or direct-address mode described in the Bulk Register Reads and Writes.

Table 14 through Table 17 list the register addresses for each readback register set (averaged data or accumulator data; with or without the status byte) for each channel. Each set of readback registers contains data for all 16 ADC channels, with each channels address being adjacent to the next channels address. For example, AVG_IN0 is next to the AVG_IN1 register, which is next to the AVG_IN2 register, and so on.

Auto-decrement mode is most efficient when reading from multiple adjacent channels. For example, when reading from all 16 AVG_INx registers, it is most efficient to send REG_ADDR = 0x021F in the instruction phase to address the MSByte of ACC_IN15 and clock out the 32 bytes of data in one SPI frame, as shown in Figure 91. The subsequent state reset must be in a second SPI frame with REG_ADDR = 0x0181.

Direct-address mode is most efficient when reading from multiple nonadjacent channels. For example, when reading from the ACC_INx registers for channels IN0, IN3, IN6, and IN9, it is most efficient to send a single SPI frame where each instruction phase contains the MSByte address for each channel, as shown in Figure 92. The subsequent state reset can occur in the same frame as the channel data readback.

In general it is recommended to use adjacent and contiguous groups of channels on the hardware, because it is more efficient to read from groups of adjacent channels with autodecrement mode than it is to read from groups of nonadjacent channels with direct-address mode. For example, if the system uses only 12 channels, connect the analog front-end circuits to channels IN0 through IN11 (rather than a random combination of 12 channels) for the fastest possible readback.

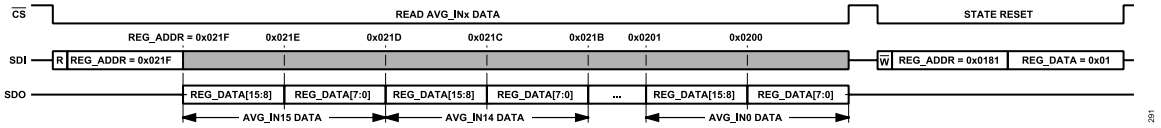


Figure 91. Reading Adjacent Channel Data with Autodecrement Mode

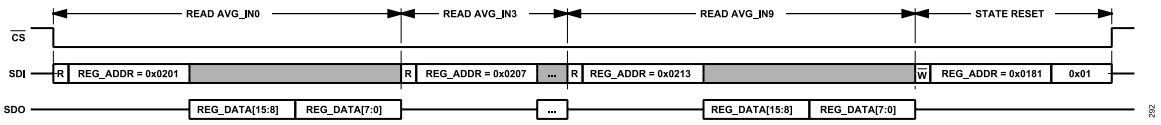


Figure 92. Reading Nonadjacent Channel Data with Direct-Address Mode

APPLICATIONS INFORMATION

CONFIGURATION FLOWCHARTS

Figure 93 through Figure 99 provide example flowcharts for configuring and operating the AD4691/AD4692 with their various features and operating modes. Refer to these flowcharts as guides for programming the device configuration registers for the desired modes.

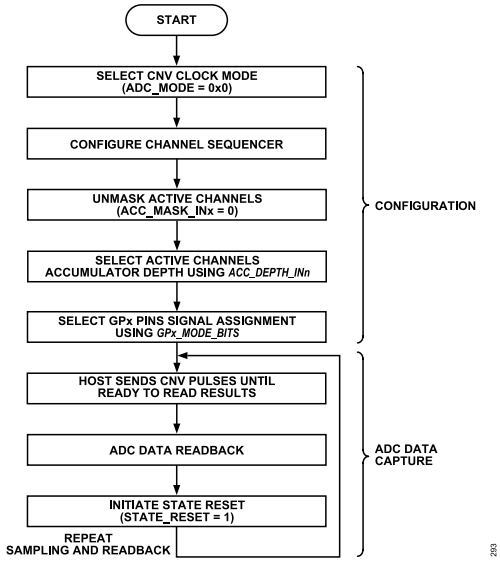


Figure 93. Device Configuration Flowchart for CNV Clock Mode

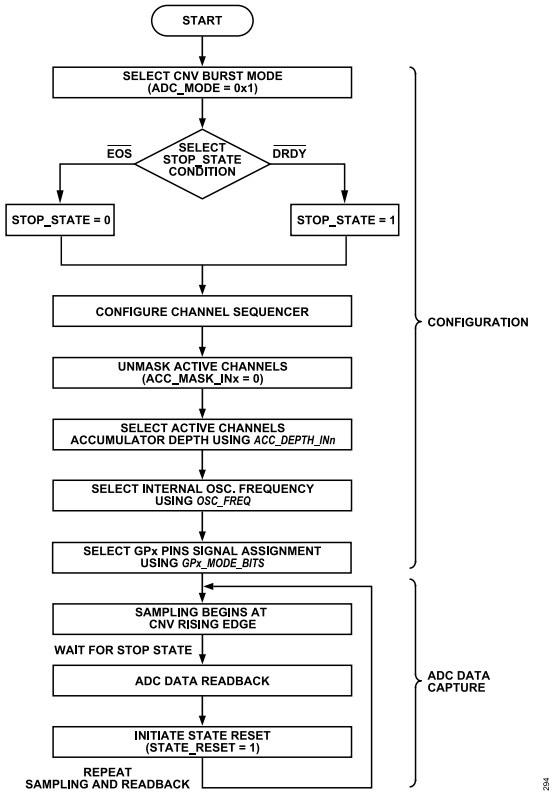


Figure 94. Device Configuration Flowchart for CNV Burst Mode

APPLICATIONS INFORMATION

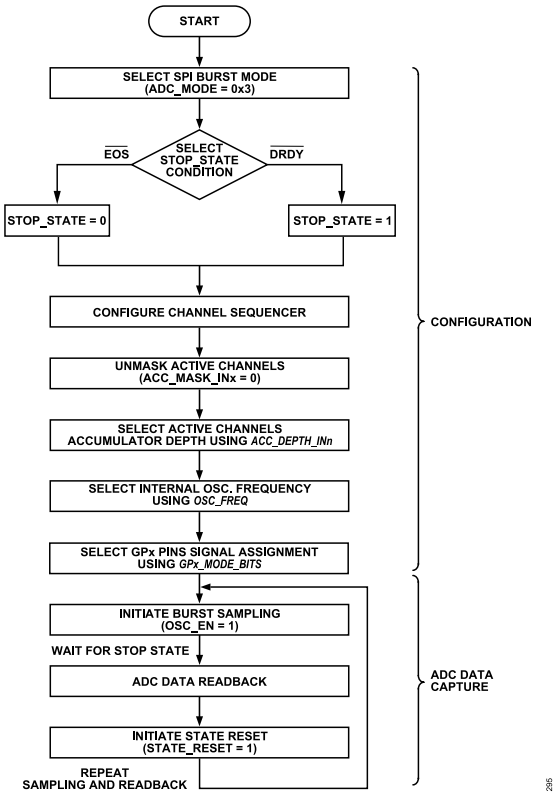


Figure 95. Device Configuration Flowchart for SPI Burst Mode

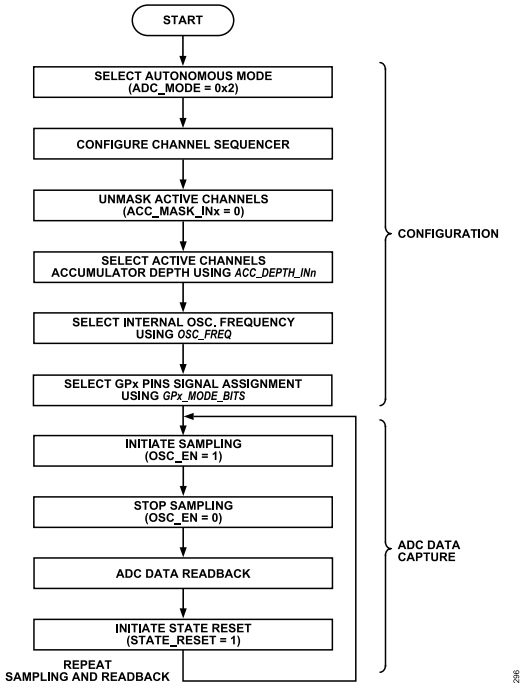


Figure 96. Device Configuration Flowchart for Autonomous Mode

APPLICATIONS INFORMATION

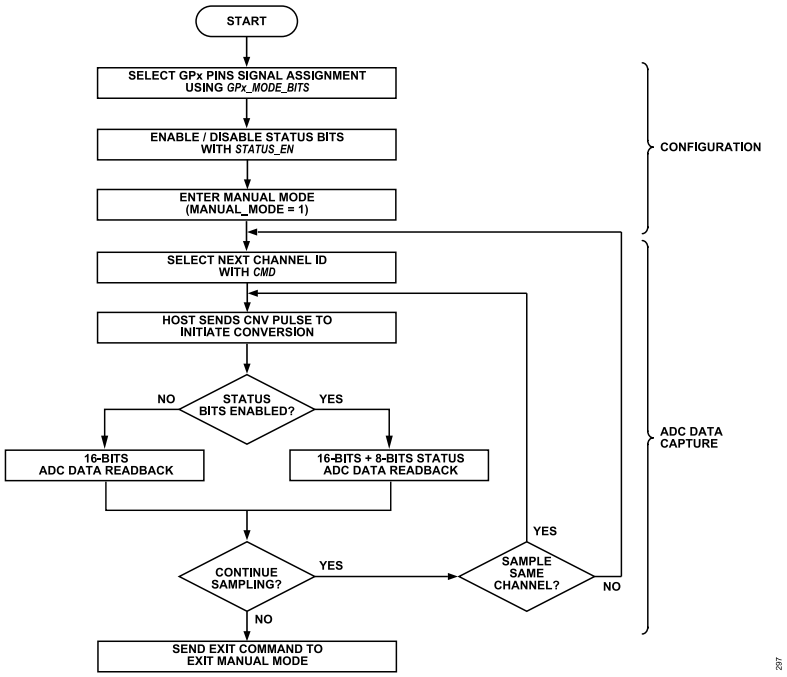


Figure 97. Device Configuration Flowchart for Manual Mode

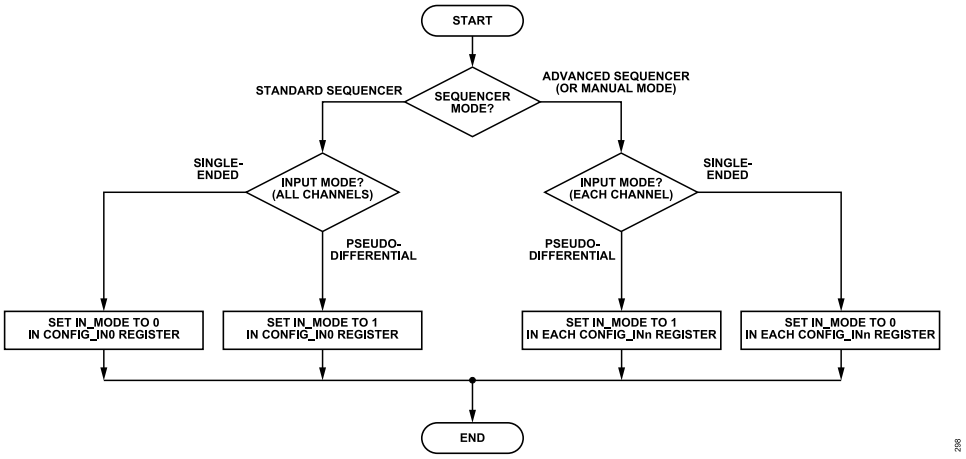


Figure 98. Device Configuration Flowchart for Analog Input Configuration

APPLICATIONS INFORMATION

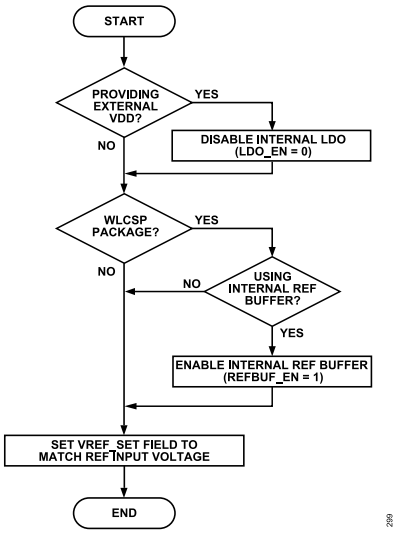


Figure 99. Device Configuration Flowchart for Reference and LDO Regulator

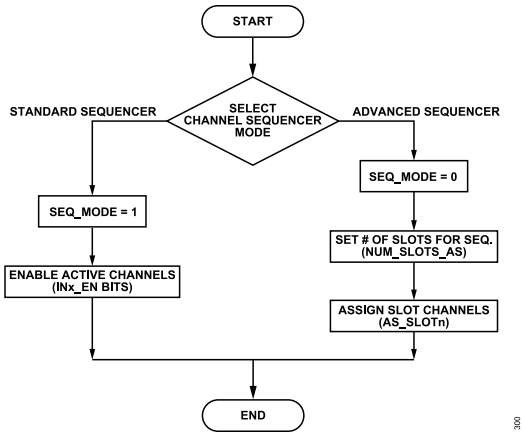


Figure 100. Flowchart for Configuring the Channel Sequencer

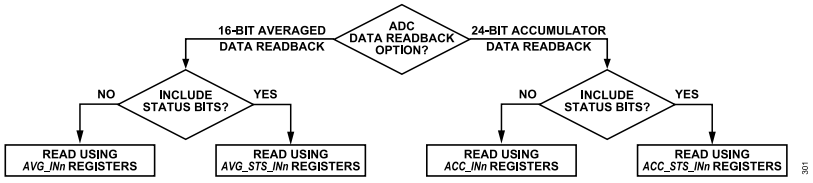


Figure 101. Flowchart for Selecting Readback Register Options

APPLICATIONS INFORMATION

LAYOUT GUIDELINES

The following are suggested layout techniques for achieving optimal performance of the AD4691/AD4692 populated on a PCB. An example PCB layout is provided in the user guide for the AD4692 evaluation board (EVAL-AD4692-ARDZ).

Analog traces (that is, traces connected to the analog inputs and reference input) must be physically separated from the digital traces (that is, traces to the CNV input, SPI, and general-purpose pins) to limit cross coupling from fast switching digital signals into the analog input signals. Add ground fill between analog and digital traces on the same PCB layer. Do not cross digital traces over the analog traces or the AD4691/AD4692 devices without a ground plane PCB layer in between. The analog and digital pins on the AD4691/AD4692 are arranged to facilitate separation of analog and digital traces.

The AD4691/AD4692 analog inputs (IN0 to IN15) have a dynamic input impedance due to the multiplexer and ADC core input switches, which toggle between conversions. An external capacitor is recommended to reduce nonlinear voltage steps at the analog inputs. Place these external capacitors as close to the analog inputs as possible to minimize parasitic impedance paths between the two, which can degrade performance.

The AD4691/AD4692 voltage reference input, REF, also has a dynamic input impedance. The effective impedance between the reference drive circuitry output and the REF input must be very low, and a decoupling capacitor must be placed as close to the REF pin as possible. If the internal reference buffer is not used, connect the external reference circuitry to the REF pin with wide traces to minimize the trace impedance.

The power supplies of the AD4691/AD4692 must be decoupled with low effective series resistance (ESR) ceramic capacitors placed close to the supply pins and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines (see the Power Supplies section). If LDO_IN is powered from the same supply as AVDD, short the pins with a wide common trace, and a single 100nF capacitor can be used to decouple both pins.

The AN-617 Application Note, *Wafer Level Chip Scale Package*, has information on PCB layout and assembly for the WLCSP.

EVALUATING THE AD4691/AD4692 PERFORMANCE

The AD4691/AD4692 evaluation tool offerings include a fully assembled and tested evaluation board (EVAL-AD4692-ARDZ), including the , evaluation software for controlling the board from a PC and support documentation for the hardware and software.

The EVAL-AD4692-ARDZ board allows for prototyping the analog front-end circuitry and reference circuitry with the various digital features offered by the AD4691/AD4692. It also features a standard Arduino Uno digital header, enabling interfacing to the EVAL-SDP-CK1Z board or third party controller boards for prototyping interface firmware and application software.

REGISTER INFORMATION

The AD4691/AD4692 device configurations are set via their configuration registers. The AD4691/AD4692 SPIs are used to read and write to the configuration registers as described in the Register Access section.

The AD4691/AD4692 configuration registers are mapped to a set of register addresses. Each address value corresponds to a byte of register data. As described in the Register Length section, most registers are one byte long, but some are multiple bytes long. Table 24 shows the register memory address assignments for all of the AD4691/AD4692 configuration registers.

Bits and fields in the AD4691/AD4692 configuration registers are defined as read only, read/write, or read/write-1-to-clear. In the access column of Table 24, registers that contain exclusively read-only bits are represented with R and registers with writable bits are represented with R/W. In the access column of Table 25 through Table 65, read only bits are represented with R, read/write bits are represented with R/W, and write 1 to clear bits are represented with R/W1C.

The SPI_STATUS register contains various error flags that indicate whether an SPI read or write transaction violated one of several aspects of the protocols outlined in the Register Access section (see Table 35). The SPI_ERROR bit in the status register is the bitwise logical OR of the error flags in the SPI_STATUS register (see Table 36).

Table 24. AD4691/AD4692 Configuration Register Summary

Address	Name	Description	Reset	Access
0x0000	SPI_CONFIG_A	SPI Configuration A.	0x10	R/W
0x0001	SPI_CONFIG_B	SPI Configuration B.	0x00	R/W
0x0003	DEVICE_TYPE	Device Type.	0x07	R
0x0004	PRODUCT_ID_LSB	Product Identification (LSB).	[1]	R
0x0005	PRODUCT_ID_MSB	Product Identification (MSB).	0x00	R
0x000A	SCRATCH_PAD	Scratch Pad.	0x00	R/W
0x000C	VENDOR_ID_LSB	Vendor ID (LSB).	0x56	R
0x000D	VENDOR_ID_MSB	Vendor ID (MSB).	0x04	R
0x000E	STREAM_MODE	Reserved.	0x00	R/W
0x0010	SPI_CONFIG_C	SPI Configuration C.	0x23	R/W
0x0011	SPI_STATUS	SPI Status.	0x00	R/W
0x0014	DEVICE_STATUS	Device status.	0x20	R
0x001A	CLAMP_STATUS1	Clamp status (IN0 to IN7).	0x00	R
0x001B	CLAMP_STATUS2	Clamp status (IN8 to IN15).	0x00	R
0x0020	DEVICE_SETUP	Device setup.	0x10	R/W
0x0021	REF_CTRL	Reference control.	0x10	R/W
0x0022	SEQ_CTRL	Sequencer control.	0x80	R/W
0x0023	OSC_FREQ_REG	Internal oscillator frequency.	0x00	R/W
0x0025	STD_SEQ_CONFIG	Standard sequencer configuration.	0x0001	R/W
0x0030 to 0x003F	CONFIG_INn	Analog input settings configuration.	0x08	R/W
0x0100 to 0x017F	AS_SLOTn	Advanced sequencer slot.	0x00	R/W
0x0180	OSC_EN_REG	Internal oscillator enable.	0x00	R/W
0x0181	STATE_RESET_REG	State reset.	0x01	R/W
0x0182	ADC_SETUP	ADC setup.	0x00	R/W
0x0184	ACC_MASK_1	Accumulator mask (IN0 to IN7).	0xFE	R/W
0x0185	ACC_MASK_2	Accumulator mask (IN8 to IN15).	0xFF	R/W
0x0186 to 0x0195	ACC_DEPTH_INn	Accumulator depth.	0x3F	R/W
0x0196	GP0_GP1_MODE	GP0 and GP1 control.	0x00	R/W
0x0197	GP2_GP3_MODE	GP2 and GP3 control.	0x00	R/W
0x01A0	GPIO_READ	GPIO logic input state.	0x00	R
0x01B0	ACC_STS_FULL_1	Accumulator full status (IN0 to IN7).	0x00	R
0x01B1	ACC_STS_FULL_2	Accumulator full status (IN8 to IN15).	0x00	R
0x01B2	ACC_STS_OVR_1	Accumulator overrun status (IN0 to IN7).	0x00	R
0x01B3	ACC_STS_OVR_2	Accumulator overrun status (IN8 to IN15).	0x00	R
0x01B4	ACC_STS_SAT_1	Accumulator saturation status (IN0 to IN7).	0x00	R
0x01BE	ACC_STS_SAT_2	Accumulator saturation status (IN8 to IN15).	0x00	R

REGISTER INFORMATION

Table 24. AD4691/AD4692 Configuration Register Summary (Continued)

Address	Name	Description	Reset	Access
0x01C0 to 0x01CF	ACC_STATUS_INn	Accumulator general status.	0x00	R
0x0201 to 0x021F	AVG_INn	Averaging filter data.	0x00	R
0x0222 to 0x024F	AVG_STS_INn	Averaging filter data plus status.	0x000	R
0x0252 to 0x027F	ACC_INn	Accumulator data.	0x000	R
0x0283 to 0x02BF	ACC_STS_INn	Accumulator data plus status.	0x0000	R

[1] See Table 28.

REGISTER DETAILS

SPI Configuration A Register

Address: 0x0000, Reset: 0x10, Name: SPI_CONFIG_A

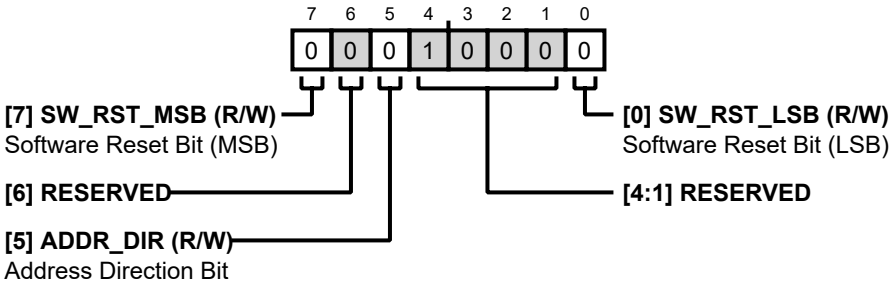


Table 25. Bit Descriptions for SPI_CONFIG_A

Bits	Bit Name	Description	Reset	Access
7	SW_RST_MSB	Software Reset Bit (MSB). Set both SW_RST_MSB and SW_RST_LSB to 1 in the same register write frame to initiate a software reset fo the device. All registers reset to their default power-up state except the SPI_CONFIG_A register.	0x0	R/W
6	RESERVED	Reserved.	0x0	R
5	ADDR_DIR	Reserved. This bit must be set to 0.	0x0	R/W
[4:1]	RESERVED	Reserved.	0x8	R
0	SW_RST_LSB	Software Reset Bit (LSB). Set both SW_RST_MSB and SW_RST_LSB to 1 in the same register write frame to initiate a software reset fo the device. All registers reset to their default power-up state except the SPI_CONFIG_A register.	0x0	R/W

SPI Configuration B Register

Address: 0x0001, Reset: 0x00, Name: SPI_CONFIG_B

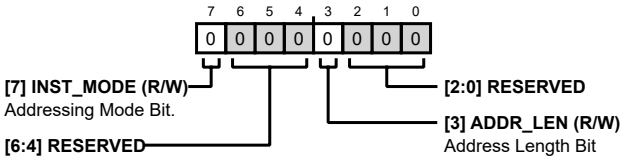


Table 26. Bit Descriptions for SPI_CONFIG_B

Bits	Bit Name	Description	Reset	Access
7	INST_MODE	Addressing Mode Bit. Selects between autodecrement and direct-address mode for bulk reading or writing registers. 0: Autodecrement mode. 1: Direct-address mode.	0x0	R/W

REGISTER INFORMATION

Table 26. Bit Descriptions for SPI_CONFIG_B (Continued)

Bits	Bit Name	Description	Reset	Access
[6:4]	RESERVED	Reserved.	0x0	R
3	ADDR_LEN	Reserved. This bit must be set to 0.	0x0	R/W
[2:0]	RESERVED	Reserved.	0x0	R

Device Type Register

Address: 0x0003, Reset: 0x07, Name: DEVICE_TYPE

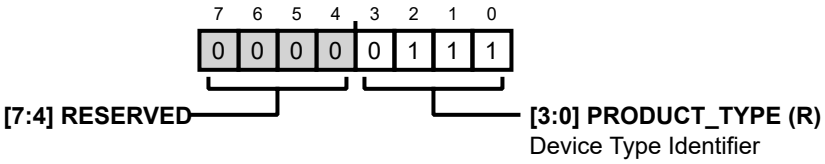


Table 27. Bit Descriptions for DEVICE_TYPE

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	DEVICE_TYPE	Device Type Indicator Field. This field identifies the Analog Devices, Inc., product category that the device belongs to. The value 0x7 corresponds to precision ADCs.	0x7	R

Product Identification (LSB)

Address: 0x0004, Reset: 0x10, Name: PRODUCT_ID_LSB

Table 28. Bit Descriptions for PRODUCT_ID_LSB

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[7:0]	Product Identifier. The product identification registers are used in conjunction with the device type register to uniquely identify the AD4692 or AD4691. The product identifier code is 16 bits long and is spread across two registers (PRODUCT_ID_LSB and PRODUCT_ID_MSB). The unique PRODUCT_ID value for the AD4691 is 0x0011 and for the AD4692 is 0x0012.	AD4691: 0x11, AD4692: 0x12	R

Product Identification (MSB)

Address: 0x0005, Reset: 0x00, Name: PRODUCT_ID_MSB

Table 29. Bit Descriptions for PRODUCT_ID_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	PRODUCT_ID[15:8]	Product Identifier. The product identification registers are used in conjunction with the device type register to uniquely identify the AD4692 or AD4691. The product identifier code is 16 bits long and is spread across two registers (PRODUCT_ID_LSB and PRODUCT_ID_MSB). The unique PRODUCT_ID value for the AD4691 is 0x0011 and for the AD4692 is 0x0012.	0x00	R

REGISTER INFORMATION

Scratch Pad Register

Address: 0x000A, Reset: 0x00, Name: SCRATCH_PAD

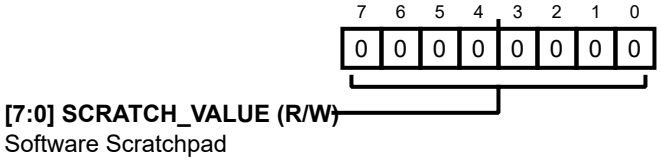


Table 30. Bit Descriptions for SCRATCH_PAD

Bits	Bit Name	Description	Reset	Access
[7:0]	SCRATCH_VALUE	Software Scratchpad. Use this register to test SPI communications with the device. Values written to this register have no impact on device configuration or behavior.	0x00	R/W

Vendor Identification (LSB) Register

Address: 0x000C, Reset: 0x56, Name: VENDOR_ID_LSB

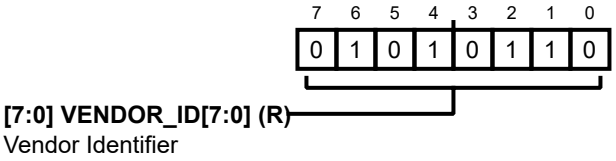


Table 31. Bit Descriptions for VENDOR_ID_LSB

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[7:0]	Vendor Identifier. The VENDOR_ID[15:0] field is the same value (0x0456) for all Analog Devices precision ADCs.	0x56	R

Vendor Identification (MSB) Register

Address: 0x000D, Reset: 0x04, Name: VENDOR_ID_MSB

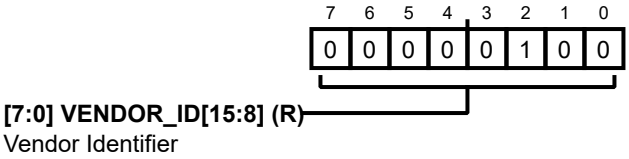


Table 32. Bit Descriptions for VENDOR_ID_MSB

Bits	Bit Name	Description	Reset	Access
[7:0]	VENDOR_ID[15:8]	Vendor Identification Field. The VENDOR_ID[15:0] field is the same value (0x0456) for all Analog Devices precision ADCs.	0x04	R

REGISTER INFORMATION

Reserved Register

Address: 0x000E, Reset: 0x00, Name: STREAM_MODE

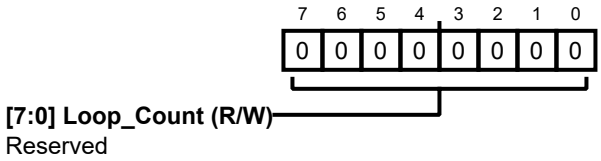


Table 33. Bit Descriptions for STREAM_MODE

Bits	Bit Name	Description	Reset	Access
[7:0]	LOOP_COUNT	Reserved. This field must be set to 0x00.	0x00	R/W

SPI Configuration C Register

Address: 0x0010, Reset: 0x23, Name: SPI_CONFIG_C

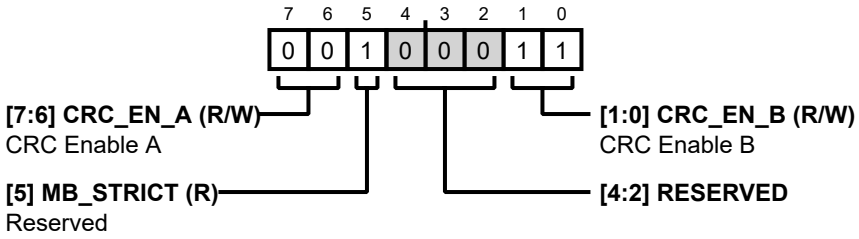


Table 34. Bit Descriptions for SPI_CONFIG_C

Bits	Bit Name	Description	Reset	Access
[7:6]	CRC_EN_A	CRC Enable A. Set CRC_EN_A to 0x1 and CRC_EN_B to 0x2 in the same register write frame to enable interface CRC. 0x0: CRC disabled. 0x1: CRC enabled.	0x0	R/W
5	MB_STRICT	Reserved. This bit must be set to 1.	0x1	R/W
[4:2]	RESERVED	Reserved.	0x0	R
[1:0]	CRC_EN_B	CRC Enable B. Set CRC_EN_A to 0x1 and CRC_EN_B to 0x2 in the same register write frame to enable interface CRC.	0x3	R/W

REGISTER INFORMATION

SPI Status Register

Address: 0x0011, Reset: 0x00, Name: SPI_STATUS

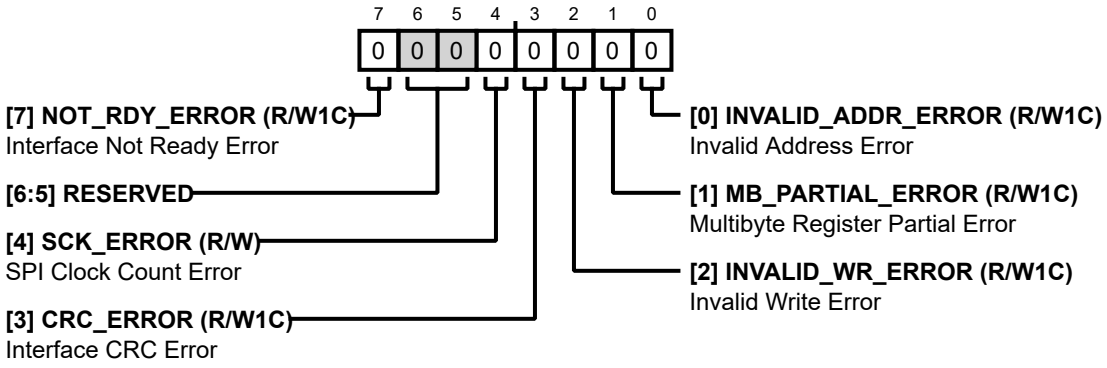


Table 35. Bit Descriptions for SPI_STATUS

Bits	Bit Name	Description	Reset	Access
7	NOT_RDY_ERROR	Interface Not Ready Error. This bit is set to 1 when the digital host initiates an SPI transaction before the device is ready to respond. For example, before a device reset is complete. NOT_RDY_ERROR is a sticky bit and is only cleared by writing it to 1.	0x0	R/W1C
[6:5]	RESERVED	Reserved.	0x0	R
4	SCK_ERROR	SPI Clock Count Error. This bit is set to 1 when an incorrect number of serial clock edges is received in an SPI transaction. For example, if the data phase does not contain an integer multiple of 8 SCK periods. SCK_ERROR is a sticky bit and is only cleared by writing it to 1.	0x0	R/W
3	CRC_ERROR	Interface CRC Error. This bit is set when the device receives an invalid CRC checksum value on SDI (in configuration mode). This error bit is only active when CRC is enabled. CRC_ERROR is a sticky bit and is only cleared by writing it to 1.	0x0	R/W1C
2	WRITE_INVALID	Invalid Write Error. This bit is set to 1 when the digital host attempts to write to a register that contains exclusively read-only bits. INVALID_WRITE_ERROR is a sticky bit and is only cleared by writing it to 1.	0x0	R/W1C
1	MB_ERROR	Multibyte Register Partial Error. This bit is set to 1 when the digital host fails to read or write from all bytes of a multibyte register in an SPI frame. For example, reading only the bottom byte of the STD_SEQ_CONFIG register. MB_PARTIAL_ERROR is a sticky bit and is only cleared by writing it to 1.	0x0	R/W1C
0	ADDR_INVALID	Invalid Address Error. This bit is set to 1 when the digital host attempts to read from or write to an undefined register address. INVALID_ADDR_ERROR is a sticky bit and is only cleared by writing it to 1.	0x0	R/W1C

REGISTER INFORMATION

Device Status Register

Address: 0x0014, Reset: 0x20, Name: DEVICE_STATUS

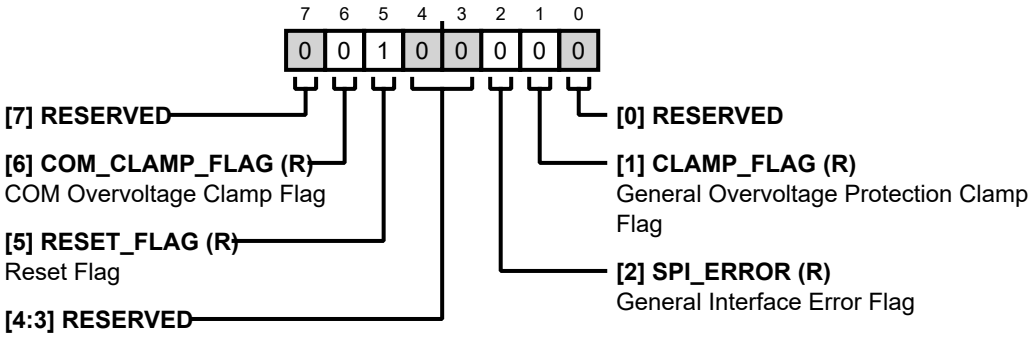
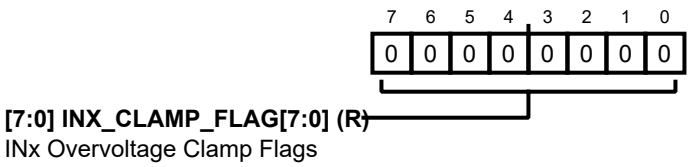


Table 36. Bit Descriptions for DEVICE_STATUS

Bits	Bit Name	Description	Reset	Access
7	RESERVED	Reserved.	0x0	R
6	COM_CLAMP_FLAG	COM Overvoltage Clamp Flag. Indicates if the COM overvoltage protection clamp is active due to an overvoltage event. This bit is not sticky, and is cleared once the COM overvoltage protection clamp deactivates. 0: Inactive COM clamp. 1: Active COM clamp.	0x0	R
5	RESET_FLAG	Reset Flag. Indicates whether a full device reset occurred since the last time this bit was read. RESET_FLAG is automatically cleared when read. 0: No reset occurred. 1: Reset occurred.	0x1	R
[4:3]	RESERVED	Reserved.	0x0	R
2	SPI_ERROR	General Interface Error Flag. Indicates if any of the error flags in the SPI_STATUS register are asserted. SPI ERROR is the logical OR of all bits in the SPI_STATUS register. 0: no interface error detected. 1: one or more interface errors detected.	0x0	R
1	CLAMP_FLAG	General Overvoltage Protection Clamp Flag. Indicates if any of the IN0 to IN15 overvoltage protection clamps were activated by an overvoltage event. CLAMP_FLAG is asserted when any of the INX_CLAMP_FLAG bits are asserted. CLAMP_FLAG is only deasserted when the DEVICE_STATUS register is read while all INX_CLAMP_FLAG bits are deasserted (that is, when all clamps are deactivated). 0: Inactive clamps. None of the IN0 to IN15 clamps were activated. 1: Active clamp(s). One or more of the IN0 to IN15 clamps were or are activated.	0x0	R
0	RESERVED	Reserved.	0x0	R

Clamp Status (IN0 to IN7) Register

Address: 0x001A, Reset: 0x00, Name: CLAMP_STATUS1



REGISTER INFORMATION

Table 37. Bit Descriptions for CLAMP_STATUS1

Bits	Bit Name	Description	Reset	Access
[7:0]	INX_CLAMP_FLAG[7:0]	INx Overvoltage Clamp Flags. Indicates if each INx overvoltage protection clamp is active due to an overvoltage event. Each bit in INX_CLAMP_FLAG[15:0] corresponds to a channel, for example bit 0 corresponds to IN0, etc. The INX_CLAMP_FLAG bits are not sticky, and are automatically cleared when the corresponding overvoltage protection clamp deactivates.	0x0	R

Clamp Status (IN8 to IN15) Register

Address: 0x001B, Reset: 0x00, Name: CLAMP_STATUS2

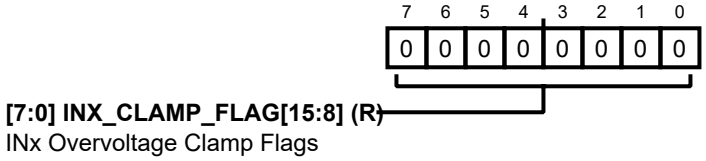


Table 38. Bit Descriptions for CLAMP_STATUS2

Bits	Bit Name	Description	Reset	Access
[7:0]	INX_CLAMP_FLAG[15:8]	INx Overvoltage Clamp Flags. Indicates if each INx overvoltage protection clamp is active due to an overvoltage event. Each bit in INX_CLAMP_FLAG[15:0] corresponds to a channel, for example bit 0 corresponds to IN0, etc. The INX_CLAMP_FLAG bits are not sticky, and are automatically cleared when the corresponding overvoltage protection clamp deactivates.	0x0	R

Device Setup Register

Address: 0x0020, Reset: 0x10, Name: DEVICE_SETUP

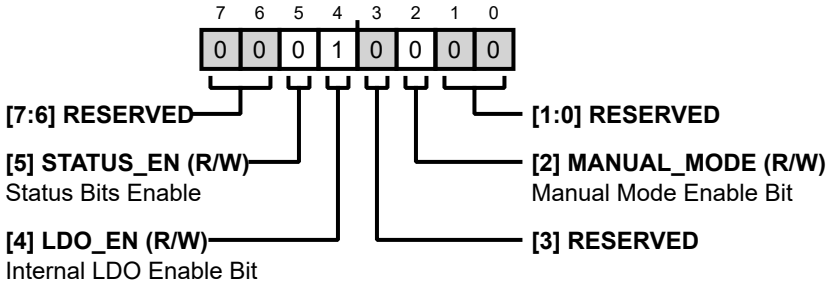


Table 39. Bit Descriptions for DEVICE_SETUP

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	STATUS_EN	Status Bits Enable. Determines whether the status bits are appended to ADC data in manual mode. 0: Status bits disabled. 1: Status bits enabled.	0x0	R/W
4	LDO_EN	Internal LDO Enable Bit. Enables or disables the internal LDO regulator. The internal LDO regulator is enabled by default. Disable the internal LDO regulator when driving VDD with an external 1.8V supply. 0: Internal LDO regulator disabled. 1: Internal LDO regulator enabled.	0x1	R/W
3	RESERVED	Reserved.	0x0	R

REGISTER INFORMATION

Table 39. Bit Descriptions for DEVICE_SETUP (Continued)

Bits	Bit Name	Description	Reset	Access
2	MANUAL_MODE	Manual Mode Enable Bit. Setting this bit to 1 puts the device into manual mode. In manual mode, the SPI is only used to access ADC data and does not support register reads or writes. Sending the exit command resets this bit to 0 and exits manual mode. 0: Manual mode disabled. 1: Manual mode enabled.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x0	R

Reference Control Register

Address: 0x0021, Reset: 0x10, Name: REF_CTRL

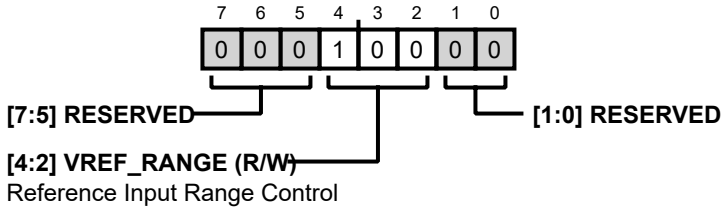


Table 40. Bit Descriptions for REF_CTRL

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R
[4:2]	VREF_SET	Reference Input Range Control. Set this field to match the reference voltage in use. 0x0: 2.4V ≤ V_{REF} ≤ 2.75V. 0x1: 2.75V < V_{REF} ≤ 3.25V. 0x2: 3.25V < V_{REF} ≤ 3.75V. 0x3: 3.75V < V_{REF} ≤ 4.50V. 0x4: 4.5V < V_{REF} ≤ 5.10V.	0x4	R/W
1	RESERVED	Reserved.	0x0	R/W
0	REFBUF_EN	Reference Buffer Enable Bit. Enables or disables the internal reference buffer. This bit is only active on the WLCSP option. Changing this bit on the LFCSP option has no effect. 0: Disables internal reference buffer. 1: Enables internal reference buffer. (WLCSP only.)	0x0	R/W

Sequencer Control Register

Address: 0x0022, Reset: 0x80, Name: SEQ_CTRL

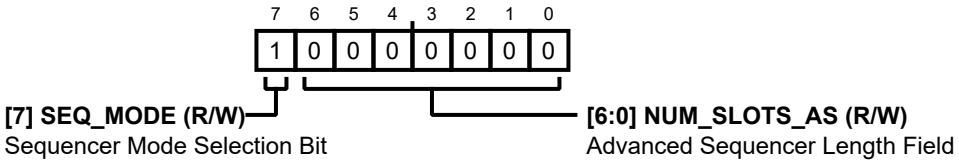


Table 41. Bit Descriptions for SEQ_CTRL

Bits	Bit Name	Description	Reset	Access
7	SEQ_MODE	Sequencer Mode Selection Bit. Selects standard sequencer mode or advanced sequencer mode. 0: Advanced sequencer mode.	0x1	R/W

REGISTER INFORMATION

Table 41. Bit Descriptions for SEQ_CTRL (Continued)

Bits	Bit Name	Description	Reset	Access
[6:0]	NUM_SLOTS_AS	1: Standard sequencer mode. Advanced Sequencer Length Field. Determines the number of slots in the channel sequence when the advanced sequencer mode is selected. The number of slots is equal to NUM_SLOTS_AS + 1, allowing a minimum of 1 slot and a maximum of 128 slots per sequence.	0x0	R/W

Internal Oscillator Frequency Register

Address: 0x0023, Reset: 0x00, Name: OSC_FREQ_REG

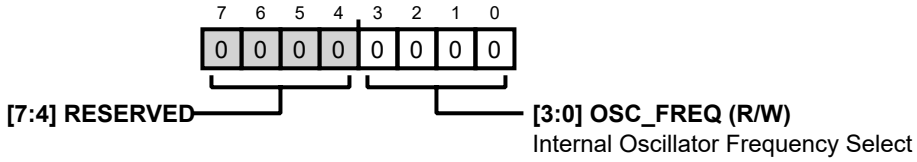


Table 42. Bit Descriptions for OSC_FREQ_REG

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
[3:0]	OSC_FREQ	Internal oscillator frequency select. Selects the nominal frequency of the internal oscillator, and by extension the sampling rate for burst and autonomous modes. 0x0: 1MHz (AD4692) or invalid (AD4691). 0x1: 500kHz. 0x2: 400kHz. 0x3: 250kHz. 0x4: 200kHz. 0x5: 167kHz. 0x6: 133kHz. 0x7: 125kHz. 0x8: 100kHz. 0x9: 50kHz. 0xA: 25kHz. 0xB: 12.5kHz. 0xC: 10kHz. 0xD: 5kHz. 0xE: 2.5kHz. 0xF: 1.25kHz.	0x0	R/W

REGISTER INFORMATION

Standard Sequencer Configuration Register

Address: 0x0025, Reset: 0x0001, Name: STD_SEQ_CONFIG

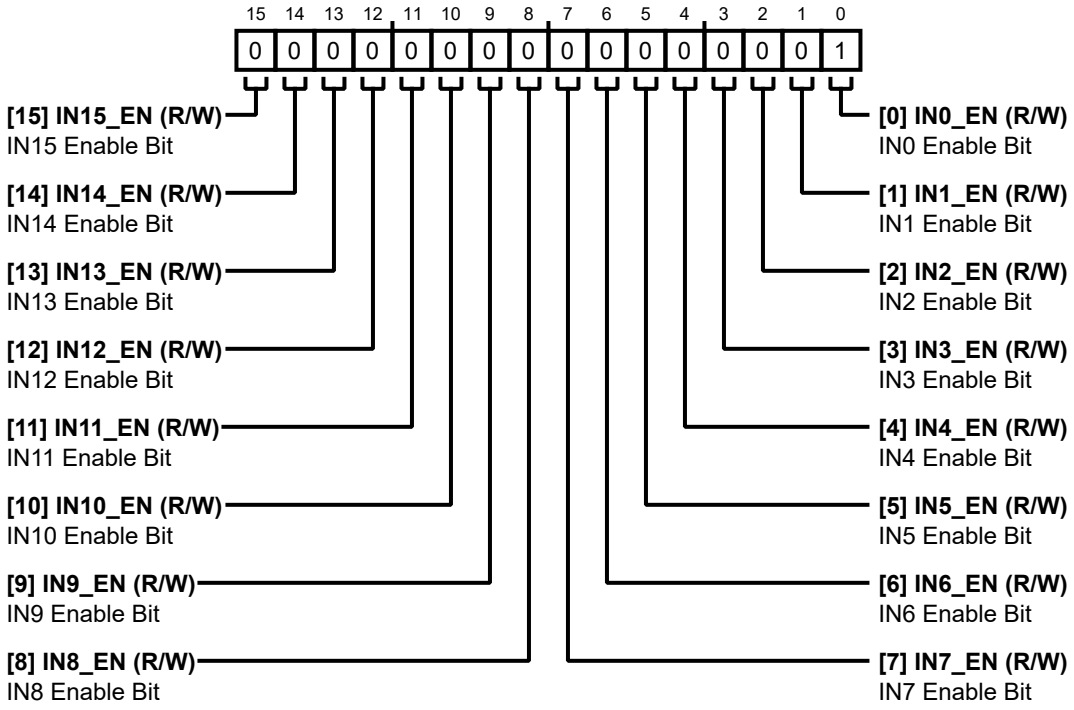


Table 43. Bit Descriptions for STD_SEQ_CONFIG

Bits	Bit Name	Description	Reset	Access
15	IN15_EN	IN15 Standard Sequencer Enable Bit. When this bit is set to 1, IN15 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
14	IN14_EN	IN14 Standard Sequencer Enable Bit. When this bit is set to 1, IN14 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
13	IN13_EN	IN13 Standard Sequencer Enable Bit. When this bit is set to 1, IN13 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
12	IN12_EN	IN12 Standard Sequencer Enable Bit. When this bit set to 1, IN12 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
11	IN11_EN	IN11 Standard Sequencer Enable Bit. When this bit is set to 1, IN11 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
10	IN10_EN	IN10 Standard Sequencer Enable Bit. When this bit is set to 1, IN10 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
9	IN9_EN	IN9 Standard Sequencer Enable Bit. When this bit is set to 1, IN9 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
8	IN8_EN	IN8 Standard Sequencer Enable Bit. When this bit is set to 1, IN8 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
7	IN7_EN	IN7 Standard Sequencer Enable Bit. When this bit is set to 1, IN7 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
6	IN6_EN	IN6 Standard Sequencer Enable Bit. When this bit is set to 1, IN6 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
5	IN5_EN	IN5 Standard Sequencer Enable Bit. When this bit is set to 1, IN5 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W

REGISTER INFORMATION

Table 43. Bit Descriptions for STD_SEQ_CONFIG (Continued)

Bits	Bit Name	Description	Reset	Access
4	IN4_EN	IN4 Standard Sequencer Enable Bit. When this bit is set to 1, IN4 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
3	IN3_EN	IN3 Standard Sequencer Enable Bit. When this bit is set to 1, IN3 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
2	IN2_EN	IN2 Standard Sequencer Enable Bit. When this bit is set to 1, IN2 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
1	IN1_EN	IN1 Standard Sequencer Enable Bit. When this bit is set to 1, IN1 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x0	R/W
0	IN0_EN	IN0 Standard Sequencer Enable Bit. When this bit is set to 1, IN0 is included in the channel sequence when the standard sequencer is enabled (see the Standard Sequencer Mode section).	0x1	R/W

Analog Input Settings Configuration Register

Address: 0x0030 to 0x003F (Increments of 0x0001), Reset: 0x08, Name: CONFIG_INn

Each channel has a corresponding channel configuration register, ranging from CONFIG_IN0 (at Address 0x0030) to CONFIG_IN15 (at Address 0x003F).

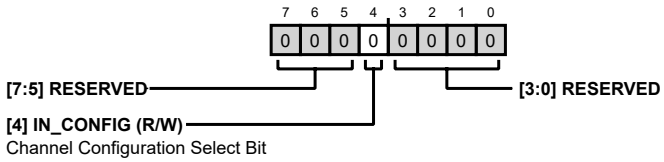


Table 44. Bit Descriptions for CONFIG_INn

Bits	Bit Name	Description	Reset	Access
[7:5]	RESERVED	Reserved.	0x0	R/W
4	IN_N_MODE	Channel Configuration Select Bit. Selects between single-ended and pseudo differential operation. When standard sequencer mode is selected, the IN_N_MODE setting in the CHANNEL_CONFIG0 is applied to all channels. When advanced sequencer mode is selected, the IN_N_MODE setting in each CHANNEL_CONFIGn register is applied independently to each INn channel. 0x0: Single-ended mode. Converts INn with respect to REFGND. 0x1: Pseudo differential mode. Converts INn with respect to COM.	0x0	R/W
[3:0]	RESERVED	Reserved.	0x0	R/W

Advanced Sequencer Slot Register

Address: 0x0100 to Address 0x017F (Increments of 0x0001), Reset: 0x00, Name: AS_SLOTn

Each advanced sequencer slot has a corresponding sequencer slot register, ranging from AS_SLOT0 (at Address 0x0100) to AS_SLOT127 (at Address 0x017F).

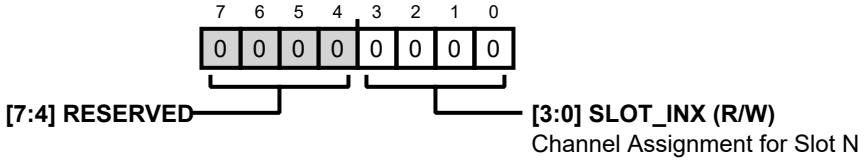


Table 45. Bit Descriptions for AS_SLOTn

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R

REGISTER INFORMATION

Table 45. Bit Descriptions for AS_SLOTn (Continued)

Bits	Bit Name	Description	Reset	Access
[3:0]	SLOT_INX	Channel Assignment for Slot N. Selects which channel (IN0 to IN15) is assigned to slot n (see the Advanced Sequencer Mode section). 0x0: IN0. 0x1: IN1. 0x2: IN2. 0x3: IN3. 0x4: IN4. 0x5: IN5. 0x6: IN6. 0x7: IN7. 0x8: IN8. 0x9: IN9. 0xA: IN10. 0xB: IN11. 0xC: IN12. 0xD: IN13. 0xE: IN14. 0xF: IN15.	0x0	R/W

Internal Oscillator Enable Register

Address: 0x0180, Reset: 0x00, Name: OSC_EN_REG

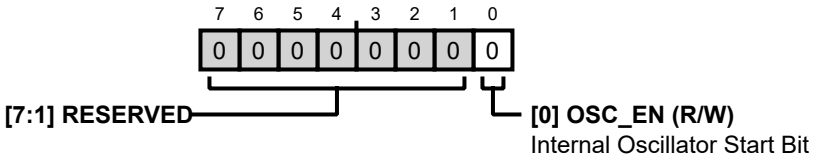


Table 46. Bit Descriptions for OSC_EN_REG

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R
0	OSC_EN	Internal Oscillator Start Bit. Enables and disables the internal burst timer in SPI burst and autonomous modes. In SPI burst mode, writing OSC_EN to 1 starts the burst sampling, and OSC_EN self-clears to 0 at the user-defined stop state. In autonomous mode, writing OSC_EN to 1 starts the autonomous sampling, which runs until the OSC_EN is manually written back to 0. 0: Internal oscillator disabled. 1: Internal oscillator enabled.	0x0	R/W

REGISTER INFORMATION

State Reset Register

Address: 0x0181, Reset: 0x01, Name: STATE_RESET_REG

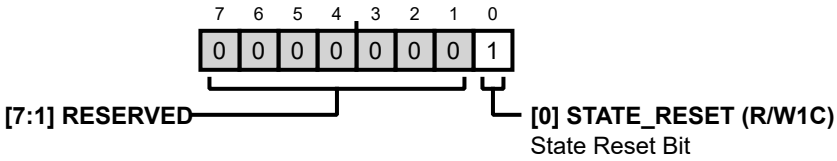


Table 47. Bit Descriptions for STATE_RESET_REG

Bits	Bit Name	Description	Reset	Access
[7:1]	RESERVED	Reserved.	0x0	R/W
0	STATE_RESET	State Reset Bit. Resets the state of the channel sequencer and accumulators. This bit is write-1-to-clear. Setting this bit is mandatory after updating configuration registers related to the channel sequencer and averaging filters to ensure proper device operation.	0x0	R/W

ADC Setup Register

Address: 0x0182, Reset: 0x00, Name: ADC_SETUP

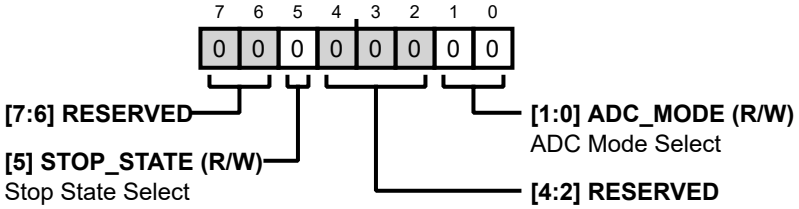


Table 48. Bit Descriptions for ADC_SETUP

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
5	STOP_STATE	Stop State Select. Selects the stop state to be used when CNV burst mode or SPI burst mode are selected. 0: $\overline{\text{EOS}}$ triggers the stop state. 1: $\overline{\text{DRDY}}$ triggers the stop state.	0x0	R/W
[4:2]	RESERVED	Reserved.	0x0	R
[1:0]	ADC_MODE	ADC mode select. 0x0: CNV clock mode. 0x1: CNV burst mode. 0x2: Autonomous mode. 0x3: SPI burst mode.		

REGISTER INFORMATION

Accumulator Mask Register (IN0 to IN7)

Address: 0x0184, Reset: 0xFE, Name: ACC_MASK_1

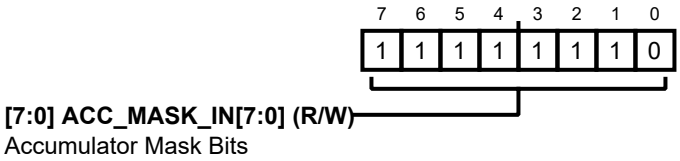


Table 49. Bit Descriptions for ACC_MASK_1

Bits	Bit Name	Description	Reset	Access
[7:0]	ACC_MASK_IN[7:0]	Accumulator Mask Bits. Sets whether the data ready signal from each channels accumulator is masked (disabled) or unmasked (enabled). Each bit in ACC_MASK_IN[15:0] corresponds to one channel. For example, ACC_MASK_IN0 controls the masking of the IN0 accumulator, and so on.	0xFE	R/W

Accumulator Mask Register (IN8 to IN15)

Address: 0x0185, Reset: 0xFF, Name: ACC_MASK_2

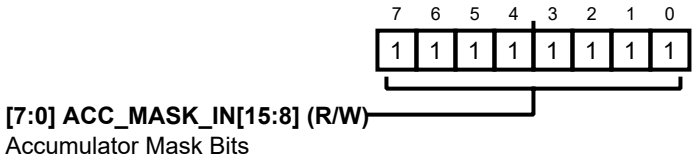


Table 50. Bit Descriptions for ACC_MASK_2

Bits	Bit Name	Description	Reset	Access
[7:0]	ACC_MASK_IN[15:8]	Accumulator Mask Bits. Sets whether the data ready signal from each channels accumulator is masked (disabled) or unmasked (enabled). Each bit in ACC_MASK_IN[15:0] corresponds to one channel. For example ACC_MASK_IN0 controls the masking of the IN0 accumulator, and so on.	0xFF	R/W

Accumulator Depth Registers

Address: 0x0186 to Address 0x0195 (Increments of 0x0001), Reset: 0x3F, Name: ACC_DEPTH_INn

Each channel has a corresponding accumulator depth register, ranging from ACC_DEPTH_IN0 (at Address 0x0186) to ACC_DEPTH_IN15 (at Address 0x0195).

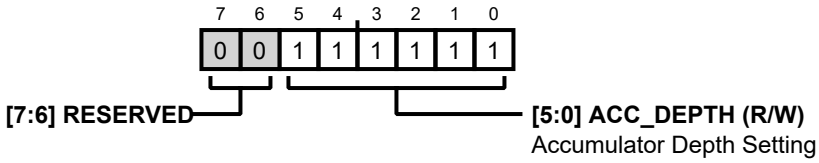


Table 51. Bit Descriptions for ACC_DEPTH_INn

Bits	Bit Name	Description	Reset	Access
[7:6]	RESERVED	Reserved.	0x0	R
[5:0]	ACC_DEPTH	Accumulator Depth Setting. Configures the accumulator full state for the corresponding channels averaging filter. The accumulator full state occurs when the number of samples used to calculate its current output (ACC_COUNT) is equal to	0x3F	R/W

REGISTER INFORMATION

Table 51. Bit Descriptions for ACC_DEPTH_INn (Continued)

Bits	Bit Name	Description	Reset	Access
		ACC_DEPTH + 1. For example, setting ACC_DEPTH = 0x0F configures the accumulator to be full when it has received 16 samples from its corresponding channel. The depth can be set between 1 and 64 samples for each accumulator.		

GP0 and GP1 Control Register

Address: 0x0196, Reset: 0x00, Name: GP0_GP1_MODE

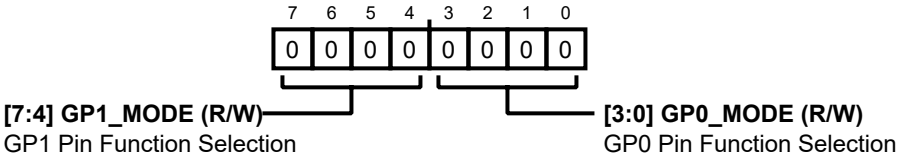
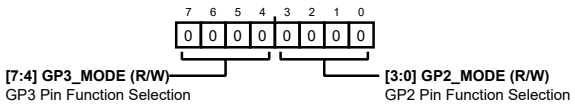


Table 52. Bit Descriptions for GP0_GP1_MODE

Bits	Bit Name	Description	Reset	Access
[7:4]	GP1_MODE	GP1 Pin Function Selection. 0x0: Disabled/high-Z. (Default.) 0x1: Static logic low. 0x2: Static logic high. 0x3: Logic input. 0x4: ADC_BUSY signal. 0x5: $\overline{EOS}$ signal. 0x6: Accumulator data ready signal. 0x7: Accumulator overflow error signal. 0x8: Accumulator saturation error signal. 0x9 to 0xF: Invalid.	0x0	R/W
[3:0]	GP0_MODE	GP0 Pin Function Selection. 0x0: Disabled/high-Z. (Default.) 0x1: Static logic low. 0x2: Static logic high. 0x3: Logic input. 0x4: ADC_BUSY signal. 0x5: $\overline{EOS}$ signal. 0x6: Accumulator data ready signal. 0x7: Accumulator overflow error signal. 0x8: Accumulator saturation error signal. 0x9 to 0xF: Invalid.	0x0	R/W

GP2 and GP3 Control Register

Address: 0x0197, Reset: 0x00, Name: GP2_GP3_MODE



REGISTER INFORMATION

Table 53. Bit Descriptions for GP2_GP3_MODE

Bits	Bit Name	Description	Reset	Access
[7:4]	GP3_MODE	GP3 Pin Function Selection. 0x0: Disabled/high-Z. (Default.) 0x1: Static logic low. 0x2: Static logic high. 0x3: Logic input. 0x4: ADC_BUSY dignal. 0x5: $\overline{EOS}$ dignal. 0x6: Accumulator data ready signal. 0x7: Accumulator overflow error signal. 0x8: Accumulator saturation error signal. 0x9 to 0xF: Invalid.	0x0	R/W
[3:0]	GP2_MODE	GP2 Pin Function Selection. 0x0: Disabled/high-Z. (Default.) 0x1: Static logic low. 0x2: Static logic high. 0x3: Logic input. 0x4: ADC_BUSY signal. 0x5: $\overline{EOS}$ signal. 0x6: Accumulator data ready signal. 0x7: Accumulator overflow error signal. 0x8: Accumulator saturation error signal. 0x9 to 0xF: Invalid.	0x0	R/W

GPIO Logic Input State Register

Address: 0x01A0, Reset: 0x00, Name: GPIO_READ

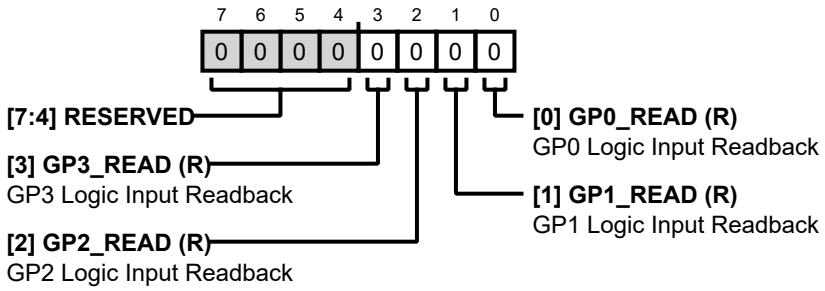


Table 54. Bit Descriptions for GPIO_READ

Bits	Bit Name	Description	Reset	Access
[7:4]	RESERVED	Reserved.	0x0	R
3	GP3_READ	GP3 Logic Input Readback. Indicates the current GP3 logic input signal state. GP3_READ is only valid when GP3 is configured as a logic input with the GP3_MODE setting.	0x0	R
2	GP2_READ	GP2 Logic Input Readback. Indicates the current GP2 logic input signal state. GP2_READ is only valid when GP2 is configured as a logic input with the GP2_MODE setting.	0x0	R
1	GP1_READ	GP1 Logic Input Readback. Indicates the current GP1 logic input signal state. GP1_READ is only valid when GP1 is configured as a logic input with the GP1_MODE setting.	0x0	R

REGISTER INFORMATION

Table 54. Bit Descriptions for GPIO_READ (Continued)

Bits	Bit Name	Description	Reset	Access
0	GP0_READ	GP0 Logic Input Readback. Indicates the current GP0 logic input signal state. GP0_READ is only valid when GP0 is configured as a logic input with the GP0_MODE setting.	0x0	R

Accumulator Full Status Register (IN0 to IN7)

Address: 0x01B0, Reset: 0x00, Name: ACC_STS_FULL_1

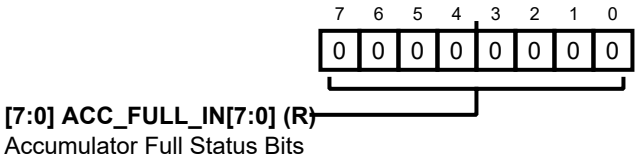


Table 55. Bit Descriptions for ACC_STS_FULL_1

Bits	Bit Name	Description	Reset	Access
[7:0]	ACC_FULL_IN[7:0]	Accumulator Full Status Bits. Indicates the full status for each of the accumulators. The full state occurs when the number of samples in the accumulator is equal to the user-programmed accumulator depth (ACC_DEPTH + 1). The ACC_FULL_IN[15:0] bits read back 0 or 1 when their corresponding channel's accumulator is not full or full, respectively.	0x0	R

Accumulator Full Status Register (IN8 to IN15)

Address: 0x01B1, Reset: 0x00, Name: ACC_STS_FULL_2

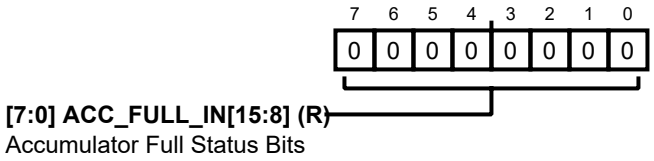
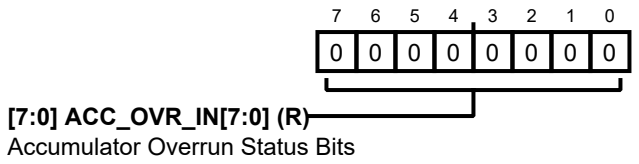


Table 56. Bit Descriptions for ACC_STS_FULL_2

Bits	Bit Name	Description	Reset	Access
[7:0]	ACC_FULL_IN[15:8]	Accumulator Full Status Bits. Indicates the full status for each of the accumulators. The full state occurs when the number of samples in the accumulator is equal to the user-programmed accumulator depth (ACC_DEPTH + 1). The ACC_FULL_IN[15:0] bits read back 0 or 1 when their corresponding channel's accumulator is not full or full, respectively.	0x0	R

Accumulator Overrun Status Register (IN0 to IN7)

Address: 0x01B2, Reset: 0x00, Name: ACC_STS_OVR_1



REGISTER INFORMATION

Table 57. Bit Descriptions for ACC_STS_OVR_1

Bits	Bit Name	Description	Reset	Access
[7:0]	ACC_OVR_IN[7:0]	Accumulator Overrun Status Bits. Indicates the overrun status for each of the accumulators. An overrun occurs when the ADC core attempts to write a new sample into the accumulator while it is already in the full state, resulting in that sample being ignored. The ACC_OVR_IN[15:0] bits read back 0 or 1 when their corresponding channel's accumulator experienced an overrun event since the most recent state reset.	0x0	R

Accumulator Overrun Status Register (IN8 to IN15)

Address: 0x01B3, Reset: 0x00, Name: ACC_STS_OVR_2

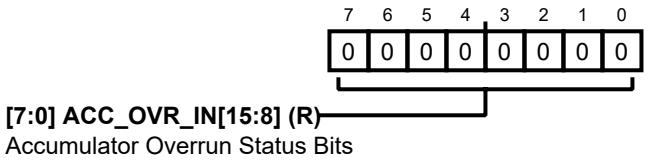


Table 58. Bit Descriptions for ACC_STS_OVR_2

Bits	Bit Name	Description	Reset	Access
[7:0]	ACC_OVR_IN[15:8]	Accumulator Overrun Status Bits. Indicates the overrun status for each of the accumulators. An overrun occurs when the ADC core attempts to write a new sample into the accumulator while it is already in the full state, resulting in that sample being ignored. The ACC_OVR_IN[15:0] bits read back 0 or 1 when their corresponding channel's accumulator experienced an overrun event since the most recent state reset.	0x0	R

Accumulator Saturation Status Register (IN0 to IN7)

Address: 0x01B4, Reset: 0x00, Name: ACC_STS_SAT_1

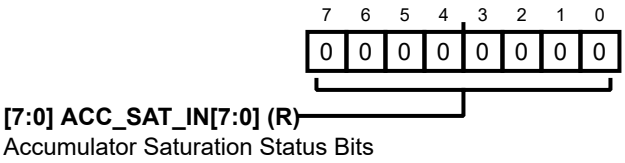


Table 59. Bit Descriptions for ACC_STS_SAT_1

Bits	Bit Name	Description	Reset	Access
[7:0]	ACC_SAT_IN[7:0]	Accumulator Saturation Status Bits. Indicates whether a saturation error occurred for each of the accumulators. A saturation error occurs when any of the samples input to the accumulator were at negative full scale or positive full scale, indicating the potential presence of ADC saturation during the accumulation. The ACC_SAT_IN[15:0] bits read back 1 when a saturation error occurred since the most recent state reset.	0x0	R

REGISTER INFORMATION

Accumulator Saturation Status Register (IN8 to IN15)

Address: 0x01B5, Reset: 0x00, Name: ACC_STS_SAT_2

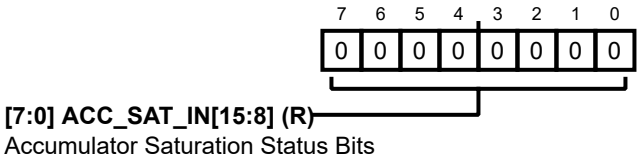


Table 60. Bit Descriptions for ACC_STS_SAT_2

Bits	Bit Name	Description	Reset	Access
[7:0]	ACC_SAT_IN[15:8]	Accumulator Saturation Status Bits. Indicates whether a saturation error occurred for each of the accumulators. A saturation error occurs when any of the samples input to the accumulator were at negative full scale or positive full scale, indicating the potential presence of ADC saturation during the accumulation. The ACC_SAT_IN[15:0] bits read back 1 when a saturation error occurred since the most recent state reset.	0x0	R

Accumulator General Status Registers

Address: 0x01C0 to Address: 0x01CF (Increments of 0x0001), Reset: 0x00, Name: ACC_STATUS_INn

Each channel has a corresponding accumulator status register, ranging from ACC_STATUS_IN0 (at Address 0x01C0) to ACC_STATUS_IN15 (at Address 0x01CF).

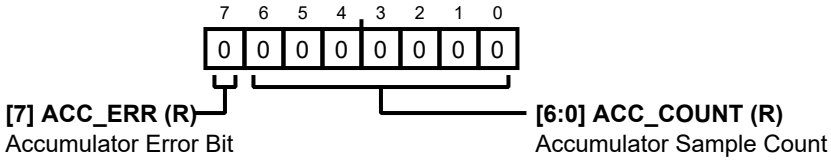


Table 61. Bit Descriptions for ACC_STATUS_INn

Bits	Bit Name	Description	Reset	Access
7	ACC_ERR	Accumulator Error Bit. Indicates when the corresponding channel's accumulator has experienced an overrun or saturation error. The ACC_ERR bit for each channel n is equal to the logical OR of the ACC_STS_SAT[n] bit and the ACC_STS_OVR[n] bit.	0x0	R
[6:0]	ACC_COUNT	Accumulator Sample Count. Indicates the number of samples used to calculate the corresponding accumulators current output. ACC_COUNT increments each time the ADC core generates a new sample from its corresponding analog input channel, up until ACC_COUNT reaches the user-programmed depth setting and reaches its full state (when ACC_COUNT = ACC_DEPTH − 1).	0x00	R

REGISTER INFORMATION

Averaging Filter Data Registers

Address: 0x0201 to Address 0x021F (Increments of 0x0002), Reset: 0x0000, Name: AVG_INn

Each channel has a corresponding 16-bit averaged data register, ranging from AVG_IN0 (at Address 0x0201) to AVG_IN15 (at Address 0x021F).

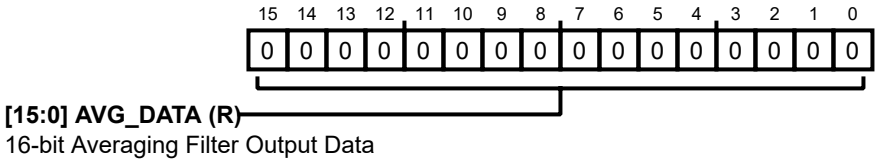


Table 62. Bit Descriptions for AVG_INn

Bits	Bit Name	Description	Reset	Access
[15:0]	AVG_DATA	16-bit Averaging Filter Output Data. Returns the current averaging filter output data.	0x0000	R

Averaging Filter Data Plus Status Registers

Address: 0x0222 to Address 0x024F (Increments of 0x0003), Reset: 0x000000, Name: AVG_STS_INn

Each channel has a corresponding 16-bit averaged data plus status register, ranging from AVG_STS_IN0 (at Address 0x0222) to AVG_STS_IN15 (at Address 0x024F).

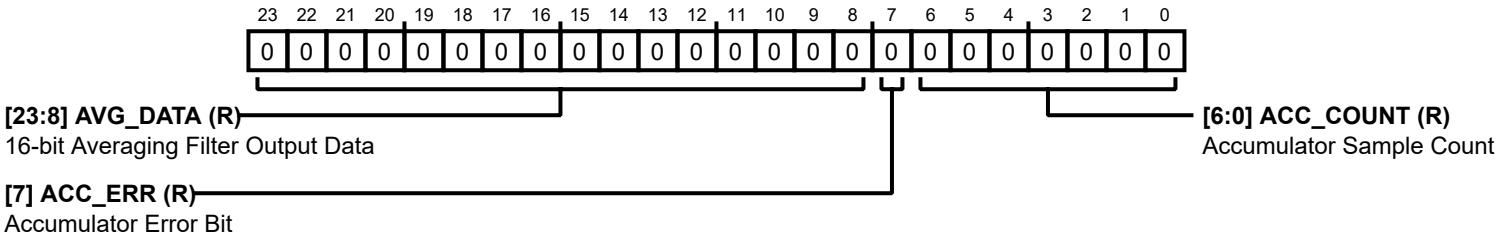


Table 63. Bit Descriptions for AVG_STS_INn

Bits	Bit Name	Description	Reset	Access
[23:8]	AVG_DATA	16-bit Averaging Filter Output Data. Returns the current averaging filter output data.	0x0000	R
[7]	ACC_ERR	Accumulator Error Bit. Indicates when the corresponding channel's accumulator has experienced an overrun or saturation error. The ACC_ERR bit for each channel n is equal to the logical OR of the ACC_STS_SAT[n] bit and the ACC_STS_OVR[n] bit.	0x0	R
[6:0]	ACC_COUNT	Accumulator Sample Count. Indicates the number of samples used to calculate the corresponding accumulator's current output. ACC_COUNT increments each time the ADC core generates a new sample from its corresponding analog input channel, up until ACC_COUNT reaches the user-programmed depth setting and reaches its full state (when ACC_COUNT = ACC_DEPTH − 1).	0x00	R

REGISTER INFORMATION

Accumulator Data Registers

Address: 0x0252 to Address 0x027F (Increments of 0x0003), Reset: 0x000000, Name: ACC_INn

Each channel has a corresponding 24-bit accumulator data register, ranging from ACC_IN0 (at Address 0x0252) to ACC_IN15 (at Address 0x027F).

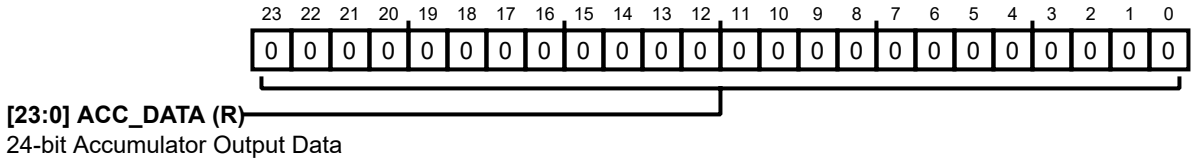


Table 64. Bit Descriptions for ACC_INn

Bits	Bit Name	Description	Reset	Access
[23:0]	ACC_DATA	24-bit Accumulator Output Data. Returns the current accumulator output data.	0x000000	R

Accumulator Data Plus Status Registers

Address: 0x0283 to Address 0x02BF (Increments of 0x0004), Reset: 0x00000000, Name: ACC_STS_INn

Each channel has a corresponding 32-bit accumulator data register, ranging from ACC_STS_IN0 (at Address 0x0283) to ACC_STS_IN15 (at Address 0x02BF).

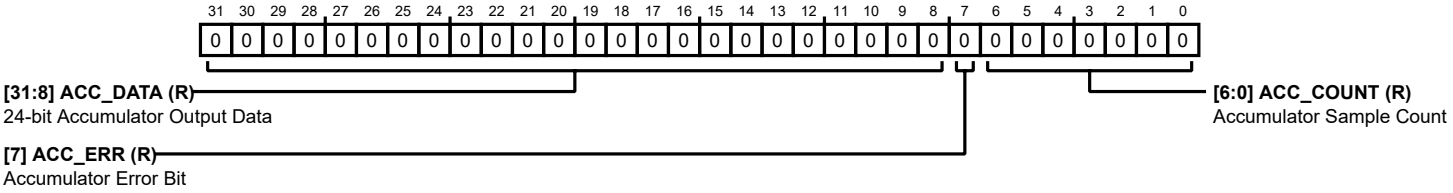


Table 65. Bit Descriptions for ACC_STS_INn

Bits	Bit Name	Description	Reset	Access
[31:8]	ACC_DATA	24-bit Accumulator Output Data. Returns the current accumulator output data.	0x000000	R
[7]	ACC_ERR	Accumulator Error Bit. Indicates when the corresponding channel's accumulator has experienced an overrun or saturation error. The ACC_ERR bit for each channel n is equal to the logical OR of the ACC_STS_SAT[n] bit and the ACC_STS_OVR[n] bit.	0x0	R
[6:0]	ACC_COUNT	Accumulator Sample Count. Indicates the number of samples used to calculate the corresponding accumulator's current output. ACC_COUNT increments each time the ADC core generates a new sample from its corresponding analog input channel, up until ACC_COUNT reaches the user-programmed depth setting and reaches its full state (when ACC_COUNT = ACC_DEPTH − 1).	0x00	R

OUTLINE DIMENSIONS

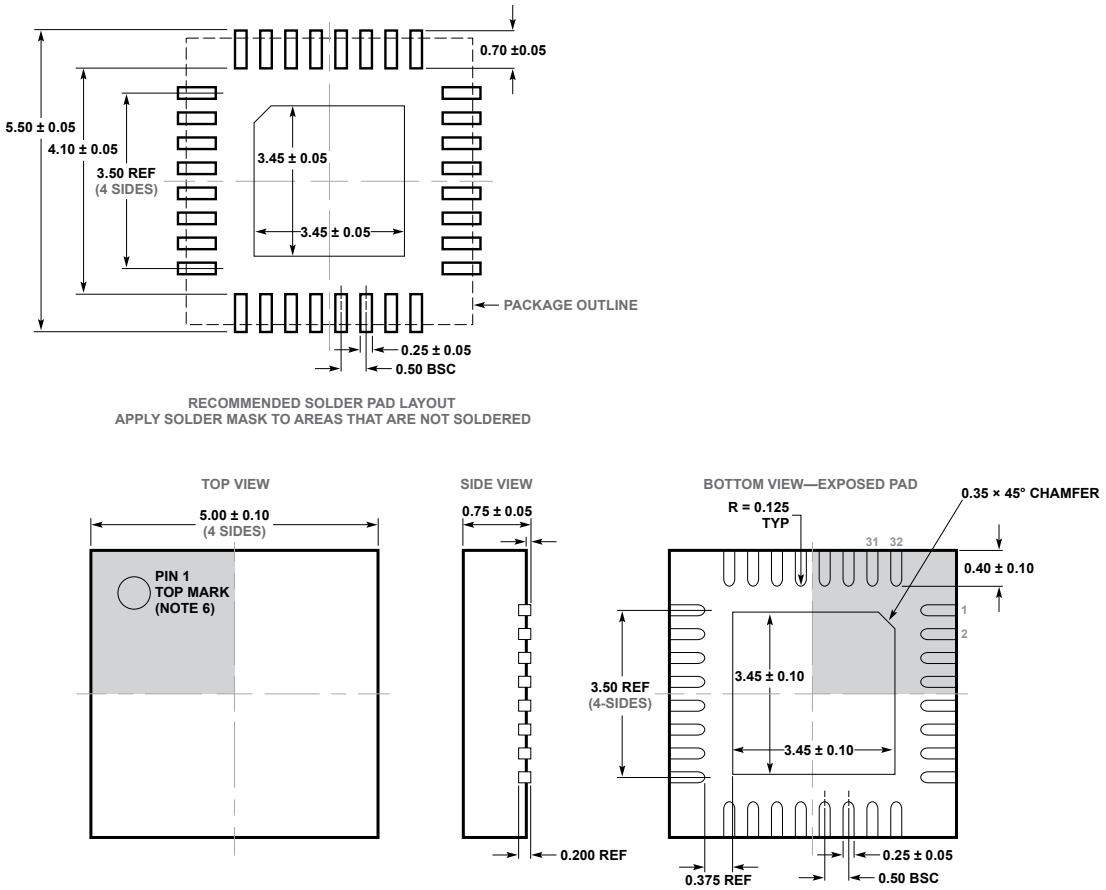


Figure 102. 32-Lead Lead Frame Chip Scale Package [LFCSP]
5mm × 5mm Body and 0.75mm Package Height
(CP-32-39)
Dimensions shown in millimeters

OUTLINE DIMENSIONS

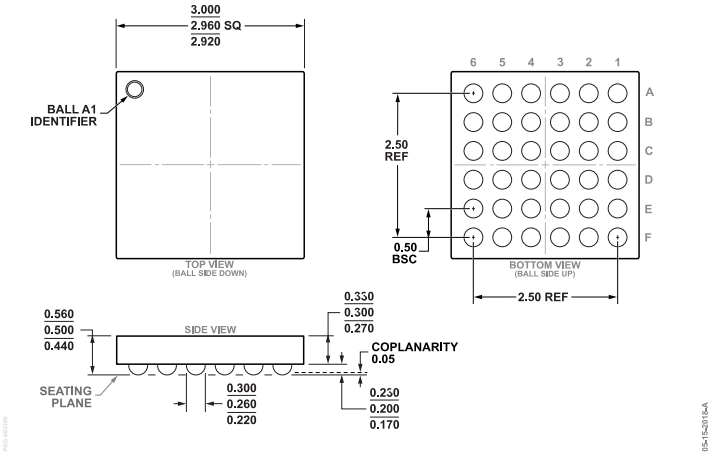


Figure 103. 36-Ball Wafer Level Chip Scale Package (WLCSP)
(CB-36-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4691BCBZ-RL7	−40°C to +125°C	36-Ball WLCSP (2.96mm × 2.96mm × 0.50mm)	Reel, 1500	CB-36-5
AD4691BCPZ	−40°C to +125°C	32-Lead LFCSP (5mm × 5mm w/ EP)	Tray, 490	CP-32-39
AD4691BCPZ-RL7	−40°C to +125°C	32-Lead LFCSP (5mm × 5mm w/ EP)	Reel, 1500	CP-32-39
AD4692BCBZ-RL7	−40°C to +125°C	36-Ball WLCSP (2.96mm × 2.96mm × 0.50mm)	Reel, 1500	CB-36-5
AD4692BCPZ	−40°C to +125°C	32-Lead LFCSP (5mm × 5mm w/ EP)	Tray, 490	CP-32-39
AD4692BCPZ-RL7	−40°C to +125°C	32-Lead LFCSP (5mm × 5mm w/ EP)	Reel, 1500	CP-32-39

[1] Z = RoHS Compliant Part.