4-/8-Channel, 125kSPS, 16-Bit, Sigma Delta ADC with ±10V Inputs, Open-Wire Detection

FEATURES

- ±10V inputs, 4 differential or 8 single-ended
  - Absolute input pin voltage up to ±20V
  - Minimum 1MΩ impedance
- Fully integrated solution
  - 16-bit ADC with integrated AFE
  - Fast and flexible output rate: 2.5SPS to 125,000SPS
  - Channel scan data rate 24.845kSPS/channel (40.25µs settling)
    - 14.4 noise free bits at 24.845kSPS per channel
    - 16 noise free bits at 4.994kSPS per channel
  - Simultaneous 50Hz and 60Hz rejection
  - On-chip, 2.5V reference and reference buffers
    - ±5ppm/°C drift (typical)
  - Internal clock oscillator
- Power supplies
  - AVDD = 4.5V to 5.5V or ±2.5V
  - IOVDD = 2V to 5.5V
  - Total current consumption AVDD + IOVDD (I_{DD}) = 10.8mA
- Temperature range: −40°C to +105°C
- 40-lead, 6mm × 6mm LFCSP
- 3-wire or 4-wire serial digital interface
  - SPI, QSPI, MICROWIRE, and DSP-compatible
  - Schmitt trigger on SCLK

APPLICATIONS

- Process control
  - PLC/DCS modules
  - Instrumentation and measurement

PRODUCT HIGHLIGHTS

- Integrated matched attenuation resistors removing the need for channel-to-channel calibration
- Guaranteed TUE, ±0.08% at 25°C
- Overvoltage protected up to ±65V
- Single supply operation eliminates the cost for external bipolar supplies and extra isolation
- Optimizes overall system cost
- Open-wire detection

FUNCTIONAL BLOCK DIAGRAM

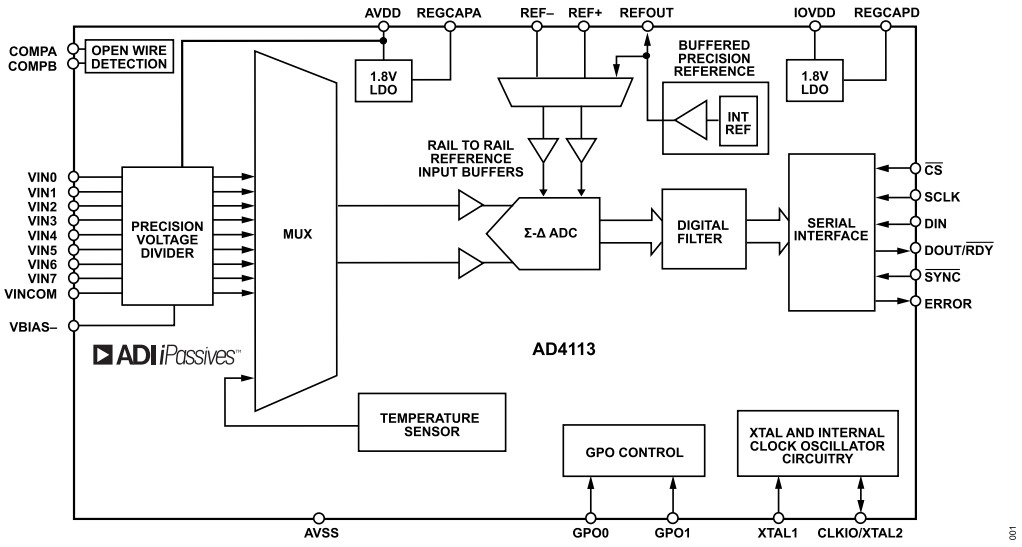

Figure 1. AD4113 Functional Block Diagram

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REVISION HISTORY

4/2026—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD4113 is a low power, low noise, 16-bit, Σ-Δ analog-to-digital converter (ADC) that integrates an analog front end (AFE) for four fully-differential or eight single-ended inputs.

The precision performance of the AD4113 is achieved by integrating the proprietary *i*Passives™ technology from Analog Devices, Inc. The AD4113 has high impedance (≥1MΩ) and can accommodate ±10V true bipolar voltage inputs at a maximum channel scan rate of 24.845kSPS (40.25µs) for fully settled data. The output data rates range from 2.5SPS to 125,000SPS.

The AD4113 also integrates key analog and digital signal conditioning blocks to configure eight individual setups for each analog input channel in use. As many as 16 channels can be enabled at any time, a channel being defined as any of the standard analog voltage input. The embedded 2.5V (5ppm/°C) band gap internal reference (with output reference buffer) reduces the external component count.

The digital filter allows flexible settings, which include simultaneous 50Hz and 60Hz rejection at a 27.27SPS output data rate. The user can select between the different filter settings depending on the demands of each channel in the application. The automatic channel sequencer enables the ADC to switch through each enabled channel.

The AD4113 operates with a single 5V power supply, which makes the device easy to use in galvanically isolated applications. The specified operating temperature range is −40°C to +105°C. The AD4113 is housed in a 40-lead, 6mm × 6mm LFCSP.

SPECIFICATIONS

AVDD = 4.5V to 5.5V, IOVDD = 2V to 5.5V, AVSS = 0V, DGND = 0V, VBIAS− = 0V, unless otherwise noted.

Internal reference, internal MCLK = 8MHz, and T_A = minimum temperature (T_{MIN}) to maximum temperature (T_{MAX}) (−40°C to +105°C), unless otherwise noted.

Table 1. Specifications

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
VOLTAGE INPUTS					
Differential Input Voltage Range[1]	Specified TUE performance	−10		+10	V
	Functional	$-V_{REF}$ × 10		$+V_{REF}$ × 10	V
Absolute (Pin) Input Voltage		−20		+20	V
Input Impedance		1	1.17		MΩ
Offset Error[2]	25°C		±1.5		mV
Offset Drift			±8		µV/°C
Gain Error			±0.05		% of FS
Gain Drift	Excludes internal reference		±1		ppm/°C
Integral Nonlinearity (INL)			±0.01		% of FSR
Total Unadjusted Error (TUE)[3]					
	+25°C, internal V_{REF}			±0.08	% of FSR
	−20°C to +85°C, internal V_{REF}			±0.1	% of FSR
	−40°C to +105°C, internal V_{REF}			±0.12	% of FSR
	+25°C, external V_{REF}			±0.07	% of FSR
	−40°C to +105°C, external V_{REF}			±0.08	% of FSR
Power Supply Rejection	AVDD for input voltage (V_{IN}) = 1V		70		dB
Common-Mode Rejection	V_{IN} = 1V				
At DC			85		dB
At 50Hz, 60Hz	20Hz output data rate (postfilter), 50Hz ± 1Hz and 60Hz ± 1Hz		120		dB
Normal Mode Rejection[3]	50Hz ± 1Hz and 60Hz ± 1Hz				
	Internal clock, 20SPS output data rate (ODR) (postfilter)	71	90		dB
	External clock, 20SPS ODR (postfilter)	85	90		dB
Resolution	See Table 7 and Table 8				
Noise	See Table 7 and Table 8				
ADC SPEED AND PERFORMANCE					
ADC ODR		2.5		125,000	SPS
No Missing Codes[3]		16			Bits
INTERNAL REFERENCE	100nF external capacitor to AVSS				
Output Voltage	REFOUT with respect to AVSS		2.5		V
Initial Accuracy[3, 4]	REFOUT, T_A = 25°C	−0.12		+0.12	% of V
Temperature Coefficient			±5	+12	ppm/°C
Reference Load Current (I_{LOAD})		−10		+10	mA
Power Supply Rejection	AVDD (line regulation)		95		dB
Load Regulation	Change in output voltage (ΔV_{OUT})[5]/change in load current (ΔI_{LOAD})		32		ppm/mA
Voltage Noise	Voltage noise (e_N), 0.1Hz to 10Hz, 2.5V reference		4.5		µV rms
Voltage Noise Density	e_N, 1kHz, 2.5V reference		215		nV/√Hz
Turn On Settling Time	100nF REFOUT capacitor		200		µs
Short-Circuit Current (I_{SC})			25		mA
EXTERNAL REFERENCE INPUTS					
Differential Input Range	V_{REF} = (REF+) − (REF−)	1	2.5	AVDD	V
Absolute Voltage Limits					
Buffers Disabled		AVSS − 0.05		AVDD + 0.05	V
Buffers Enabled		AVSS		AVDD	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
REF± Input Current					
Buffers Disabled					
Input Current			±36		µA/V
Input Current Drift	External clock		±1.2		nA/V/°C
	Internal clock		±3		nA/V/°C
Buffers Enabled					
Input Current			±400		nA
Input Current Drift			0.6		nA/°C
Normal Mode Rejection	See the Rejection parameter				
Common-Mode Rejection			95		dB
Temperature Sensor					
Accuracy	After user calibration at 25°C		±2		°C
Sensitivity			477		µV/K
GENERAL-PURPOSE OUTPUTS (GPO0, GPO1)	With respect to AVSS				
Floating State Output Capacitance			5		pF
Output Voltage[3]					
High, (V_{OH})	Source current (I_{SOURCE}) = 200µA	AVDD − 1			V
Output Low Voltage, (V_{OL})	Sink current (I_{SINK}) = 800µA			AVSS + 0.4	V
CLOCK					
Internal Clock					
Frequency			8		MHz
Accuracy		−2.5%		+2.5%	%
Duty Cycle			50		%
Output Voltage					
High (V_{OH})		0.8 × IOVDD			V
Low (V_{OL})				0.4	V
Crystal					
Frequency		14	16	16.384	MHz
Start-Up Time			10		µs
External Clock (CLKIO)			8	8.192	MHz
Duty Cycle		30	50	70	%
LOGIC INPUTS					
Input Voltage[3]					
High (V_{INH})	2V ≤ IOVDD < 2.3V	0.65 × IOVDD			V
	2.3V ≤ IOVDD ≤ 5.5V	0.7 × IOVDD			V
Low (V_{INL})	2V ≤ IOVDD < 2.3V			0.35 × IOVDD	V
	2.3V ≤ IOVDD ≤ 5.5V			0.7	V
Hysteresis	IOVDD ≥ 2.7V	0.08		0.25	V
	IOVDD < 2.7V	0.04		0.2	V
Leakage Current		−10		+10	µA
LOGIC OUTPUT (DOUT/$\overline{RDY}$)					
Output Voltage[3]					
V_{OH}	IOVDD ≥ 4.5V, I_{SOURCE} = 1mA	0.8 × IOVDD			V
	2.7V ≤ IOVDD < 4.5V, I_{SOURCE} = 500µA	0.8 × IOVDD			V
	IOVDD < 2.7V, I_{SOURCE} = 200µA	0.8 × IOVDD			V
V_{OL}	IOVDD ≥ 4.5V, I_{SINK} = 2mA			0.4	V
	2.7V ≤ IOVDD < 4.5V, I_{SINK} = 1mA			0.4	V

SPECIFICATIONS

Table 1. Specifications (Continued)

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
	IOVDD < 2.7V, I_{SINK} = 400µA			0.4	V
Leakage Current[3]	Floating state	−10		+10	µA
Output Capacitance	Floating state		10		pF
POWER REQUIREMENTS					
Power Supply Voltage					
AVDD to AVSS		4.5		5.5	V
AVSS to DGND		−2.75		0	V
IOVDD to DGND		2		5.5	V
IOVDD to AVSS	For AVSS < DGND			6.35	V
POWER SUPPLY CURRENTS[6]	All outputs unloaded, digital inputs connected to IOVDD or DGND				
Full Operating Mode					
AVDD Current	Including internal reference		9.4	11.5	mA
IOVDD Current	Internal clock		1.4	1.8	mA
Standby Mode	All V_{IN} = 0V		210		µA
Power-Down Mode	All V_{IN} = 0V		185		µA
Total Current Consumption (I_{DD})			10.8		mA
POWER DISSIPATION					
Full Operating Mode			52		mW
Standby Mode			1		mW
Power-Down Mode			925		µW

[1] The full specification is guaranteed for a differential input signal of ±10V. The device is functional up to a differential input signal of ±VREF × 10. However, the specified absolute (pin) voltage must not be exceeded for the proper function.

[2] Following a system zero-scale calibration, the offset error is in the order of the noise for the programmed output data rate selected.

[3] Specification is not production tested but is supported by characterization data at the initial product release.

[4] This specification includes moisture sensitivity level (MSL) preconditioning effects.

[5] V_{OUT} is the output voltage.

[6] This specification is with no load on the REFOUT pin and the digital output pins.

TIMING CHARACTERISTICS

IOVDD = 2V to 5.5V, DGND = 0V, Input Logic 0 = 0V, Input Logic 1 = IOVDD, and load capacitance (C_{LOAD}) = 20pF, unless otherwise noted.

Table 2. Timing Characteristics

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description[1, 2]
SCLK			
t_3	25	ns minimum	SCLK high pulse width
t_4	25	ns minimum	SCLK low pulse width
READ OPERATION			
t_1	0	ns minimum	$\overline{CS}$ falling edge to DOUT/$\overline{RDY}$ active time
	15	ns maximum	IOVDD = 4.75V to 5.5V
	40	ns maximum	IOVDD = 2V to 3.6V
t_2[3]	0	ns minimum	SCLK active edge to data valid delay[4]
	12.5	ns maximum	IOVDD = 4.75V to 5.5V
	25	ns maximum	IOVDD = 2V to 3.6V
t_5[5]	2.5	ns minimum	Bus relinquish time after $\overline{CS}$ inactive edge
	20	ns maximum	
t_6	0	ns minimum	SCLK inactive edge to $\overline{CS}$ inactive edge
t_7	10	ns minimum	SCLK inactive edge to DOUT/$\overline{RDY}$ high/low

SPECIFICATIONS

Table 2. Timing Characteristics (Continued)

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Description[1, 2]
WRITE OPERATION			
t_8	0	ns minimum	$\overline{CS}$ falling edge to SCLK active edge setup time[4]
t_9	8	ns minimum	Data valid to SCLK edge setup time
t_{10}	8	ns minimum	Data valid to SCLK edge hold time
t_{11}	5	ns minimum	$\overline{CS}$ rising edge to SCLK edge hold time

1 Sample tested during initial release to ensure compliance.

2 See Figure 2 and Figure 3.

3 This parameter is defined as the time required for the output to cross the V_{OL} or V_{OH} limits.

4 The SCLK active edge is the falling edge of SCLK.

5 DOUT/ $\overline{RDY}$ returns high after a read of the data register. In single-conversion and continuous conversion modes, the same data can be read again, if required, while DOUT/ $\overline{RDY}$ is high. However, care must be taken to ensure that subsequent reads do not occur close to the next output update. If the continuous read feature is enabled, the digital word can be read only once.

TIMING DIAGRAMS

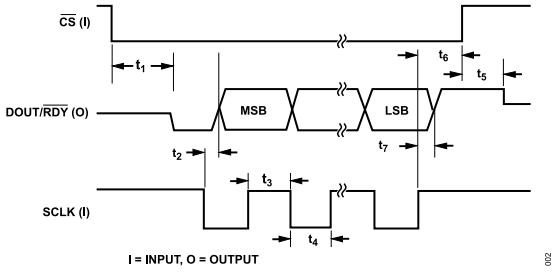


Figure 2. Read Cycle Timing Diagram

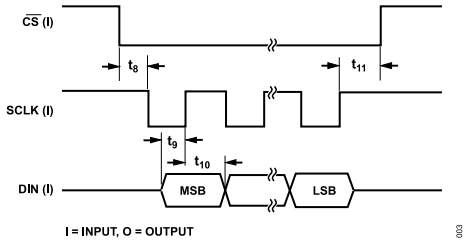


Figure 3. Write Cycle Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3. Absolute Maximum Ratings

Parameter	Rating
AVDD to AVSS	−0.3V to +6.5V
AVDD to DGND	−0.3V to +6.5V
IOVDD to DGND	−0.3V to +6.5V
IOVDD to AVSS	−0.3V to +7.5V
AVSS to DGND	−3.25V to +0.3V
Voltage Inputs (VINx) Voltage to AVSS	−65V to +65V
Reference Input Voltage to AVSS	−0.3V to AVDD + 0.3V
Digital Input Voltage to DGND	−0.3V to IOVDD + 0.3V
Digital Output Voltage to DGND	−0.3V to IOVDD + 0.3V
Digital Input Current	10mA
Temperature	
Operating Range	−40°C to +105°C
Storage Range	−65°C to +150°C
Maximum Junction	150°C
Lead Soldering, Reflow	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction-to-ambient thermal resistance measured in a one cubic foot sealed enclosure.

θ_{JC} is the junction-to-case thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
CP-40-15[1]	34[2]	2.63[3]	°C/W

1 4-Layer JEDEC PCB.

2 Thermal impedance simulated values are based on JEDEC 2S2P thermal test PCB with 16 thermal vias. θ_{JA} is specified for a device soldered on a JEDEC test PCB for surface-mount packages. For more details, refer to the JEDEC JESD51.

3 A cold plate is attached to the PCB bottom and measured at the exposed paddle.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for AD4113

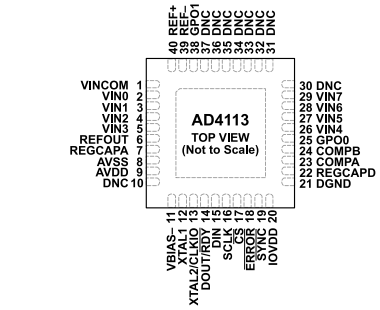
Table 5. AD4113, 40-Lead LFCSP

ESD Model	Withstand Threshold (v)	Class
HBM	±1000	1C
CDM	±1250	C3

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS



NOTES
1. DNC = DO NOT CONNECT. DO NOT CONNECT ANYTHING TO THIS PIN.
2. EXPOSED PAD. SOLDER THE EXPOSED PAD TO A SIMILAR PAD ON THE PCB UNDER THE EXPOSED PAD TO CONFER MECHANICAL STRENGTH TO THE PACKAGE AND FOR HEAT DISSIPATION. THE EXPOSED PAD MUST BE CONNECTED TO AVSS THROUGH THIS PAD ON THE PCB.

004

Figure 4. Pin Configuration

Table 6. Pin Function Descriptions

Pin Number	Mnemonic[1]	Type[2]	Description
1	VINCOM	AI	Voltage Input Common. Voltage inputs are referenced to this pin in single-ended configuration. Connect this pin to analog ground.
2	VIN0	AI	Voltage Input 0. Input referenced to VINCOM in single-ended configuration or a positive input of an input pair with VIN1 in differential configuration.
3	VIN1	AI	Voltage Input 1. Input referenced to VINCOM in single-ended configuration or a negative input of an input pair with VIN0 in differential configuration.
4	VIN2	AI	Voltage Input 2. Input referenced to VINCOM in single-ended configuration or a positive input of an input pair with VIN3 in differential configuration.
5	VIN3	AI	Voltage Input 3. Input referenced to VINCOM in single-ended configuration or a negative input of an input pair with VIN2 in differential configuration.
6	REFOUT	AO	Buffered Output of Internal Reference. The output is 2.5V with respect to AVSS. Decouple this pin to AVSS by a 0.1µF capacitor.
7	REGCAPA	AO	Analog Low Dropout (LDO) Regulator Output. Decouple this pin to AVSS by a 1µF capacitor.
8	AVSS	P	Negative Analog Supply. This supply ranges from −2.75V to 0V and is nominally set to 0V.
9	AVDD	P	Analog Supply Voltage. This voltage ranges from 4.5V to 5.5V with respect to AVSS.
10, 30 to 37	DNC	N/A	Do Not Connect. Do not connect anything to this pin.
11	VBIAS−	AI	Voltage Bias Negative. The pin is setting bias voltage for the voltage input analog front-end. Connect this pin to AVSS.
12	XTAL1	AI	Input 1 for Crystal.
13	XTAL2/CLKIO	AI/DI	Input 2 for Crystal (XTAL2)/Clock Input or Output (CLKIO). For more details, see the CLOCKSEL bit settings in the ADC Mode Register.
14	DOUT/$\overline{\text{RDY}}$	DO	Serial Data Output (DOUT)/Data Ready Output ($\overline{\text{RDY}}$). This pin serves a dual purpose. This pin functions as a serial data output pin to access the output shift register of the ADC. The output shift register can contain data from any of the on-chip data or control registers. The data word/control word information is placed on the DOUT/$\overline{\text{RDY}}$ pin on the SCLK falling edge and is valid on the SCLK rising edge. When $\overline{\text{CS}}$ is high, the DOUT/$\overline{\text{RDY}}$ output is tristated. When $\overline{\text{CS}}$ is low, and a register is not being read, DOUT/$\overline{\text{RDY}}$ operates as a data ready pin, going low to indicate the completion of a conversion. If the data is not read after the conversion, the pin goes high before the next update occurs. The DOUT/$\overline{\text{RDY}}$ falling edge can be used as an interrupt to a processor, which indicates that the valid data is available.
15	DIN	DI	Serial Data Input to the Input Shift Register on the ADC. Data in this shift register is transferred to the control registers in the ADC, with the register address (RA) bits of the communications register identifying the appropriate register. Data is clocked in on the rising edge of SCLK.
16	SCLK	DI	Serial Clock Input. This serial clock input is for data transfers to and from the ADC. SCLK has a Schmitt triggered input, which makes the interface suitable for opto-isolated applications.
17	$\overline{\text{CS}}$	DI	Chip Select Input. This pin is an active low logic input used to select the ADC. Use $\overline{\text{CS}}$ to select the ADC in systems with more than one device on the serial bus. $\overline{\text{CS}}$ can be hardwired low, which allows the ADC to operate in 3-wire

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 6. Pin Function Descriptions (Continued)

Pin Number	Mnemonic[1]	Type[2]	Description
			mode with SCLK, DIN, and DOUT/$\overline{RDY}$ used to interface with the device. When $\overline{CS}$ is high, the DOUT/$\overline{RDY}$ output is tristated.
18	$\overline{ERROR}$	DI/O	Error Input/Output or General-Purpose Output. This pin can be used in one of the following three modes: Active low error input mode. This mode sets the ADC_ERROR bit in the status register. Active low, open-drain error output mode. The status register error bits are mapped to the $\overline{ERROR}$ pin. The $\overline{ERROR}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed. General-purpose output mode. The status of the pin is controlled by the ERR_DAT bit in the GPIOCON register. The pin is referenced between IOVDD and DGND.
19	$\overline{SYNC}$	DI	Synchronization Input. Allows synchronization of the digital filters and analog modulators when using multiple AD4113 devices.
20	IOVDD	P	Digital Input/Output Supply Voltage. The IOVDD voltage ranges from 2V to 5.5V (nominal). IOVDD is independent of AVDD. For example, IOVDD operate at 3.3V when AVDD equals 5V, or vice versa. If AVSS is set to −2.5V, the voltage on IOVDD must not exceed 3.6V.
21	DGND	P	Digital Ground.
22	REGCAPD	AO	Digital LDO Regulator Output. This pin is for decoupling purposes only. Decouple this pin to DGND using a 1µF capacitor.
23	COMPA	AO	Compensation Pin for VIN0, VIN2, VIN4, and VIN6. Connect this pin to the corresponding voltage input pins through a 1kΩ resistor and 680pF capacitor when using open-wire detection (for more details, see the Open-Wire Detection section).
24	COMPB	AO	Compensation Pin for VIN1, VIN3, VIN5, and VIN7. Connect this pin to the corresponding voltage input pins through a 1kΩ resistor and 680pF capacitor when using open-wire detection (for more details, see the Open-Wire Detection section).
25, 38	GPO0, GPO1	DO	General-Purpose Output. Logic output on this pin is referred to the AVDD and AVSS supplies.
26	VIN4	AI	Voltage Input 4. Input referenced to VINCOM in single-ended configuration or a positive input of an input pair with VIN5 in differential configuration.
27	VIN5	AI	Voltage Input 5. Input referenced to VINCOM in single-ended configuration or a negative input of an input pair with VIN4 in differential configuration.
28	VIN6	AI	Voltage Input 6. Input referenced to VINCOM in single-ended configuration or a positive input of an input pair with VIN7 in differential configuration.
29	VIN7	AI	Voltage Input 7. Input referenced to VINCOM in single-ended configuration or a negative input of an input pair with VIN6 in differential configuration.
39	REF−	AI	Reference Input Negative Terminal. REF− can span from AVSS to AVDD − 1V. Reference can be selected through the REF_SELx bits in the setup configuration registers.
40	REF+	AI	Reference Input Positive Terminal. An external reference can be applied between REF+ and REF−. REF+ can span from AVDD to AVSS + 1V. Reference can be selected through the REF_SELx bits in the setup configuration registers.
	EP	P	Exposed Pad. Solder the exposed pad to a similar pad on the PCB under the exposed pad to confer mechanical strength to the package and for heat dissipation. The exposed pad must be connected to AVSS through this pad on the PCB.

[1] Note that, throughout this data sheet, the dual function pin mnemonics are referenced by the relevant function only.

[2] AI means analog input, AO means analog output, P means power supply, N/A means not applicable, DI means digital input, DO means digital output, and DI/O means bidirectional digital input/output.

TYPICAL PERFORMANCE CHARACTERISTICS

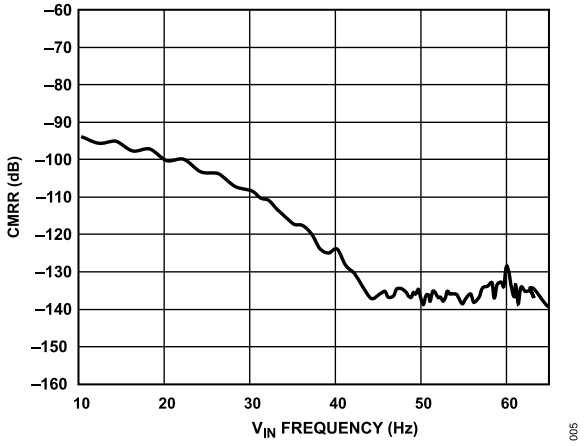


Figure 5. Common-Mode Rejection Ratio (CMRR) vs. V_{IN} Frequency (V_{IN} = 0.1V, 10Hz to 70Hz, Output)

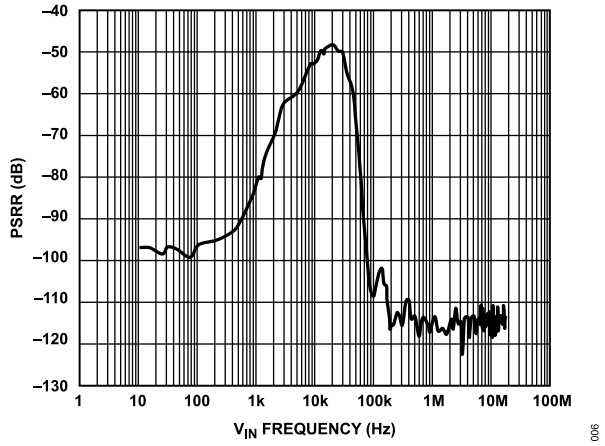


Figure 6. Power-Supply Rejection Ratio (PSRR) vs. V_{IN} Frequency

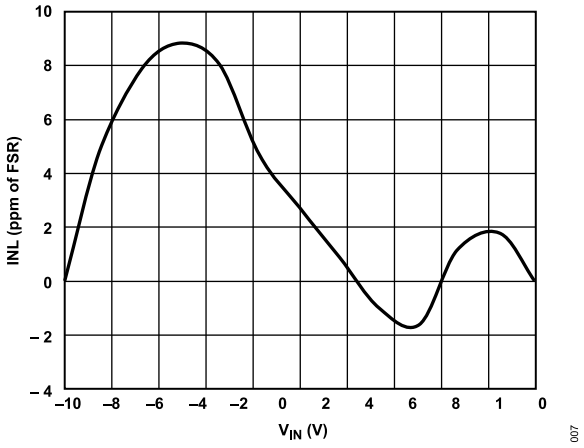


Figure 7. Integral Nonlinearity (INL) vs. V_{IN}

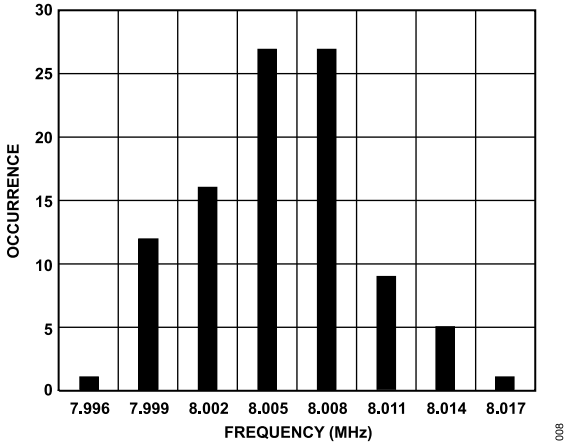


Figure 8. Internal Oscillator Frequency/Accuracy Distribution Histogram

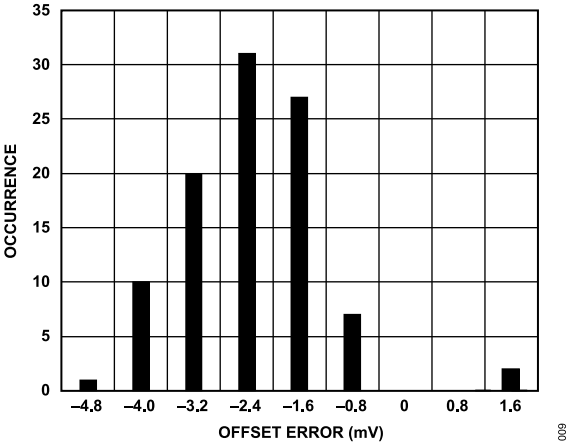


Figure 9. Offset Error Distribution Histogram

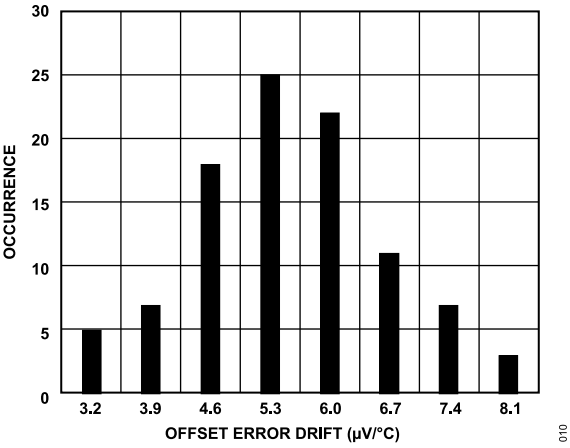


Figure 10. Offset Error Drift Distribution Histogram

TYPICAL PERFORMANCE CHARACTERISTICS

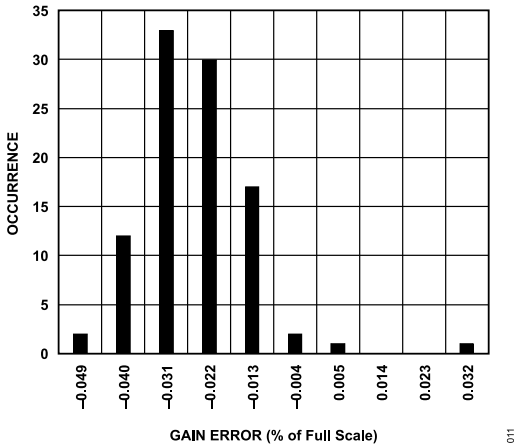


Figure 11. Gain Error Distribution Histogram

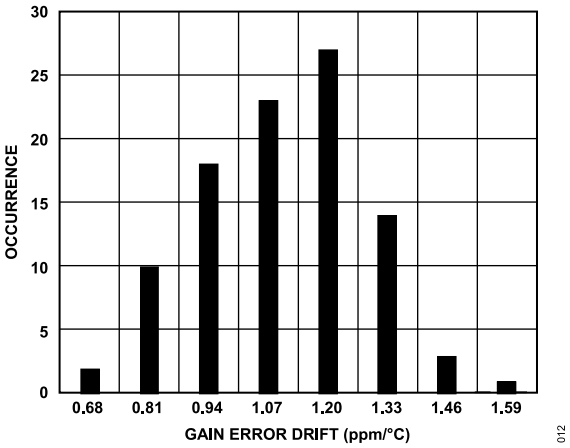


Figure 12. Gain Error Drift Distribution Histogram

NOISE PERFORMANCE AND RESOLUTION

Table 7 and Table 8 show the rms noise, peak-to-peak noise, effective resolution, and the noise free (peak-to-peak) resolution of the AD4113 for various ODRs. These values are typical and are measured with an external 2.5V reference and with the ADC continuously converting on multiple channels. The values in Table 7 and Table 8 are generated for the ±10V voltage input range with a differential input voltage of 0V. It is important to note that the peak-to-peak resolution is calculated based on the peak-to-peak noise. The peak-to-peak resolution represents the resolution for which there is no code flicker.

Table 7. ±10V Voltage Input RMS Noise Resolution vs. ODR Using a Sinc5 + Sinc1 Filter

Default Output Data Rate (SPS), SING_CYC = 0 and Single-Channel Enabled	Output Data Rate (SPS per Channel), SING_CYC = 1 or Multiple Channels Enabled	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)[2]	Effective Resolution (Bits)	Noise (µV p-p)	Peak-to-Peak Resolution (Bits)
125,000	24,845	40.25µs	125,000	140.36	16	926.38	14.40
62,500	20,725	48.25µs	62,500	124.42	16	821.17	14.57
31,250	15,564	64.25µs	31,250	99.14	16	654.32	14.90
25,000	13,841	72.25µs	25,000	89.57	16	591.16	15.05
15,625	10,390	96.25µs	15,625	72.94	16	481.40	15.34
10,390	10,390	96.25µs	15,625	71.01	16	468.67	15.38
4,994	4,994	200.25µs	5952.4	45.67	16	301.42	16
2,498	2,499	400.25µs	2717.4	32.42	16	213.97	16
1,000	1,000	1ms	1033.1	20.24	16	133.58	16
500	500	2ms	508.1	13.88	16	91.61	16
395.5	395.5	2.53ms	400.6	12.61	16	83.23	16
200	200	5ms	201.3	9.702	16	64.03	16
100	100	10ms	100.3	7.36	16	48.58	16
59.87	59.89	16.7ms	59.98	5.38	16	35.51	16
49.92	49.92	20.03ms	50	5.52	16	36.43	16
20	20.	50ms	20.01	4.52	16	29.83	16
16.7	16.66	60.03ms	16.67	4.07	16	26.86	16
10	10	100ms	10	3.15	16	16.1	16
5	5	200ms	5	2.92	16	12.1	16
2.5	2.5	400ms	2.5	2.49	16	12	16

[1] The settling time is rounded to the nearest microsecond, which is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.

[2] Based on 1000 samples for data rates ≥ 395.5SPS per channel, based on 100 samples for data rates ≤ 200SPS per channel.

Table 8. ±10V Voltage Input RMS Noise Resolution vs. ODR Using a Sinc3 Filter

Default Output Data Rate (SPS), SING_CYC = 0 and Single-Channel Enabled	Output Data Rate (SPS per Channel), SING_CYC = 1 or Multiple Channels Enabled	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)[2]	Effective Resolution (Bits)	Noise (µV p-p)	Peak-to-Peak Resolution (Bits)
125,000	41,237	24.3µs	125,000	1,008	14.28	6,652	11.55
62,500	20,725	48.3µs	62,500	176.41	16	1,164	14.07
31,250	10,389.6	96.3µs	31,250	82.49	16	544.43	15.16
25,000	8,316.0	120.3µs	25,000	73.71	16	486.49	15.33
15,625	5,201.6	192.3µs	15,625	57.99	16	382.73	15.67
10,416.7	3,469.2	288.3µs	10,417	46.93	16	309.74	15.98
5,000	1,666.0	600.3µs	5,000	31.45	16	207.57	16
2,500	833.2	1.2ms	2,500	22.83	16	150.68	16
1,000	333.33	3ms	1,000	14.35	16	94.71	16
500	166.67	6ms	500.0	10.82	16	71.41	16
400.6	133.51	7.49ms	400.6	9.66	16	63.76	16
200	66.67	15ms	200.0	7.30	16	48.18	16
100	33.33	30ms	100.0	5.81	16	38.35	16
59.98	19.99	50.02ms	59.98	4.70	16	31.02	16

NOISE PERFORMANCE AND RESOLUTION

Table 8. ±10V Voltage Input RMS Noise Resolution vs. ODR Using a Sinc3 Filter (Continued)

Default Output Data Rate (SPS), SING_CYC = 0 and Single-Channel Enabled	Output Data Rate (SPS per Channel), SING_CYC = 1 or Multiple Channels Enabled	Settling Time[1]	Notch Frequency (Hz)	Noise (µV rms)[2]	Effective Resolution (Bits)	Noise (µV p-p)	Peak-to-Peak Resolution (Bits)
50	16.67	60ms	50.00	4.48	16	29.57	16
20	6.67	150ms	20.00	3.30	16	21.78	16
16.67	5.56	180ms	16.67	2.78	16	18.35	16
10	3.33	300ms	10.00	2.95	16	14.9	16
5	1.67	600ms	5.00	2.63	16	11.9	16
2.5	0.83	1.2s	2.50	2.43	16	11.9	16

[1] The settling time is rounded to the nearest microsecond, which is reflected in the output data rate and channel switching rate. Channel switching rate = 1 ÷ settling time.

[2] Based on 1000 samples for data rates ≥ 381SPS per channel, based on 100 samples for data rates ≤ 200.3SPS per channel.

THEORY OF OPERATION

The AD4113 offers a fast settling, high resolution, and multiplexed ADC with high levels of configurability, and also includes the following features:

- Four fully-differential or eight single-ended voltage inputs.
- High-impedance voltage divider with integrated precision matched resistors.
- Embedded proprietary *i*Passives technology within a very small device footprint.
- Per-channel configurability. Up to eight different setups can be defined. A separate setup can be mapped to each of the channels. Each setup allows the user to configure whether the buffers are enabled or disabled, gain and offset correction, filter type, ODR, and reference source selection.
- Highly-configurable digital filter enabling conversion rates up to 125kSPS on a single channel and 24.845kSPS switching.

The AD4113 includes a precision 2.5V band gap internal reference. This reference can be selected for use in ADC conversions, which reduces the external component count. When enabled, the internal reference is output to the REFOUT pin. The internal reference can be used as a low noise biasing voltage for the external circuitry and must be connected to a 0.1µF decoupling capacitor.

The AD4113 includes two separate linear regulator blocks for both the analog and digital circuitry. The analog LDO regulator regulates the AVDD supply to 1.8V, which supplies the ADC core.

The linear regulator for the digital IOVDD supply performs a similar function, which regulates the input voltage applied at the IOVDD pin to 1.8V for the internal digital filtering. The serial interface signals always operate from the IOVDD supply seen at the pin. This means that, if 3.3V is applied to the IOVDD pin, the interface logic inputs and outputs operate at this level.

The AD4113 is designed for a multitude of factory automation and process control applications, such as a programmable logic controller (PLC) and distributed control system (DCS) modules. The device reduces overall system cost and design burden while maintaining a high level of accuracy. The AD4113 offers the following system benefits:

- A single 5V power supply
- Guaranteed minimum 1MΩ input impedance
- Overrange voltage > ±10V
- Reduced calibration costs

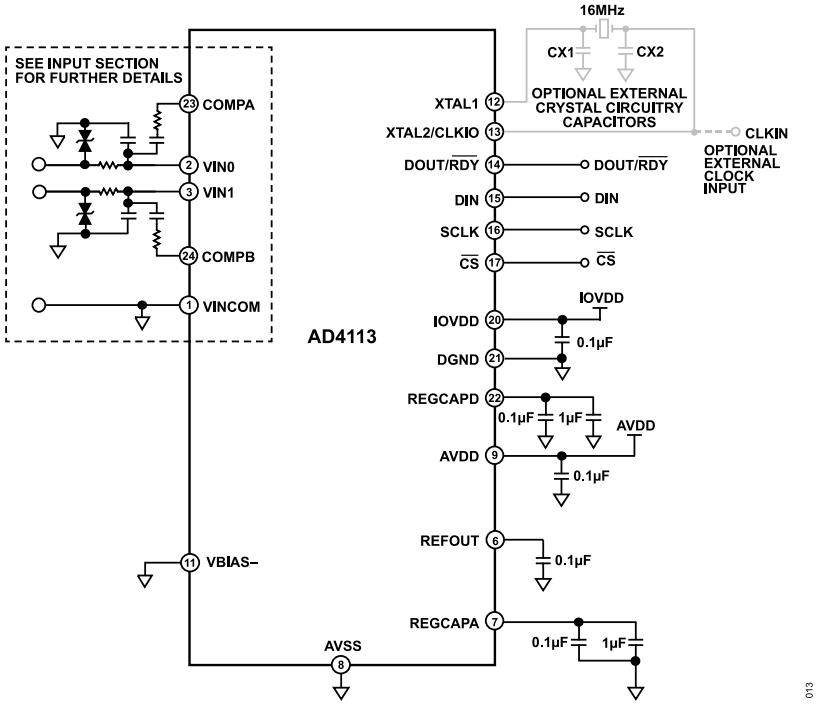


Figure 13. Typical Connection Diagram

THEORY OF OPERATION

POWER SUPPLIES

The AD4113 has two independent power supply pins: AVDD and IOVDD. The AD4113 has no specific requirements for a power supply sequence. When all power supplies are stable, a device reset is required. For more details on how to reset the device, see the AD4113 Reset section.

The AVDD powers the internal 1.8V analog LDO regulator, which powers the ADC core. The AVDD also powers the crosspoint multiplexer and integrated input buffers. The AVDD is referenced to AVSS and AVDD − AVSS = 5V. The AVDD and AVSS can be a single 5V supply or ±2.5V split supplies. When using split supplies, consider the absolute maximum ratings (see the Absolute Maximum Ratings section).

The IOVDD powers the internal 1.8V digital LDO regulator. The LDO regulator powers the digital logic of the ADC. The IOVDD sets the voltage levels for the serial-peripheral interface (SPI) of the ADC. The IOVDD is referenced to DGND, and IOVDD to DGND can vary from 2V (minimum) to 5.5V (maximum).

Single-Supply Operation (AVSS = DGND)

When the AD4113 is powered from a single supply connected to AVDD, the supply must be 5V. In this configuration, AVSS and DGND can be shorted together on a single ground plane.

The IOVDD can range from 2V to 5.5V in this unipolar input configuration.

DIGITAL COMMUNICATION

The AD4113 has a 3-wire or 4-wire SPI interface that is compatible with QSPI™, MICROWIRE®, and DSPs. The interface operates in SPI Mode 3 and can be operated with $\overline{CS}$ connected low. In SPI Mode 3, SCLK idles high, the falling edge of SCLK is the drive edge, and the rising edge of SCLK is the sample edge. This means that data is clocked out on the falling/drive edge and data is clocked in on the rising/sample edge.

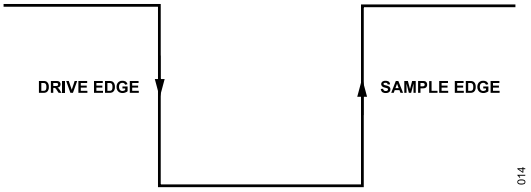


Figure 14. SPI Mode 3 SCLK Edges

Accessing the ADC Register Map

The communications register controls access to the full register map of the ADC. This register is an 8-bit write only register. On power-up or after a reset, the digital interface defaults to a state where it is expecting a write to the communications register. Therefore, all communication begins by writing to the communications register.

The data written to the communications register determines which register is being accessed and if the next operation is a read or write. The RA bits (Bits[5:0] in Register 0x00) determine the specific register to which the read or write operation applies.

When the read or write operation to the selected register is complete, the interface returns to its default state, where the interface expects a write operation to the communications register.

In situations where interface synchronization is lost, a write operation of at least 64 serial clock cycles with DIN high returns the ADC to its default state by resetting the entire device, including the register contents. Alternatively, if $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high resets the digital interface to its default state and aborts any current operation.

Figure 15 and Figure 16 show writing to and reading from a register by first writing the 8-bit command to the communications register followed by the data for the addressed register.

Reading the ID register is the recommended method for verifying correct communication with the device. The ID register is a read only register and contains the value 0x39DX for the AD4113. The communication register and ID register details are described in Table 9 and Table 10.

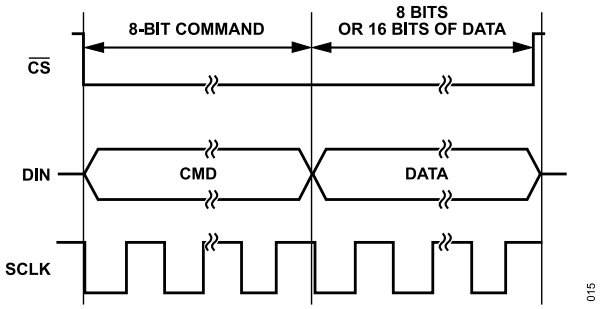


Figure 15. Writing to a Register (8-Bit Command with Register Address Followed by Data of 8 Bits or 16 Bits, Data Length is Dependent on the Register Selected)

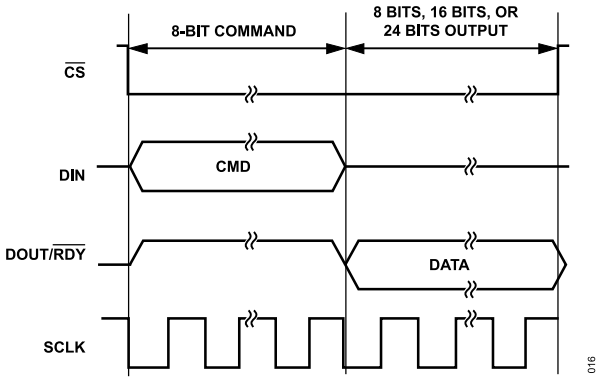


Figure 16. Reading from a Register (8-Bit Command with Register Address Followed by Data of 8 Bits, 16 Bits, or 24 Bits, Data Length on DOUT is Dependent on the Register Selected)

THEORY OF OPERATION

AD4113 RESET

After a power-up cycle and when the power supplies are stable, a device reset is required. In situations where interface synchronization is lost, a device reset is also required. A write operation of at least 64 serial clock cycles with DIN high returns the ADC to the default state by resetting the entire device, including the register contents. Alternatively, If $\overline{CS}$ is being used with the digital interface, returning $\overline{CS}$ high sets the digital interface to the default state and halts any serial interface operation.

Table 9. Communications Register Details

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W

Table 10. ID Register Details

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x07	ID	[15:8]	ID[15:8]								0x39DX[1]	R
		[7:0]	ID[7:0]									

[1] X means don't care.

CONFIGURATION OVERVIEW

After a power-on or a reset, the AD4113 default configuration is as follows:

- Channel configuration. Channel 0 is enabled, the VIN0 and VIN1 pair is selected as the input. Setup 0 is selected.
- Setup configuration. The analog input buffers are disabled and the reference input buffers are also disabled. The REF± pins are selected as the reference source. For this setup, the default channel does not operate properly because the input buffers must be enabled for a VINx input.
- Filter configuration. The Sinc5 + Sinc1 filter is selected and the maximum output data rate of 125kSPS is selected.
- ADC mode. The continuous conversion mode and the internal oscillator are enabled. The internal reference is disabled.
- Interface mode. The CRC and the data and status output are disabled.

In the following list, only a few of the register setting options are shown. For full register information, see the Register Details section.

Figure 17 shows an overview of the suggested flow for changing the ADC configuration, divided into the following three blocks:

- Channel configuration (see Box A in Figure 17).
- Setup configuration (see Box B in Figure 17).
- ADC mode and interface mode configuration (see Box C in Figure 17).

Channel Configuration

The AD4113 has 16 independent channels and eight independent setups. The user can select any of the input pairs on any channel, as well as any of the eight setups for any channel, which give the user full flexibility in the channel configuration. This flexibility also allows per-channel configuration when using differential inputs and single-ended inputs because each channel can have its own dedicated setup.

Channel Registers

The channel registers select which of the voltage inputs is used for that channel. The channel registers also contain a channel enable/disable bit and the setup selection bits that are used to select which of the eight available setups to use for this channel.

When the AD4113 is operating with more than one channel enabled, the channel sequencer cycles through the enabled channels in sequential order, from Channel 0 to Channel 15. If a channel is disabled, it is skipped by the sequencer. Details of the channel register for Channel 0 are shown in Table 11.

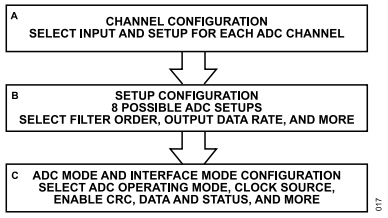


Figure 17. Suggested ADC Configuration Flow

THEORY OF OPERATION

Table 11. Channel Register 0 Details

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL0			Reserved		INPUT[9:8]		0x8001	R/W
		[7:0]	INPUT[7:0]									

ADC Setups

The AD4113 has eight independent setups. Each setup consists of the following four registers:

- Setup configuration register
- Filter configuration register
- Gain register
- Offset register

For example, Setup 0 consists of Setup Configuration Register 0, Filter Configuration Register 0, Gain Register 0, and Offset Register 0. Figure 18 shows the grouping of these registers. The setup is selectable from the channel registers (see the Channel Configuration section), which allows each channel to be assigned to one of eight separate setups. Table 12 through Table 15 show the four registers that are associated with Setup 0. This structure is repeated for Setup 1 to Setup 7.

Setup Configuration Registers

The setup configuration registers allow the user to select the output coding of the ADC by selecting between bipolar and unipolar modes. The user can select the reference source using these registers. Three options are available: a reference connected between the REF+ and REF− pins, the internal reference, or using AVDD − AVSS. The input and reference buffers can also be enabled or disabled using these registers.

Filter Configuration Registers

The filter configuration registers select which digital filter is used at the output of the ADC modulator. The order of the filter and the output data rate are selected by setting the bits in these registers. For more details, see the Digital Filter section.

Gain Registers

The gain registers are 16-bit registers that hold the gain calibration coefficient for the ADC. The gain registers are read/write registers.

Offset Registers

The offset registers hold the offset calibration coefficient for the ADC. The power-on reset value of the offset registers is 0x8000. The offset registers are 16-bit read and write registers.

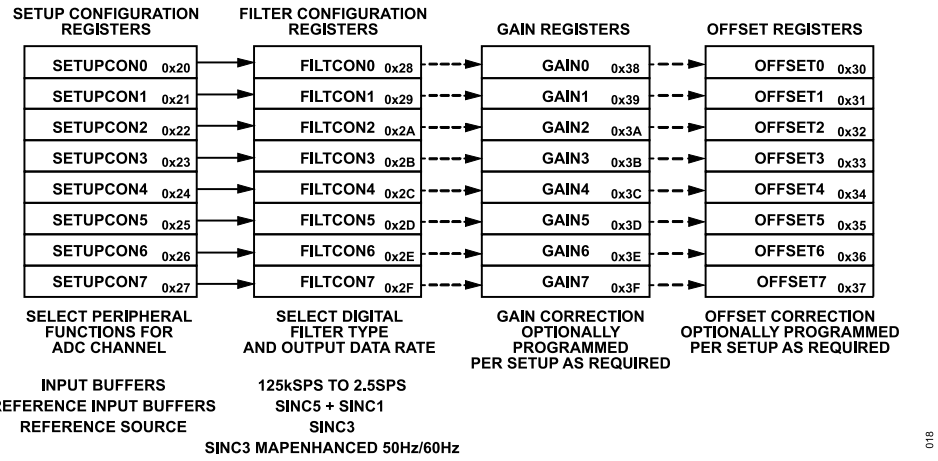


Figure 18. ADC Setup Register Grouping

THEORY OF OPERATION

Table 12. Setup Configuration Register 0

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x20	SETUPCON0	[15:8]	Reserved			BI_UNIPOLAR0	REFBUF0+	REFBUF0−	INBUF0		0x1000	R/W
		[7:0]	Reserved	Reserved	REF_SEL0		Reserved					

Table 13. Filter Configuration Register 0

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x28	FILTCON0	[15:8]	SINC3_MAP0	Reserved			ENHFILTEN0	ENHFILT0			0x0500	R/W
		[7:0]	Reserved	ORDER0	ODR0							

Table 14. Gain Register 0

Reg.	Name	Bits	Bits[15:0]	Reset	Access
0x38	GAIN0	[15:0]	GAIN0[15:0]	0x5XXX	R/W

Table 15. Offset Register 0

Reg.	Name	Bits	Bits[15:0]	Reset	Access
0x30	OFFSET0	[15:0]	OFFSET0[15:0]	0x8000	R/W

ADC Mode and Interface Mode Configuration

The ADC mode register and the interface mode register configure the core peripherals for use by the AD4113 and the mode for the digital interface.

ADC Mode Register

The ADC mode register primarily sets the conversion mode of the ADC to either continuous or single conversion. The user can also select the standby and power-down modes, as well as any of the calibration modes. In addition, this register contains the clock source select bits and internal reference enable bit. The reference select bits are contained in the setup configuration registers (for more details, see the ADC Setups section). The details of this register are shown in Table 16.

Interface Mode Register

The interface mode register configures the digital interface operation. This register allows the user to control data-word length, CRC enable, data plus status read, and continuous read mode. The details of this register are shown in Table 17. For more details, see the Digital Interface section.

Table 16. ADC Mode Register Details

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x01	ADCMODE	[15:8]	REF_EN	Reserved	SING_CYC	Reserved		Delay			0x2000	R/W
		[7:0]	Reserved	Mode			CLOCKSEL	Reserved				

Table 17. Interface Mode Register Details

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x02	IFMODE	[15:8]	Reserved			ALT_SYNC	IOSTRENGTH	Reserved		DOUT_RESET	0x0000	R/W
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	Reserved	CRC_EN		Reserved	WL16		

CIRCUIT DESCRIPTION

MULTIPLEXER

There are nine voltage pins: VIN0 to VIN7, and VINCOM. Each of these pins connects to the internal multiplexer. The multiplexer enables these inputs to be configured as input pairs. For more details on how to set up these inputs, see the Voltage Inputs section. The AD4113 can have up to sixteen active channels. When more than one channel is enabled, the channels are automatically sequenced in order from the lowest enabled channel number to the highest enabled channel number. The output of the multiplexer is connected to the input of the integrated true rail-to-rail buffers. These buffers are disabled by default on power-up but must be enabled for correct operation of the device. The simplified voltage input circuit is shown in Figure 19.

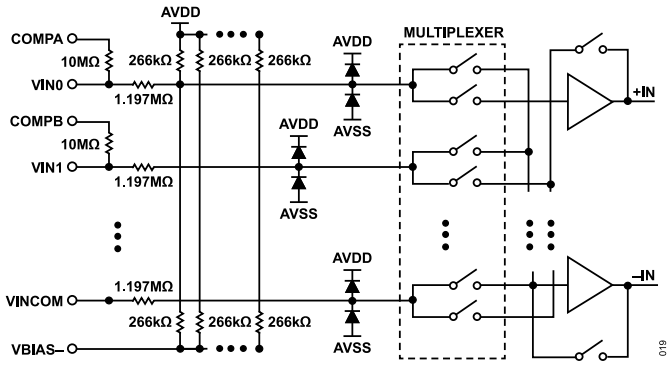


Figure 19. Simplified Voltage Input Circuit

VOLTAGE INPUTS

The AD4113 can be set up to have eight single-ended inputs or four fully-differential inputs. The voltage divider on the analog front end has a division ratio of 10 and consists of precision matched resistors that enable an input range of ±20V from a single, 5V power supply.

Enable the input buffers in the setup register for voltage input channels.

Fully-Differential Inputs

Due to the matching resistors on the analog front end, the differential inputs of the voltage inputs must be paired together in the following pairs to ensure correct operation: VIN0 and VIN1, VIN2 and VIN3, VIN4 and VIN5, and VIN6 and VIN7.

Single-Ended Inputs

The user can also choose to measure up to eight different single-ended voltage inputs. In this case, each of the voltage inputs must be paired with VINCOM. Connect VINCOM externally to AVSS.

Open-Wire Detection

Open-wire detection is a system level diagnostic that detects when an external sensor or source signal is disconnected from the system input. The AD4113 incorporates a unique feature that enables open-wire detection on ±10V voltage inputs while operating on a 5V single power supply, which in existing designs requires a supply greater than ±10V. Open-wire detection must be supported in user software. This section describes how to set up the AD4113 for open-wire detection together with the associated calculations required.

Open-wire detection is enabled by setting Bit 12 (OW_EN) and Bit 13 (OP_EN0_1) in the GPIO configuration register to 1 (see Table 26). Bit 6 (DATA_STAT) in the interface mode register, must also be set (see Table 23).

Voltage inputs must be assigned two channels per measurement when using open-wire detection. Voltage inputs must also be assigned to specific channel pairs to ensure that open-wire detection measurements work correctly. For single-ended input, open-wire detection measurements, the channel pairings that must be used are as follows:

- Channel 15 and Channel 0
- Channel 1 and Channel 2
- Channel 3 and Channel 4
- Channel 5 and Channel 6
- Channel 7 and Channel 8
- Channel 9 and Channel 10
- Channel 11 and Channel 12
- Channel 13 and Channel 14

For differential input, open-wire detection measurements, the channel pairings that must be used are as follows:

- Channel 1 and Channel 2
- Channel 5 and Channel 6
- Channel 9 and Channel 10
- Channel 13 and Channel 14

CIRCUIT DESCRIPTION

Additionally, for differential inputs, the inputs must be set up in the following differential pairs to ensure correct operation:

- VIN0 and VIN1
- VIN2 and VIN3
- VIN4 and VIN5
- VIN6 and VIN7

For more details on the channel registers, see Table 26.

After the AD4113 is configured correctly, the output data must be processed in user software to implement open-wire detection. An open wire on an input is detected by comparing the absolute difference between the two channels associated with an input to a threshold. The suggested threshold is 300mV input referred. This threshold is approximately 393 (0x0189) in decimal output code from the ADC when operating in bipolar configuration with a 2.5V voltage reference. This threshold is approximately 786 (0x0312) codes when operating in unipolar configuration. For more details on converting ADC output codes to volts, see the Data Output Coding section. If the difference is greater than this threshold, an open wire must be flagged by the user software. Open-wire detection operation is shown in the Example 1—Open-Wire Detection (Single-Ended Input) and the Example 2—Open-Wire Detection (Differential Input) sections.

Note that the following registers and settings are used in the examples shown in the Example 1—Open-Wire Detection (Single-Ended Input) and the Example 2—Open-Wire Detection (Differential Input) sections:

- IFMODE = 0x0040 enables data and status.
- GPIOCON = 0x3800 enables open-wire detection.
- SETUPCON0 = 0x1300 enables input buffers and the external reference (2.5V), and selects bipolar mode.
- All other registers are set to default values.

Example 1—Open-Wire Detection (Single-Ended Input)

In this example:

- Channel 0 and Channel 15 = 0x8010 enables the single-ended input (VIN0 and VINCOM) and Setup 0.
- The VIN0 pin is left floating, while the VINCOM pin is connected to GND for single-ended configuration.
- Channel 0 = 35,661 (2.2075V).
- Channel 15 = 36,566 (2.8975V).
- |35,661 − 36,566| = 905 (691mV) > 393(300mV).
- Open wire is flagged.
- A 1V input is connected to the VIN0 and VINCOM is connected to GND.
- Channel 0 = 34,083 (1.00315V).
- Channel 15 = 34,073 (0.99564V).
- |34,083 – 34,073| = 10 (7.63mV) < 393 (300mV).
- Open wire is not flagged.

Example 2—Open-Wire Detection (Differential Input)

In this example:

- Channel 1 and Channel 2 = 0x8001 enables the differential input (VIN0 and VIN1) and Setup 0.
- Channel 0 cannot be used for the differential input. Disable Channel 0 by setting it to 0x0000.
- The VIN0 and VIN1 pins are left floating. Nothing is connected to the pins.
- Channel 1 = 33,668 (687mV).
- Channel 2 = 31,868 (−687mV).
- |33,668 − 31,868| = 1,800 (1.3734V) > 393 (300mV).
- Open wire is flagged.
- A 1V differential input is connected the VIN0 and VIN1 input pins.
- Channel 1 = 34,081 (1.0017V).
- Channel 2 = 34,045 (0.9750V).
- |34,081 − 34,045| = 36 (27.47mV) < 393 (300mV).
- Open wire is not flagged.

Open-Wire Detection Compensation Pins

For the correct function of open-wire detection, connect a capacitor and resistor in series between each compensation and voltage input pin. The recommended values are a 1kΩ resistor and a 680pF capacitor. There are two compensation pins, COMPA and COMPB. COMPA must be connected through the resistor and capacitor to VIN0, VIN2, VIN4, and VIN6. COMPB must be connected to VIN1, VIN3, VIN5, and VIN7. For VINCOM, the RC connection is not necessary (see Table 6 and Figure 13).

ABSOLUTE INPUT PIN VOLTAGES

The AD4113 voltage input pins are specified for an accuracy of ±10V, specifically for the differential voltage between any two voltage input pins.

The voltage input pins have separate specifications for the absolute voltage that can be applied, and the unique design of the voltage divider network of the analog front end enables overvoltage robustness on the AD4113, which means the allowed overvoltages vary depending on the AVDD supply. Figure 20 shows the different degrees of robustness that can be achieved for AVDD = 5V. Figure 20 provides a visual representation and guidance on how an overvoltage on a voltage pin can affect the overall device accuracy.

The guaranteed accuracy section of Figure 20 shows the voltage range that can be applied to a voltage input pin and achieve guaranteed accuracy.

The no loss of accuracy sections show the voltage levels that can be applied without degrading the accuracy of other channels.

CIRCUIT DESCRIPTION

The no damage to device sections show the allowable positive and negative voltages that can be applied to a voltage input pin without exceeding the absolute maximum. The performance of other channels is degraded, but the performance recovers when the overvoltage is removed. This voltage range is specified as an absolute maximum rating of ±65V.

Operation beyond the maximum operating conditions for extended periods can affect product reliability.

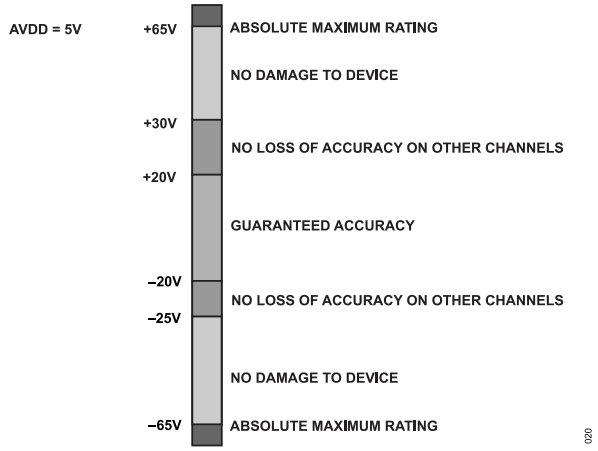


Figure 20. Absolute Input Pin Voltages, AVDD = 5V

DATA OUTPUT CODING

When the ADC is configured for unipolar operation, the output code is natural (straight) binary with a zero differential input voltage resulting in a code of 00 … 00, a midscale voltage resulting in a code of 100 … 000, and a full-scale input voltage resulting in a code of 111 … 111. The output code for any input voltage is shown as:

$$Code = (2^N \times V_{IN} \times 0.1)/V_{REF}$$

When the ADC is configured for bipolar operation, the output code is offset binary with a negative full-scale voltage resulting in a code of 000 … 000, a zero differential input voltage resulting in a code of 100 … 000, and a positive full-scale input voltage resulting in a code of 111 … 111. The output code for any analog input voltage is shown as:

$$Code = 2^{N-1} \times ((V_{IN} \times 0.1/V_{REF}) + 1)$$

where:

N = 16.

V_{IN} is the input voltage.

V_{REF} is the reference voltage.

AD4113 REFERENCE

The AD4113 offers the user the option of either supplying an external reference to the REF+ and REF− pins of the device, using AVDD – AVSS, or by allowing the use of the internal 2.5V, low noise, and low drift reference. Select the reference source to be used by the analog input by setting the REF_SELx bits, Bits[5:4], in the setup configuration registers appropriately. The structure of Setup Configuration 0 register is shown in Table 12. The AD4113 defaults on power-up to use the external reference.

Internal Reference

The AD4113 includes a low noise, low-drift voltage reference. The internal reference has a 2.5V output. The internal reference is output on the REFOUT pin after the REF_EN bit in the ADC mode register is set and is decoupled to AVSS with a 0.1µF capacitor. The AD4113 internal reference is disabled by default on power-up.

External Reference

The AD4113 has a fully-differential reference input applied through the REF+ and REF− pins. Standard low noise, low-drift voltage references, such as the ADR4525, are recommended for use. Apply the external reference to the AD4113 reference pins, as shown in Figure 21. Decouple the output of any external reference to AVSS. As shown in Figure 21, the ADR4525 output is decoupled with a 0.1µF capacitor at the output for stability purposes. The output is then connected to a 4.7µF capacitor, which acts as a reservoir for any dynamic charge required by the ADC, and is followed by a 0.1µF decoupling capacitor at the REF+ input. This capacitor is placed as close as possible to the REF+ and REF− pins.

The REF− pin is connected directly to the AVSS potential. When an external reference is used instead of the internal reference to supply the AD4113, attention must be paid to the output of the REFOUT pin. The internal reference is controlled by the REF_EN bit (Bit 15) in the ADC mode register, which is shown in Table 16. If the internal reference is not being used elsewhere in the application, ensure that the REF_EN bit is disabled.

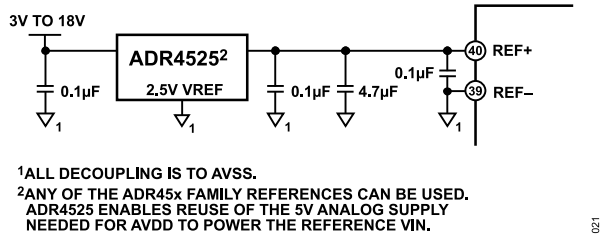


Figure 21. ADR4525 Connected to AD4113 REF± Pins

BUFFERED REFERENCE INPUT

The AD4113 has true rail-to-rail, integrated, precision, unity-gain buffers on both ADC reference inputs. The buffers provide the benefit of providing high input impedance and allowing high impedance external sources to be directly connected to the reference inputs. The integrated reference buffers can fully drive the internal reference switch capacitor sampling network, simplifying the reference circuit requirements. Each reference input buffer amplifier is fully chopped, which means that the amplifier minimizes the offset error

CIRCUIT DESCRIPTION

drift and 1/f noise of the buffer. When using a reference, such as the ADR4525, the integrated reference buffers are not required because these external references, such as the ADR4525, with proper decoupling, can drive the reference inputs directly.

CLOCK SOURCE

The AD4113 uses a nominal MCLK of 8MHz. The AD4113 can source its sampling clock from one of three sources:

- An internal oscillator.
- An external crystal (use a 16MHz crystal automatically divided internally to set the 8MHz clock).
- An external clock source.

All output data rates listed in the data sheet relate to a MCLK rate of 8MHz. Using a lower clock frequency from an external source, for instance, scales any listed data rate proportionally. To achieve the specified data rates, particularly rates for rejection of 50Hz and 60Hz, use a 8MHz clock. The source of the MCLK is selected by setting the CLOCKSEL bits (Bits[3:2]) in the ADC mode register, as shown in Table 16. The default operation on power-up and reset of the AD4113 is to operate with the internal oscillator. It is possible to fine tune the output data rate and filter notch at low output data rates using the SINC3_MAPx bit.

Internal Oscillator

The internal oscillator runs at 16MHz and is internally divided down to 8MHz for the modulator and can be used as the ADC MCLK. The internal oscillator is the default clock source for the AD4113 and is specified with an accuracy of −2.5% to +2.5%.

There is an option to allow the internal clock oscillator to be output on the XTAL2/CLKIO pin. The clock output is driven to the IOVDD logic level. This option can affect the DC performance of the AD4113 due to the disturbance introduced by the output driver. The extent to which the performance is affected depends on the IOVDD voltage supply. Higher IOVDD voltages create a wider logic output swing from the driver and affect performance to a greater extent. This effect is further exaggerated if the IOSTRENGTH bit is set at higher IOVDD levels (for more details, see Table 23).

External Crystal

If higher precision, lower jitter clock sources are required, the AD4113 can use an external crystal to generate the MCLK. The crystal is connected to the XTAL1 and XTAL2/CLKIO pins. A recommended crystal for use is the FA-20H, a 16MHz, 10ppm, and 9pF crystal from Epson-Toyocom that is available in a surface-mount package. As shown in Figure 22, insert two capacitors (CX1 and CX2) from the traces connecting the crystal to the XTAL1 and XTAL2/CLKIO pins. These capacitors allow circuit tuning. Connect these capacitors to the DGND pin. The value for these capacitors depends on the length and capacitance of the trace connections between the crystal and the XTAL1 and XTAL2/CLKIO pins. Therefore, the values of these capacitors differ, which depend on the PCB layout and the crystal employed.

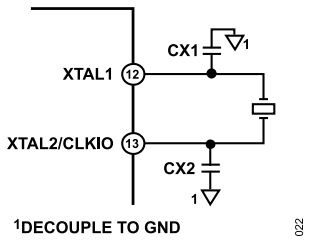


Figure 22. External Crystal Connections

The external crystal circuitry can be sensitive to the SCLK edges, which depend on the SCLK frequency, IOVDD voltage, crystal circuitry layout, and the crystal used. During crystal startup, any disturbances caused by the SLCK edges can cause double edges on the crystal input, which results in invalid conversions until the crystal voltage reaches a high enough level such that any interference from the SCLK edges is insufficient to cause double clocking. This double clocking can be avoided by ensuring that the crystal circuitry has reached a sufficient voltage level after startup before applying any SCLK.

Due to the nature of the crystal circuitry, it is therefore recommended that empirical testing of the circuit be performed under the required conditions, with the final PCB layout and crystal, to ensure correct operation.

External Clock

The AD4113 can also use an externally supplied clock. In systems where this is required, the external clock is routed to the XTAL2/ CLKIO pin. In this configuration, the XTAL2/ CLKIO pin accepts the externally sourced clock and routes it to the modulator. The logic level of this clock input is defined by the voltage applied to the IOVDD pin.

DIGITAL FILTER

The AD4113 has three flexible filter options to allow optimization of noise, settling time, and rejection:

- The Sinc5 + Sinc1 filter
- The Sinc3 filter
- The enhanced 50Hz and 60Hz rejection filters

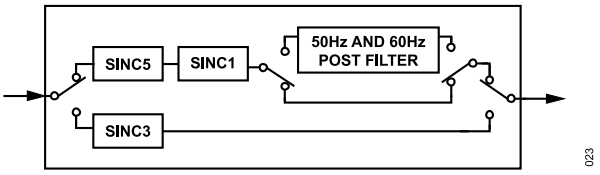


Figure 23. Digital Filter Block Diagram

The filter and output data rate are configured by setting the appropriate bits in the filter configuration register for the selected setup. Each channel can use a different setup and therefore, a different filter and output data rate. For more details, see the Register Details section.

SINC5 + SINC1 FILTER

The Sinc5 + Sinc1 filter is targeted at multiplexed applications and achieves single cycle settling at output data rates of ≤10kSPS. The Sinc5 block output is fixed at the maximum rate of 125kSPS, and the Sinc1 block output data rate can be varied to control the final ADC output data rate. Figure 24 shows the frequency domain response of the Sinc5 + Sinc1 filter at an ODR of 50SPS. The Sinc5 + Sinc1 filter has a slow roll-off over frequency and narrow notches.

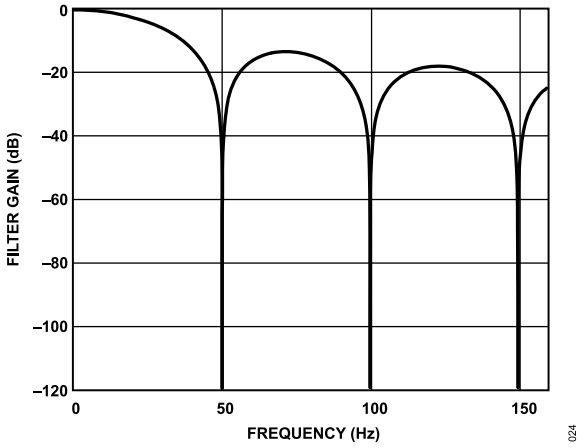


Figure 24. Sinc5 + Sinc1 Filter Response at 50SPS ODR

The output data rates with the accompanying settling time and rms noise for the Sinc5 + Sinc1 filter are shown in Table 7.

SINC3 FILTER

The Sinc3 filter achieves the best single-channel noise performance at lower rates and is, therefore, most suitable for single-channel applications. The Sinc3 filter always has a settling time equal to:

t_{SETTLE} = 3/*Output Data Rate*

Figure 25 shows the frequency domain filter response for the Sinc3 filter. The Sinc3 filter has good roll-off over frequency and has wide notches for good notch frequency rejection.

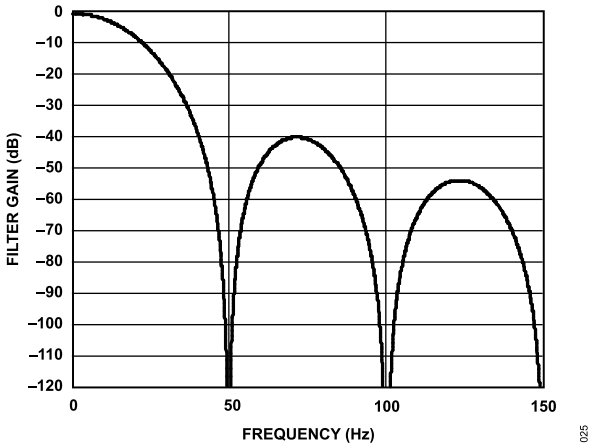


Figure 25. Sinc3 Filter Response

The output data rates with the accompanying settling time and rms noise for the Sinc3 filter are shown in Table 8. It is possible to fine tune the output data rate for the Sinc3 filter by setting the SINC3_MAPx bit in the filter configuration registers. If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the Sinc3 filter. All other options are eliminated. The data rate when on a single channel can be calculated using the following equation:

Output Data Rate = f_{MOD}/(32 × *FILTCONx*[*14:0*])

where: f_{MOD} is the modulator rate (MCLK/2) and is equal to 4MHz. *FILTCONx*[*14:0*] are the contents on the filter configuration registers, excluding the MSB.

For example, an output data rate of 50SPS can be achieved with SINC3_MAPx enabled by setting the FILTCONx[14:0] bits to a value of 2500.

SINGLE-CYCLE SETTLING

The AD4113 can be configured by setting the SING_CYC bit in the ADC mode register so that only fully settled data is output, effectively putting the ADC into a single-cycle settling mode. This mode achieves single-cycle settling by reducing the output data rate to be equal to the settling time of the ADC for the selected output data rate. This bit has no effect with the Sinc5 + Sinc1 filter at output data rates of ≤10kSPS and has no effect when multiple channels are enabled.

Figure 26 shows a step on the analog input with single-cycle settling mode disabled and the Sinc3 filter selected. The analog input requires at least three cycles after the step change for the output to reach the final settled value.

DIGITAL FILTER

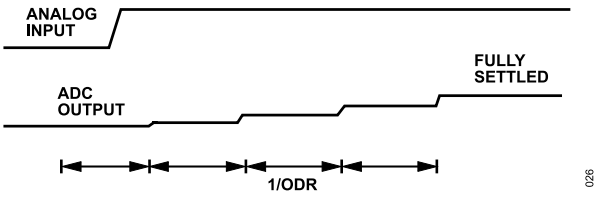


Figure 26. Step Input without Single-Cycle Settling

Figure 27 shows the same step on the analog input but with single-cycle settling enabled. The analog input requires at least a single-cycle for the output to be fully settled. The output data rate, as indicated by the $\overline{RDY}$ signal, is now reduced to equal the settling time of the filter at the selected output data rate.

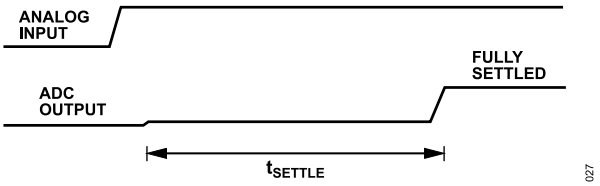


Figure 27. Step Input with Single-Cycle Settling

ENHANCED 50HZ AND 60HZ REJECTION FILTERS

The enhanced filters provide rejection of 50Hz and 60Hz simultaneously and allow the user to trade off settling time and rejection. These filters can operate up to 27.27SPS or can reject up to 90dB of 50Hz ± 1Hz and 60Hz ± 1Hz interference. These filters are operated by postfiltering the output of the Sinc5 + Sinc1 filter. For this reason, the Sinc5 + Sinc1 filter must be selected when using the enhanced filters to achieve the specified settling time and noise performance. Table 18 shows the output data rates with the accompanying settling time, rejection, and rms noise. Figure 28 to Figure 35 show the frequency domain plots of the responses from the enhanced filters.

Table 18. Enhanced Filters Output Data Rate, Voltage Input Noise, Settling Time, and Rejection Using the Enhanced Filters

Output Data Rate (SPS)	Settling Time (ms)	Simultaneous Rejection of 50Hz ± 1Hz and 60Hz ± 1 Hz (dB)[1]	Noise (µV rms)	Peak-to-Peak Resolution (Bits)	Comments
27.27	36.67	47	6.44	16	See Figure 28 and Figure 31
25	40.0	62	6.09	16	See Figure 29 and Figure 32
20	50.0	85	5.54	16	See Figure 30 and Figure 33
16.667	60.0	90	5.38	16	See Figure 34 and Figure 35

[1] MCLK = 2.00MHz.

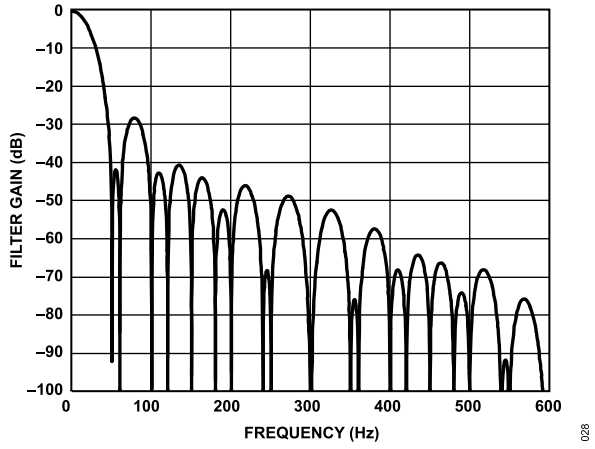


Figure 28. 27.27SPS ODR, 36.67ms Settling Time

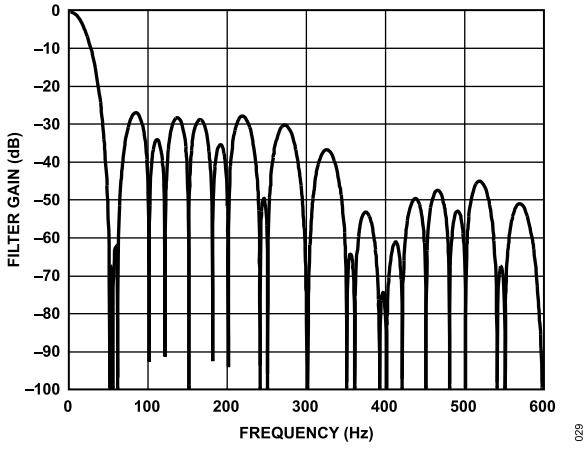


Figure 29. 25SPS ODR, 40ms Settling Time

DIGITAL FILTER

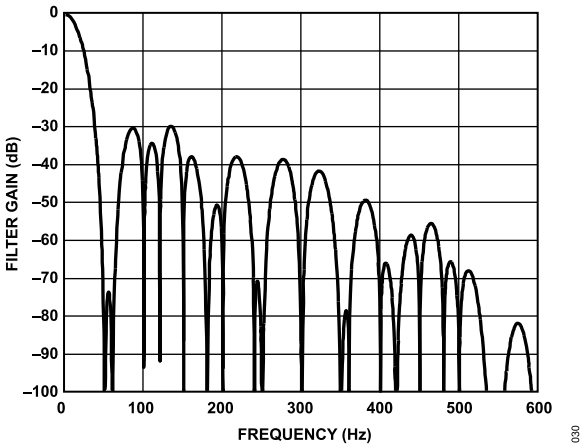


Figure 30. 20SPS ODR, 50ms Settling Time

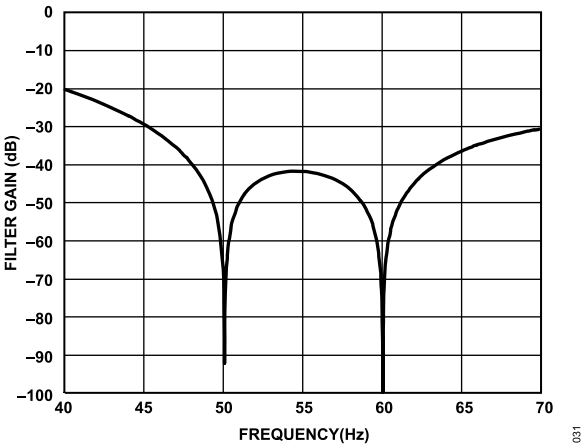


Figure 31. 27.27SPS ODR, 36.67ms Settling Time (40Hz to 70Hz)

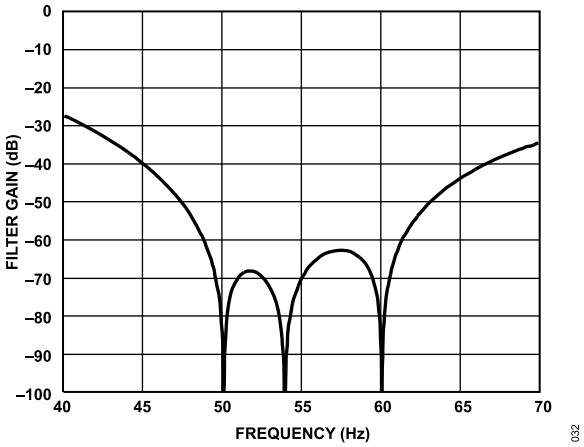


Figure 32. 25SPS ODR, 40ms Settling Time (40Hz to 70Hz)

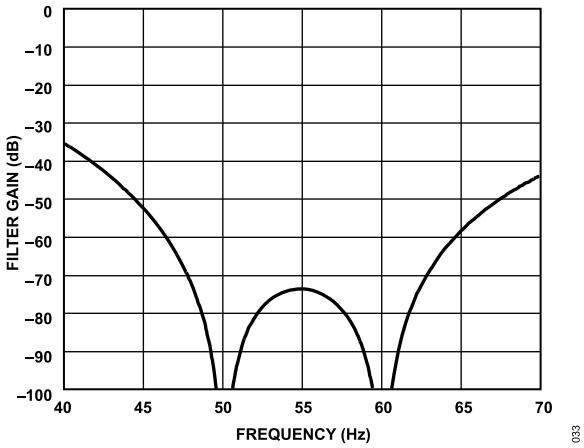


Figure 33. 20SPS ODR, 50ms Settling Time (40Hz to 70Hz)

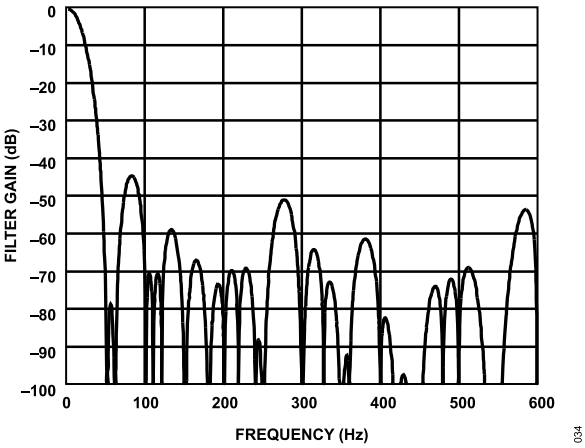


Figure 34. 16.667SPS ODR, 60ms Settling Time

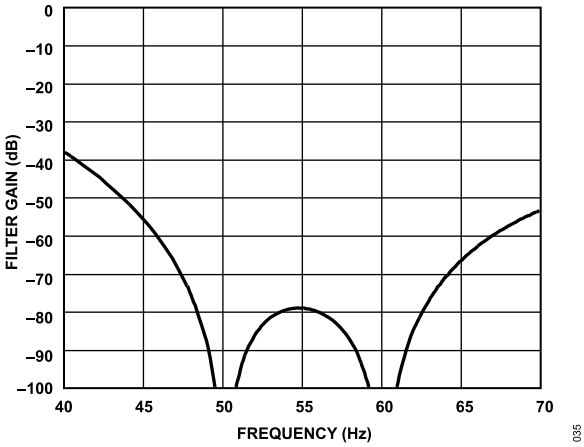


Figure 35. 16.667SPS ODR, 60ms Settling Time (40Hz to 70Hz)

OPERATING MODES

The AD4113 has a number of operating modes that can be set from the ADC and interface mode registers (see Table 22 and Table 23). These modes are as follows:

- Continuous conversion mode
- Continuous read mode
- Single conversion mode
- Standby mode
- Power-down mode
- Calibration modes (four) mode

CONTINUOUS CONVERSION MODE

Continuous conversion mode is the default power-up mode. The AD4113 converts continuously, and the $\overline{RDY}$ bit in the status register goes low each time a conversion is complete. If $\overline{CS}$ is low, the $\overline{RDY}$ output also goes low when a conversion is complete. To read a conversion, write to the communications register to indicate that the next operation is a read of the data register. When the data-word is read from the data register, the DOUT/$\overline{RDY}$ pin goes high. The user can read this register additional times, if required. However, ensure that the data register is not being accessed at the completion of the next conversion. Otherwise, the new conversion word is lost.

When several channels are enabled, the ADC automatically sequences through the enabled channels, performing one conversion on each channel. When all the channels are converted, the sequence starts again with the first channel. The channels are converted in a sequence from the lowest enabled channel to the highest enabled channel. The data register is updated as soon as each conversion is available. The $\overline{RDY}$ output pulses low each time a conversion is available. The user can then read the conversion while the ADC converts the next enabled channel.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion data, are output each time the data register is read. The four LSBs of the status register indicate that the channel to which the conversion corresponds.

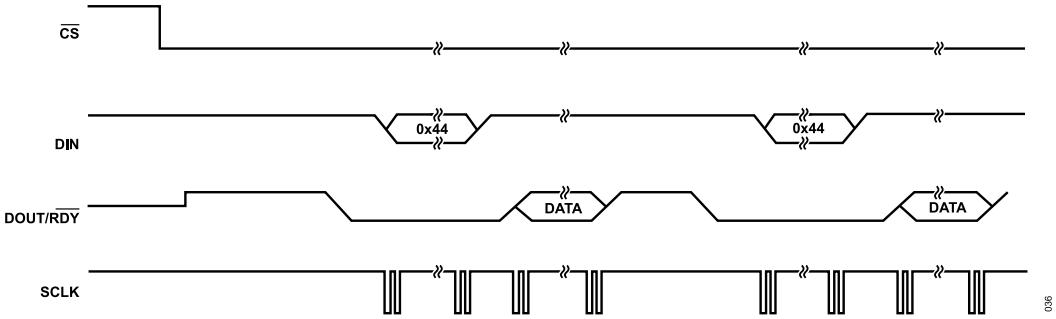


Figure 36. Continuous Conversion Mode

CONTINUOUS READ MODE

In continuous read mode, it is not required to write to the communications register before reading ADC data. Apply only the required number of SCLKs after the $\overline{RDY}$ output goes low to indicate the end of a conversion. When the conversion is read, the $\overline{RDY}$ output returns high until the next conversion is available. In this mode, the data can be read only once. Ensure that the data-word is read before the next conversion is complete. If the user has not read the conversion before the completion of the next conversion or if insufficient serial clocks are applied to the AD4113 to read the data-word, the serial output register is reset shortly before the next conversion is complete, and the new conversion is placed in the output serial register. The ADC must be configured for continuous conversion mode to use continuous read mode. To enable continuous read mode, set the CONTREAD bit in the interface mode register. When this bit is set, the only serial interface operations possible are reads from the data register. To exit continuous read mode, issue a dummy read of the ADC data register command (0x44) while the $\overline{RDY}$ output is low. Alternatively, apply a software reset, that is, 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1. This resets the ADC and all register contents. These are the only commands that the interface recognizes after it is placed in continuous read mode. Hold DIN low in continuous read mode until an instruction is to be written to the device.

If multiple ADC channels are enabled, each channel is output in turn, with the status bits being appended to the data if the DATA_STAT bit is set in the interface mode register. The status register indicates the channel to which the conversion corresponds.

OPERATING MODES

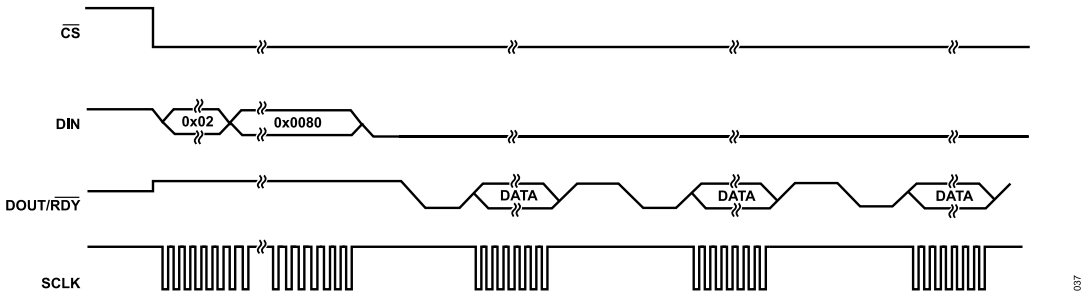


Figure 37. Continuous Read Mode

SINGLE CONVERSION MODE

In single conversion mode, the AD4113 performs a single conversion and is placed in standby mode after the conversion is complete. The RDY output goes low to indicate the completion of a conversion. When the data-word is read from the data register, the RDY output goes high. The data register can be read several times, if required, even when the RDY output goes high.

If several channels are enabled, the ADC automatically sequences through the enabled channels and performs a conversion on each channel. When a conversion starts, the RDY output goes high and remains high until a valid conversion is available and CS is low.

When the conversion is available, the RDY output goes low. The ADC then selects the next channel and begins a conversion. The user can read the present conversion while the next conversion is being performed. When the next conversion is complete, the data register is updated. Therefore, the user has a limited period in which to read the conversion. When the ADC has performed a single conversion on each of the selected channels, it returns to standby mode.

If the DATA_STAT bit in the interface mode register is set to 1, the contents of the status register, along with the conversion, are output each time the data register is read. The two LSBs of the status register indicate the channel to which the conversion corresponds.

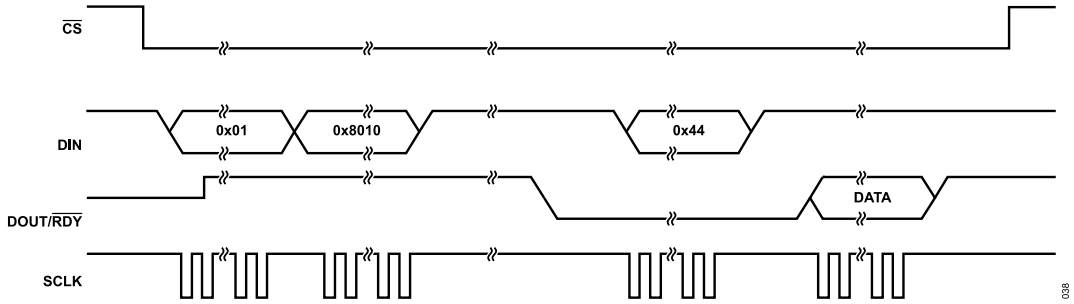


Figure 38. Single Conversion Mode

STANDBY AND POWER-DOWN MODES

In standby mode, most blocks are powered down. The LDO regulators remain active so that the registers maintain their contents. The crystal oscillator remains active if selected. To power down the clock in standby mode, set the CLOCKSEL bits in the ADC mode register to 00 (internal oscillator mode).

In power-down mode, all blocks are powered down, including the LDO regulators. All registers lose their contents, and the GPIO outputs are placed in three-state. To prevent accidental entry to power-down mode, the ADC must first be placed in standby mode. Exiting power-down mode requires 64 SCLKs with CS = 0 and DIN = 1, that is, a serial interface reset. A delay of 500µs is recommended before issuing a subsequent serial interface command to allow the LDO regulator to power up.

OPERATING MODES

CALIBRATION

The AD4113 allows a two-point calibration to be performed to eliminate any offset and gain errors. Four calibration modes are used to eliminate these offset and gain errors on a per setup basis:

- Internal zero-scale mode
- Internal full-scale mode
- System zero-scale mode
- System full-scale mode

Only one channel can be active during calibration. After each conversion, the ADC conversion result is scaled using the ADC calibration registers before being written to the data register.

The default value of the offset register is 0x8000, and the nominal value of the gain register can vary from 0x5000 to 0x5FFF. The following equations show the calculations that are used. In unipolar mode, the ideal relationship for a voltage input is:

$$Data = ((0.075 \times V_{IN})/V_{REF}) \times 2^{15} - (Offset - 0x8000)) \times (Gain/0x4000) \times 2$$

In bipolar mode, the ideal relationship for a voltage input is:

$$Data = ((0.075 \times V_{IN})/V_{REF}) \times 2^{15} - (Offset - 0x8000)) \times (Gain/0x4000) + 0x8000$$

To start a calibration, write the relevant value to the mode bits in the ADC mode register. The DOUT/$\overline{RDY}$ pin and the $\overline{RDY}$ bit in the status register go high when the calibration initiates. When the calibration is complete, the contents of the corresponding offset or gain register update, the $\overline{RDY}$ bit in the status register resets and the $\overline{RDY}$ output pin returns low (if $\overline{CS}$ is low), and the AD4113 reverts to standby mode.

During an internal offset calibration, both modulator inputs are connected internally to the selected negative analog input pin. Therefore, it is necessary to ensure that the voltage on the selected negative analog input pin does not exceed the allowed limits and is free from excessive noise and interference. To perform an internal full-scale calibration, a full-scale input voltage is automatically connected to the ADC input for this calibration.

However, for system calibrations, the system zero-scale (offset) and system full-scale (gain) voltages must be applied to the ADC pins before initiating the calibration modes. As a result, errors external to the AD4113 are removed. The calibration range of the ADC gain for a system full-scale calibration on a voltage input is from 3.75 × V_{REF} to 10.5 × V_{REF}. However, if 10.5 × V_{REF} is greater than the absolute input voltage specification for the applied AVDD, use the specification as the upper limit instead of 10.5 × V_{REF} (see the Specifications section).

An internal zero-scale calibration only removes the offset error of the ADC core. It does not remove error from the resistive front end. A system zero-scale calibration reduces the offset error to the order of the noise on that channel.

From an operational point of view, treat a calibration as another ADC conversion. An offset calibration, if required, must always be performed before a full-scale calibration. Set the system software to monitor the $\overline{RDY}$ bit in the status register or the $\overline{RDY}$ output to determine the end of a calibration by a polling sequence or an interrupt driven routine. All calibrations require a time equal to the settling time of the selected filter and output data rate to be completed.

Any calibration can be performed at any output data rate. Using lower output data rates results in better calibration accuracy and is accurate for all output data rates. A new offset calibration is required for a given channel if the reference source for that channel is changed.

The AD4113 provides the user with access to the on-chip calibration registers, which allow the microprocessor to read the calibration coefficients of the device and to write its own calibration coefficients. A read or write of the offset and gain registers can be performed at any time except during an internal calibration or self calibration.

DIGITAL INTERFACE

The programmable functions of the AD4113 are controlled via the SPI serial interface. The serial interface of the AD4113 consists of four signals: $\overline{CS}$, DIN, SCLK, and DOUT/$\overline{RDY}$. The DIN line transfers data into the on-chip registers, and DOUT output accesses data from the on-chip registers. SCLK is the serial clock input for the device, and all data transfers (either on DIN or on DOUT) occur with respect to the SCLK signal.

The DOUT/$\overline{RDY}$ pin also functions as a data-ready signal, with the line going low if $\overline{CS}$ is low when a new data-word is available in the data register. The pin is reset high when a read operation from the data register is complete. The $\overline{RDY}$ output also goes high before updating the data register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. Take care to avoid reading from the data register when $\overline{RDY}$ is about to go low. The best method to ensure that no data read occurs is to always monitor the $\overline{RDY}$ output. Start reading the data register as soon as $\overline{RDY}$ goes low, and ensure a sufficient SCLK rate, such that the read is completed before the next conversion result. $\overline{CS}$ is used to select a device. It can be used to decode the AD4113 in systems where several components are connected to the serial bus.

Figure 2 and Figure 3 show timing diagrams for interfacing to the AD4113 using $\overline{CS}$ to decode the device. Figure 2 shows the timing for a read operation from the AD4113, and Figure 3 shows the timing for a write operation to the AD4113. It is possible to read from the data register several times, even though the $\overline{RDY}$ output returns high after the first read operation. However, take care to ensure that the read operations are completed before the next output update occurs. In continuous read mode, the data register can be read only once.

The serial interface can operate in 3-wire mode by connecting $\overline{CS}$ low. In this case, the SCLK, DIN, and DOUT/$\overline{RDY}$ lines are used to communicate with the AD4113. The end of the conversion can also be monitored using the $\overline{RDY}$ bit in the status register.

The serial interface can be reset by writing 64 SCLKs with $\overline{CS}$ = 0 and DIN = 1. A reset returns the interface to the state in which it expects a write to the communications register. This operation resets the contents of all registers to their power-on values. Following a reset, allow a period of 500µs before addressing the serial interface.

CHECKSUM PROTECTION

The AD4113 has a checksum mode that can be used to improve interface robustness. Using the checksum ensures that only valid data is written to a register and allows data read from a register to be validated. If an error occurs during a register write, the CRC_ERROR bit is set in the status register. However, to ensure that the register write is successful, it is important to read back the register and verify the checksum.

For CRC checksum calculations during a write operation, the following polynomial is always used:

$x^8 + x^2 + x + 1$

During read operations, the user can select between this polynomial and a simpler, exclusive OR (XOR) function. The XOR function requires less time to process on the host microcontroller than the polynomial-based checksum. The CRC_EN bits in the interface mode register enable and disable the checksum and allow the user to select between the polynomial check and the simple XOR check.

The checksum is appended to the end of each read and write transaction. The checksum calculation for the write transaction is calculated using the 8-bit command word and the 8-bit to 16-bit data. For a read transaction, the checksum is calculated using the command word and the 8-bit to 24-bit data output. Figure 39 and Figure 40 show SPI write and read transactions, respectively.

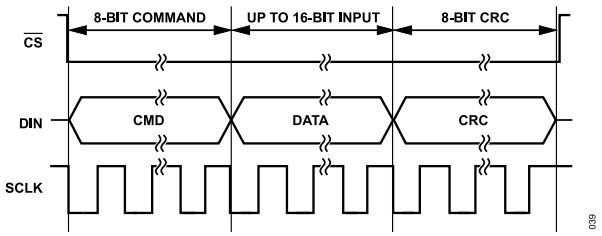


Figure 39. SPI Write Transaction with CRC

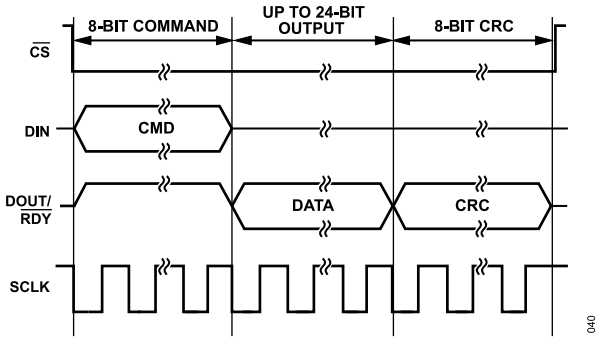


Figure 40. SPI Read Transaction with CRC

If checksum protection is enabled when continuous read mode is active, there is an implied read data command of 0x44 before every data transmission that must be accounted for when calculating the checksum value. This ensures a nonzero checksum value, even if the ADC data equals 0x0000.

CRC CALCULATION

Polynomial

The checksum, which is 8 bits wide, is generated using the following polynomial:

$x^8 + x^2 + x + 1$

To generate the checksum, the data is left shifted by 8 bits to create a number ending in 8 Logic 0s. The polynomial is aligned so that its MSB is adjacent to the leftmost Logic 1 of the data. An exclusive OR (XOR) function is applied to the data to produce a new, shorter

DIGITAL INTERFACE

number. The polynomial is again aligned so that its MSB is adjacent to the leftmost Logic 1 of the new result, and the procedure is repeated. This process is repeated until the original data is reduced to a value less than the polynomial. This is the 8-bit checksum.

Example of a Polynomial CRC Calculation—24-Bit Word: 0x654321 (8 Command Bits and 16-Bit Data)

An example of generating the 8-bit checksum using the polynomial based checksum is as follows:

```
Initial value      011001010100001100100001
                   011001010100001100100001000000000          left shifted 8 bits
x^8 + x^2 + x + 1 = 100000111                              polynomial
 100100100000110010000100000000          XOR result
 100000111                               polynomial
    100011000110010000100000000          XOR result
    100000111                            polynomial
        111111100100001000000000         XOR result
        100000111                        polynomial value
         111110111000010000000           XOR result
         100000111                       polynomial value
          111100000000100000000          XOR result
          100000111                      polynomial value
           111001110001000000000         XOR result
           100000111                     polynomial value
            110010010010000000000        XOR result
            100000111                    polynomial value
             100101010100000000          XOR result
             100000111                   polynomial value
                101101100000000          XOR result
                100000111                polynomial value
                  1101011000000          XOR result
                  100000111              polynomial value
                   101010110000          XOR result
                   100000111             polynomial value
                     1010001000          XOR result
                     100000111           polynomial value
                       10000110          checksum = 0x86
```

XOR Calculation

The checksum, which is 8 bits wide, is generated by splitting the data into bytes and then performing an XOR of the bytes.

Example of an XOR Calculation—24-Bit Word: 0x654321 (8 Command Bits and 16-Bit Data)

Using the previous example, divide into three bytes (0x65, 0x43, and 0x21), which results in the following XOR calculation:

```
01100101          0x65
01000011          0x43
00100110          XOR result
00100001          0x21
00000111          CRC
```

INTEGRATED FUNCTIONS

The AD4113 has a number of integrated functions.

GENERAL-PURPOSE OUTPUTS

The AD4113 has two general-purpose digital output pins (GPO0 and GPO1). The GPO pins are enabled using the following OP_EN0_1 bit in the GPIOCON register.

The GP_DATA0 bit and GP_DATA1 bit determine the logic level output at the pin, respectively. The logic levels for these pins are referenced to AVDD and AVSS. Therefore, outputs have an amplitude of either 5V or, depending on the AVDD − AVSS voltage.

The $\overline{\text{ERROR}}$ pin can also be used as a general-purpose output if the ERR_EN bits in the GPIOCON register are set to 11. In this configuration, the ERR_DAT bit in the GPIOCON register determines the logic level output at the $\overline{\text{ERROR}}$ pin. The logic level for the pin is referenced to IOVDD and DGND, and the $\overline{\text{ERROR}}$ pin has an active pull-up.

DELAY

It is possible to insert a programmable delay before the AD4113 begins taking samples. This delay allows an external amplifier or multiplexer to settle and can also alleviate the specification requirements for the external amplifier or multiplexer. Eight programmable settings, ranging from 0µs to 2ms, can be set using the delay bits in the ADCMODE register (Register 0x01, Bits[10:8]).

DOUT_RESET

The serial interface uses a shared DOUT/ $\overline{\text{RDY}}$ pin. By default, this pin outputs the $\overline{\text{RDY}}$ signal. During a data read, this pin outputs the data from the register being read. After the read is complete, the pin reverts to outputting the $\overline{\text{RDY}}$ signal after a short fixed period of time (t_7). However, this time may be too short for some microcontrollers and can be extended until the $\overline{\text{CS}}$ pin is brought high by setting the DOUT_RESET bit in the IFMODE register to 1. This setting means that $\overline{\text{CS}}$ must frame each read operation and compete the serial interface transaction.

SYNCHRONIZATION

Normal Synchronization

When the SYNC_EN bit in the GPIOCON register is set to 1, the $\overline{\text{SYNC}}$ pin functions as a synchronization pin. The $\overline{\text{SYNC}}$ input allows the user to reset the modulator and the digital filter without affecting any of the setup conditions on the device. This allows the user to start gathering samples of the analog input from a known point in time, that is, the rising edge of $\overline{\text{SYNC}}$. This pin must be low for at least one MCLK cycle to ensure that synchronization occurs. If multiple channels are enabled, the sequencer is reset to the first enabled channel.

If multiple AD4113 devices are operated from a common MCLK, they can be synchronized so that their data registers are updated simultaneously. The devices are normally synchronized after each AD4113 has performed its own calibration or has calibration coefficients loaded into its calibration registers. A falling edge on the $\overline{\text{SYNC}}$ pin resets the digital filter and the analog modulator and places the AD4113 into a consistent known state. While the $\overline{\text{SYNC}}$ pin is low, the AD4113 is maintained in this state. On the $\overline{\text{SYNC}}$ rising edge, the modulator and filter are taken out of this reset state, and on the next MCLK edge, the device starts to gather input samples again.

The device is taken out of reset on the MCLK falling edge following the $\overline{\text{SYNC}}$ low-to-high transition. Therefore, when multiple devices are being synchronized, take the $\overline{\text{SYNC}}$ pin high on the MCLK rising edge to ensure that all devices begin sampling on the MCLK falling edge. If the $\overline{\text{SYNC}}$ pin is not taken high in sufficient time, it is possible to have a difference of one MCLK cycle between the devices, that is, the instant at which conversions are available differs from device to device by a maximum of one MCLK cycle.

The $\overline{\text{SYNC}}$ input can also be used as a start conversion command for a single channel when in normal synchronization mode. In this mode, the rising edge of the $\overline{\text{SYNC}}$ input starts a conversion, and the falling edge of the $\overline{\text{RDY}}$ output indicates when the conversion is complete. The settling time of the filter is required for each data register update. After the conversion is complete, bring the $\overline{\text{SYNC}}$ input low in preparation for the next conversion start signal.

Alternate Synchronization

In alternate synchronization mode, the $\overline{\text{SYNC}}$ input operates as a start conversion command when several channels of the AD4113 are enabled. Setting the ALT_SYNC bit in the IFMODE register to 1 enables an alternate synchronization scheme. When the $\overline{\text{SYNC}}$ input goes low, the ADC completes the conversion on the current channel, selects the next channel in the sequence, and then waits until the $\overline{\text{SYNC}}$ input goes high to start the conversion. The $\overline{\text{RDY}}$ output goes low when the conversion is complete on the current channel, and the data register is updated with the corresponding conversion. Therefore, the $\overline{\text{SYNC}}$ input does not interfere with the sampling on the currently selected channel but allows the user to control the instant at which the conversion begins on the next channel in the sequence.

Alternate synchronization mode can be used only when several channels are enabled. It is not recommended to use this mode when a single channel is enabled.

ERROR FLAGS

The status register contains three error bits (ADC_ERROR, CRC_ERROR, and REG_ERROR) that flag errors with the ADC conversion, errors with the CRC check, and errors caused by changes in the registers, respectively. In addition, the $\overline{\text{ERROR}}$ output can indicate that an error has occurred.

ADC_ERROR

The ADC_ERROR bit in the status register flags any errors that occur during the conversion process. The flag is set when an

INTEGRATED FUNCTIONS

overrange or underrange result is output from the ADC. The ADC also outputs all 0s or all 1s when an undervoltage or overvoltage occurs. This flag is reset only when the overvoltage or undervoltage is removed. This flag is not reset by a read of the data register.

CRC_ERROR

If the CRC value that accompanies a write operation does not correspond with the information sent, the CRC_ERROR flag is set. The flag is reset as soon as the status register is explicitly read.

REG_ERROR

The REG_ERROR flag is used in conjunction with the REG_CHECK bit in the IFMODE register. When the REG_ CHECK bit is set, the AD4113 monitors the values in the on-chip registers. If a bit changes, the REG_ERROR bit is set to 1. Therefore, for writes to the on-chip registers, set the REG_ CHECK bit to 0. When the registers have been updated, the REG_CHECK bit can be set to 1. The AD4113 calculates a checksum of the on-chip registers. If one of the register values are changed, the REG_ERROR bit is set to 1. If an error is flagged, the REG_CHECK bit must be set to 0 to clear the REG_ERROR bit in the status register. The register check function does not monitor the data register, status register, or IFMODE register.

$\overline{\text{ERROR}}$ Input/Output

The $\overline{\text{ERROR}}$ pin functions as an error input/output pin or as a general-purpose output pin. The ERR_EN bits in the GPIOCON register determine the function of the pin.

When ERR_EN is set to 10, the $\overline{\text{ERROR}}$ pin functions as an open-drain error output. The three error bits in the status register (ADC_ERROR, CRC_ERROR, and REG_ERROR) are OR'ed, inverted, and mapped to the $\overline{\text{ERROR}}$ output. Therefore, the $\overline{\text{ERROR}}$ output indicates that an error has occurred. The status register must be read to identify the error source.

When ERR_EN is set to 01, the $\overline{\text{ERROR}}$ pin functions as an error input. The error output of another component can be connected to the AD4113 $\overline{\text{ERROR}}$ input so that the AD4113 indicates when an error occurs on either itself or the external component. The value on the $\overline{\text{ERROR}}$ input is inverted and OR'ed with the errors from the ADC conversion, and the result is indicated via the ADC_ERROR bit in the status register. The value of the $\overline{\text{ERROR}}$ input is reflected in the ERR_DAT bit in the GPIOCON register.

The $\overline{\text{ERROR}}$ input/output is disabled when ERR_EN is set to 00. When the ERR_EN bits are set to 11, the $\overline{\text{ERROR}}$ pin operates as a general-purpose output.

DATA_STAT

The contents of the status register can be appended to each conversion on the AD4113 using the DATA_STAT bit in the IFMODE register. This function is useful if several channels are enabled. Each time a conversion is output, the contents of the status register are appended. The two LSBs of the status register indicate to which channel the conversion corresponds. In addition, the user can determine if any errors are being flagged by the error bits.

IOSTRENGTH

The serial interface can operate with a power supply as low as 2V. However, at this low voltage, the DOUT/$\overline{\text{RDY}}$ pin may not have sufficient drive strength if there is moderate parasitic capacitance on the board or if the SCLK frequency is high. The IOSTRENGTH bit in the IFMODE register increases the drive strength of the DOUT/$\overline{\text{RDY}}$ pin.

INTERNAL TEMPERATURE SENSOR

The AD4113 has an integrated temperature sensor. The temperature sensor can be used as a guide for the ambient temperature at which the device is operating. The ambient temperature can be used for diagnostic purposes or as an indicator of when the application circuit must rerun a calibration routine to take into account a shift in operating temperature. The temperature sensor is selected using the multiplexer and is selected in the same way as an input channel.

The temperature sensor requires that the input buffers be enabled on both inputs and the internal reference be enabled.

To use the temperature sensor, the first step is to calibrate the device in a known temperature (25°C) and take a conversion as a reference point. The temperature sensor has a nominal sensitivity of 477µV/K. The difference in this ideal slope and the slope measured can calibrate the temperature sensor. The temperature sensor is specified with a ±2°C typical accuracy after calibration at 25°C. Calculate the temperature as follows:

Temperature (°C) = (*Conversion Result* ÷ 477µV) − 273.15

APPLICATIONS INFORMATION

GROUNDING AND LAYOUT

The inputs and reference inputs are differential and most of the voltages in the analog modulator are common-mode voltages. The high common-mode rejection of the device removes common-mode noise on these inputs. The analog and digital supplies to the AD4113 are independent and separately pinned out to minimize coupling between the analog and digital sections of the device. The digital filter provides rejection of broadband noise on the power supplies, except at integer multiples of the MCLK frequency.

The digital filter also removes noise from the analog inputs and reference inputs, provided that these noise sources do not saturate the analog modulator. As a result, the AD4113 is more immune to noise interference than a conventional high resolution converter. However, because the resolution of the AD4113 is high and the noise levels from the converter are so low, take care with regard to grounding and layout.

The PCB that houses the ADC must be designed so that the analog and digital sections are separated and confined to certain areas of the board. A minimum etch technique is recommended for ground planes because it results in the best shielding.

In any layout, the user must keep in mind the flow of currents in the system, which ensures that the paths for all return currents are as close as possible to the paths that the currents took to reach their destinations.

Avoid running digital lines under the device because this couples noise onto the die and allows the analog ground plane to run under the AD4113 to prevent noise coupling. The power supply lines to the AD4113 must use as wide a trace as possible to provide low impedance paths and reduce glitches on the power supply line. Shield fast switching signals, such as clocks with digital ground to prevent radiating noise to other sections of the board and never run clock signals near the inputs. Avoid crossover of digital and analog signals. Run traces on opposite sides of the board at right angles to each other. This layout reduces the effects of feedthrough on the board. A microstrip technique is recommended, but is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground planes, whereas signals are placed on the solder side.

Proper decoupling is important when using high resolution ADCs. The AD4113 has two power supply pins: AVDD and IOVDD. The AVDD pin is referenced to AVSS, and the IOVDD pin is referenced to DGND. Decouple AVDD with a 10µF tantalum capacitor in parallel with a 0.1µF capacitor to AVSS on each pin. Place the 0.1µF capacitor as near as possible to the device on each supply, ideally right up against the device. Decouple IOVDD with a 10µF tantalum capacitor, in parallel with a 0.1µF capacitor to DGND. Decouple all inputs to AVSS. If an external reference is used, decouple the REF+ and REF− pins to AVSS.

The AD4113 also has two on-board LDO regulators: one that regulates the AVDD supply, and one that regulates the IOVDD supply. For the REGCAPA pin, it is recommended to use 1µF and 0.1µF capacitors to AVSS. Similarly, for the REGCAPD pin, it is recommended to use 1µF and 0.1µF capacitors to DGND.

REGISTER SUMMARY

This section contains details about the functions of each of the bit fields. The access column in the register tables specifies that the bit fields are read-only (R) and read/write (R/W) bits.

Table 19. Register Summary

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x00	COMMS	[7:0]	$\overline{WEN}$	R/$\overline{W}$	RA						0x00	W
0x00	Status	[7:0]	$\overline{RDY}$	ADC_ERROR	CRC_ERROR	REG_ERROR	Channel				0x80	R
0x01	ADCMODE	[15:8]	REF_EN	Reserved	SING_CYC	Reserved		Delay			0x2000	R/W
		[7:0]	Reserved	Mode			CLOCKSEL		Reserved			
0x02	IFMODE	[15:8]	Reserved			ALT_SYNC	IOSTRENGTH	Reserved		DOUT_RESET	0x0000	R/W
		[7:0]	CONTREAD	DATA_STAT	REG_CHECK	Reserved	CRC_EN		Reserved			
0x03	REGCHECK	[23:16]	REGISTER_CHECK[23:16]								0x000000	R
		[15:8]	REGISTER_CHECK[15:8]									
		[7:0]	REGISTER_CHECK[7:0]									
0x04	Data	[15:8]	Data[15:8]								0x0000	R
		[7:0]	Data[7:0]									
0x06	GPIOCON	[15:8]	Reserved		OP_EN0_1	OW_EN	SYNC_EN	ERR_EN		ERR_DAT	0x0800	R/W
		[7:0]	GP_DATA1	GP_DATA0	Reserved							
0x07	ID	[15:8]	ID[15:8]								0x39Dx	R
		[7:0]	ID[7:0]									
0x10	CH0	[15:8]	CH_EN0	SETUP_SEL0			Reserved		INPUT0[9:8]		0x8001	R/W
		[7:0]	INPUT0[7:0]									
0x11	CH1	[15:8]	CH_EN1	SETUP_SEL1			Reserved		INPUT1[9:8]		0x0001	R/W
		[7:0]	INPUT1[7:0]									
0x12	CH2	[15:8]	CH_EN2	SETUP_SEL2			Reserved		INPUT2[9:8]		0x0001	R/W
		[7:0]	INPUT2[7:0]									
0x13	CH3	[15:8]	CH_EN3	SETUP_SEL3			Reserved		INPUT3[9:8]		0x0001	R/W
		[7:0]	INPUT3[7:0]									
0x14	CH4	[15:8]	CH_EN4	SETUP_SEL4			Reserved		INPUT4[9:8]		0x0001	R/W
		[7:0]	INPUT4[7:0]									
0x15	CH5	[15:8]	CH_EN5	SETUP_SEL5			Reserved		INPUT5[9:8]		0x0001	R/W
		[7:0]	INPUT5[7:0]									
0x16	CH6	[15:8]	CH_EN6	SETUP_SEL6			Reserved		INPUT6[9:8]		0x0001	R/W
		[7:0]	INPUT6[7:0]									
0x17	CH7	[15:8]	CH_EN7	SETUP_SEL7			Reserved		INPUT7[9:8]		0x0001	R/W
		[7:0]	INPUT7[7:0]									
0x18	CH8	[15:8]	CH_EN8	SETUP_SEL8			Reserved		INPUT8[9:8]		0x0001	R/W
		[7:0]	INPUT8[7:0]									
0x19	CH9	[15:8]	CH_EN9	SETUP_SEL9			Reserved		INPUT9[9:8]		0x0001	R/W
		[7:0]	INPUT9[7:0]									
0x1A	CH10	[15:8]	CH_EN10	SETUP_SEL10			Reserved		INPUT10[9:8]		0x0001	R/W
		[7:0]	INPUT10[7:0]									
0x1B	CH11	[15:8]	CH_EN11	SETUP_SEL11			Reserved		INPUT11[9:8]		0x0001	R/W
		[7:0]	INPUT11[7:0]									
0x1C	CH12	[15:8]	CH_EN12	SETUP_SEL12			Reserved		INPUT12[9:8]		0x0001	R/W
		[7:0]	INPUT12[7:0]									

REGISTER SUMMARY

Table 19. Register Summary (Continued)

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
0x1D	CH13	[15:8]	CH_EN13	SETUP_SEL13			Reserved		INPUT13[9:8]		0x0001	R/W
		[7:0]	INPUT13[7:0]									
0x1E	CH14	[15:8]	CH_EN14	SETUP_SEL14			Reserved		INPUT14[9:8]		0x0001	R/W
		[7:0]	INPUT14[7:0]									
0x1F	CH15	[15:8]	CH_EN15	SETUP_SEL15			Reserved		INPUT15[9:8]		0x0001	R/W
		[7:0]	INPUT15[7:0]									
0x20	SETUPCON0	[15:8]	Reserved			BI_UNIPOLAR0	REFBUF0+	REFBUF0−	INBUF0		0x1000	R/W
		[7:0]	Reserved		REF_SEL0		Reserved					
0x21	SETUPCON1	[15:8]	Reserved			BI_UNIPOLAR1	REFBUF1+	REFBUF1−	INBUF1		0x1000	R/W
		[7:0]	Reserved		REF_SEL1		Reserved					
0x22	SETUPCON2	[15:8]	Reserved			BI_UNIPOLAR2	REFBUF2+	REFBUF2−	INBUF2		0x1000	R/W
		[7:0]	Reserved		REF_SEL2		Reserved					
0x23	SETUPCON3	[15:8]	Reserved			BI_UNIPOLAR3	REFBUF3+	REFBUF3−	INBUF3		0x1000	R/W
		[7:0]	Reserved		REF_SEL3		Reserved					
0x24	SETUPCON4	[15:8]	Reserved			BI_UNIPOLAR4	REFBUF4+	REFBUF4−	INBUF4		0x1000	R/W
		[7:0]	Reserved		REF_SEL4		Reserved					
0x25	SETUPCON5	[15:8]	Reserved			BI_UNIPOLAR5	REFBUF5+	REFBUF5−	INBUF5		0x1000	R/W
		[7:0]	Reserved		REF_SEL5		Reserved					
0x26	SETUPCON6	[15:8]	Reserved			BI_UNIPOLAR6	REFBUF6+	REFBUF6−	INBUF6		0x1000	R/W
		[7:0]	Reserved		REF_SEL6		Reserved					
0x27	SETUPCON7	[15:8]	Reserved			BI_UNIPOLAR7	REFBUF7+	REFBUF7−	INBUF7		0x1000	R/W
		[7:0]	Reserved		REF_SEL7		Reserved					
0x28	FILTCON0	[15:8]	SINC3_MAP0	Reserved			ENHFILTEN0	ENHFILT0			0x0500	R/W
		[7:0]	Reserved	ORDER0		ODR0						
0x29	FILTCON1	[15:8]	SINC3_MAP1	Reserved			ENHFILTEN1	ENHFILT1			0x0500	R/W
		[7:0]	Reserved	ORDER1		ODR1						
0x2A	FILTCON2	[15:8]	SINC3_MAP2	Reserved			ENHFILTEN2	ENHFILT2			0x0500	R/W
		[7:0]	Reserved	ORDER2		ODR2						
0x2B	FILTCON3	[15:8]	SINC3_MAP3	Reserved			ENHFILTEN3	ENHFILT3			0x0500	R/W
		[7:0]	Reserved	ORDER3		ODR3						
0x2C	FILTCON4	[15:8]	SINC3_MAP4	Reserved			ENHFILTEN4	ENHFILT4			0x0500	R/W
		[7:0]	Reserved	ORDER4		ODR4						
0x2D	FILTCON5	[15:8]	SINC3_MAP5	Reserved			ENHFILTEN5	ENHFILT5			0x0500	R/W
		[7:0]	Reserved	ORDER5		ODR5						
0x2E	FILTCON6	[15:8]	SINC3_MAP6	Reserved			ENHFILTEN6	ENHFILT6			0x0500	R/W

REGISTER SUMMARY

Table 19. Register Summary (Continued)

Reg.	Name	Bits	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset	Access
		[7:0]	Reserved	ORDER6		ODR6						
0x2F	FILTCON7	[15:8]	SINC3_MAP7	Reserved			ENHFILTEN7	ENHFILT7			0x0500	R/W
		[7:0]	Reserved	ORDER7		ODR7						
0x30	OFFSET0	[15:0]	OFFSET0[15:0]								0x8000	R/W
0x31	OFFSET1	[15:0]	OFFSET1[15:0]								0x8000	R/W
0x32	OFFSET2	[15:0]	OFFSET2[15:0]								0x8000	R/W
0x33	OFFSET3	[15:0]	OFFSET3[15:0]								0x8000	R/W
0x34	OFFSET4	[15:0]	OFFSET4[15:0]								0x8000	R/W
0x35	OFFSET5	[15:0]	OFFSET5[15:0]								0x8000	R/W
0x36	OFFSET6	[15:0]	OFFSET6[15:0]								0x8000	R/W
0x37	OFFSET7	[15:0]	OFFSET7[15:0]								0x8000	R/W
0x38	GAIN0	[15:0]	GAIN0[15:0]								0x5XXX	R/W
0x39	GAIN1	[15:0]	GAIN1[15:0]								0x5XXX	R/W
0x3A	GAIN2	[15:0]	GAIN2[15:0]								0x5XXX	R/W
0x3B	GAIN3	[15:0]	GAIN3[15:0]								0x5XXX	R/W
0x3C	GAIN4	[15:0]	GAIN4[15:0]								0x5XXX	R/W
0x3D	GAIN5	[15:0]	GAIN5[15:0]								0x5XXX	R/W
0x3E	GAIN6	[15:0]	GAIN6[15:0]								0x5XXX	R/W
0x3F	GAIN7	[15:0]	GAIN7[15:0]								0x5XXX	R/W

REGISTER DETAILS

COMMUNICATIONS REGISTER

Address: 0x00, Reset: 0x00, Name: COMMS

All access to the on-chip registers must start with a write to the communications register. This write determines which register is accessed next and whether that operation is a write or a read.

Table 20. Bit Descriptions for COMMS

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{WEN}$		This bit must be low to begin communications with the ADC.	0x0	W
6	R/$\overline{W}$		This bit determines if the command is a read or write operation.	0x0	W
		0	Write command.		
		1	Read command.		
[5:0]	RA		The register address bits determine the register to be read from or written to as part of the current communication.	0x00	W
		000000	Status register.		
		000001	ADC mode register.		
		000010	Interface mode register.		
		000011	Register checksum register.		
		000100	Data register.		
		000110	GPIO configuration register.		
		000111	ID register.		
		010000	Channel 0 register.		
		010001	Channel 1 register.		
		010010	Channel 2 register.		
		010011	Channel 3 register.		
		010100	Channel 4 register.		
		010101	Channel 5 register.		
		010110	Channel 6 register.		
		010111	Channel 7 register.		
		011000	Channel 8 register.		
		011001	Channel 9 register.		
		011010	Channel 10 register.		
		011011	Channel 11 register.		
		011100	Channel 12 register.		
		011101	Channel 13 register.		
		011110	Channel 14 register.		
		011111	Channel 15 register.		
		100000	Setup Configuration 0 register.		
		100001	Setup Configuration 1 register.		
		100010	Setup Configuration 2 register.		
		100011	Setup Configuration 3 register.		
		100100	Setup Configuration 4 register.		
		100101	Setup Configuration 5 register.		
		100110	Setup Configuration 6 register.		
		100111	Setup Configuration 7 register.		
		101000	Filter Configuration 0 register.		
		101001	Filter Configuration 1 register.		
		101010	Filter Configuration 2 register.		
		101011	Filter Configuration 3 register.		
		101100	Filter Configuration 4 register.		

REGISTER DETAILS

Table 20. Bit Descriptions for COMMS (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		101101	Filter Configuration 5 register.		
		101110	Filter Configuration 6 register.		
		101111	Filter Configuration 7 register.		
		110000	Offset 0 register.		
		110001	Offset 1 register.		
		110010	Offset 2 register.		
		110011	Offset 3 register.		
		110100	Offset 4 register.		
		110101	Offset 5 register.		
		110110	Offset 6 register.		
		110111	Offset 7 register.		
		111000	Gain 0 register.		
		111001	Gain 1 register.		
		111010	Gain 2 register.		
		111011	Gain 3 register.		
		111100	Gain 4 register.		
		111101	Gain 5 register.		
		111110	Gain 6 register.		
		111111	Gain 7 register.		

STATUS REGISTER

Address: 0x00, Reset: 0x80, Name: Status

The status register is an 8-bit register that contains ADC and serial interface status information. The register can optionally be appended to the data register by setting the DATA_STAT bit in the interface mode register.

Table 21. Bit Descriptions for Status

Bits	Bit Name	Settings	Description	Reset	Access
7	$\overline{\text{RDY}}$		The status of $\overline{\text{RDY}}$ is output to the DOUT/$\overline{\text{RDY}}$ pin when $\overline{\text{CS}}$ is low and a register is not being read. This bit goes low when the ADC writes a new result to the data register. In ADC calibration modes, this bit goes low when the ADC writes the calibration result. $\overline{\text{RDY}}$ is brought high automatically by a read of the data register.	0x1	R
		0	New data result available.		
		1	Awaiting new data result.		
6	ADC_ERROR		By default, this bit indicates if an ADC overrange or underrange occurred. The ADC result is clamped to 0xFFFF for overrange errors and 0x0000 for underrange errors. This bit is updated when the ADC result is written and is cleared at the next update after removing the overrange or underrange condition.	0x0	R
		0	No error.		
		1	Error.		
5	CRC_ERROR		This bit indicates if a CRC error occurred during a register write. For register reads, the host microcontroller determines if a CRC error occurred. This bit is cleared by a read of this register.	0x0	R
		0	No error.		
		1	CRC error.		
4	REG_ERROR		This bit indicates if the content of one of the internal registers changes from the value calculated when the register integrity check is activated. The check is activated by setting the REG_CHECK bit in the interface mode register. This bit is cleared by clearing the REG_CHECK bit.	0x0	R
		0	No error.		

REGISTER DETAILS

Table 21. Bit Descriptions for Status (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		1	Error.		
[3:0]	Channel		These bits indicate which channel is active for the ADC conversion whose result is currently in the data register. This may be different from the channel currently being converted. The mapping is a direct map from the channel register. Therefore, Channel 0 results in 0x0 and Channel 15 results in 0xF.	0x0	R
		0000	Channel 0.		
		0001	Channel 1.		
		0010	Channel 2.		
		0011	Channel 3.		
		0100	Channel 4.		
		0101	Channel 5.		
		0110	Channel 6.		
		0111	Channel 7.		
		1000	Channel 8.		
		1001	Channel 9.		
		1010	Channel 10.		
		1011	Channel 11.		
		1100	Channel 12.		
		1101	Channel 13.		
		1110	Channel 14.		
		1111	Channel 15.		

ADC MODE REGISTER

Address: 0x01, Reset: 0x2000, Name: ADCMODE

The ADC mode register controls the operating mode of the ADC and the MCLK selection. A write to the ADC mode register resets the filter and the bits and starts a new conversion or calibration.

Table 22. Bit Descriptions for ADCMODE

Bits	Bit Name	Settings	Description	Reset	Access
15	REF_EN		Enables internal reference and outputs a buffered 2.5V to the REFOUT pin.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
14	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
13	SING_CYC		This bit can be used when only a single channel is active to set the ADC to only output at the settled filter data rate.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
[12:11]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
[10:8]	Delay		These bits allow a programmable delay to be added after a channel switch to allow the settling of external circuitry before the ADC starts processing its input.	0x0	R/W
		000	0µs.		
		001	8µs.		
		010	32µs.		
		011	80µs.		
		100	200µs.		
		101	400µs.		
		110	1ms.		
		111	2ms.		

REGISTER DETAILS

Table 22. Bit Descriptions for ADCMODE (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		This bit is reserved. Set this bit to 0.	0x0	R
[6:4]	Mode		These bits control the operating mode of the ADC. For more details, see the Operating Modes and Configuration Overview sections.	0x0	R/W
		000	Continuous conversion mode.		
		001	Single conversion mode.		
		010	Standby mode.		
		011	Power-down mode.		
		100	Internal offset calibration.		
		110	System offset calibration.		
		111	System gain calibration.		
[3:2]	CLOCKSEL		These bits select the ADC clock source. Selecting the internal oscillator also enables the internal oscillator.	0x0	R/W
		00	Internal oscillator.		
		01	Internal oscillator output on the XTAL2/CLKIO pin.		
		10	External clock input on the XTAL2/CLKIO pin.		
		11	External crystal on the XTAL1 pin and the XTAL2/CLKIO pin.		
[1:0]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R

INTERFACE MODE REGISTER

Address: 0x02, Reset: 0x0000, Name: IFMODE

The interface mode register configures various serial interface options.

Table 23. Bit Descriptions for IFMODE

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
12	ALT_SYNC		This bit enables a different behavior of the $\overline{SYNC}$ pin to allow the use of $\overline{SYNC}$ as a control for conversions when cycling channels.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
11	IOSTRENGTH		This bit controls the drive strength of the DOUT/$\overline{RDY}$ pin. Set this bit when reading from the serial interface at high speed with a low IOVDD supply and moderate capacitance.	0x0	R/W
		0	Disabled (default).		
		1	Enabled.		
[10:9]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
8	DOUT_RESET			0x0	R/W
		0	Disabled.		
		1	Enabled.		
7	CONTREAD		This bit enables the continuous read mode of the ADC data register. The ADC must be configured in continuous conversion mode to use continuous read mode. For more details, see the Operating Modes section.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
6	DATA_STAT		This bit enables the status register to be appended to the data register when read so that channel and status information are transmitted with the data. This is the only way to be sure that the channel bits read from the status register correspond to the data in the data register.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
5	REG_CHECK		This bit enables a register integrity checker, which can be used to monitor any change in the value of the user registers. To use this feature, configure all other registers as desired with this bit cleared.	0x0	R/W

REGISTER DETAILS

Table 23. Bit Descriptions for IFMODE (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
			Then, write to this register to set the REG_CHECK bit to 1. If the contents of any of the registers change, the REG_ERROR bit is set in the status register. To clear the error, set the REG_CHECK bit to 0. Neither the interface mode register nor the ADC data or status registers are included in the registers that are checked. If a register must have a new value written, this bit must first be cleared. Otherwise, an error is flagged when the new register contents are written.		
		0	Disabled.		
		1	Enabled.		
4	Reserved		This bit is reserved. Set this bit to 0.	0x0	R
[3:2]	CRC_EN		These bits enable CRC protection of register reads and writes. CRC increases the number of bytes in a serial interface transfer by one.	0x00	R/W
		00	Disabled.		
		01	XOR checksum enabled for register read transactions. Register writes still use CRC with these bits set.		
		10	CRC checksum enabled for read and write transactions.		
[1:0]	Reserved		This bit is reserved. Set this bit to 0.	0x0	R

REGISTER CHECK

Address: 0x03, Reset: 0x000000, Name: REGCHECK

The register check register is a 24-bit checksum calculated by exclusively OR'ing the contents of the user registers. The REG_CHECK bit in the interface mode register must be set for this checksum to operate. Otherwise, the register reads 0.

Table 24. Bit Descriptions for REGCHECK

Bits	Bit Name	Settings	Description	Reset	Access
[23:0]	REGISTER_CHECK		This register contains the 24-bit checksum of user registers when the REG_CHECK bit is set in the interface mode register.	0x000000	R

DATA REGISTER

Address: 0x04, Reset: 0x0000, Name: Data

The data register contains the ADC conversion result. The encoding is offset binary, or it can be changed to unipolar by the BI_UNIPOLARx bits in the setup configuration registers. Reading the data register brings the $\overline{RDY}$ bit and the $\overline{RDY}$ output high if it is low. The ADC result can be read multiple times. However, because the $\overline{RDY}$ output is brought high, it is not possible to know if another ADC result is imminent. After the command to read the ADC register is received, the ADC does not write a new result into the data register.

Table 25. Bit Descriptions for Data

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	Data		This register contains the ADC conversion result. If DATA_STAT is set in the interface mode register, the status register is appended to this register when read, making this a 24-bit register.	0x0000	R

GPIO CONFIGURATION REGISTER

Address: 0x06, Reset: 0x0800, Name: GPIOCON

The GPIO configuration register controls the general-purpose input/output pins of the ADC.

Table 26. Bit Descriptions for GPIOCON

Bits	Bit Name	Settings	Description	Reset	Access
[15:14]	Reserved		Reserved.	0x0	R
13	OP_EN0_1		GPO0/GPO1 output enable. This bit enables the GPO0 and GPO1 pins. The outputs are referenced between AVDD and AVSS.	0x0	R/W
		0	Disabled.		

REGISTER DETAILS

Table 26. Bit Descriptions for GPIOCON (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
		1	Enabled.		
12	OW_EN		This bit enables the use of open-wire detection.	0x0	R/W
		1	Disabled.		
		0	Enabled.		
11	SYNC_EN		SYNC input enable. This bit enables the $\overline{\text{SYNC}}$ pin as a sync input. When set low, the $\overline{\text{SYNC}}$ pin holds the ADC and filter in reset until $\overline{\text{SYNC}}$ goes high. An alternative operation of the $\overline{\text{SYNC}}$ pin is available when the ALT_SYNC bit in the interface mode register is set. This mode works only when multiple channels are enabled. In such cases, a low on the $\overline{\text{SYNC}}$ pin does not immediately reset the filter/modulator. Instead, if the $\overline{\text{SYNC}}$ pin is low when the channel is due to be switched, the modulator and filter are prevented from starting a new conversion. Bringing $\overline{\text{SYNC}}$ high begins the next conversion. This alternative sync mode allows $\overline{\text{SYNC}}$ to be used while cycling through channels.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
[10:9]	ERR_EN		Error pin mode. These bits enable the $\overline{\text{ERROR}}$ pin as an error input/output.	0x0	R/W
		00	Disabled.		
		01	Enable error input (active low). $\overline{\text{ERROR}}$ is an error input. The inverted readback state is OR'ed with other error sources and is available in the ADC_ERROR bit in the status register. The $\overline{\text{ERROR}}$ pin state can also be read from the ERR_DAT bit in this register.		
		10	Enable open-drain error output (active low). $\overline{\text{ERROR}}$ is an open-drain error output. The status register error bits are OR'ed, inverted, and mapped to the $\overline{\text{ERROR}}$ pin. $\overline{\text{ERROR}}$ pins of multiple devices can be wired together to a common pull-up resistor so that an error on any device can be observed.		
		11	General-purpose output (active low). $\overline{\text{ERROR}}$ is a general-purpose output. The status of the pin is controlled by the ERR_DAT bit in this register. This output is referenced between IOVDD and DGND, as opposed to the AVDD and AVSS levels used by the GPIO pins. The output has an active pull-up in this case.		
8	ERR_DAT		Error pin data. This bit determines the logic level at the $\overline{\text{ERROR}}$ pin if the pin is enabled as a general-purpose output. This bit reflects the readback status of the pin if the pin is enabled as an input.	0x0	R/W
		0	Logic 0.		
		1	Logic 1.		
7	GP_DATA1		GPO1 data. This bit is the write data for GPO1.	0x0	R/W
		0	GPO1 = 0.		
		1	GPO1 = 1.		
6	GP_DATA0		GPO0 data. This bit is the write data for GPO0.	0x0	R/W
		0	GPO0 = 0.		
		1	GPO0 = 1.		
[5:0]	Reserved		Reserved.	0x0	R

ID REGISTER

Address: 0x07, Reset: 0x39DX, Name: ID

The ID register returns a 16-bit ID. For the AD4113, this value is 0x39DX.

Table 27. Bit Descriptions for ID

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	ID		Product ID. The ID register returns a 16-bit ID code that is specific to the ADC.	0x39DX	R

REGISTER DETAILS

CHANNEL REGISTER 0 TO CHANNEL REGISTER 15

Address: 0x10 to 0x1F, Reset: 0x8001, Name: CH0 to CH15

The channel registers are 16-bit registers that select the currently active channels, the selected inputs for each channel, and the setup to be used to configure the ADC for that channel. The layout for CH0 to CH15 is identical.

Table 28. Bit Descriptions for CH0 to CH15

Bits	Bit Name	Settings	Description	Reset	Access
15	CH_ENx		This bit enables Channel x. If more than one channel is enabled, the ADC automatically sequences between them.	0x1	R/W
		0	Disabled.		
		1	Enabled.		
[14:12]	SETUP_SELx		These bits identify which of the eight setups is used to configure the ADC for this channel. A setup comprises a set of four registers: a setup configuration register, a filter configuration register, an offset register, and a gain register. All channels can use the same setup, in which case the same 3-bit value must be written to these bits on all active channels, or up to eight channels can be configured differently.	0x0	R/W
		000	Setup 0.		
		001	Setup 1.		
		010	Setup 2.		
		011	Setup 3.		
		100	Setup 4.		
		101	Setup 5.		
		110	Setup 6.		
		111	Setup 7.		
[11:10]	Reserved		Reserved.	0x0	R
[9:0]	INPUTx		These bits select which input pair is connected to the input of the ADC for this channel.	0x1	R/W
		0000000001	VIN0, VIN1.		
		0000010000	VIN0, VINCOM.		
		0000100000	VIN1, VIN0.		
		0000110000	VIN1, VINCOM.		
		0001000011	VIN2, VIN3.		
		0001010000	VIN2, VINCOM.		
		0001100010	VIN3, VIN2.		
		0001110000	VIN3, VINCOM.		
		0010000101	VIN4, VIN5.		
		0010010000	VIN4, VINCOM.		
		0010100100	VIN5, VIN4.		
		0010110000	VIN5, VINCOM.		
		0011000111	VIN6, VIN7.		
		0011010000	VIN6, VINCOM.		
		0011100110	VIN7, VIN6.		
		0011110000	VIN7, VINCOM.		
		1000110010	Temperature sensor.		
		1010110110	Reference.		

REGISTER DETAILS

SETUP CONFIGURATION REGISTER 0 TO SETUP CONFIGURATION REGISTER 7

Address: 0x20 to 0x27, Reset: 0x1000 Name: SETUPCON0 to SETUPCON7

The setup configuration registers are 16-bit registers that configure the reference selection, input buffers, and output coding of the ADC. The layout for SETUPCON0 to SETUPCON7 is identical.

Table 29. Bit Descriptions for SETUPCON0 to SETUPCON7

Bits	Bit Name	Settings	Description	Reset	Access
[15:13]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
12	BI_UNIPOLARx		Bipolar/unipolar. This bit sets the output coding of the ADC for Setup x.	0x1	R/W
		0	Unipolar coded output.		
		1	Bipolar coded output.		
11	REFBUFx+		REF+ buffer. This bit enables or disables the REF+ input buffer.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
10	REFBUFx−		REF− buffer. This bit enables or disables the REF− input buffer.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
[9:8]	INBUFx		Input buffer. This bit field is disabled by default but must be enabled for correct operation.	0x0	R/W
		00	Disabled.		
		11	Enabled.		
[7:6]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
[5:4]	REF_SELx		These bits allow the user to select the reference source for ADC conversion on Setup 0.	0x0	R/W
		00	External reference − REF±.		
		10	Internal 2.5V reference.		
		11	AVDD − AVSS.		
[3:0]	Reserved		Reserved.	0x0	R

FILTER CONFIGURATION REGISTER 0 TO FILTER CONFIGURATION REGISTER 7

Address: 0x28 to 0x2F, Reset: 0x0500, Name: FILTCON0 to FILTCON7

The filter configuration registers are 16-bit registers that configure the ADC data rate and filter options. Writing to any of these registers resets any active ADC conversion and restarts converting at the first channel in the sequence. The layout for FILTCON0 to FILTCON7 is identical.

Table 30. Bit Descriptions for FILTCON0 to FILTCON7

Bits	Bit Name	Settings	Description	Reset	Access
15	SINC3_MAPx		If this bit is set, the mapping of the filter register changes to directly program the decimation rate of the Sinc3 filter for Setup x. All other options are eliminated, this allows fine tuning of the output data rate and filter notch for rejection of specific frequencies. The data rate when on a single channel equals $f_{MOD}/(32 \times FILTCON0[14:0])$.	0x0	R/W
[14:12]	Reserved		These bits are reserved. Set these bits to 0.	0x0	R
11	ENHFILTENx		This bit enables various postfilters for enhanced 50Hz/60Hz rejection for Setup x. The ORDER0 bits must be set to 00 to select the Sinc5 + Sinc1 filter for this function to work.	0x0	R/W
		0	Disabled.		
		1	Enabled.		
[10:8]	ENHFILTx		These bits select between various postfilters for enhanced 50Hz/60Hz rejection for Setup x.	0x5	R/W
		010	27SPS, 47dB rejection, 36.7ms settling.		
		011	25SPS, 62dB rejection, 40ms settling.		
		101	20SPS, 86dB rejection, 50ms settling.		
		110	16.67SPS, 92dB rejection, 60ms settling.		

REGISTER DETAILS

Table 30. Bit Descriptions for FILTCON0 to FILTCON7 (Continued)

Bits	Bit Name	Settings	Description	Reset	Access
7	Reserved		This bit is reserved, set this bit to 0.	0x0	R
[6:5]	ORDERx		These bits control the order of the digital filter that processes the modulator data for Setup x.	0x0	R/W
		00	Sinc5 + Sinc1 (default).		
		11	Sinc3.		
[4:0]	ODRx		These bits control the output data rate of the ADC and, therefore, the settling time and noise for Setup x. Rates shown are for single channel enabled Sinc5 + Sinc1 filter. For multiple channels enabled, see Table 7 and Table 8.	0x0	R/W
		00000	125,000SPS.		
		00001	125,000SPS.		
		00010	62,500SPS.		
		00011	62,500SPS.		
		00100	31,250SPS.		
		00101	25,000SPS.		
		00110	15,625 SPS.		
		00111	10,390 (10416.7SPS for sinc3).		
		01000	4994 (5000SPS for sinc3).		
		01001	2498SPS (2500SPS for Sinc3).		
		01010	1000.00SPS.		
		01011	500.00SPS.		
		01100	395.5SPS (400.6SPS for Sinc3).		
		01101	200.00SPS.		
		01110	100.00SPS.		
		01111	59.87SPS.		
		10000	49.92SPS (50SPS for Sinc3).		
		10001	20.01SPS.		
		10010	16.67SPS		
		10011	10SPS.		
		10100	5SPS.		
		10101	2.5SPS.		
		10110	2.5SPS.		

OFFSET REGISTER 0 TO OFFSET REGISTER 7

Address: 0x30 to 0x37, Reset: 0x8000, Name: OFFSET0 to OFFSET7

The offset (zero-scale) registers are 16-bit registers that can be used to compensate for any offset error in the ADC or in the system. The layout for OFFSET0 to OFFSET7 is identical.

Table 31. Bit Descriptions for OFFSET0 to OFFSET7

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	OFFSETx		Offset calibration coefficient for Setup 0.	0x8000	R/W

REGISTER DETAILS

GAIN REGISTER 0 TO GAIN REGISTER 7

Address: 0x38 to 0x3F, Reset: 0x5XXX, Name: GAIN0 to GAIN7

The gain (full-scale) registers are 16-bit registers that can be used to compensate for any gain error in the ADC or in the system. The layout for GAIN0 to GAIN7 is identical.

Table 32. Bit Descriptions for GAIN0

Bits	Bit Name	Settings	Description	Reset	Access
[15:0]	GAINx		Gain calibration coefficient for Setup x.	0x5XXX	R/W

OUTLINE DIMENSIONS

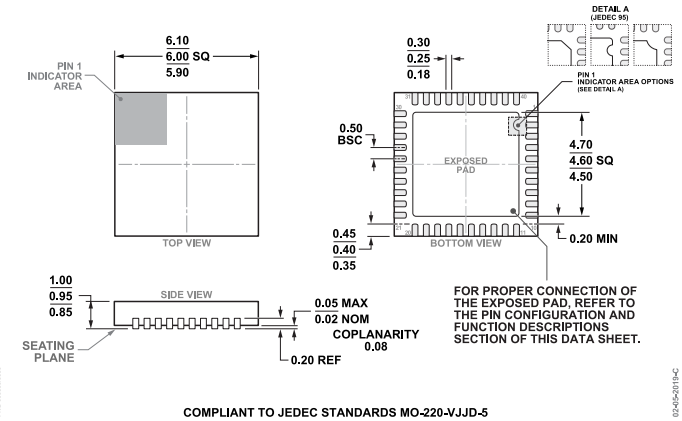


Figure 41. 40-Lead Lead Frame Chip-Scale Package [LFCSP], 6mm × 6mm Body and 0.95mm Package Height (CP-40-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
AD4113BCPZ	−40°C to +105°C	40-Lead LFCSP	Tray, 490	CP-40-15
AD4113BCPZ-RL7	−40°C to +105°C	40-Lead LFCSP	Reel, 750	CP-40-15

[1] Z = RoHS Compliant Part.

Updated: April 14, 2026

EVALUATION BOARDS

Model[1]	Description
EVAL-AD4113ARDZ	Evaluation Board

[1] Z = RoHS Compliant Part.