Optimized all Hardware Edge Node, 10BASE-T1S Ethernet to the Edge Bus (E^2B) Transceiver

FEATURES

- 10BASE-T1S IEEE 802.3-2022 compliant PHY with support for PLCA and an integrated MAC
- 10BASE-T1S PHY operating modes
  - Point-to-point half-duplex (≥ 15 m)
  - Multidrop configuration half-duplex (≥ 25 m, ≥ 8 nodes)
- PLCA features: PLCA coordinator (head node), burst mode, precedence mode, and multiple PLCA IDs
- MAC Features
  - AD3300 only: OPEN Alliance 10BASE-T1x MAC-PHY serial interface
  - AD3300 only: Transmit priority queues
  - 16 MAC address filters
- IEEE 802.1AS / IEEE 1588 support for TSN using the gPTP combined with sensor timestamping and actuator synchronization
- Low Complexity Ethernet Engine
  - Provides a deterministic, low-latency data path between 10BASE-T1S to the SAIF
  - 12 SAIF pins support simultaneous operation of several common sensor/actuator interface standards and functions, including SPI, I^2C, UART, PWM, GPIO, Flexible I/O, and bridge to LIN
  - SMC enables periodic read and write functions on all interfaces
  - AD3300 supports dual mode: MAC-PHY and LCE operation simultaneously
  - AD3304/5 only: Bridge to ISELED and ILaS
- OPEN Alliance features sleep/wake-up, topology discovery, and advanced diagnostics
  - Enable output pin (EN) to power down the regulated supply inputs in sleep mode
  - Support for local (WAKE input pin) and network (wake-up pulse) wake
- Suitable for 12 V, 24 V, 48 V automotive electrical systems or operating from 5 V levels only
- Detection capability for overvoltage and undervoltage events when monitoring the VBAT pin
- General-purpose ADC
- SSC for handling fault conditions
- Low-current 3.3 V LDO using the LVDD pin as an output
- Compatible with power delivery over data cable
- Provides robust EMC/EMI performance
  - Low cost bus interface network with no external ESD components required
  - Enhanced noise immunity providing additional performance for noisy environments
- Low power consumption: maximum current of 50 mA in functional modes of operation and 40 µA in sleep mode
- 1.8 V to 3.3 V I/O logic levels with support for 5 V inputs and open drain outputs
- −40°C to +150°C junction temperature range
- Small package: 4 mm x 4 mm 24-lead LFCSP (QFN) package
- AEC-Q100 qualified for automotive applications

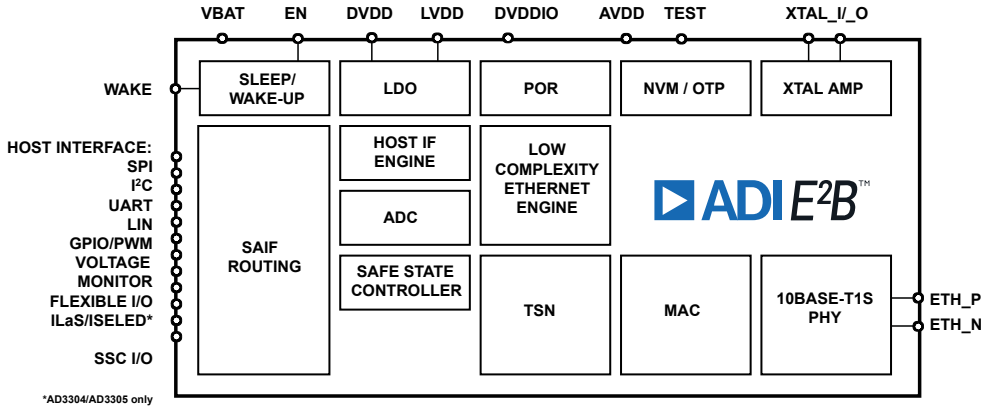

Figure 1. AD3301/4/5 Functional Block Diagram

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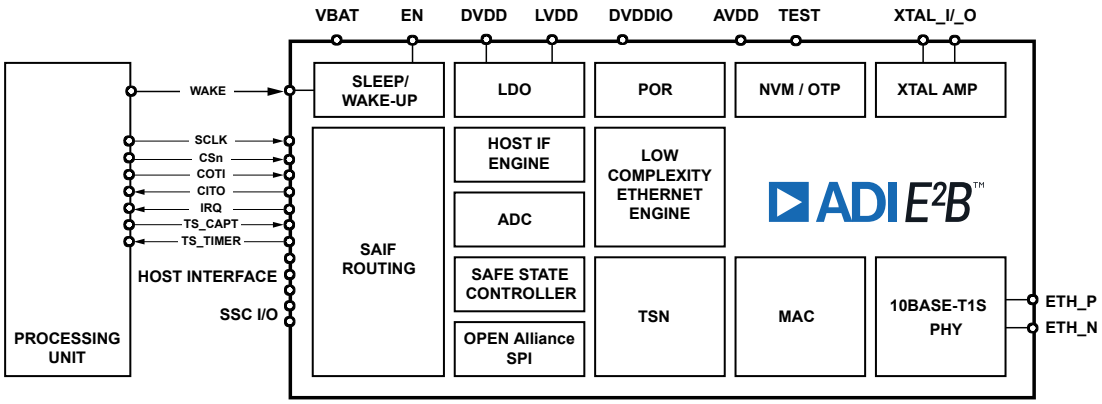

Figure 2. AD3300 Functional Block Diagram (Dual-mode)

APPLICATIONS

- Automotive internal and external lighting
- Automotive body and chassis domain control
- Automotive sensor and actuator networking
- Automotive Ethernet based zonal architectures
- Automotive in-vehicle networking

For more information about the AD3300/1/4/5, contact your local Analog Devices, Inc. representative, sales office at analog.com/sales or contact e2b.support@analog.com.

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