



# Variable Resolution Resolver-to-Digital Converter

## AD2S80

### 1.0 SCOPE

This specification documents the detail requirements for space qualified product manufactured on Analog Devices, Inc.'s QML certified line per MIL-PRF-38535 Level V except as modified herein. The manufacturing flow described in the STANDARD SPACE LEVEL PRODUCTS PROGRAM brochure is to be considered a part of this specification. <http://www.analog.com/aerospace>

This data sheet specifically details the space grade version of this product. A more detailed operational description and a complete data sheet for commercial product grades can be found at [www.analog.com/AD2S80](http://www.analog.com/AD2S80)

### 2.0 Part Number. The complete part number(s) of this specification follow:

<u>Part Number</u>	<u>Description</u>
<b>AD2S80-703D</b>	Variable Resolution Resolver-to-Digital Converter

#### 2.1 Case Outline.

<u>Letter</u>	<u>Descriptive designator</u>	<u>Case Outline (Lead Finish per MIL-PRF-38535)</u>
D	GDIP2-T40	40-Lead ceramic dual-in-line package (SIDEBRAZED)

### 3.0 Absolute Maximum Ratings. (TA = 25°C, unless otherwise noted)

+Vs to GND <sup>1,2</sup> .....	+14V
-Vs to GND <sup>1,2</sup> .....	-14V
+VL to GND <sup>2</sup> .....	+VS
Digital Input Voltage to GND <sup>2</sup> .....	-0.4V to +VL
Demod I/P .....	+14V to -VS
Integrator I/P .....	+14V to -VS
VCO Input .....	+14V to -VS
VREF to GND <sup>3,4</sup> .....	+14V to -VS
Analog Input Voltage (SIN, COS) to GND .....	+14V to -VS
Power Dissipation .....	860mW
Storage Temperature Range .....	-65°C to +150°C
Operating Temperature Range .....	-55°C to +125°C
Junction Temperature (Tj) .....	+150°C

<sup>1</sup> The device should be powered up as follows: -Vs should be applied before or simultaneously with the +Vs. VL can be applied at any time with respect to +Vs and -Vs.

<sup>2</sup> GND refers to ANALOG GND; ANALOG GND must be externally connected to DIGITAL GND.

<sup>3</sup> SIGNAL GND is internally connected to ANALOG GND.

<sup>4</sup> SIN, COS, and REF input voltage may be present without +VS, -VS, or +VL.

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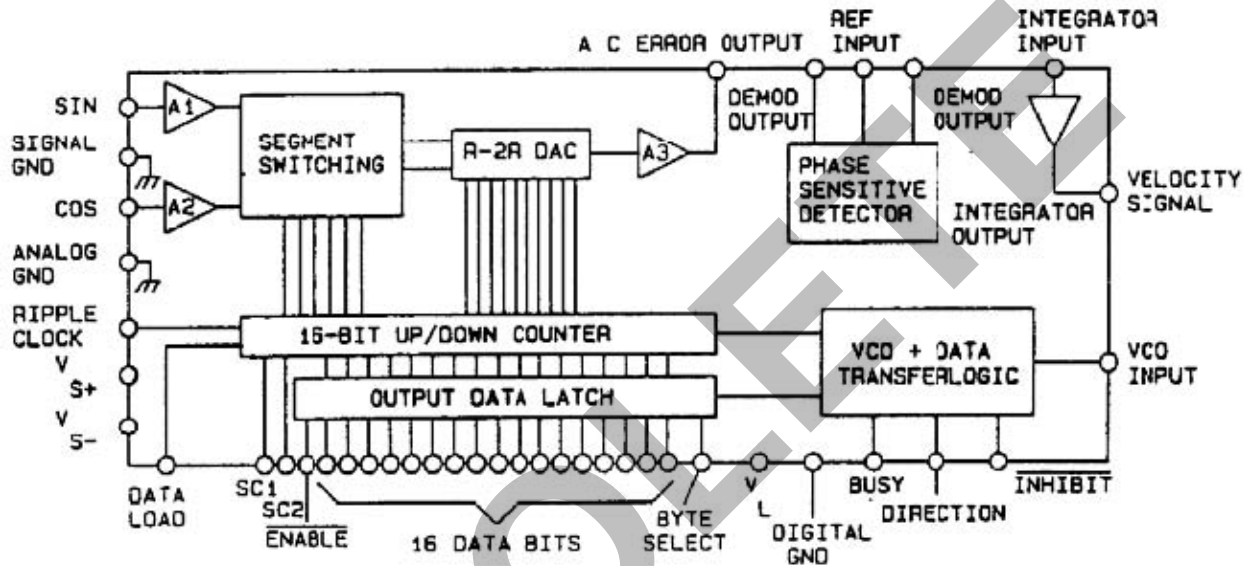
## 3.1 Thermal Characteristics:

Thermal Resistance, D (sidebrazed) Package

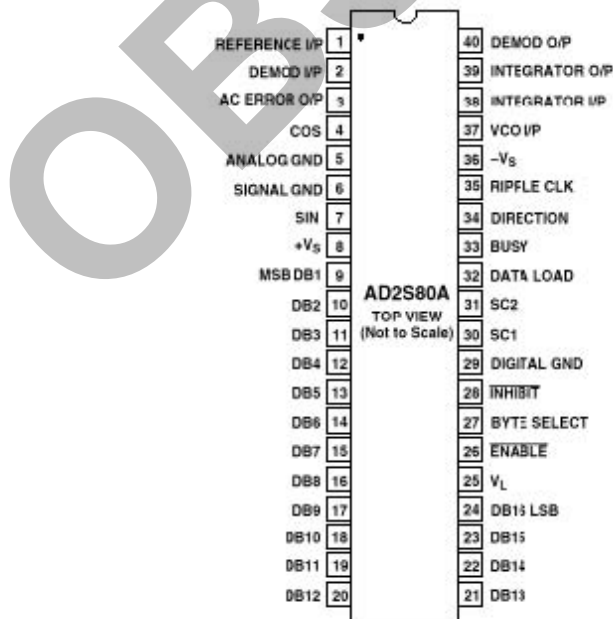
Junction-to-Case ( $\Theta_{JC}$ ) = 11°C/W Max

Junction-to-Ambient ( $\Theta_{JA}$ ) = 48°C/W Max

## 3.2 Functional Block Diagram:



## 3.3 Terminal Assignments:



## 4.0 Electrical Table: (See notes at end of table)

Table I						
Parameter	Symbol	Conditions <u>1/</u>	Sub-group	Limit Min	Limit Max	Units
Angular Accuracy <u>2/</u>		$V_S = \pm 10.8V$ , SC1=SC2=High $V_S = \pm 13.2V$ , SC1=SC2=High 16 bit resolution	1, 2, 3		$\pm 8$	Arc mins
Missing Codes <u>2/</u>		$V_S = \pm 10.8V$ , SC1=SC2=High $V_S = \pm 13.2V$ , SC1=SC2=High 16 bit resolution	1 2, 3		$\pm 4$ $\pm 6$	Codes
Total effective angular offset		Output data nulled by application of offset current to integrator input	1, 2, 3		$\pm 800$	nA
Integrator output range		1 mA load	1, 2, 3	$\pm 8$		V
		$\pm V_S = 10.8V$ , 1 mA load	1, 2, 3	$\pm 7$		
Demod O/P Scaling <u>2/</u>			1, 2, 3	90	110	nA/Bit
VCO Maximum Rate			4, 5, 6		1.0	MHz
VCO Gain Scaling		Measured with VCO input, Current of $\pm 10\mu A$	4, 5, 6	7110	8690	Hz/ $\mu A$
VCO Linearity <u>6/</u>		VCO measured at 10 points over the frequency range 0 to 1MHz	4, 5, 6		$\pm 3$	%
VCO Total Effective Offset		Measured with 68K $\Omega$ Input R	1, 2		380	nA
			3		400	
Digital Inputs High Voltage <u>3/</u>	$V_{IH}$	$\pm V_S = 10.8V$	1, 2, 3	2.0		V
Digital Inputs Low Voltage <u>3/</u>	$V_{IL}$	$\pm V_S = 13.2V$	1, 2, 3		0.8	
Digital Inputs High Current <u>3/</u>	$I_{IH}$	$\pm V_S = 13.2V$ , $V_L = 5.5V$ $V_{IH} = 5.5V$	1, 2, 3		$\pm 100$	$\mu A$
Digital Inputs Low Current <u>3/</u>	$I_{IL}$	$\pm V_S = 13.2V$ , $V_L = 5.5V$ $V_{IL} = 0V$	1, 2, 3		$\pm 100$	
Digital Inputs Low Voltage <u>4/</u>	$V_{IL}$	$\overline{ENABLE} = HIGH$	1, 2, 3		1.0	V
Digital Inputs Low Current <u>4/</u>	$I_{IL}$	$\overline{ENABLE} = HIGH$	1, 2, 3	-400		$\mu A$
Digital Outputs High Voltage <u>5/</u>	$V_{OH}$	$V_L = 4.5V$ , $I_{OH} = 100\mu A$	1, 2, 3	2.4		V
Digital Outputs Low Voltage <u>5/</u>	$V_{OL}$	$V_L = 5.5V$ , $I_{OL} = 1.2mA$	1, 2, 3		0.4	
High Level Three State Leakage Current	$I_{OZH}$	$V_{OH} = 5.0V$ , $V_L = 5.5V$	1, 2, 3		$\pm 100$	$\mu A$
Low level Three State Leakage Current	$I_{OZL}$	$V_{OL} = 0V$ , $V_L = 5.5V$	1, 2, 3		$\pm 100$	
Busy Pulse Width	$t_{BUSY}$		9, 10, 11	200	600	nS
Power Supply Current	$+I_S$	$\pm V_S = \pm 13.2V$	1, 2, 3		30	mA
	$-I_S$		1, 2, 3	-30		
	$+I_L$	$V_L = 5.5V$	1, 2, 3		1.5	

## TABLE I NOTES:

1/  $V_S = \pm 12V$ ,  $V_L = +5V$ , unless otherwise specified

2/  $V_{SIN}$ ,  $V_{COS} = 2 V_{RMS}$  Maximum at 5KHz,  $V_{REF} = 2 V_{RMS}$  at 5KHz.

3/ DB1-DB16,  $\overline{INHIBIT}$ ,  $\overline{ENABLE}$ , BYTE SELECT

4/ Digital inputs SC1, SC2, DATA LOAD are internally pulled up to  $+V_S$ .

5/ DB1-DB16, RIPPLE CLOCK, DIRECTION.

6/ VCO linearity is expressed as % (percentage) of reading.

**4.1 Electrical Test Requirements:**

<b>Table II</b>	
Test Requirements	Subgroups (in accordance with MIL-PRF-38535, Table III)
Interim Electrical Parameters	1, 4, 9
Final Electrical Parameters	1, 2, 3, 4, 5, 6, 9, 10, 11 <u>1/</u>
Group A Test Requirements	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters	1, 4, 9
Group D end-point electrical parameters	1, 4, 9
Group E end-point electrical parameters	Not applicable

1/ PDA applies to Subgroup 1.

**5.0 Life Test/Burn-In Circuit:**

- 5.1 HTRB is not applicable for this drawing.
- 5.2 Burn-in is per MIL-STD-883 Method 1015 test condition B.
- 5.3 Steady state life test is per MIL-STD-883 Method 1005.

Rev	Description of Change	Date
A	Initiate	Oct. 12, 2000
B	Update web address	Feb. 7, 2002
C	Add subgroups 4, 5, 6, 9, 10, 11 to table II	Mar. 19, 2002
D	Update web address. Delete burn-in circuit.	June 26, 2003
E	Update header/footer and add to 1.0 Scope description.	March 11, 2008
F	Add Junction Temperature (T <sub>J</sub> )...+150°C to section 3.0-Absolute Max. Ratings	April 3, 2008

OBSOLETE

