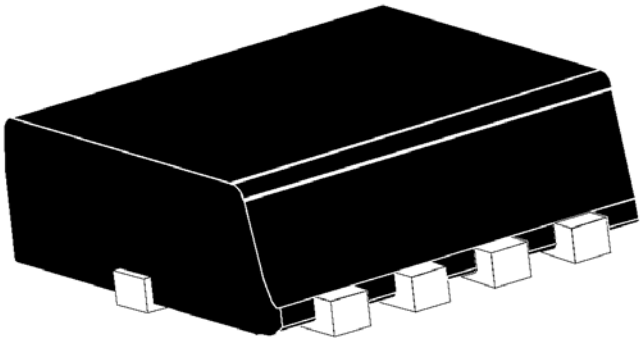
TMC32NP-MLP

Manual

Complementary 30V Enhancement Mode MOSFET
In Miniature Package
For use with e.g. TMC239 or TMC249



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TRINAMIC
MOTION CONTROL

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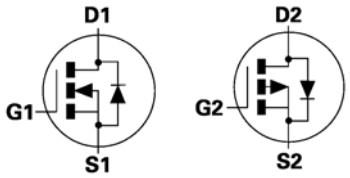
1 Features

Packaged in the new innovative 3mm x 2mm MLP (Micro Leaded Package) outline this dual 30V N and P channel Trench MOSFET utilizes a unique structure combining the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage power management applications, such as stepper motor drivers. Its low gate charge makes it an ideal power driver for the TMC239A and TMC249A family of stepper motor drivers. Using only four of these transistor packages, and the miniaturized TMC239A-LA or TMC249A-LA, a 2A stepper driver can be build in the size of a stamp. Up to 2.8A peak (2A RMS) are possible with limited duty cycle. A second set of transistors doubles the current capability.

SUMMARY

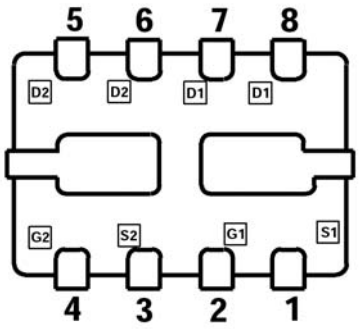
- N-Channel = $V_{(BR)DSS}$= 30V : $R_{DS(on)}$= 0.12 Ω; I_D= 3.7A
- P-Channel = $V_{(BR)DSS}$= -30V : $R_{DS(on)}$= 0.21 Ω; I_D= -2.7A



Applications

- Stepper motor driver stages

Pinout



Underside view

Highlights

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- PCB area and device placement savings

Other

- 3mm x 2mm Dual Die MLP package
- RoHS compliant

Order code	Description
TMC32NP-MLP	Miniature Complementary 30V Enhancement Mode MOSFET

Table 1.1: Order codes

2 Life support policy

TRINAMIC Motion Control GmbH & Co. KG does not authorize or warrant any of its products for use in life support systems, without the specific written consent of TRINAMIC Motion Control GmbH & Co. KG.

Life support systems are equipment intended to support or sustain life, and whose failure to perform, when properly used in accordance with instructions provided, can be reasonably expected to result in personal injury or death.

3 Operational Ratings

3.1 Absolute Maximum Ratings

Symbol	Parameter	N-Channel	P-Channel	Unit
V_{DSS}	Drain-source voltage	30	-30	V
V_{GS}	Gate-source voltage	± 20	± 20	V
I_D	Continuos drain current (V_{GS}= 10V; T_A=25°C) (a) (f) (V_{GS}= 10V; T_A=25°C) (b) (f) (V_{GS}= 10V; T_A=70°C) (b) (f)	 2.9 3.7 3.0	 -2.1 -2.7 -2.2	 A
I_{DM}	Pulsed drain current	12.4	-9.2	A
I_S	Continuous source current (body diode)(b)(f)	2.4	-2.8	A
I_{SM}	Pulsed source current (body diode)	12.4	-9.2	A
P_D	Power dissipation at T_A =25°C (a) (f) Linear derating factor	1.5 12		W mW/°C
P_D	Power dissipation at T_A =25°C (b) (f) Linear derating factor	2.45 19.6		W mW/°C
P_D	Power dissipation at T_A =25°C (c) (f) Linear derating factor	1 8		W mW/°C
P_D	Power dissipation at T_A =25°C (d) (f) Linear derating factor	1.13 8		W mW/°C
P_D	Power dissipation at T_A =25°C (d) (g) Linear derating factor	1.7 13.6		W mW/°C

Table 3.1: Absolute Maximum Ratings

3.2 Thermal Resistance

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Junction to ambient (a) (f)	83.3	°C/W
$R_{\theta JA}$	Junction to ambient (b) (f)	51	°C/W
$R_{\theta JA}$	Junction to ambient (c) (f)	125	°C/W
$R_{\theta JA}$	Junction to ambient (d) (f)	111	°C/W
$R_{\theta JA}$	Junction to ambient (d) (g)	73.5	°C/W
$R_{\theta JA}$	Junction to ambient (e) (g)	41.7	°C/W

Table 3.2: Thermal Resistance

(a) For a dual device surface mounted on 8 sq cm single sided 70µm copper on FR4 PCB, in still air conditions **with all exposed pads attached**.

(b) Measured at t<5 secs for a dual device surface mounted on 8 sq cm single sided 70µm copper on FR4 PCB, in still air conditions **with all exposed pads attached.**

(c) For a dual device surface mounted on 8 sq cm single sided 70µm copper on FR4 PCB, in still air conditions **with minimal lead connections only.**

(d) For a dual device surface mounted on 10 sq cm single sided 35µm copper on FR4 PCB, in still air conditions **with all exposed pads attached**.

(e) For a dual device surface mounted on 85 sq cm single sided 70µm copper on FR4 PCB, in still air conditions **with all exposed pads attached**.

(f) For a dual device with one active die.

(g) For dual device with 2 active die running at equal power.

3.3 Characteristics

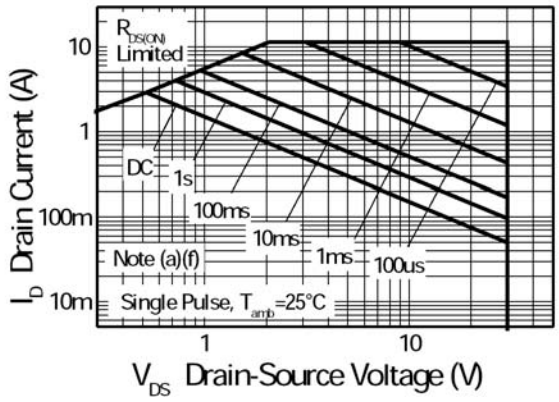


Figure 3.1: N-channel Safe Operating Area

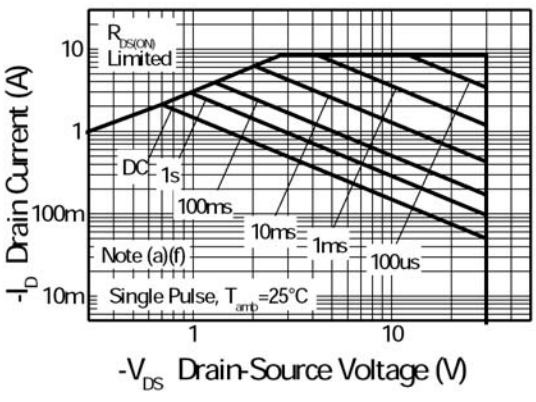


Figure 3.2: P-channel Safe Operating Area

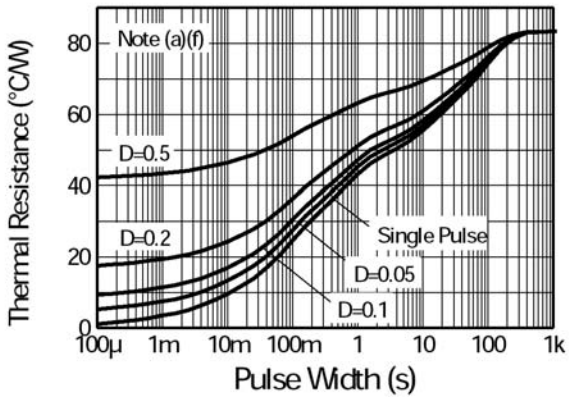


Figure 3.3: Transient Thermal Impedance

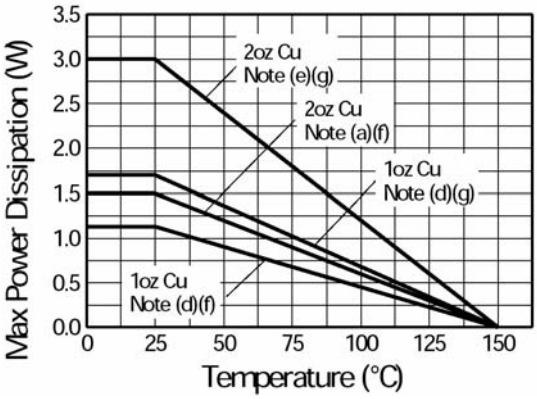


Figure 3.4: Derating Curve

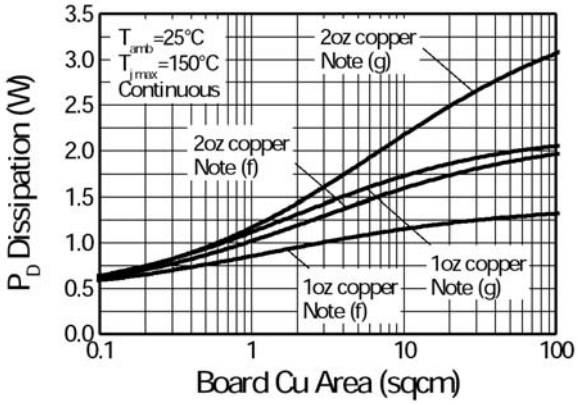


Figure 3.5: Power Dissipation v Board Area

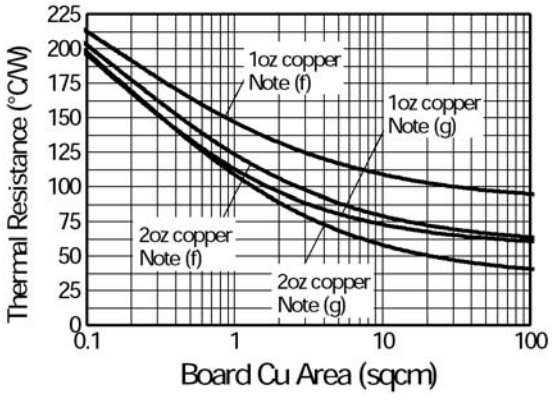


Figure 3.6: Thermal Resistance v Board Area

4 N-Channel

4.1 Electrical Characteristics

at T_{amb} = 25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
STATIC						
$V_{(BR)DSS}$	Drain-source breakdown voltage	30			V	I_D= 250µA, V_{GS}= 0V
I_{DSS}	Zero gate voltage drain current			0.5	µA	V_{DS}= 30V, V_{GS}= 0V
I_{GSS}	Gate-body leakage			100	nA	V_{GS}= ±20V, V_{DS}= 0V
$V_{GS(th)}$	Gate-source threshold voltage	1.0			V	I_D= 250µA, V_{DS}= V_{GS}
$R_{DS(on)}$	Static drain-source on-state resistance (1)		0.106	0.12 0.18	Ω Ω	V_{GS}= 10V, I_D= 2.5A V_{GS}= 4.5V, I_D= 2.0A
g_{fs}	Forward transconductance (1) (3)		3.5		S	V_{DS}= 4.5V, I_D= 2.5A
DYNAMIC (3)						
C_{iss}	Input capacitance		190		pF	V_{DS}= 25V, V_{GS}= 0V F = 1MHz
C_{oss}	Output capacitance		38		pF	
C_{rss}	Reverse transfer capacitance		20		pF	
SWITCHING (2) (3)						
$t_{d(on)}$	Turn-on-delay time		1.7		ns	V_{DD}= 15V, I_D= 2.5A R_G= 6.0Ω, V_{GS}= 10V
t_r	Rise time		2.3		ns	
$t_{d(off)}$	Turn-off delay time		6.6		ns	
t_f	Fall time		2.9		ns	
Q_g	Gate Charge		2.3		nC	V_{DS}= 15V, V_{GS}= 5V I_D= 2.5A
Q_g	Total gate charge		3.9		nC	V_{DS}= 15V, V_{GS}= 10V I_D= 2.5A
Q_{gs}	Gate-source charge		0.6		nC	
Q_{gd}	Gate drain charge		0.9		nC	
SOURCE-DRAIN-DIODE						
V_{SD}	Diode forward voltage (1)		0.85	0.95	V	T_j= 25°C, I_S= 1.7A, V_{GS}= 0V
t_{rr}	Reverse recovery time (3)		17.7		ns	T_j= 25°C, I_S= 2.5A, di/dt = 100A/µs
Q_{rr}	Reverse recovery charge (3)		13.0		nC	

Table 4.1: Electrical Characteristics, N-Channel

(1) Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) For design aid only, not subject to production testing.

4.2 Typical Characteristics

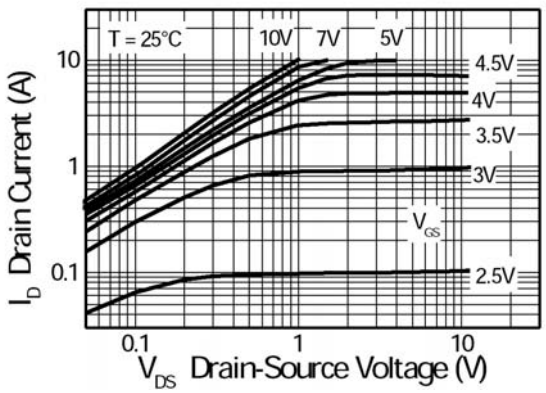


Figure 4.1: Output Characteristics (N)

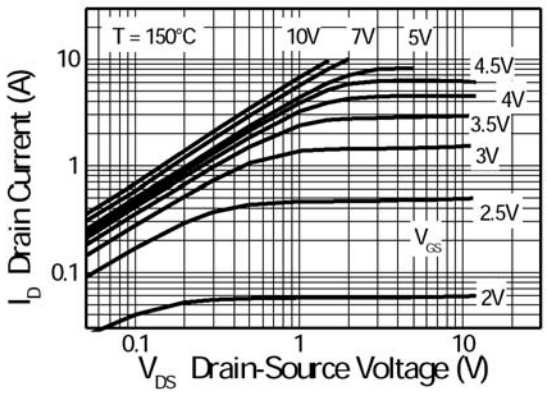


Figure 4.2: Output Characteristics (N)

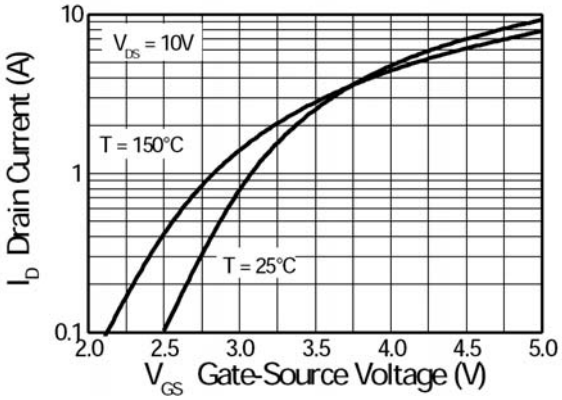


Figure 4.3: Typical Transfer Characteristics (N)

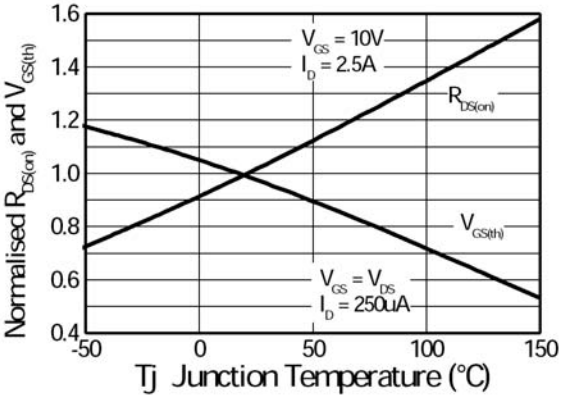


Figure 4.4: Normalized Curves v Temperature (N)

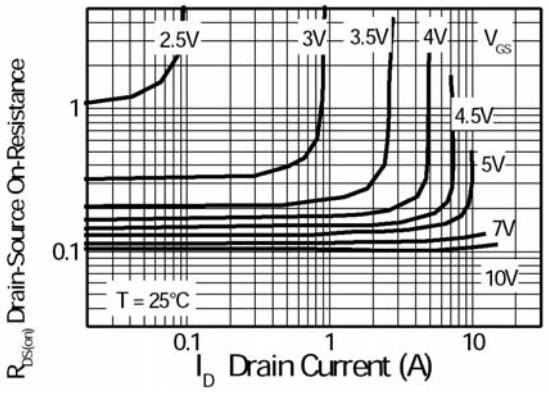


Figure 4.5: On-Resistance v Drain Current (N)

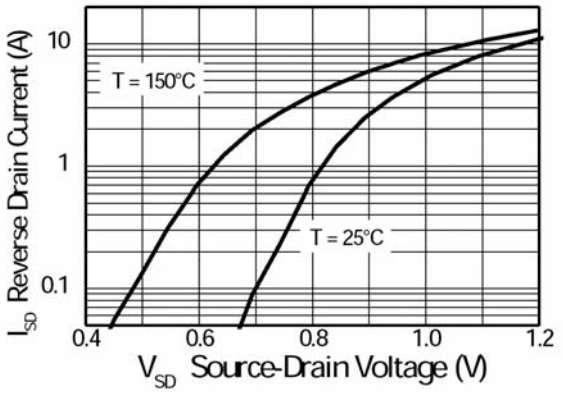


Figure 4.6: Source-Drain Diode Forward Voltage (N)

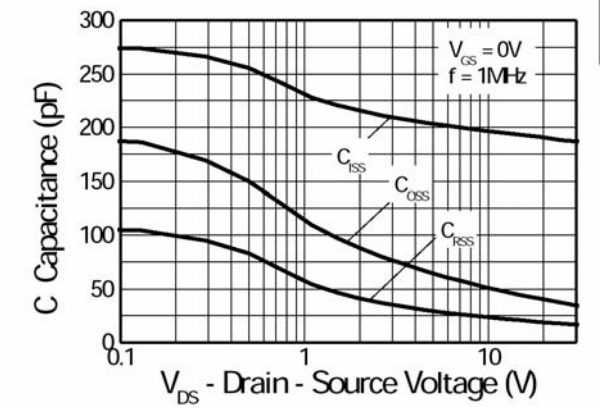


Figure 4.7: Capacitance v Drain-Source Voltage (N)

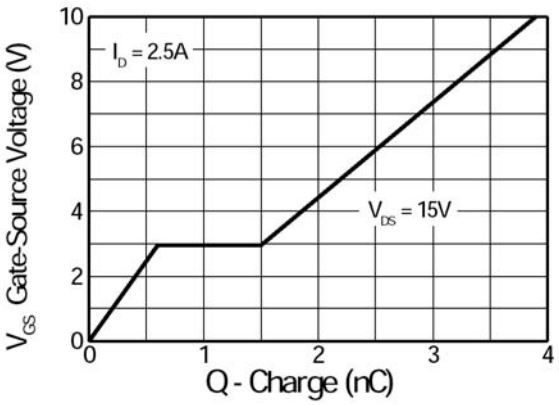


Figure 4.8: Gate-Source Voltage v Gate Charge (N)

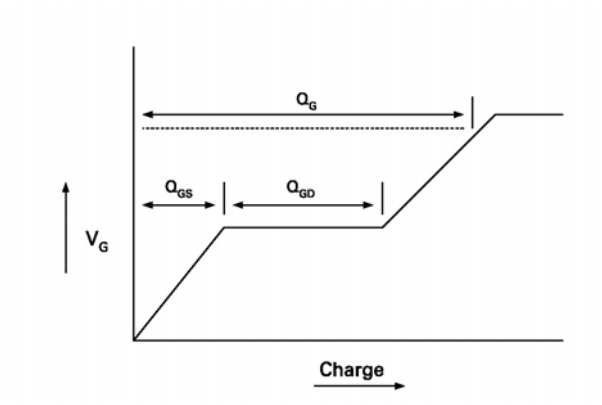


Figure 4.9: Basic Gate Charge Waveform (N)

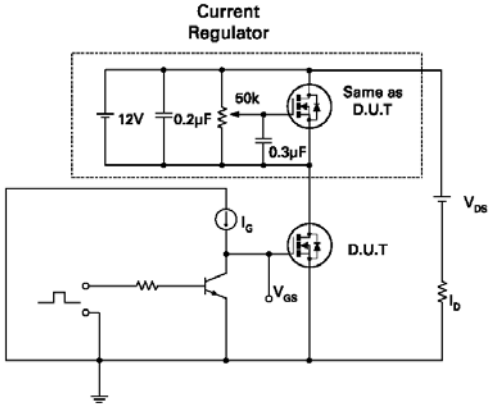


Figure 4.10: Gate Charge Test Circuit (N)

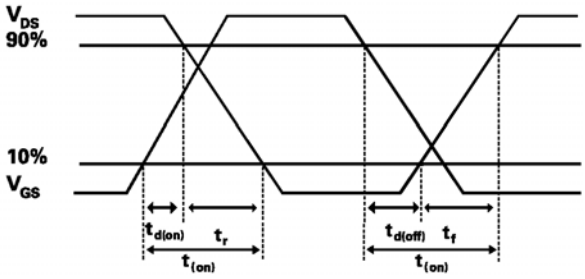


Figure 4.11: Switching Time Waveforms (N)

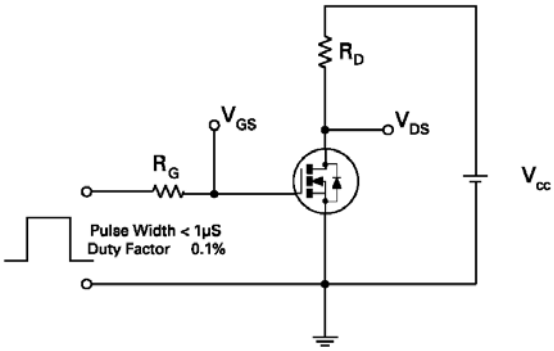


Figure 4.12: Switching Time Test Circuit (N)

5 P-Channel

5.1 Electrical Characteristics

at T_{amb} = 25°C unless otherwise stated

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
STATIC						
$V_{(BR)DSS}$	Drain-source breakdown voltage	-30			V	I_D= -250µA, V_{GS}= 0V
I_{DSS}	Zero gate voltage drain current			-1.0	µA	V_{DS}= -30V, V_{GS}= 0V
I_{GSS}	Gate-body leakage			100	nA	V_{GS}= ±20V, V_{DS}= 0V
$V_{GS(th)}$	Gate-source threshold voltage	-0.8			V	I_D= -250µA, V_{DS}= V_{GS}
$R_{DS(on)}$	Static drain-source on-state resistance (1)			0.210 0.330	Ω Ω	V_{GS}= -10V, I_D= -1.4A V_{GS}= -4.5V, I_D= -1.1A
g_{fs}	Forward transconductance (1) (3)		2.48		S	V_{DS}= -15V, I_D= 1.4A
DYNAMIC (3)						
C_{iss}	Input capacitance		204		pF	V_{DS}= -15V, V_{GS}= 0V F = 1MHz
C_{oss}	Output capacitance		39.8		pF	
C_{rss}	Reverse transfer capacitance		25.8		pF	
SWITCHING (2) (3)						
$t_{d(on)}$	Turn-on-delay time		1.5		ns	V_{DD}= -15V, I_D= -1A R_G= 6.0Ω, V_{GS}= -10V
t_r	Rise time		2.8		ns	
$t_{d(off)}$	Turn-off delay time		11.3		ns	
t_f	Fall time		7.5		ns	
Q_g	Gate charge		2.58		nC	V_{DS}= -15V, V_{GS}= -5V I_D= -1.4A
Q_g	Total gate charge		5.15		nC	V_{DS}= -15V, V_{GS}= -10V I_D= -1.4A
Q_{gs}	Gate-source charge		0.65		nC	
Q_{gd}	Gate drain charge		0.92		nC	
SOURCE-DRAIN-DIODE						
V_{SD}	Diode forward voltage (1)		-0.85	-0.95	V	T_j= 25°C, I_S= -1.1A, V_{GS}= 0V
t_{rr}	Reverse recovery time (3)		18.6		ns	T_j= 25°C, I_S= -0.95A, di/dt = 100A/µs
Q_{rr}	Reverse recovery charge (3)		14.8		nC	

Table 5.1: Electrical Characteristics, P-Channel

(1) Measured under pulsed conditions. Pulse width ≤ 300_s; duty cycle ≤ 2%.
(2) Switching characteristics are independent of operating junction temperature.
(3) For design aid only, not subject to production testing.

5.2 Typical Characteristics

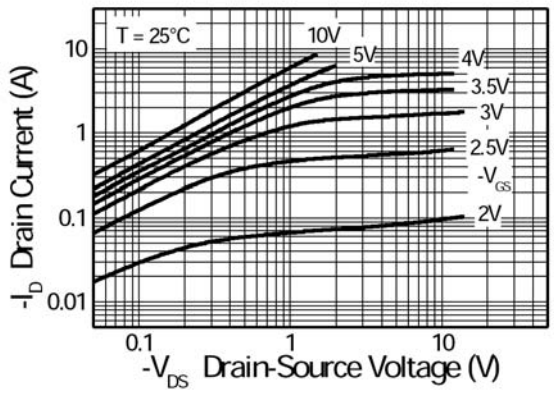


Figure 5.1: Output Characteristics (P)

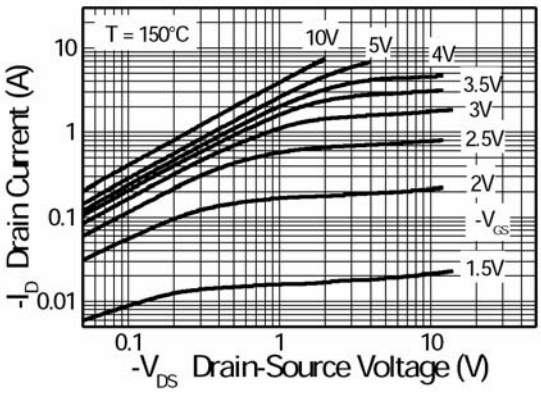


Figure 5.2: Output Characteristics (P)

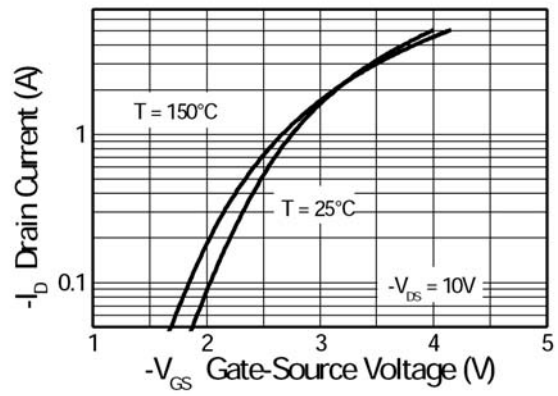


Figure 5.3: Typical Transfer Characteristics (P)

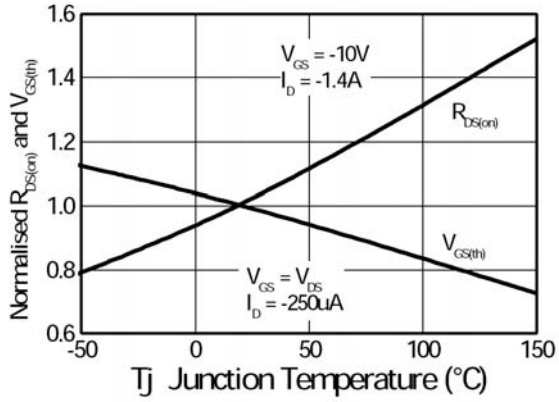


Figure 5.4: Normalized Curves v Temperature (P)

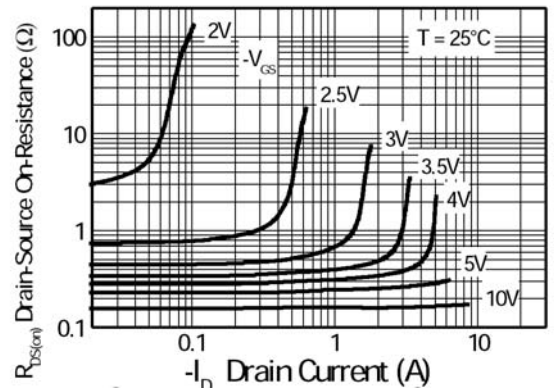


Figure 5.5: On-Resistance v Drain Current (P)

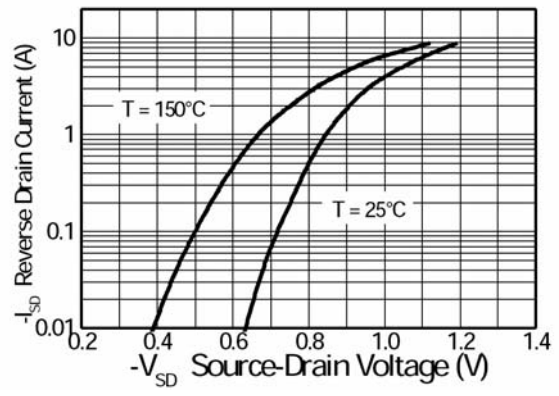


Figure 5.6: Source-Drain Diode Forward Voltage (P)

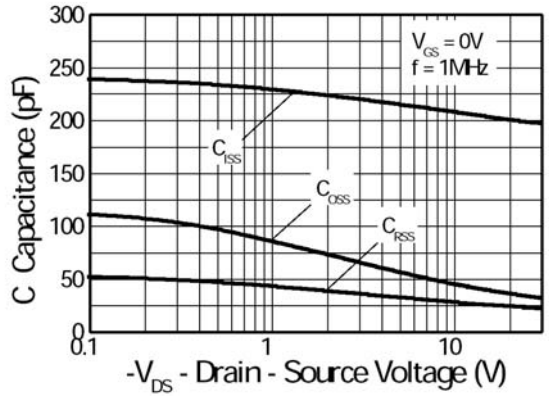


Figure 5.7: Capacitance v Drain-Source Voltage (P)

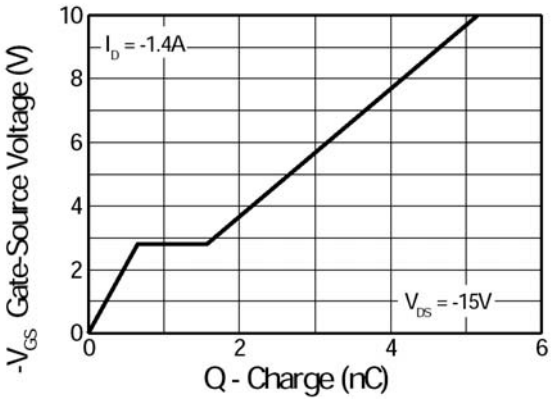


Figure 5.8: Gate-Source Voltage v Gate Charge (P)

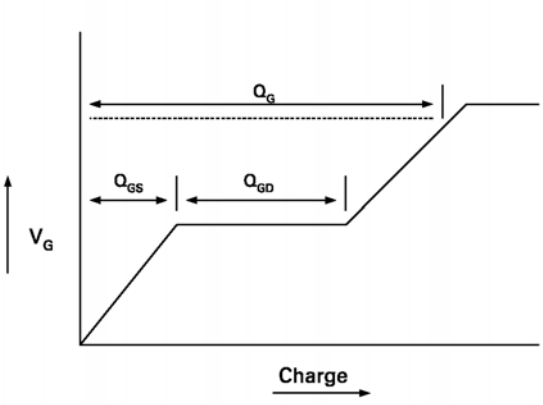


Figure 5.9: Basic Gate Charge Waveform (P)

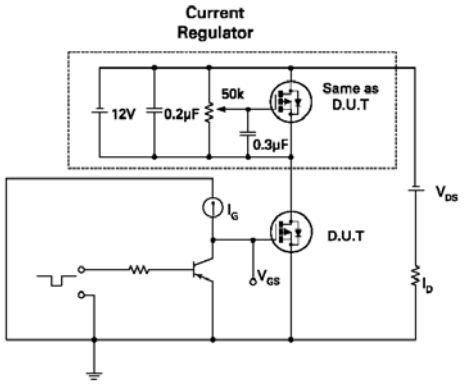


Figure 5.10: Gate Charge Test Circuit (P)

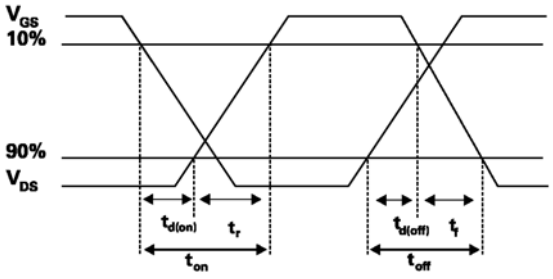


Figure 5.11: Switching Time Waveforms (P)

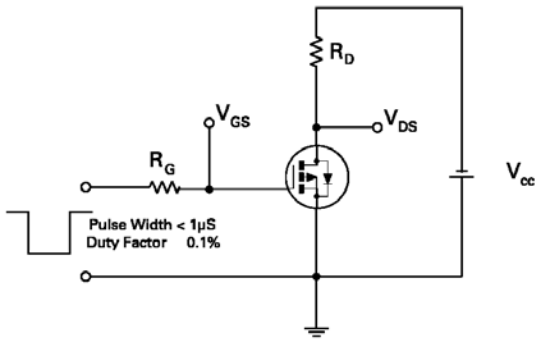


Figure 5.12: Switching Time Test Circuit (P)

6 Application with TMC239 / TMC249

6.1 Example Wiring

Example wiring with four TMC32NP-MLP and a TMC239. Sense resistors shown are selected for 2.26A peak current (1.6A RMS). (Power supply filter capacitors not shown.)

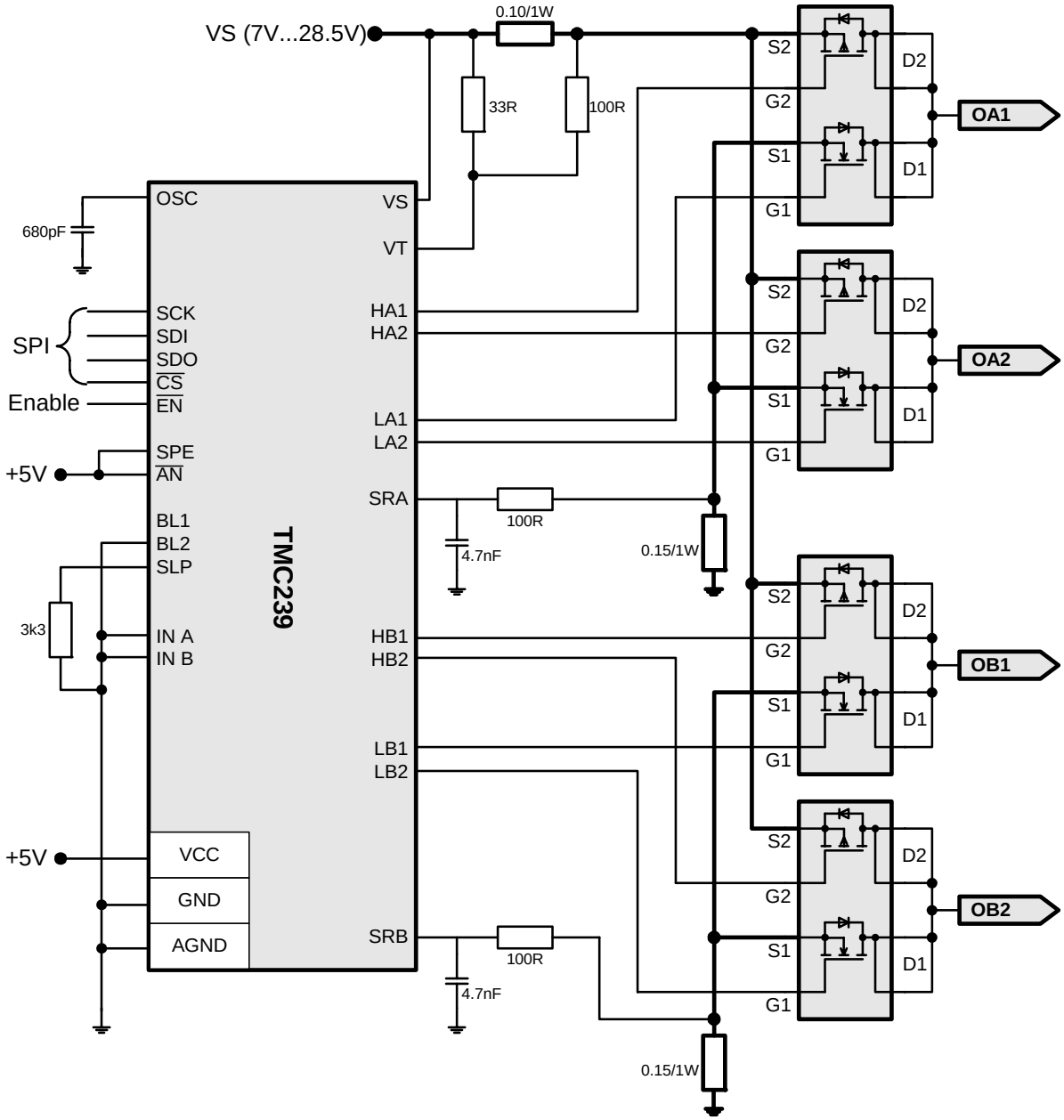


Figure 6.1: Example wiring with a TMC239

6.2 Example Layout

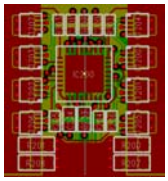


Table 6.1 shows an example layout for four TMC32NP-MLP with a TMC249A-LA driver chip. Be aware that T204 to T207, C203 and C204 and R206 to R208 are not equipped. Original size of this layout on a PCB is about 21x23mm, see Figure 6.2. Current capability with one set of transistors is 2A peak (1.4A RMS) respectively 2.8A peak (2A RMS) with limited duty cycle. A second set of transistors doubles current capability.

Figure 6.2: Example Layout in original size on PCB

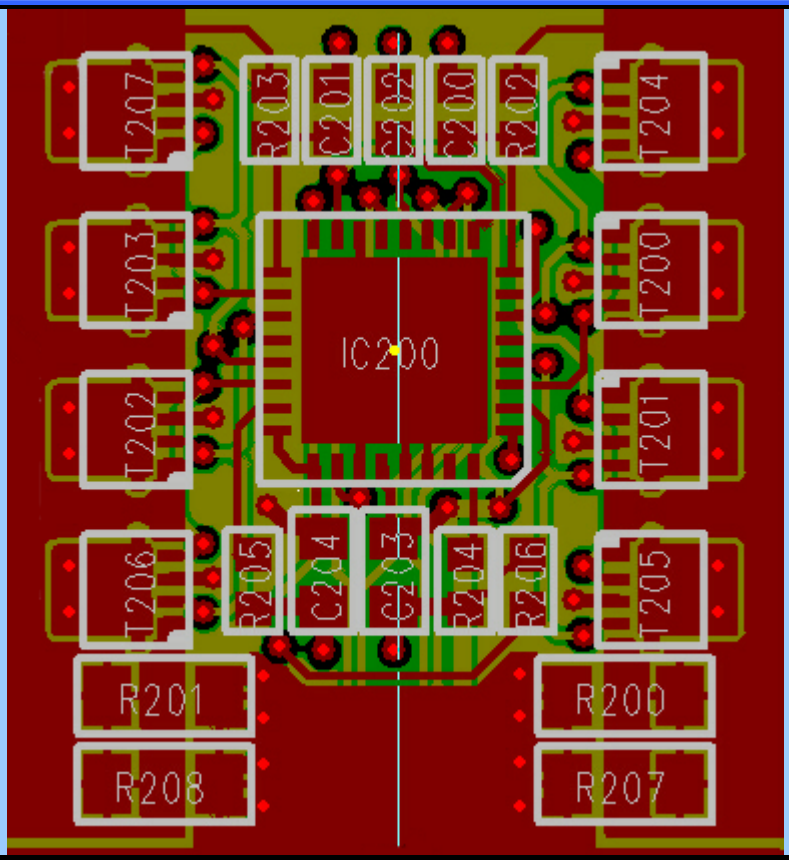
Layout	Name	Value/Description
	IC200	TMC249A-LA
	T200	TMC32NP-MLP
	T201	
	T202	
	T203	
	R200	0R15/0.5W (0805)
	R201	
	R202	100R/1% (0603)
	R203	
	R204	3k30/1% (RSLP)
	R205	0R (BL2 input)
	C200	4.7nF/50V (0603)
	C201	
	C202	680pF/50V (0603)
	C203	100nF/50V (0805)
	C204	
	T204	Not equipped, optional TMC32NP-MLP for double current
	T205	
	T206	
	T207	
	R206	Spare (BL1 input)
	R207	Optional sense resistors 0R15
	R208	

Table 6.1: Example Layout

Please refer to the evaluation board manual / website for more details.

7 Package Outline / Dimensions

MLP832 Package Outline (3mm x 2mm Micro Leaded Package)

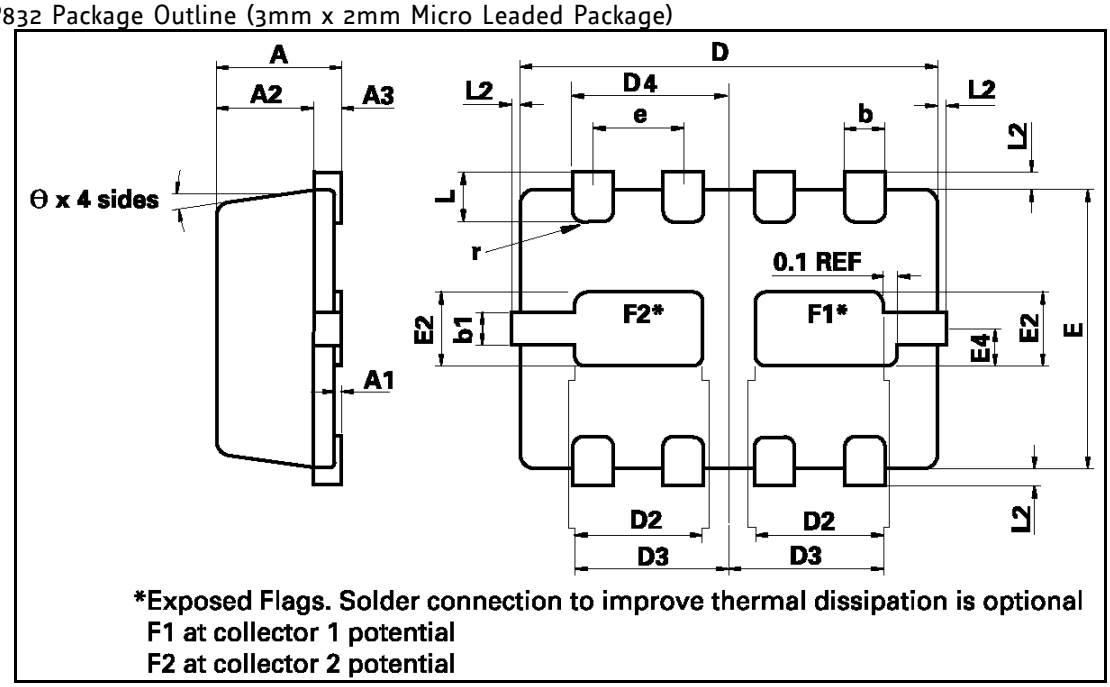


Figure 7.1: Package Outline

Controlling dimensions are in millimeters. Approximate conversions are given in inches.

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min	Max	Min	Max		Min	Max	Min	Max
A	0.80	1.00	0.0315	0.0394	e	0.65 BSC		0.0256 BSC	
A1	0.00	0.05	0.00	0.002	E	2.00 BSC		0.0787 BSC	
A2	0.65	0.75	0.0256	0.0295	E2	0.43	0.63	0.017	0.0248
A3	0.15	0.25	0.006	0.0098	L	0.20	0.45	0.0079	0.0177
b	0.24	0.34	0.0095	0.0134	L2	0.00	0.125	0.00	0.005
b1	0.17	0.30	0.0068	0.0118	r	0.075 BSC		0.0029 BSC	
D	3.00 BSC		0.118 BSC		□	0°	12°	0°	12°
D2	0.82	1.02	0.0323	0.0402	-	-	-	-	-
D3	1.01	1.20	0.0398	0.0476	-	-	-	-	-

Table 7.1: Package Dimensions

8 Revision History

8.1 Documentation Revision

Version	Comment	Author	Description
1.0	16-Mar-2007	HC	Initial Version
1.01	11-Apr-2007	HC	Example layout added

Table 8.1: Documentation Revisions

9 References

[TMC239] Microstep driver manual (see http://www.trinamic.com)
[TMC249] Microstep driver manual, with StallGuard (see http://www.trinamic.com)