

Figure 9. THD + N vs. Frequency, PVDD = 3.6 V, $R_L = 32 \Omega$

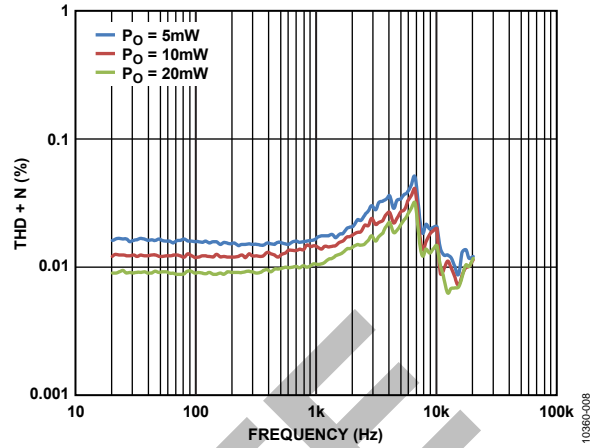


Figure 12. THD + N vs. Frequency, PVDD = 3.6 V, $R_L = 16 \Omega$

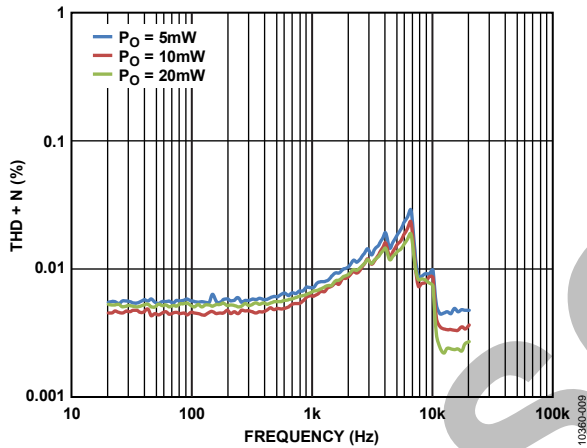


Figure 10. THD + N vs. Frequency, PVDD = 2.5 V, $R_L = 32 \Omega$

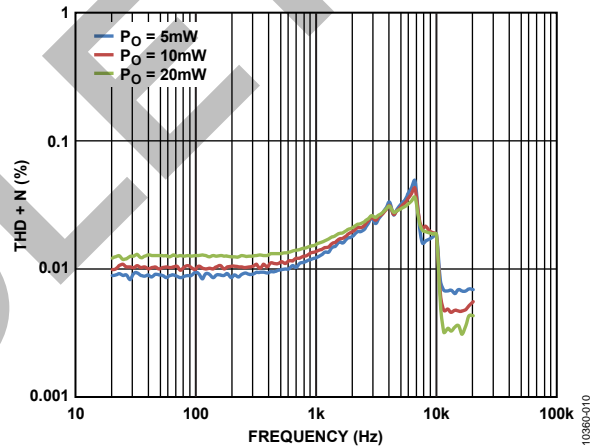


Figure 13. THD + N vs. Frequency, PVDD = 2.5 V, $R_L = 16 \Omega$

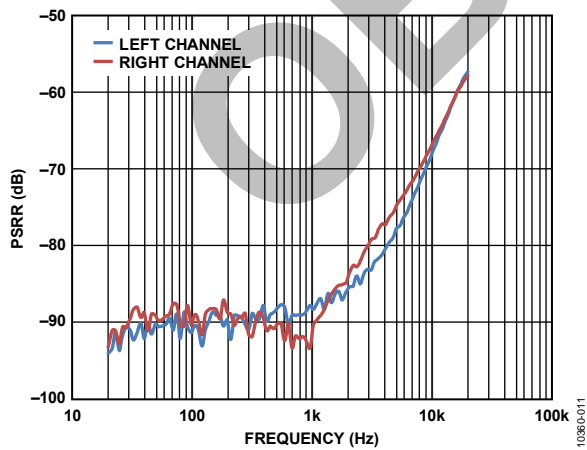


Figure 11. PSRR vs. Frequency, PVDD = 3.0 V, $R_L = 32 \Omega$

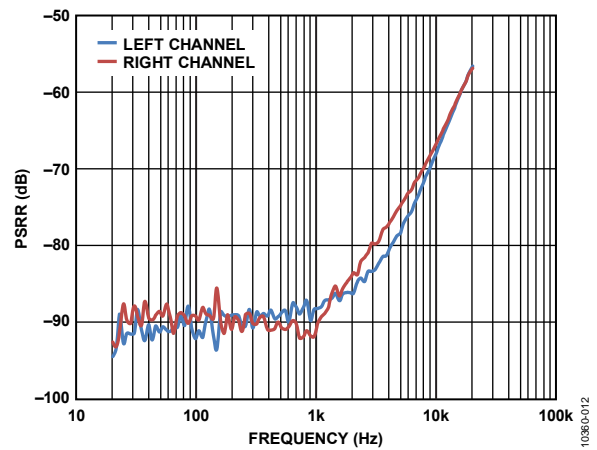


Figure 14. PSRR vs. Frequency, PVDD = 3.0 V, $R_L = 16 \Omega$

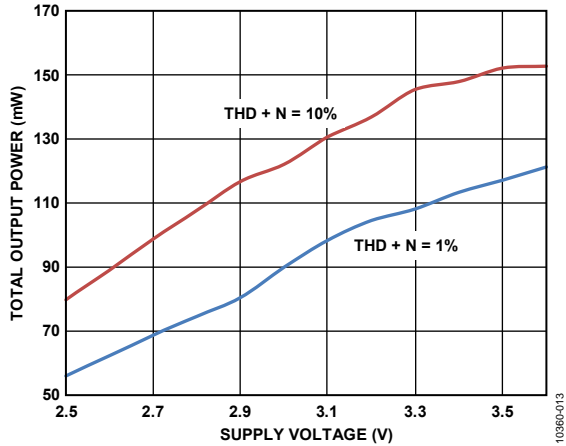


Figure 15. Output Power vs. Supply Voltage, $R_L = 32 \Omega$

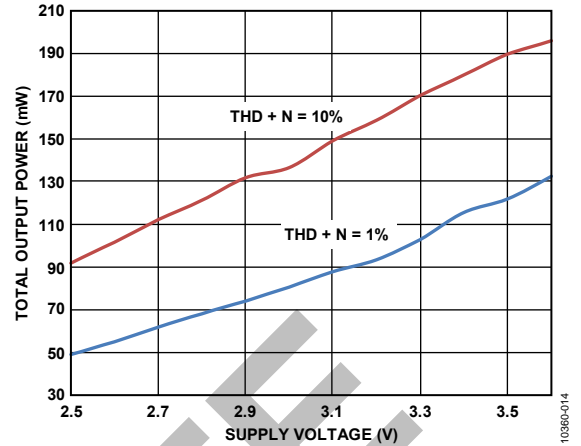


Figure 18. Output Power vs. Supply Voltage, $R_L = 16 \Omega$

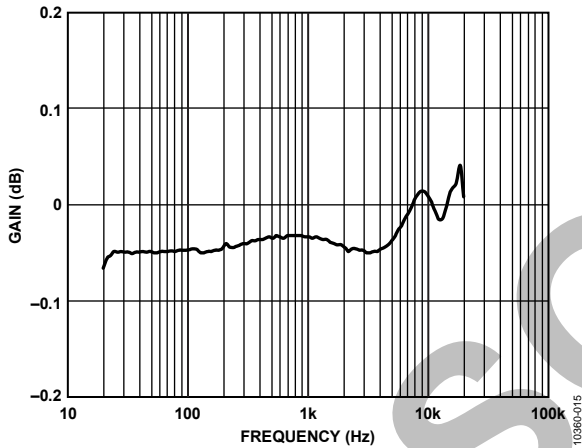


Figure 16. Frequency Response, $PVDD = 3.0 V$

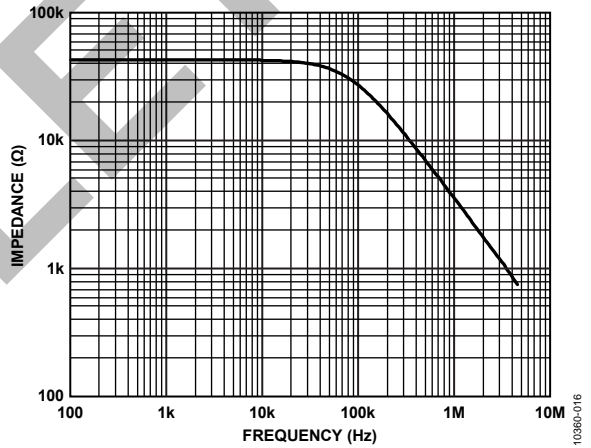


Figure 19. High-Z Mode Output Impedance vs. Frequency

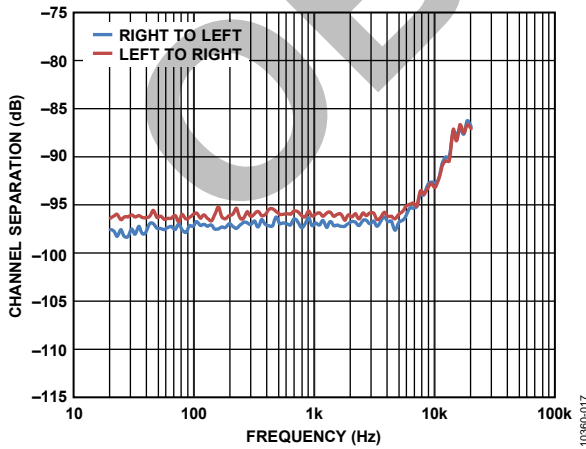


Figure 17. Channel Separation vs. Frequency, $PVDD = 3.0 V$, $R_L = 32 \Omega$

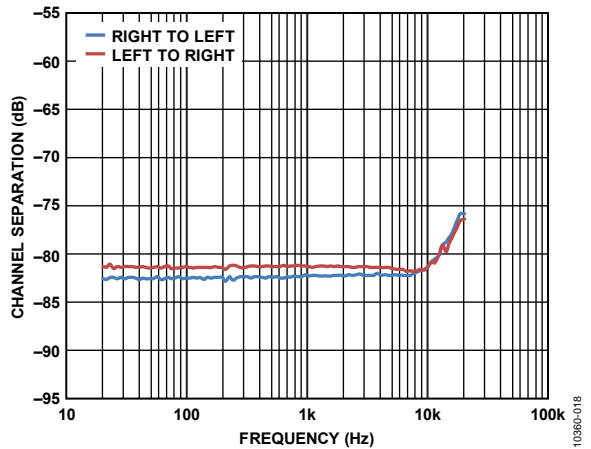


Figure 20. Channel Separation vs. Frequency, $PVDD = 3.0 V$, $R_L = 16 \Omega$

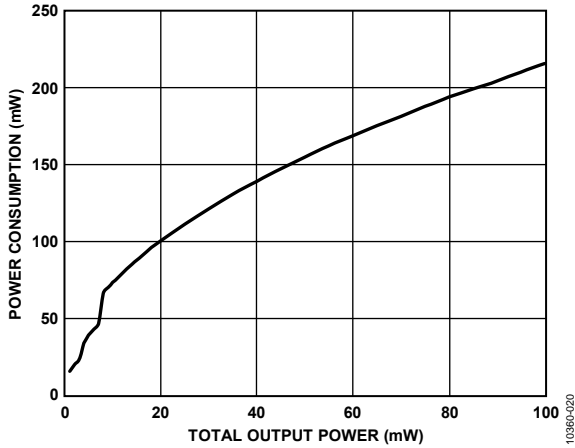


Figure 21. Power Consumption vs. Output Power, PVDD = 3.0 V, $R_L = 32 \Omega$

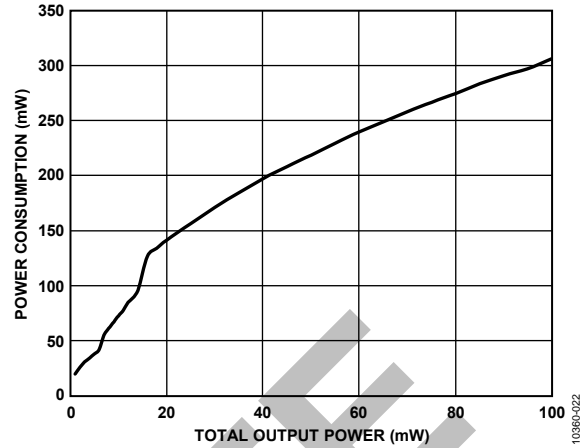


Figure 24. Power Consumption vs. Output Power, PVDD = 3.0 V, $R_L = 16 \Omega$

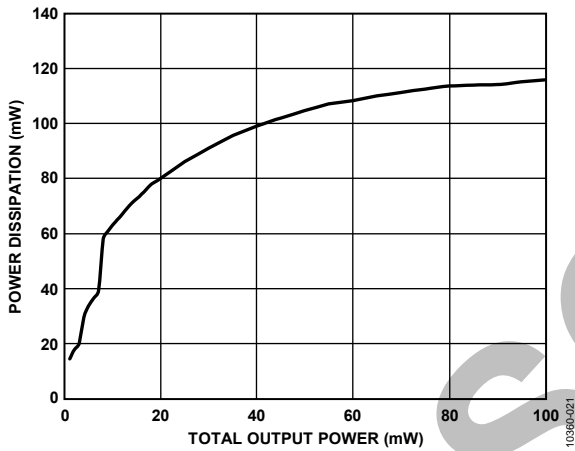


Figure 22. Power Dissipation vs. Output Power, PVDD = 3.0 V, $R_L = 32 \Omega$

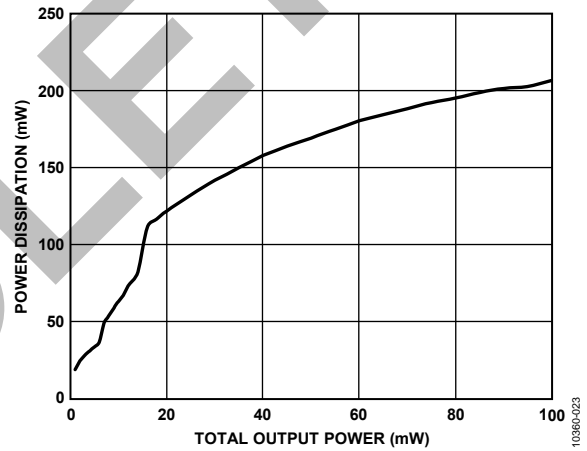


Figure 25. Power Dissipation vs. Output Power, PVDD = 3.0 V, $R_L = 16 \Omega$

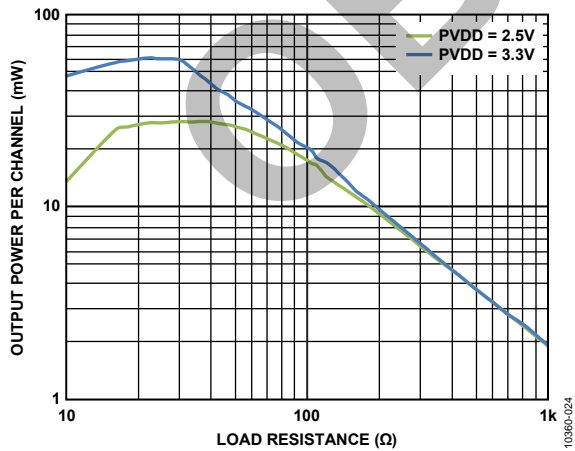


Figure 23. Maximum Output Power per Channel vs. Load Resistance, Flying Capacitor = 1 μ F, THD + N = 1%

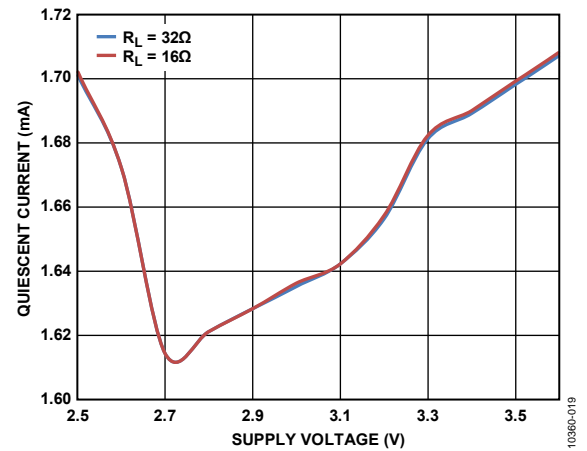


Figure 26. Quiescent Current vs. Supply Voltage

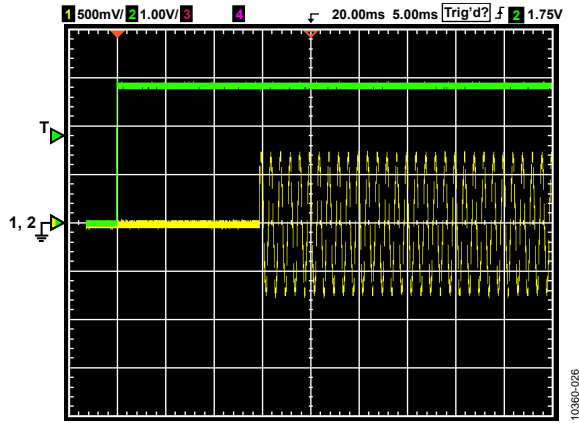


Figure 27. Start-Up Waveform vs. Time

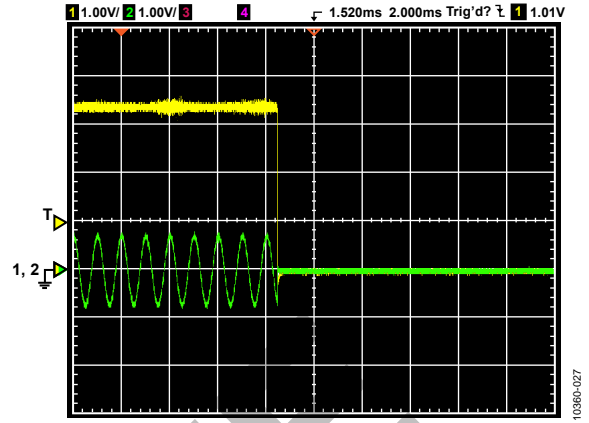


Figure 29. Shutdown Waveform vs. Time

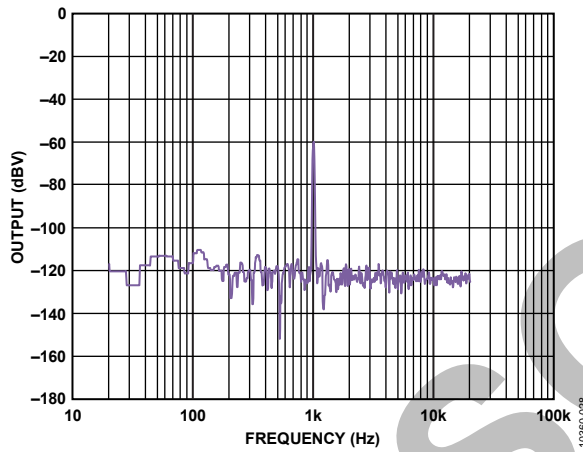


Figure 28. Output Spectrum vs. Frequency, $PVDD = 3.0\text{ V}$, $R_L = 32\ \Omega$

THEORY OF OPERATION

The [SSM2932](#) provides a high efficiency Class-G stereo headphone output that is true ground-referenced; therefore, no external coupling capacitors are required for connection to the headphones. The headphones can be connected directly to the headphone output pins, OUTL (Ball A3) and OUTR (Ball D3). The headphone amplifier uses the supply provided at PVDD (Ball A2). This supply voltage must be decoupled with a 1 μ F electrolytic capacitor, along with a 100 nF ceramic X7R capacitor.

The headphone amplifier uses Class-G architecture and generates the required power supplies with a built-in charge pump that uses a flying capacitor connected across CF1 (Ball B2) and CF2 (Ball C1). The charge pump switching frequency is approximately 54 kHz in the idle state with no input signal detected and 550 kHz when a signal is present. The generated supply voltages are available at CPVDD (Ball B3, positive rail) and CPVSS (Ball C2, negative rail).

The supply voltage of the headphone amplifier depends on the input signal to the amplifier. For lower input signal levels, the positive and negative rails are lowered, typically to \pm PVDD/2. As the signal level increases, CPVDD and CPVSS are raised to \pm 2.2 V. This rail switching allows the amplifier to achieve higher efficiency.

In most typical usage conditions, the amplifier works on the lower CPVDD and CPVSS voltages (\pm PVDD/2), thereby consuming less power. In addition, because the amplifier generates the positive and negative rails, the output amplifier is true ground-referenced, thereby eliminating the need for large coupling capacitors to drive the load.

For best audio performance, it is recommended that 2.2 μ F, X7R ceramic decoupling capacitors be used for CPVDD and CPVSS. These capacitors serve as a reservoir for the headphone amplifier.

The headphone amplifier has built-in short-circuit protection and, therefore, shuts down in the event of a short circuit on the headphone outputs.

The amplifier is designed to drive headphones with a minimum impedance of 16 Ω . Capacitive loads of up to 150 pF are supported.

AMPLIFIER GAIN

The [SSM2932](#) amplifier gain can be set to either 0 dB or 6 dB by applying the appropriate logic level to the GAIN pin (see Table 6).

Table 6. Amplifier Gain and GAIN Pin Logic Levels

Amplifier Gain	GAIN Pin Logic Level
0 dB	Low (\leq 0.5 V)
6 dB	High (\geq 1.2 V)

AMPLIFIER SHUTDOWN

Shutdown of the [SSM2932](#) amplifier is controlled by the $\overline{\text{SD}}$ pin. If a logic low is applied to this pin, the amplifier becomes inactive and draws only minimal current from the supply.

Table 7. Amplifier Shutdown

Amplifier State	$\overline{\text{SD}}$ Pin Logic Level
Shutdown	Low (\leq 0.5 V)
Power-On	High (\geq 1.2 V)

HIGH OUTPUT IMPEDANCE

The [SSM2932](#) has a HI-Z control pin that mutes the amplifier and sets the output to a high impedance. If both HI-Z and $\overline{\text{SD}}$ are set high, the amplifier remains in a high impedance state. This feature allows the headphone output jack to be shared for other functions such as video output or data transmission.

GROUND SENSE

SGND (Ball C3) is provided for sensing the dc potential at the headphone jack. It is recommended that SGND be connected directly to the ground pin of the headphone jack to ensure the lowest dc offset at the amplifier output and to eliminate pop-and-click noises when the amplifier is turned on or off. In addition, connecting the SGND ball directly to the ground pin of the headphone jack helps to reduce crosstalk between the left and right channel outputs. A dc path between the SGND pin and the system ground must also be provided.

LAYOUT

Care must be taken to lay out PCB traces and wires properly between the amplifier, load, and power supply. A good practice is to use short, wide PCB tracks to decrease voltage drops and minimize inductance. Ensure that track widths are at least 200 mil per inch of track length for lowest DCR, and use at least 1 oz or 2 oz copper thickness to minimize resistance. A poor layout increases voltage drops, consequently affecting efficiency. Use large traces for the power supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance.

Proper grounding guidelines help to improve audio performance, minimize crosstalk between channels, and prevent switching noise from coupling into the audio signal. The PCB traces that connect the output pins to the load, as well as the PCB traces to the supply pins, should be as wide as possible to maintain the minimum trace resistances. It is also recommended that a large ground plane be used for minimum impedances. The SGND pin should be connected directly to the ground pin of the headphone jack.

In addition, good PCB layout isolates critical analog paths from sources of high interference. High frequency circuits (analog and digital) should be separated from low frequency circuits.

Properly designed multilayer PCBs can reduce EMI emissions and increase immunity to the RF field by a factor of 10 or more compared with double-sided boards. A multilayer board allows a complete layer to be used for the ground plane, whereas the ground plane side of a double-sided board is often disrupted by signal crossover.

If the system has separate analog and digital ground and power planes, the analog ground plane should be directly beneath the analog power plane, and, similarly, the digital ground plane should be directly beneath the digital power plane. There should be no overlap between analog and digital ground planes or between analog and digital power planes.

OBSOLETE

TYPICAL APPLICATION CIRCUIT

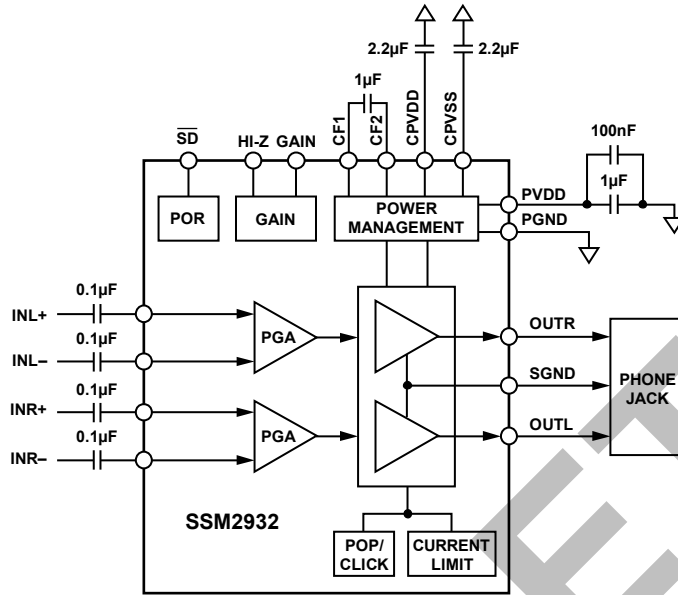


Figure 30. Application Circuit (Differential Input Configuration)

103860-031

OUTLINE DIMENSIONS

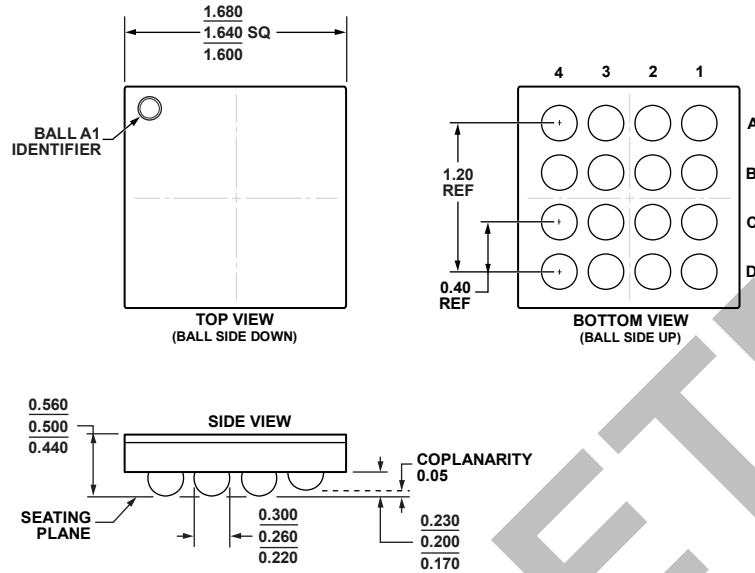


Figure 31. 16-Ball Wafer Level Chip Scale Package [WLCSP]
 1.6 mm × 1.6 mm Body
 (CB-16-11)
 Dimensions shown in millimeters

02-03-2012.A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
SSM2932ACBZ-RL	-40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-11
SSM2932ACBZ-R7	-40°C to +85°C	16-Ball Wafer Level Chip Scale Package [WLCSP]	CB-16-11
EVAL-SSM2932Z		Evaluation Board	

¹ Z = RoHS Compliant Part.

NOTES

OBSOLETE