**FUNCTIONAL BLOCK DIAGRAM**

**FEATURES**
- High Common-Mode Rejection
  - DC: 100 dB typ
  - 60 Hz: 100 dB typ
  - 20 kHz: 70 dB typ
  - 40 kHz: 62 dB typ
- Low Distortion: 0.001% typ
- Fast Slew Rate: 9.5 V/μs typ
- Wide Bandwidth: 3 MHz typ
- Low Cost
- Complements SSM2142 Differential Line Driver

**APPLICATIONS**
- Line Receivers
- Summing Amplifiers
- Buffer Amplifiers—Drives 600 Ω Load

**GENERAL DESCRIPTION**

The SSM2141 is an integrated differential amplifier intended to receive balanced line inputs in audio applications requiring a high level of noise immunity and optimum common-mode rejection. The SSM2141 typically achieves 100 dB of common-mode rejection (CMR), whereas implementing an op amp with four off-the-shelf precision resistors will typically achieve only 40 dB of CMR— inadequate for high-performance audio.

The SSM2141 achieves low distortion performance by maintaining a large slew rate of 9.5 V/μs and high open-loop gain. Distortion is less than 0.002% over the full audio bandwidth. The SSM2141 complements the SSM2142 balanced line driver. Together, these devices comprise a fully integrated solution for equivalent transformer balancing of audio signals without the problems of distortion, EMI fields, and high cost.

Additional applications for the SSM2141 include summing signals, differential preamplifiers, and 600 Ω low distortion buffer amplifiers. For similar performance with G = 1/2, see SSM2143.

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**REV. C**

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### SSM2141- SPECIFICATIONS

**ELECTRICAL CHARACTERISTICS** (@ $V_S = \pm 18 \, \text{V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td>$V_{OS}$</td>
<td>$V_{CM} = 0 , \text{V}$</td>
<td>25</td>
<td>1000</td>
<td>25</td>
<td>µV</td>
</tr>
<tr>
<td>GAIN ERROR</td>
<td></td>
<td>No Load, $V_{IN} = \pm 10 , \text{V}$, $R_S = 0 , \Omega$</td>
<td>0.001</td>
<td>0.01</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>$IVR$</td>
<td>(Note 1)</td>
<td>±10</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>COMMON-MODE REJECTION</td>
<td>$CMR$</td>
<td>$V_{CM} = \pm 10 , \text{V}$</td>
<td>80</td>
<td>100</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>POWER SUPPLY REJECTION RATIO</td>
<td>$PSRR$</td>
<td>$V_S = \pm 6 , \text{V}$ to $\pm 18 , \text{V}$</td>
<td>0.7</td>
<td>15</td>
<td></td>
<td>µV/V</td>
</tr>
<tr>
<td>OUTPUT SWING</td>
<td>$V_O$</td>
<td>$R_L = 2 , \text{k}\Omega$</td>
<td>±13</td>
<td>±14.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SHORT-CIRCUIT CURRENT LIMIT</td>
<td>$I_{SC}$</td>
<td>Output Shorted to Ground</td>
<td>+45/-15</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>SMALL-SIGNAL BANDWIDTH (-3 dB)</td>
<td>$BW$</td>
<td>$R_L = 2 , \text{k}\Omega$</td>
<td>3</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>SLEW RATE</td>
<td>$SR$</td>
<td>$R_L = 2 , \text{k}\Omega$</td>
<td>6</td>
<td>9.5</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>TOTAL HARMONIC DISTORTION</td>
<td>$THD$</td>
<td>$R_L = 100 , \text{k}\Omega$</td>
<td>0.001</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 600 , \Omega$</td>
<td>0.01</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>CAPACITIVE LOAD DRIVE CAPABILITY</td>
<td>$C_L$</td>
<td>No Oscillation</td>
<td>300</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>SUPPLY CURRENT</td>
<td>$I_{SY}$</td>
<td>No Load</td>
<td>2.5</td>
<td>3.5</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES**

1. Input Voltage Range Guaranteed by CMR test.
2. Specifications subject to change without notice

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**ELECTRICAL CHARACTERISTICS** (@ $V_S = \pm 18 \, \text{V}$, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$)

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<th>Parameter</th>
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<th>Units</th>
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</thead>
<tbody>
<tr>
<td>OFFSET VOLTAGE</td>
<td>$V_{OS}$</td>
<td>$V_{CM} = 0 , \text{V}$</td>
<td>-2500</td>
<td>200</td>
<td>2500</td>
<td>µV</td>
</tr>
<tr>
<td>GAIN ERROR</td>
<td></td>
<td>No Load, $V_{IN} = \pm 10 , \text{V}$, $R_S = 0 , \Omega$</td>
<td>0.002</td>
<td>0.02</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>$IVR$</td>
<td>(Note 1)</td>
<td>±10</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>COMMON-MODE REJECTION</td>
<td>$CMR$</td>
<td>$V_{CM} = \pm 10 , \text{V}$</td>
<td>75</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>POWER SUPPLY REJECTION RATIO</td>
<td>$PSRR$</td>
<td>$V_S = \pm 6 , \text{V}$ to $\pm 18 , \text{V}$</td>
<td>1.0</td>
<td>20</td>
<td></td>
<td>µV/V</td>
</tr>
<tr>
<td>OUTPUT SWING</td>
<td>$V_O$</td>
<td>$R_L = 2 , \text{k}\Omega$</td>
<td>±13</td>
<td>±14.7</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SLEW RATE</td>
<td>$SR$</td>
<td>$R_L = 2 , \text{k}\Omega$</td>
<td>9.5</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>SUPPLY CURRENT</td>
<td>$I_{SY}$</td>
<td>No Load</td>
<td>2.6</td>
<td>4.0</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

**NOTES**

1. Input Voltage Range Guaranteed by CMR test.
2. Specifications subject to change without notice
ABSOLUTE MAXIMUM RATINGS

Supply Voltage ...................... ±18 V
Input Voltage \(^1\) ................. Supply Voltage
Output Short-Circuit Duration ........ Continuous
Storage Temperature Range
\( P \) Package ..................... -65°C to +150°C
Lead Temperature (Soldering, 60 sec) +300°C
Junction Temperature ............... +150°C
Operating Temperature Range .......... -40°C to +85°C

NOTES
\(^1\) For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
\(^2\) \( \theta_J \) is specified for worst case mounting conditions, i.e., \( \theta_J \) is specified for device in socket for P-DIP package.

Typical Performance Characteristics

Small Signal Transient Response

Common-Mode Rejection vs. Frequency

Power Supply Rejection vs. Frequency

Total Harmonic Distortion vs. Frequency

Dynamic Intermodulation Distortion vs. Frequency

Package Type | \( \theta_J \) \(^2\) | \( \theta_J \) | Units
---|---|---|---
8-Pin Plastic DIP (P) | 103 | 43 | °C/W

NOTES
\(^1\) For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.
\(^2\) \( \theta_J \) is specified for worst case mounting conditions, i.e., \( \theta_J \) is specified for device in socket for P-DIP package.
SSM2141 - Typical Performance Characteristics

Input Offset Voltage vs. Temperature

Closed-Loop Gain vs. Frequency

Closed-Loop Output Impedance vs. Frequency

Gain Error vs. Temperature

Slew Rate vs. Temperature

Supply Current vs. Temperature

Supply Current vs. Supply Voltage

Maximum Output Voltage vs. Output Current (Source)

Maximum Output Voltage vs. Output Current (Sink)
APPLICATIONS INFORMATION

The SSM 2141 represents a versatile analog building block. In order to capitalize on fast settling time, high slew rate, and high CMR, proper decoupling and grounding techniques must be employed. For decoupling, place 0.1 µF capacitor located within close proximity from each supply pin to ground.

Slew Rate Test Circuit
MAINTAINING COMMON-MODE REJECTION

In order to achieve the full common-mode rejection capability of the SSM2141, the source impedance must be carefully controlled. Slight imbalances of the source resistance will result in a degradation of DC CMR—even a 5 Ω imbalance will degrade CMR by 20 dB. Also, the matching of the reactive source impedance must be matched in order to preserve the CMRR over frequency.

Figure 1. Precision Difference Amplifier. Rejects Common-Mode Signal \( \frac{E_1 + E_2}{2} \) by 100 dB

Figure 2. Precision Unity Gain Inverting Amplifier

Figure 3. Precision Summing Amplifier

Figure 4. Precision Summing Amplifier with Gain

Figure 5. Suitable Instrumentation Amplifier Requirements can be Addressed by Using an Input Stage Consisting of A1, A2, R1 and R2
OUTLINE DIMENSIONS

Figure 6. 8-Lead Plastic Dual In-Line Package [PDIP] Narrow Body (N-8)
Dimensions shown in inches and (millimeters)

Figure 7. 8-Lead Standard Small Outline Package [SOIC N] Narrow Body (R-8)
Dimensions shown in millimeters and (inches)
## SSM2141

### ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>SSM2141PZ</td>
<td>−40°C ≤ T_A ≤ +85°C</td>
<td>8-Lead PDIP</td>
<td>N-8</td>
</tr>
<tr>
<td>SSM2141SZ</td>
<td>−40°C ≤ T_A ≤ +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
</tr>
<tr>
<td>SSM2141SZ-REEL</td>
<td>−40°C ≤ T_A ≤ +85°C</td>
<td>8-Lead SOIC_N</td>
<td>R-8</td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.

### REVISION HISTORY

6/11—Rev. B to Rev. C

Updated Outline Dimensions ......................................................... 7
Changes to Ordering Guide ............................................................ 8

5/91—Rev. A to Rev. B