FEATURES

- High slew rate: 9 V/µs
- Wide bandwidth: 4 MHz
- Low supply current: 250 µA/amplifier maximum
- Low offset voltage: 3 mV maximum
- Low bias current: 100 pA maximum
- Fast settling time
- Common-mode range includes V+
- Unity-gain stable
- 14-ball wafer level chip scale for quad

APPLICATIONS

- Active filters
- Fast amplifiers
- Integrators
- Supply current monitoring

GENERAL DESCRIPTION

The OP282/OP482 dual and quad operational amplifiers feature excellent speed at exceptionally low supply currents. The slew rate is typically 9 V/µs with a supply current of less than 250 µA per amplifier. These unity-gain stable amplifiers have a typical gain bandwidth of 4 MHz.

The JFET input stage of the OP282/OP482 ensures that the bias current is typically a few picoamps and is less than 500 pA over the full temperature range. The offset voltage is less than 3 mV for the dual amplifier and less than 4 mV for the quad amplifier.

With a wide output swing (within 1.5 V of each supply), low power consumption, and high slew rate, the OP282/OP482 are ideal for battery-powered systems or power-restricted applications. An input common-mode range that includes the positive supply makes the OP282/OP482 an excellent choice for high-side signal conditioning.

The OP282/OP482 are specified over the extended industrial temperature range. The OP282 is available in the standard 8-lead, narrow SOIC and MSOP packages. The OP482 is available in the PDIP and narrow SOIC packages, as well as a 14-ball WLCSP.
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9/13—Rev. H to Rev. I
   Changes to Figure 5 .................................................. 1
   Updated Outline Dimensions ................................... 14
   Changes to Ordering Guide ..................................... 16
9/10—Rev. G to Rev. H
   Added WLCSP ....................................................... Universal
   Changes to Features Section ................................... 1
   Changes to General Description Section .................. 1
   Added Figure 5; Renumbered Sequentially ............... 1
   Changes to Large-Signal Voltage Gain Parameter, Table 1 .................................................. 3
   Changes to Table 2, Thermal Resistance Section, and Table 3 ........................................ 4
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   Added Figure 53 .................................................... 16
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   Changes to Phase Inversion Section ................. 12
   Deleted Figure 45 .................................................. 12
   Added Figure 45 and Figure 46 ............................... 12
   Updated Outline Dimensions ................................ 14
   Changes to Ordering Guide ................................... 16
10/04—Rev. E to Rev. F
   Deleted 8-Lead PDIP ............................................ Universal
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   Changes to Format and Layout ................................. 1
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# SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS

At $V_S = \pm 15.0 \text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted; applies to both A and G grades.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>$V_{OS}$</td>
<td>OP282</td>
<td>0.2</td>
<td>3</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OP282, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$</td>
<td>4.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OP482</td>
<td>0.2</td>
<td>4</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>OP482, $-40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$</td>
<td>6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_B$</td>
<td>$V_{CM} = 0 \text{ V}$</td>
<td>3</td>
<td>100</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CM} = 0 \text{ V}$</td>
<td>500</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$I_{OS}$</td>
<td>$V_{CM} = 0 \text{ V}$</td>
<td>1</td>
<td>50</td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{CM} = 0 \text{ V}$</td>
<td>250</td>
<td></td>
<td></td>
<td>pA</td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td></td>
<td>$-11 \text{ V} \leq V_{CM} \leq +15 \text{ V}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>CMRR</td>
<td>$-11 \text{ V} \leq V_{CM} \leq +15 \text{ V}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$</td>
<td>70</td>
<td>90</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Large-Signal Voltage Gain</td>
<td>$A_{VO}$</td>
<td>$R_L = 10 \text{ k}\Omega, V_O = \pm 13.5 \text{ V}$</td>
<td>20</td>
<td></td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10 \text{ k}\Omega, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$</td>
<td>15</td>
<td></td>
<td></td>
<td>V/mV</td>
</tr>
<tr>
<td>Offset Voltage Drift</td>
<td>$\Delta V_{OS}/\Delta T$</td>
<td>OP282</td>
<td>10</td>
<td></td>
<td></td>
<td>µV/°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>OP482</td>
<td>8</td>
<td></td>
<td></td>
<td>pA/°C</td>
</tr>
<tr>
<td>OUTPUT CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage High</td>
<td>$V_{OH}$</td>
<td>$R_L = 10 \text{ k}\Omega$</td>
<td>13.5</td>
<td>13.9</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage Low</td>
<td>$V_{OL}$</td>
<td>$R_L = 10 \text{ k}\Omega$</td>
<td></td>
<td>-13.9</td>
<td>-13.5</td>
<td>V</td>
</tr>
<tr>
<td>Short-Circuit Limit</td>
<td>$I_{SC}$</td>
<td>Source</td>
<td>3</td>
<td>10</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Sink</td>
<td></td>
<td>-12</td>
<td>-8</td>
<td>mA</td>
</tr>
<tr>
<td>Open-Loop Output Impedance</td>
<td>$Z_{OUT}$</td>
<td>$f = 1 \text{ MHz}$</td>
<td></td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>$V_S = \pm 4.5 \text{ V} \text{ to } \pm 18 \text{ V}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$</td>
<td>25</td>
<td>316</td>
<td></td>
<td>µV/V</td>
</tr>
<tr>
<td>Supply Current/Amplifier</td>
<td>$I_{SY}$</td>
<td>$V_O = 0 \text{ V}, -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$</td>
<td>210</td>
<td>250</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Supply Voltage Range</td>
<td>$V_S$</td>
<td>$\pm 4.5 \text{ V}$</td>
<td></td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>DYNAMIC PERFORMANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>$R_L = 10 \text{ k}\Omega$</td>
<td>7</td>
<td>9</td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>Full-Power Bandwidth</td>
<td>BWp</td>
<td>1% distortion</td>
<td>125</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>Settling Time</td>
<td>$t_s$</td>
<td>To 0.01%</td>
<td>1.6</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>GBP</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Phase Margin</td>
<td>$\phi_M$</td>
<td></td>
<td>55</td>
<td></td>
<td></td>
<td>Degrees</td>
</tr>
<tr>
<td>NOISE PERFORMANCE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Noise</td>
<td>$e_n, p-p$</td>
<td>0.1 Hz to 10 Hz</td>
<td>1.3</td>
<td></td>
<td></td>
<td>µV p-p</td>
</tr>
<tr>
<td>Voltage Noise Density</td>
<td>$e_n$</td>
<td>$f = 1 \text{ kHz}$</td>
<td>36</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>Current Noise Density</td>
<td>$i_n$</td>
<td></td>
<td>0.01</td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
</tbody>
</table>

1 The input bias and offset currents are characterized at $T_A = T_J = 85^\circ\text{C}$. Bias and offset currents are guaranteed but not tested at $-40^\circ\text{C}$. 
ABSOLUTE MAXIMUM RATINGS

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>±18 V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>±18 V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>36 V</td>
</tr>
<tr>
<td>Output Short-Circuit Duration</td>
<td>Indefinite</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>Junction Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering 60 sec)</td>
<td>300°C</td>
</tr>
</tbody>
</table>

1 For supply voltages less than ±18 V, the absolute maximum input voltage is equal to the supply voltage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

\( \theta_{JA} \) is specified for the worst-case conditions, that is, a device in socket for PDIP. \( \theta_{JA} \) is specified for a device soldered in the circuit board for SOIC, MSOP, and WLCSP packages. This was measured using a standard 4-layer board.

Table 3.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>( \theta_{JA} )</th>
<th>( \theta_{JC} )</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Lead MSOP [RM]</td>
<td>142</td>
<td>45</td>
<td>°C/W</td>
</tr>
<tr>
<td>8-Lead SOIC_N (S-Suffix) [R]</td>
<td>120</td>
<td>45</td>
<td>°C/W</td>
</tr>
<tr>
<td>14-Lead PDIP (P-Suffix) [N]</td>
<td>83</td>
<td>39</td>
<td>°C/W</td>
</tr>
<tr>
<td>14-Lead SOIC_N (S-Suffix) [R]</td>
<td>112</td>
<td>35</td>
<td>°C/W</td>
</tr>
<tr>
<td>14-Ball WLCSP [CB]²</td>
<td>70</td>
<td>16</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1 Simulated thermal numbers per JESD51-9.
2 Junction-to-board thermal resistance.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
TYPICAL PERFORMANCE CHARACTERISTICS

**Figure 6. OP282 Open-Loop Gain and Phase vs. Frequency**

**Figure 7. OP282 Open-Loop Gain vs. Temperature**

**Figure 8. OP282 Small-Signal Overshoot vs. Load Capacitance**

**Figure 9. OP282 Closed-Loop Gain vs. Frequency**

**Figure 10. OP282 Slew Rate vs. Temperature**

**Figure 11. OP282 Input Bias Current vs. Temperature**
**Figure 12. OP282 Voltage Noise Density vs. Frequency**

**Figure 15. OP282 Output Voltage Swing vs. Supply Voltage**

**Figure 13. OP282 Input Bias Current vs. Common-Mode Voltage**

**Figure 16. OP282 Closed-Loop Output Impedance vs. Frequency**

**Figure 14. OP282 Supply Current vs. Supply Voltage**

**Figure 17. OP282 Supply Current vs. Temperature**
Figure 18. OP282 Absolute Output Voltage vs. Load Resistance

Figure 19. OP282 PSRR vs. Frequency

Figure 20. OP282 Short-Circuit Current vs. Temperature

Figure 21. OP282 Maximum Output Swing vs. Frequency

Figure 22. OP282 CMRR vs. Frequency

Figure 23. OP282 VOS Distribution, SOIC_N Package
### OP282/OP482 Data Sheet

#### INPUT BIAS CURRENT (pA) vs. TEMPERATURE (°C)

- **Figure 30. OP482 Input Bias Current vs. Temperature**

#### COMMON-MODE VOLTAGE (V)

- **Figure 33. OP482 Input Bias Current vs. Common-Mode Voltage**

#### PHASE MARGIN (Degrees) vs. TEMPERATURE (°C)

- **Figure 31. OP482 Phase Margin and Gain Bandwidth Product vs. Temperature**

#### GAIN BANDWIDTH PRODUCT (MHz) vs. TEMPERATURE (°C)

- **Figure 34. OP482 Relative Supply Current vs. Supply Voltage**

#### VOLTAGE NOISE DENSITY (nV/√Hz) vs. FREQUENCY (Hz)

- **Figure 32. OP482 Voltage Noise Density vs. Frequency**

#### OUTPUT VOLTAGE SWING (V) vs. SUPPLY VOLTAGE (V)

- **Figure 35. OP482 Output Voltage Swing vs. Supply Voltage**
Figure 42. OP482 Common-Mode Rejection Ratio (CMRR) vs. Frequency

Figure 43. OP482 VOS Distribution, PDIP Package

Figure 44. OP482 TCVos Distribution, PDIP Package
APPLICATIONS INFORMATION

The OP282 and OP482 are dual and quad JFET op amps that are optimized for high speed at low power. This combination makes these amplifiers excellent choices for battery-powered or low power applications that require above average performance. Applications benefiting from this performance combination include telecommunications, geophysical exploration, portable medical equipment, and navigational instrumentation.

HIGH-SIDE SIGNAL CONDITIONING

Many applications require the sensing of signals near the positive rail. OP282 and OP482 were tested and are guaranteed over a common-mode range (\(-11 \text{ V} \leq V_{\text{CM}} \leq +15 \text{ V}\)) that includes the positive supply.

One application where such sensing is commonly used is in the sensing of power supply currents. Therefore, the OP282/OP482 can be used in current sensing applications, such as the partial circuit shown in Figure 45. In this circuit, the voltage drop across a low value resistor, such as the 0.1 \(\Omega\) shown here, is amplified and compared to 7.5 V. The output can then be used for current limiting.

![Figure 45. High-Side Signal Conditioning](image)

PHASE INVERSION

Most JFET input amplifiers invert the phase of the input signal if either input exceeds the input common-mode range. For the OP282/OP482, a negative signal in excess of 11 V causes phase inversion. This is caused by saturation of the input stage, leading to the forward-biasing of a gate-drain diode. Phase reversal in the OP282/OP482 can be prevented by using Schottky diodes to clamp the input terminals to each other and to the supplies. In the simple buffer circuit shown in Figure 46, D1 protects the op amp against phase reversal. R1, D2, and D3 limit the input current when the input exceeds the supply rail. The resistor should be selected to limit the amount of input current below the absolute maximum rating.

![Figure 46. Phase Reversal Solution Circuit](image)

ACTIVE FILTERS

The wide bandwidth and high slew rates of the OP282/OP482 make either one an excellent choice for many filter applications. There are many active filter configurations, but the four most popular configurations are Butterworth, elliptic, Bessel, and Chebyshev. Each type has a response that is optimized for a given characteristic, as shown in Table 4.

![Figure 47. No Phase Reversal](image)

<table>
<thead>
<tr>
<th>Type</th>
<th>Selectivity</th>
<th>Overshoot</th>
<th>Phase</th>
<th>Amplitude (Pass Band)</th>
<th>Amplitude (Stop Band)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Butterworth</td>
<td>Moderate</td>
<td>Good</td>
<td>Nonlinear</td>
<td>Maximum flat</td>
<td>Equal ripple</td>
</tr>
<tr>
<td>Chebyshev</td>
<td>Good</td>
<td>Moderate</td>
<td>Equal ripple</td>
<td>Equal ripple</td>
<td>Equal ripple</td>
</tr>
<tr>
<td>Elliptic</td>
<td>Best</td>
<td>Poor</td>
<td>Linear</td>
<td>Equal ripple</td>
<td>Equal ripple</td>
</tr>
<tr>
<td>Bessel (Thompson)</td>
<td>Poor</td>
<td>Best</td>
<td>Linear</td>
<td>Equal ripple</td>
<td></td>
</tr>
</tbody>
</table>

Table 4. Active Filter Configurations
PROGRAMMABLE STATE VARIABLE FILTER

The circuit shown in Figure 48 can be used to accurately program the Q, the cutoff frequency \( (f_C) \), and the gain of a two-pole state variable filter. OP482 devices have been used in this design because of their high bandwidths, low power, and low noise. This circuit takes only three packages to build because of the quad configuration of the op amps and DACs.

The DACs shown are used in the voltage mode; therefore, many values are dependent on the accuracy of the DAC only and not on the absolute values of the DAC’s resistive ladders. This makes this circuit unusually accurate for a programmable filter. Adjusting DAC 1 changes the signal amplitude across R1; therefore, the DAC attenuation times R1 determines the amount of signal current that charges the integrating capacitor, C1.

This cutoff frequency can now be expressed as

\[
f_C = \frac{1}{2\pi R1C1} \left( \frac{D1}{256} \right)
\]

where \( D1 \) is the digital code for the DAC.

The gain of this circuit is set by adjusting D3. The gain equation is

\[
Gain = \frac{R4}{R5} \left( \frac{D3}{256} \right)
\]

DAC 2 is used to set the Q of the circuit. Adjusting this DAC controls the amount of feedback from the band-pass node to the input summing node. Note that the digital value of the DAC is in the numerator; therefore, zero code is not a valid operating point.

\[
Q = \frac{R2}{R3} \left( \frac{256}{D2} \right)
\]
OUTLINE DIMENSIONS

Figure 49. 8-Lead Mini Small Outline Package (MSOP) (RM-8)
Dimensions shown in millimeters

Figure 50. 8-Lead Standard Small Outline Package [SOIC, N] Narrow Body S-Suffix (R-8)
Dimensions shown in millimeters and (inches)
Figure S1. 14-Lead Plastic Dual In-Line Package [PDIP]  
P-Suffix (N-14)  
Dimension shown in inches and (millimeters)

Figure S2. 14-Lead Standard Small Outline Package [SOIC_N]  
Narrow Body  
S-Suffix (R-14)  
Dimensions shown in millimeters and (inches)
Figure 53. 14-Ball Wafer Level Chip Scale Package [WLCSP] CB-14-2

Controlling dimensions are millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
<th>Branding</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP282ARMZ</td>
<td>−40°C to +85°C</td>
<td>8-Lead MSOP</td>
<td>RM-8</td>
<td>A0B</td>
</tr>
<tr>
<td>OP282ARMZ-REEL</td>
<td>−40°C to +85°C</td>
<td>8-Lead MSOP</td>
<td>RM-8</td>
<td>A0B</td>
</tr>
<tr>
<td>OP282GS</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>S-Suffix (R-8)</td>
<td></td>
</tr>
<tr>
<td>OP282GS-REEL</td>
<td>−40°C to +85°C</td>
<td>8-Lead SOIC_N</td>
<td>S-Suffix (R-8)</td>
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1 Z = RoHS Compliant Part.