**FEATURES**

- Enables Safe Board Insertion and Removal from a Power Supply
- 4µA Supply Current
- 0.3µA Shutdown Current
- Wide Operating Voltage Range: 2.7V to 36V
- Reverse Supply Protection to –40V
- Adjustable Analog Current Limit with Circuit Breaker
- Automatic Retry or Latchoff on Current Fault
- Overvoltage and Undervoltage Monitoring
- Controls Single or Back-to-Back N-Channel MOSFETs
- 12-Lead MSOP and 3mm × 3mm QFN Packages
- AEC-Q100 Qualified for Automotive Applications

**APPLICATIONS**

- Battery Powered Equipment
- Solar Powered Systems
- Portable Instruments
- Automotive Battery Protection
- Energy Harvesting

**DESCRIPTION**

The **LTC®4231** is a micropower Hot Swap controller that allows safe circuit board insertion and removal from a live power supply. An internal high side switch driver controls the gate of an external N-channel MOSFET. Back-to-back MOSFETs can be used for reverse supply protection down to –40V.

The LTC4231 provides a debounce delay and allows the GATE to be ramped up at an adjustable rate. After start-up, the LTC4231’s quiescent current drops to 4µA during normal operation with output active. UVL, UVH, OV and GNDSW monitor overvoltage and undervoltage periodically, keeping total quiescent current low. Pulling SHDN low shuts down the LTC4231 and quiescent current drops to 0.3µA.

During an overcurrent fault, the LTC4231 actively limits current while running an adjustable timer. The LTC4231-1 remains off after a current fault while the LTC4231-2 automatically reapplies power after a cool-down period.

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**LTC4231**

### ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

**Supply Voltage**
- IN..................................................−40V to 40V

**Input Voltages**
- SENSE, SOURCE......................................−40V to 40V
- IN−SENSE.............................................−40V to 40V
- SHDN, UVL, UVH, OV, GNDSW..............−0.3V to 40V

**Input Currents**
- SHDN, UVL, UVH, OV, GNDSW (Note 3)...........−1mA

**Output Voltages**
- GATE−SOURCE (Note 4)...........................−0.3V to 13V
- GATE−SENSE...........................................−40V to 20V
- STATUS..................................................−0.3V to 40V
- TIMER..................................................−0.3V to 40V

**Operating Ambient Temperature Range**
- LTC4231C...........................................−40°C to 70°C
- LTC4231I.............................................−40°C to 85°C
- LTC4231H.............................................−40°C to 125°C

**Storage Temperature Range**...........−65°C to 150°C

**Lead Temperature (Soldering, 10 sec)**
- MSOP Package........................................300°C

### PIN CONFIGURATION

![PIN CONFIGURATION Diagram]

**TOP VIEW**

**UD PACKAGE**
- 12-LEAD (3mm × 3mm) PLASTIC QFN
- T_JMAX = 150°C, θ_JA = 68°C/W
- EXPOSED PAD (PIN 13) PCB CONNECTION TO GND IS OPTIONAL

### ORDER INFORMATION

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC4231CU−1#PBF</td>
<td>LTC4231CU−1#TRPBF</td>
<td>LGMX</td>
<td>12-Lead (3mm × 3mm) Plastic QFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC4231CU−2#PBF</td>
<td>LTC4231CU−2#TRPBF</td>
<td>LGSP</td>
<td>12-Lead (3mm × 3mm) Plastic QFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC4231UD−1#PBF</td>
<td>LTC4231UD−1#TRPBF</td>
<td>LGMX</td>
<td>12-Lead (3mm × 3mm) Plastic QFN</td>
<td>−40°C to 85°C</td>
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<tr>
<td>LTC4231UD−2#PBF</td>
<td>LTC4231UD−2#TRPBF</td>
<td>LGSP</td>
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<td>−40°C to 85°C</td>
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<tr>
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<td>LTC4231HUD−1#TRPBF</td>
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<td>LTC4231HUD−2#PBF</td>
<td>LTC4231HUD−2#TRPBF</td>
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<td>12-Lead (3mm × 3mm) Plastic QFN</td>
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<td>42311</td>
<td>12-Lead Plastic MSOP</td>
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<td>LTC4231CMS−2#TRPBF</td>
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<td>12-Lead Plastic MSOP</td>
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<td>LTC4231IM−1#TRPBF</td>
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<td>12-Lead Plastic MSOP</td>
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<td>LTC4231IM−2#TRPBF</td>
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<td>12-Lead Plastic MSOP</td>
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<td>12-Lead Plastic MSOP</td>
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<td>12-Lead Plastic MSOP</td>
<td>−40°C to 125°C</td>
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</table>

Rev. B

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ORDER INFORMATION

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<td>LTC4231JMS-1#WTRPBF</td>
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<td>12-Lead Plastic MSOP</td>
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<td>LTC4231HMS-2#WTRPBF</td>
<td>42312</td>
<td>12-Lead Plastic MSOP</td>
<td>−40°C to 125°C</td>
</tr>
</tbody>
</table>

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**Versions of this part are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. These models are designated with a #W suffix. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

ELECTRICAL CHARACTERISTICS

The * denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. IN = 12V, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>$V_{IN}$</td>
<td>Input Supply Voltage Range</td>
<td></td>
<td>2.7</td>
<td>36</td>
<td>V</td>
<td></td>
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<tr>
<td>$V_{IN(UVL)}$</td>
<td>Input Supply Undervoltage Lockout</td>
<td>IN Rising</td>
<td>2</td>
<td>2.3</td>
<td>2.6</td>
<td>V</td>
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<tr>
<td>$\Delta V_{IN(HYST)}$</td>
<td>Input Supply Undervoltage Lockout</td>
<td>Hysteresis</td>
<td>200</td>
<td>mV</td>
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<tr>
<td>$I_{CC}$</td>
<td>Supply Current (Average)</td>
<td>Normal On, Voltage or Current Fault</td>
<td>4</td>
<td>10</td>
<td>µA</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Start-Up or Overcurrent</td>
<td>4</td>
<td>20</td>
<td>µA</td>
<td></td>
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<td></td>
<td></td>
<td>Shutdown</td>
<td>300</td>
<td>600</td>
<td>µA</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td>Reverse Input</td>
<td>0.3</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>0.3</td>
<td>2</td>
<td>µA</td>
<td></td>
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<tr>
<td></td>
<td></td>
<td></td>
<td>−2.5</td>
<td>−5</td>
<td>mA</td>
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<tr>
<td>$\Delta V_{SENSE(CB)}$</td>
<td>Circuit Breaker Threshold ($V_{IN} - V_{SENSE}$)</td>
<td></td>
<td>47</td>
<td>50</td>
<td>53</td>
<td>mV</td>
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<tr>
<td>$\Delta V_{SENSE(AL)}$</td>
<td>Analog Current Limit</td>
<td>During Output Short-Circuit</td>
<td>65</td>
<td>80</td>
<td>90</td>
<td>mV</td>
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<tr>
<td>$I_{SENSE}$</td>
<td>SENSE Input Current</td>
<td>$SHDN = $ High, $SENSE = $ 12V</td>
<td>0.3</td>
<td>1</td>
<td>µA</td>
<td></td>
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</table>

GATE, SOURCE

| $\Delta V_{GATE}$    | External N-Channel Gate Drive ($V_{GATE} - V_{SOURCE}$) | $V_{IN} < 7V, I_{GATE} = 0, −0.1µA$ | 4.5   | 6.2  | 10    | V     |
|                      |                                                          | $V_{IN} ≥ 7V, I_{GATE} = 0, −0.1µA$ | 10    | 11.4 | 18    | V     |
| $\Delta V_{GATE(H)}$ | $V_{GATE} (V_{GATE} - V_{SOURCE})$ Threshold             | $V_{IN} < 7V$                       | 5.5   | 6.5  | 10    | V     |
|                      | That Deactivates the Charge Pump                        | $V_{IN} ≥ 7V$                       | 11    | 11.7 | 18    | V     |
| $V_{GATE(L)}$        | GATE Low Threshold                                     | To Enter Shutdown or Voltage Fault  | 0.4   | 1.2  | 1.8   | V     |
| $I_{GATE(UP)}$       | GATE Pull-Up Current                                   | $GATE On, GATE = 1V$                | −7    | −10  | −13   | µA    |
| $I_{GATE(FAST)}$     | GATE Fast Pull-Down Current                            | $\Delta V_{SENSE} = 0.5V, \Delta V_{GATE} = 5V$ | 70    | 130  | mAh   |
| $I_{GATE(SLOW)}$     | GATE Slow Pull-Down Current                            | $SHDN = 0V, \Delta V_{GATE} = 5V$   | 0.6   | 1    | mA    |
| $I_{(D)}$            | Turn-On Debounce Delay                                 | $UVL = UVH = 2V, OV = 0V, SHDN = $ Step 0V to 5V | 20    | 40   | 60    | ms    |
| $I_{RETRY}$          | Auto-Retry Delay                                       | LTC4231-2                           | 0.27  | 0.5  | 0.73  | s     |
| $I_{PHL(LIM)}$       | Overcurrent to GATE Low Propagation Delay              | $\Delta V_{SENSE} = Step 0mV to 300mV, CGATE = 1nF, \Delta V_{GATE} Crosses 1V$ | 0.5   | 1    | µs    |

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### ELECTRICAL CHARACTERISTICS

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</tr>
</thead>
<tbody>
<tr>
<td>VUV</td>
<td>UVL, UVH, OV Threshold</td>
<td>● 0.776 0.795 0.814</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VOV</td>
<td>OV Threshold ( \text{OV Rising} )</td>
<td>● 0.776 0.795 0.814</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>VO/HYST</td>
<td>OV Hysteresis</td>
<td>● 3 15 30</td>
<td>mV</td>
<td></td>
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<tr>
<td>ILEAK(O.9V)</td>
<td>UVL, UVH and OV Leakage Current ( V = 0.9V ), ( \text{(C-Grade, I-Grade)} ) ( \text{(H-Grade)} )</td>
<td>● 0 ±10</td>
<td>nA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILEAK(12V)</td>
<td>UVL, UVH, OV, GNDSW, STATUS and SHDN Leakage Current ( V = 12V ), ( \text{(C-Grade, I-Grade)} ) ( \text{(H-Grade)} )</td>
<td>● 0 ±100</td>
<td>nA</td>
<td></td>
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<tr>
<td>RON(GNDSW)</td>
<td>Switch Resistance</td>
<td>● 80 200</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>VDL</td>
<td>STATUS Output Low Voltage ( I = 2mA )</td>
<td>● 0.2 0.4</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VSHDN</td>
<td>SHDN Input Threshold</td>
<td>● 0.4 0.8 1.5</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TPERIOD</td>
<td>Sampling Period</td>
<td>● 5 10 15</td>
<td>ms</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TSAMPLE</td>
<td>Sampling Width</td>
<td>● 100 200 300</td>
<td>µs</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TIMER</td>
<td>Timestamp</td>
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<td></td>
<td></td>
<td></td>
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</tr>
<tr>
<td>TCB</td>
<td>Circuit Breaker Delay ( C_T = 100nF )</td>
<td>● 1.7 2.4 3.5</td>
<td>ms</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VTIMER(H)</td>
<td>TIMER High Threshold ( \text{TIMER Rising} )</td>
<td>● 1.170 1.193 1.216</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>VTIMER(L)</td>
<td>TIMER Low Threshold ( \text{TIMER Falling} )</td>
<td>● 0.07 0.1 0.13</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>ITIMER(UP)</td>
<td>TIMER Pull-Up Current ( \text{TIMER} = 0.5V, \text{Circuit Breaker Tripped} )</td>
<td>● –35 –50 –65</td>
<td>µA</td>
<td></td>
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<tr>
<td>ITIMER(DN)</td>
<td>TIMER Pull-Down Current ( \text{TIMER} = 0.5V, \text{Circuit Breaker Recovery} )</td>
<td>● 3 5 7</td>
<td>µA</td>
<td></td>
<td></td>
<td></td>
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</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

**Note 3:** These pins can be tied to voltages below \(-0.3V\) through a resistance that limits the current below 1mA.

**Note 4:** An internal clamp limits GATE to a minimum of 13V above SOURCE. Driving this pin to voltages beyond this clamp may damage the device.

**Note 5:** For modes where GATE is pulled to GND, \( I_{CC} = I_{IN} + I_{\text{SENSE}} \). Else \( I_{CC} = I_{IN} + I_{\text{SENSE}} + I_{\text{SOURCE}} \).
TYPICAL PERFORMANCE CHARACTERISTICS

Average Supply Current vs IN

Supply Current (Reverse Input) vs IN

∆VGATE (Average) vs IN

Average Supply Current (Normal On) vs GATE Leakage

Average Supply Current vs Temperature

∆VGATE (Average) vs GATE Leakage
TYPICAL PERFORMANCE CHARACTERISTICS

GATE Pull-Up Current vs $V_{\text{GATE}}$

$V_{\text{IN}} = 12V$

$$I_{\text{GATE(UP)}} \ (\mu A)$$

-20
-15
-10
-5
0
5
10
15
20
25

$V_{\text{GATE}} \ (V)$

Overcurrent to GATE Low Propagation Delay

$$V_{\text{IN}} - V_{\text{SENSE}} \ (mV)$$

0.1
1
10
100
1000

$V_{\text{IN}} - V_{\text{SENSE}} \ (mV)$

UVL, UVH, OV Thresholds vs Temperature

$V_{\text{IN}} = 12V$

$$V_{\text{SENSE}} \ (mV)$$

0.770
0.775
0.780
0.785
0.790
0.795
0.800

$V_{\text{SENSE}} \ (mV)$

TEMPERATURE ($^\circ C$)

0
25
50
75
100
125
150

STATUS Output Low Voltage vs Current

$V_{\text{IN}} = 12V$

$$V_{\text{STATUS}} \ (mV)$$

0
100
200
300
400
500
600

$I_{\text{STATUS}} \ (mA)$

0
1
2
3
4
5

STATUS Output Low Voltage vs Temperature

$V_{\text{IN}} = 12V$

$$V_{\text{STATUS}} \ (mV)$$

0
100
200
300
400

$V_{\text{STATUS}} \ (mV)$

TEMPERATURE ($^\circ C$)

0
25
50
75
100
125
150

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**PIN FUNCTIONS**

**GATE:** Gate Drive for External N-Channel MOSFET. After all start-up conditions are satisfied, a 10μA pull-up current from the internal charge pump charges up $\Delta V_{GATE}$ to the high threshold voltage $\Delta V_{GATE(H)}$ and then turns off. The charge pump turns on again when $\Delta V_{GATE}$ decays by more than 0.7V or every 15ms, whichever comes first, and recharges $\Delta V_{GATE}$ to $\Delta V_{GATE(H)}$. During GATE turn-off, a 1mA pull-down current discharges GATE to GND. During severe short circuits, a 130mA pull-down current is activated to discharge GATE to SOURCE.

**GND:** Device Ground.

**GNDSW:**Switched GND. Connect this pin to an external resistive network to monitor IN for overvoltage or undervoltage (OV/UV). To reduce the power dissipated by this resistive divider, the LTC4231 periodically samples IN by connecting GNDSW to GND once every 10ms. Tie this pin to GND if unused.

**IN:** Supply Voltage and Current Sense Input. This pin has a nominal undervoltage lockout threshold of 2.3V.

**SHDN:** Shutdown Control Input. A logic high at SHDN enables the LTC4231. GATE ramps up after a debounce delay of 40ms. A logic low at SHDN activates a 1mA pull-down current at GATE, discharging it to GND. Once GATE < 1.2V, the LTC4231 enters a low current Shutdown. Connect to IN if unused. When connected to IN, if IN goes below ground, use a resistor to limit the current to ≤1mA.

**OV:** Overvoltage Comparator Input. Connect this pin to an external resistive network to monitor IN for OV. This pin connects internally to an overvoltage comparator with a 0.795V threshold. To reduce the power dissipated by this resistive divider, the LTC4231 periodically samples IN by connecting GNDSW to GND once every 10ms. Once an OV is detected at IN, GATE and STATUS pull low. Tie this pin to GND if unused.

**SENSE:** Current Sense Input. Connect to the output of the current sense resistor. The circuit breaker comparator and the analog current limit amplifier monitor the voltage across the current sense resistor. During an overcurrent fault when $\Delta V_{SENSE}$ exceeds 50mV, the circuit breaker comparator trips and triggers TIMER to ramp up. For more severe overcurrent faults, the analog current limit amplifier controls the gate of the external MOSFET to keep $\Delta V_{SENSE}$ at 80mV. To disable the circuit breaker comparator and analog current limit amplifier, connect this pin to IN.

**SOURCE:** N-Channel MOSFET Source Connection. Connect this pin to the source of the external MOSFET.

**STATUS:** Status Output. Open-drain output that goes high impedance when $\Delta V_{GATE}$ first exceeds $\Delta V_{GATE(H)}$. The state of the pin is latched and resets (pulls low) when SHDN goes low, an UVLO occurs, an OV/UV is detected at IN or an overcurrent fault sets the internal current fault latch. This pin may be left open if unused.

**TIMER:** Timer Input. Connect a capacitor between this pin and GND to set a 24ms/μF duration for overcurrent before the internal current fault latch trips and turns off the MOSFET. For the LTC4231-1 latchoff option, the MOSFET remains off until the current fault latch is cleared by pulling SHDN low or by cycling power. For the LTC4231-2 auto-retry option, the current fault latch is cleared automatically and the GATE is ramped up after a 500ms delay.

**UVH, UVL:** Undervoltage Comparator Input. Connect these pins to an external resistive network to monitor IN for UV. These pins connect internally to an undervoltage comparator with a 0.795V threshold. The comparator monitors UVH when GATE is low and UVL when GATE is high to implement separate undervoltage turn-on and undervoltage turn-off thresholds. To reduce the power dissipated by this resistive divider, the LTC4231 periodically samples IN by connecting GNDSW to GND once every 10ms. Once an UV is detected at these pins, GATE and STATUS pull low. Tie both pins to IN if unused. When connected to IN, for applications where IN goes below ground, use a resistor to limit the current to ≤1mA.

**Exposed Pad (QFN Package):** The exposed pad may be left open or connected to device ground.
OPERATION

The LTC4231 is a micropower Hot Swap controller that controls an external N-channel MOSFET to turn on and off a supply voltage in a controlled manner. This allows a circuit to be safely inserted and removed from a powered connector without glitches or connector damage from uncontrolled inrush current.

When the LTC4231 is first powered up, the gate of the MOSFET is held at GND to keep it off. Pulling SHDN high and IN above undervoltage lockout (UVLO) starts an internal clock that monitors the resistive divider at IN once every 10ms by connecting GNDSW to GND. A 40ms debounce cycle is also started. Average $I_{CC}$ during this debounce mode is 4µA.

After the 40ms debounce cycle, the LTC4231 goes into start-up mode to ramp up GATE. In this mode, all circuits blocks except the overvoltage or undervoltage (OV/UV) block are activated and $I_{CC} = 300$µA. The internal charge pump supplies a 10µA pull-up current to GATE. Once $\Delta V_{GATE}$ exceeds $\Delta V_{GATE(H)}$, STATUS goes high impedance. This indicates that GATE is high and the power path is on. Average $I_{CC}$ drops to 4µA during this normal on mode as some circuit blocks are shut down and the internal charge pump periodically turns on to recharge GATE as needed. The periodic monitoring of the IN resistive divider continues as long as SHDN is high and IN $\geq 2.3V$.

If an OV/UV violation is detected during the IN monitoring time, the part goes into voltage fault mode where $I_{CC}$ drops to 4µA where GATE and STATUS is pulled to GND. The debounce cycle restarts when no OV/UV violation is detected during a subsequent IN monitoring window.

The LTC4231 has a circuit breaker comparator that monitors the voltage across the current sense resistor. This comparator trips when $\Delta V_{SENSE}$ exceeds 50mV, bringing the LTC4231 into overcurrent mode. In this mode, all circuits blocks except the OV/UV block are activated and $I_{CC} = 300$µA. If $\Delta V_{SENSE} > 80$µV, the analog current limit amplifier limits $\Delta V_{SENSE}$ to 80mV by servoing $\Delta V_{GATE}$ in an active control loop. The TIMER capacitor is ramped up with a 50µA pull-up when $\Delta V_{SENSE} > 50$µV. When TIMER $> 1.193V$, the current fault latch is set, causing GATE and STATUS to pull low. The part goes into current fault mode.

In current fault mode, the latchoff (LTC4231-1) version keeps TIMER and GATE low. The auto-retry (LTC4231-2) version waits 500ms before GATE is ramped up again. For both versions, the part can be reset by cycling SHDN low then high or by cycling IN to GND and back. After the reset, the LTC4231 goes through a debounce cycle before re-starting GATE.

SHDN acts as a shutdown switch for the supply path. When it goes high, the LTC4231 ramps GATE up after a debounce cycle to turn on the external MOSFET. When it goes low, GATE is pulled to GND to turn off the external MOSFET. The LTC4231 then goes into shutdown mode where $I_{CC}$ drops to 0.3µA.

IN, SENSE, GATE and SOURCE are protected against reverse inputs of up to −40V. Two reverse voltage comparators detect negative input potentials at SENSE or GATE and quickly connect GATE to SENSE. When used with back-to-back MOSFETs as shown in Figure 5, this feature will isolate the load from a negative input.
The micropower capability of the LTC4231 makes it ideal for Hot Swap applications in battery powered systems where current load is light or intermittent and power draw is a concern. It can implement battery short circuit protection, reverse battery protection, battery voltage monitoring, power path control, hot-plug and inrush current control in off-grid, autonomous systems.

**Turn-On Sequence**

When $\text{IN}$ is less than the UVLO level of 2.3V or $\text{SHDN}$ is low, $\text{GATE}$ is pulled to GND and $\text{STATUS}$ pulls low. When $\text{IN} \geq 2.3\text{V}$ and $\text{SHDN}$ goes high, an internal clock starts timing a 40ms debounce cycle. The clock also times a $200\mu\text{s}$ strobe of the resistive divider at $\text{IN}$ every $10\text{ms}$ to make sure $\text{IN}$ is not in OV/UV. Average $I_{\text{CC}}$ during this debounce mode is $4\mu\text{A}$.

Any OV/UV detected will stop and reset the debounce timing cycle. During this voltage fault mode, average $I_{\text{CC}}$ is $4\mu\text{A}$. The debounce cycle only restarts when a subsequent $\text{IN}$ strobe indicates that the input power is within the acceptable range, $\text{IN} \geq 2.3\text{V}$ and $\text{SHDN}$ is high.

When the debounce cycle of 40ms successfully completes, the LTC4231 turns on its charge pump, analog current limit amplifier and TIMER control circuit blocks as it goes into start-up mode ($I_{\text{CC}} = 300\mu\text{A}$). The external MOSFET is turned on by charging up the GATE with a $10\mu\text{A}$ charge pump generated current source.

At start-up, the MOSFET current is typically dominated by the current charging the load capacitor $C_L$. If $\Delta V_{\text{SENSE}} > 80\text{mV}$, the analog current limit amplifier controls the gate of the MOSFET in a closed loop. This keeps the start-up inrush current at $80\text{mV}/R_{\text{SENSE}}$. When $\Delta V_{\text{SENSE}} > 50\text{mV}$, the TIMER capacitor charges up with an internal $50\mu\text{A}$ pull-up current.

**Figure 1. Channel Controller with Connector Enable**

**Figure 2. Inrush Control by Analog Current Limit**
APPLICATIONS INFORMATION

In most applications, keeping the inrush current at analog current limit is an acceptable start-up method if the TIMER delay is long enough to avoid setting the current fault latch and the MOSFET has adequate safe operating margin. However, for more flexibility in design (See the Design Example section), a capacitor from GATE to GND (Figure 1) can be used to limit the \( V_{\text{GATE}} \) slew rate for inrush current control. \( V_{\text{GATE}} \) rises with a slope equal to \( 10\mu\text{A}/C_G \) (Figure 3). The supply inrush current is then limited to:

\[
I_{\text{INRUSH}} = \frac{C_L}{C_G} \cdot 10\mu\text{A}
\]

Once \( \Delta V_{\text{GATE}} \) exceeds \( \Delta V_{\text{GATE(H)}} \), STATUS goes high impedance. \( I_{\text{CC}} \) drops from \( 300\mu\text{A} \) to \( 4\mu\text{A} \) (average) during this normal on mode as some circuit blocks are shut down and the internal charge pump periodically turns on when \( \Delta V_{\text{GATE}} \) droops by \( 0.7\text{V} \) or every \( 15\text{ms} \), whichever comes first (Figure 7).

In the back-to-back MOSFET configuration as shown in Figure 5, SOURCE will also be pulled to GND via the parasitic body diode between GATE and SOURCE, cutting off the load from IN. This configuration is suitable in power path control and reverse battery protection applications where IN is likely to go below GND.

In the single MOSFET configuration (Figure 1), the 1mA pull-down from GATE to GND also discharges the load capacitor \( C_L \) to GND once GATE goes below SOURCE.

Overcurrent Fault

The 50mV circuit breaker threshold sets the maximum load current allowed under steady state conditions. However, the LTC4231 allows mild overcurrents during supply or load transients when \( \Delta V_{\text{SENSE}} \) momentarily exceeds 50mV but stays below the 80mV analog current limit threshold. For severe overcurrents when \( \Delta V_{\text{SENSE}} \) exceeds 80mV, the analog current limit amplifier controls \( \Delta V_{\text{GATE}} \) to regulate \( \Delta V_{\text{SENSE}} \) to 80mV. The durations of these transient overcurrents must be less than the circuit breaker delay \( (t_{\text{CB}}) \) which can be adjusted using the capacitor \( C_T \) at the TIMER pin.

When \( \Delta V_{\text{SENSE}} \) exceeds 50mV, the LTC4231 goes into overcurrent mode. \( C_T \) is charged with a 50\mu\text{A} pull-up. If the overcurrent is transient and \( \Delta V_{\text{SENSE}} \) goes below 50mV before TIMER reaches 1.193V, the 50\mu\text{A} pull-up on TIMER switches to a 5\mu\text{A} pull-down. Multiple overcurrents with a duty cycle > 10% can thus eventually integrate TIMER to 1.193V. When TIMER reaches 1.193V, the LTC4231 goes into current fault mode and sets an internal current fault latch. The external MOSFET will be cut off by a 1mA pull-down from GATE to GND while STATUS pull-down is asserted.

The time in which LTC4231 stays in overcurrent mode before going into current fault mode is called the circuit breaker delay and is given by:

\[
t_{\text{CB}} = C_T \cdot 24 \text{[ms/\muF]}
\]

Turn-Off Sequence

The MOSFET switch can be turned off by SHDN going low, an OV/UV event, an overcurrent setting the current fault latch or IN dropping below its UVLO voltage. Under any of these conditions, STATUS pulls low and the MOSFET is turned off with a 1mA current pulling down from GATE to GND.
Figure 4. LTC4231-1 Overcurrent
APPLICATIONS INFORMATION

Auto-Retry vs Latchoff

During current fault mode, GATE is held low and TIMER is discharged to GND. Once TIMER < 0.1V, average I_{CC} goes to 4\mu A and the internal current fault latch is ready to be reset. The LTC4231-2 (automatic retry) waits for a 500ms retry delay after which the internal current fault latch is reset and GATE ramps up to turn the MOSFET back on.

The LTC4231-1 (latchoff) version does not restart automatically. Pulling SHDN low for >100\mu s will reset the internal current fault latch. When SHDN goes high, GATE ramps up after a debounce cycle. Alternatively, IN can be pulled to GND for >100\mu s then cycled back up again. This UVLO event will reset the internal current fault latch and GATE ramps up after a debounce cycle. A UV/OV detected at IN also resets the internal current fault latch and GATE ramps up after a debounce delay.

Analog Current Limit Loop Stability

The analog current limit loop on GATE is compensated by the parasitic gate capacitance of the external MOSFET. No further compensation components are normally required. If a small MOSFET with C_{ISS} ≤ 1nF is chosen, an R_G and C_G compensation network connected at GATE may be required (Figure 1) to ensure stability. The resistor, R_G, connected in series with C_G accelerates the MOSFET gate recovery after a fast gate pull-down. The value of C_G should be ≤100nF. An additional 10\Omega resistor (R5 in Figure 1) should be added close to the MOSFET gate to prevent possible parasitic oscillation due to trace/wire inductance and capacitance.

Monitor OV and UV Faults

When IN is above UVLO and SHDN is high, an internal clock times a 200\mu s strobe of the resistive divider at IN every 10ms. During this 200\mu s strobe, the normally high impedance GNDSW is connected to GND with an internal 80\Omega switch and the comparators connected to UVH, UVL and OV are awakened from sleep mode. The comparators sense the voltages on the resistive divider, and their outputs are latched at the end of the strobe window.

If an OV or UV violation is detected, the STATUS pulls low and a 1mA pull-down will be activated between GATE and GND to turn off the external MOSFET. When GATE goes <1.2V, average I_{CC} drops to 4\mu A as the LTC4231 goes into voltage fault mode. It stays in this mode until a subsequent IN strobe sees no OV/UV. The LTC4231 then re-starts after a debounce cycle.

Strobing the resistive divider reduces power consumption as the external resistors as well as the internal OV/UV comparators do not dissipate power in between strobes. For a 1M string of resistors used to monitor a V_{IN} of 24V, this strobing scheme reduces the current consumption from 24\mu A to 0.48\mu A as the strobing duty cycle is 2\% (200\mu s/10ms). The OV/UV comparators dissipate 35\mu A during IN strobing. The 2\% duty cycle reduces this to an average current of 0.7\mu A. Note that the response time to an OV/UV event can be as long as 10ms.

The four resistors allow three thresholds to be configured. They are the UV rising threshold (V_{UVON}), the UV falling threshold (V_{UVOFF}) and the OV rising threshold (V_{OVOFF}). The OV falling threshold is set by internal hysteresis to be 1.8\% below the OV rising threshold. Using the comparator threshold as 0.795V and choosing appropriate values for R_{TOTAL} and R4, the resistor values can be calculated as follows:

\[ R_{TOTAL} = R1 + R2 + R3 + R4 \]

\[ R4 = \left( \frac{0.795V}{V_{OVOFF}} \right) \cdot R_{TOTAL} \]

\[ R3 = \left( \frac{V_{OVOFF}}{V_{UVON}} \right) \cdot R4 \]

\[ R2 = \left( \frac{V_{UVON}}{V_{UVOFF}} \right) \cdot \left( \frac{V_{OVOFF}}{V_{UVON}} \right) \cdot R4 \]

\[ R1 = \left( \frac{V_{OVOFF}}{0.795V} \right) \cdot R4 - R3 - R2 \]

It is recommended that the total value of the resistor string be less than 2M and traces at UVH, UVL, and OV kept short to minimize parasitic capacitance and improve settling time.
Reverse Input Protection

Negative voltages at IN can occur if a battery is plugged in backwards or a negative supply is inadvertently connected. Back-to-back N-channel MOSFETs can be used as in Figure 5 to prevent the negative voltage from passing to the output load.

IN, SENSE, GATE and SOURCE are protected against reverse inputs of up to $-40\text{V}$. When the LTC4231’s reverse voltage comparators detect a negative voltage at SENSE, an internal switch is activated to connect GATE to SENSE. The body diode of M1 pulls SOURCE to a diode above SENSE. Since M2 is off and its body diode is in the reverse blocking mode, the negative voltage is blocked by the $V_{DS}$ of M2.

Figure 6 shows the waveforms when the application circuit in Figure 5 is hot plugged to $-24\text{V}$. Due to the parasitic inductance at IN, SENSE and GATE, the voltages ring significantly below $-24\text{V}$. The TransZorb helps to clamp the negative undershoot and a 40V MOSFET is selected for M2 to survive this undershoot.
APPLICATIONS INFORMATION

Achieving Low Quiescent Current

Table 1 summarizes the average $I_{CC}$ of the various operating modes of the LTC4231.

<table>
<thead>
<tr>
<th>MODE</th>
<th>$I_{CC}$ (NORM)</th>
<th>$I_{CC}$ (MAX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Start-Up or Overcurrent</td>
<td>300µA</td>
<td>600µA</td>
</tr>
<tr>
<td>Debounce, Normal On, Voltage or</td>
<td>4µA</td>
<td>10µA</td>
</tr>
<tr>
<td>Current Fault</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown</td>
<td>0.3µA</td>
<td>1µA</td>
</tr>
<tr>
<td>Reverse Input</td>
<td>−2.5mA</td>
<td>−5mA</td>
</tr>
</tbody>
</table>

To lower $I_{CC}$ when GATE is high, the LTC4231 operates in normal on mode, where the charge pump delivers pulses of current to the GATE capacitance (either an external $C_G$ or the parasitic capacitance of the external MOSFETs) to boost $\Delta V_{GATE}$ to $\Delta V_{GATE(H)}$ followed by sleep periods when the GATE capacitance holds up GATE. Leakage will cause $\Delta V_{GATE}$ to droop during these sleep periods. When the $\Delta V_{GATE}$ low comparator detects $\Delta V_{GATE}$ drooping by more than 0.7V, it will activate the charge pump to boost $\Delta V_{GATE}$ back to $\Delta V_{GATE(H)}$ before returning to sleep mode. In addition to the $\Delta V_{GATE}$ low comparator, there is a charge pump refresh timer that turns on the charge pump every 15ms to boost $\Delta V_{GATE}$ back to $\Delta V_{GATE(H)}$. This timer is reset when the charge pump turns on.

When in charge pump sleep mode the LTC4231 consumes 2µA. When the charge pump is on to deliver a current pulse to GATE, $I_{CC}$ briefly goes up to 200µA. The amount of leakage at GATE ($I_{GATE(LEAKAGE)}$) will determine the duty cycle of the charge pump. Figure 7 shows start-up and $\Delta V_{GATE}$ regulation (with different $I_{GATE(LEAKAGE)}$) waveforms from the Figure 5 application circuit.

As the average current delivered to GATE during the current pulse is around 15µA, the duty cycle of the charge pump for a $I_{GATE(LEAKAGE)}$ of 0.1µA is 0.1/15 = 0.67%. The average current due to $\Delta V_{GATE}$ regulation is then 0.67% • 200µA = 1.3µA. When added to the average current due to OV/UV strobing (0.7µA) and charge pump sleep mode current (2µA), the average quiescent current of the LTC4231 during the normal on mode is 1.3µA + 0.7µA + 2µA = 4µA. The normal on mode average supply current can be estimated using the formula:

$$I_{CC} = 2.7\mu A + 13.3 \times I_{GATE(LEAKAGE)}$$

The Typical Performance Characteristics section shows a graph of average $I_{CC}$ (normal on) against $I_{GATE(LEAKAGE)}$.

Shutdown Mode

When $SHDN$ goes low, STATUS pulls low and a 1mA pull-down will be activated between GATE and GND to cut off the external MOSFET. When GATE reaches $<1.2V$, $I_{CC}$ drops to 0.3µA as the LTC4231 goes into shutdown mode. When $SHDN$ goes high, GATE ramps up after the 40ms debounce cycle. Figure 8 shows the application in Figure 5 going into shutdown mode.

---

**Figure 7.** Regulating $\Delta V_{GATE}$ During Normal On Mode

**Figure 8.** $SHDN$ Going Low Activates Shutdown Mode
APPLICATIONS INFORMATION

Supply Transient Protection

When the capacitances at the input and output are very small, rapid changes in current during an output short-circuit event can cause transients that exceed the 40V absolute maximum ratings of IN, SENSE and SOURCE. To minimize such spikes, use wider traces or heavier trace plating to reduce the power trace inductance. Also, bypass locally with a 10μF electrolytic and 0.1μF ceramic if hot plug inrush current is not a concern. Alternatively, clamp the input with a transient voltage suppressor (Z1 in Figure 5). A 10Ω, 0.1μF snubber damps the response and reduces ringing (R_X and C_X in Figure 5).

Design Example

As a design example, take the following specifications for the Figure 5 application circuit. The application is rated for a V_IN of 24V at 2A, C_L = 100µF. UV rising = 23V, UV falling = 22V, OV rising = 26V.

Sense resistor:

\[ R_{\text{SENSE}} = \frac{\Delta V_{\text{SENSE}}(\text{CB})(\text{MIN})}{2A} = \frac{47mV}{2A} = 23.5m\Omega \]

Use R_{\text{SENSE}} = 22.5mΩ for margin. Worst case analog current limit:

\[ I_{\text{LIMIT}}(\text{MIN}) = \frac{\Delta V_{\text{SENSE}}(\text{ACL})(\text{MIN})}{22.5m\Omega} = \frac{65mV}{22.5m\Omega} = 2.89A \]
\[ I_{\text{LIMIT}}(\text{MAX}) = \frac{\Delta V_{\text{SENSE}}(\text{ACL})(\text{MAX})}{22.5m\Omega} = \frac{90mV}{22.5m\Omega} = 4A \]

Calculate the worst case time it takes to charge up C_L in analog current limit:

\[ t_{\text{CHARGE}}(\text{MAX}) = \frac{C_L \cdot V_{\text{IN}}}{I_{\text{LIMIT}}(\text{MIN})} = \frac{100\mu F \cdot 24V}{2.89A} = 0.9ms \]

For inrush control using analog current limit, t_{\text{CHARGE}}(\text{MAX}) must be less than the circuit breaker delay (t_CB) for a proper start-up.

The worst case power dissipation in MOSFET M1 occurs during a severe overcurrent fault when the current is controlled by analog current limit for the duration of t_CB:

\[ P_{\text{DISS}} = V_{\text{IN}} \cdot I_{\text{LIMIT}}(\text{MAX}) = 24V \cdot 4A = 96W \]

The SOA (safe operating area) curve for the Si7164DP MOSFET shows that it can withstand 180W for 10ms. So choose a t_CB that is less than 10ms but higher than 0.9ms (t_{CHARGE}(\text{MAX})). In this case, use t_CB = 2ms.

\[ C_T = \frac{t_{\text{CB}}}{24} = \frac{2ms}{24} = 0.082\mu F = 82nF \]

If a low inrush current (< \Delta V_{\text{SENSE}}(\text{CB})) is preferred, refer to the Figure 1 application circuit which uses a gate capacitor C_G to limit the inrush current. Choose I_{\text{INRUSH}} = 0.5A which is set using C_G:

\[ C_G = \frac{C_L \cdot 10\mu A}{I_{\text{INRUSH}}} = \frac{1000\mu F \cdot 10\mu A}{0.5A} = 20nF \]

The time to charge up C_L with 0.5A is:

\[ t_{\text{CHARGE}} = \frac{C_L \cdot V_{\text{IN}}}{I_{\text{INRUSH}}} = \frac{1000\mu F \cdot 24V}{0.5A} = 48ms \]

In this case t_{\text{CHARGE}} can be longer than t_CB with no start-up issue.

The average power dissipation in the MOSFET M1 during this start-up is:

\[ P_{\text{DISS}} = \frac{V_{\text{IN}} \cdot I_{\text{INRUSH}}}{2} = \frac{24V \cdot 0.5A}{2} = 6W \]

The SOA of the MOSFET M1 must be evaluated to ensure that it can withstand 6W for 48ms. The SOA curve of the Si7120ADN withstands 10W for 360ms, satisfying the requirement.

The purpose of MOSFET M2 is to block the reverse path from OUT (drain of M2) to IN when GATE pulls to GND so that IN can go lower than OUT or even negative. Choose a 40V MOSFET to withstand a worse case reverse DC voltage of −24V. The Si5410DU offers a good choice with a maximum R_{DS(ON)} of 18mΩ at V_GS = 10V.
**APPLICATIONS INFORMATION**

The IN monitoring resistors R1–R4 should be chosen to yield a total divider resistance of between 1M to 2M for both low power and good transient response. Using the formulas from the Monitor OV and UV Faults section, R1–R4 are calculated as follows (with all resistor values rounded up to the nearest 1% accurate standard values):

Choose \( R1 + R2 + R3 + R4 = 1000k\Omega \)

\[
R4 = \left( \frac{0.795V}{V_{OVOFF}} \right) \times 1000k\Omega
\]

Choose \( R4 = 32.4k\Omega \) to give total divider resistance: \( R1 + R2 + R3 + R4 = 1060k\Omega \).

\[
R3 = \left( \frac{V_{UVON}}{V_{UVOFF}} - 1 \right) \times R4 = \left( \frac{26V}{23V} - 1 \right) \times 32.4k\Omega = 4.22k\Omega
\]

\[
R2 = \left( \frac{V_{UVON}}{V_{UVOFF}} - 1 \right) \times \left( \frac{V_{OVFF}}{V_{UVON}} \right) \times R4
\]

\[
= \left( \frac{23V}{22V} - 1 \right) \times \left( \frac{26V}{23V} \right) \times 32.4k\Omega = 1.65k\Omega
\]

\[
R1 = \left( \frac{V_{OVFF}}{0.795V} - 1 \right) \times R4 - R3 - R2
\]

**Layout Considerations**

To achieve accurate current sensing, a Kelvin connection for the sense resistor is recommended. The PCB layout for the resistor should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistors and the power MOSFETs should include good thermal management techniques for optimal device power dissipation. In Hot Swap applications where load currents can be high, narrow PCB tracks exhibit more resistance than wider tracks and operate at elevated temperatures. 1oz copper exhibits a sheet resistance of about 0.5mΩ/square. The minimum trace width for 1oz copper foil is 0.5mm per amp to make sure the trace stays at a reasonable temperature. Using 0.8mm per amp or wider is recommended. Thicker top and bottom copper such as 3oz or more can improve electrical conduction and reduce PCB trace dissipation.

If a resistor R5 (see Figure 1) is used, place it as close as possible to M1’s gate input. This will limit the parasitic trace capacitance that leads to M1 self-oscillation. The transient voltage suppressor, Z1, when used, should be mounted close to the LTC4231 using short lead lengths. A recommended PCB layout for the sense resistor and back-to-back power MOSFETs is shown in Figure 9.

---

**Figure 9. Recommended Layout**
APPLICATIONS INFORMATION

Additional Applications

Figure 10 shows a reverse-battery protected application featuring the LTC2955 micropower push-button controller. A press on the push button switch will turn on the LTC4231 while a subsequent press will turn off the LTC4231. In the event the LTC4231 is unable to power-up successfully when EN goes high, the STATUS output is fed back to the KILL input in order to place the LTC4231 back in the very low-power Shutdown mode.

Figure 11 illustrates a 36V application with an UV rising threshold of 35V, an UV falling threshold of 33V and an OV rising threshold of 38V. As the IN operating voltage is so near to its 40V absolute maximum rating, a suitable TransZorb is not available to protect IN. Instead, a floating GND architecture is used to help the LTC4231 survive possible voltage transients during short circuit events. This architecture is strictly for handling IN transients during 36V operation. It does not allow DC \( V_{\text{IN}} \) operation > 39V.

![Figure 10. Micropower Push Button and Hot Swap Controllers with Reverse Battery Protection](image-url)
PACKAGE DESCRIPTION

MS Package
12-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1668 Rev A)

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

For more information www.analog.com
PACKAGE DESCRIPTION

UD Package
12-Lead Plastic QFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1855 Rev 0)

NOTE:
1. DRAWING CONFORMS TO JEDEC PACKAGE OUTLINE MO-220 VARIATION (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

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# Revision History

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<th>REV</th>
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<td>A</td>
<td>09/15</td>
<td>Added H-grade information</td>
<td>2, 3, 4</td>
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<td>Updated specifications: V_{\text{GATE(L)}}, I_{\text{GATE(UP)}}, I_{\text{D(ON)}}, I_{\text{RETRY}}, I_{\text{PERIOD}}, I_{\text{SAMPLE}}, I_{\text{CB}}</td>
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<td>B</td>
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<td>Added AEC-Q100</td>
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**RELATED PARTS**

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<th>DESCRIPTION</th>
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<td>Overvoltage/Overcurrent Protection Controller</td>
<td>220µA I_D, 2.5V to 5.5V Operation, 80V Protection</td>
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<tr>
<td>LTC4365</td>
<td>OV, UV and Reverse Supply Protection Controller</td>
<td>25µA I_D, 2.5V to 34V Operation, –40V Reverse Input</td>
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<tr>
<td>LTC4359</td>
<td>Ideal Diode Controller with Reverse Input Protection</td>
<td>150µA I_D, 9µA in Shutdown, 4V to 80V Operation</td>
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<tr>
<td>LTC4364</td>
<td>Surge Stopper/Hot Swap with Ideal Diode</td>
<td>370µA I_DC, 4V to 80V Operation, –40V Reverse Input, –20V Reverse Output</td>
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<tr>
<td>LTC2960</td>
<td>Nano-Current Dual Voltage Monitor</td>
<td>850nA I_Q, 2.5V to 36V Operation, 1.5% Accuracy</td>
</tr>
<tr>
<td>LTC4229</td>
<td>Ideal Diode and Hot Swap Controller</td>
<td>2.9V to 18V Operation, 2mA I_IN, 0.5µs Ideal Diode Turn-On/Off</td>
</tr>
<tr>
<td>LTC4232</td>
<td>5A Integrated Hot Swap Controller</td>
<td>Integrated 33mΩ MOSFET with Sense Resistor, 2.9V to 15V Operation</td>
</tr>
<tr>
<td>LTC2955</td>
<td>Pushbutton On/Off Controller</td>
<td>Automatic Turn-On, 1.2µA I_D, 1.5V to 36V Operation</td>
</tr>
<tr>
<td>LTC4417</td>
<td>Prioritized PowerPath™ Controller</td>
<td>28µA I_D, 2.5V to 36V Operation, –42V Reverse Input</td>
</tr>
</tbody>
</table>

**Figure 11. 36V Hot Swap Application with Reverse Protection**

**TYPICAL APPLICATION**

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**PART NUMBER**

- LTC4231
- LTC2955
- LTC4232
- LTC4359
- LTC4364
- LTC4361
- LTC4365
- LTC4229
- LTC2960
- LTC4417

**DESCRIPTION**

- Overvoltage/Overcurrent Protection Controller
- OV, UV and Reverse Supply Protection Controller
- Ideal Diode Controller with Reverse Input Protection
- Surge Stopper/Hot Swap with Ideal Diode
- Nano-Current Dual Voltage Monitor
- Ideal Diode and Hot Swap Controller
- 5A Integrated Hot Swap Controller
- Pushbutton On/Off Controller
- Prioritized PowerPath™ Controller

**COMMENTS**

- 220µA I_D, 2.5V to 5.5V Operation, 80V Protection
- 25µA I_D, 2.5V to 34V Operation, –40V Reverse Input
- 150µA I_D, 9µA in Shutdown, 4V to 80V Operation
- 370µA I_DC, 4V to 80V Operation, –40V Reverse Input, –20V Reverse Output
- 850nA I_Q, 2.5V to 36V Operation, 1.5% Accuracy
- 2.9V to 18V Operation, 2mA I_IN, 0.5µs Ideal Diode Turn-On/Off
- Integrated 33mΩ MOSFET with Sense Resistor, 2.9V to 15V Operation
- Automatic Turn-On, 1.2µA I_D, 1.5V to 36V Operation
- 28µA I_D, 2.5V to 36V Operation, –42V Reverse Input