**FEATURES**

- Fully Enhances N-Channel Power MOSFETs
- 8μA Standby Current
- 85μA ON Current
- Short-Circuit Protection
- Wide Power Supply Range: 4.5V to 18V
- Controlled Switching ON and OFF Times
- No External Charge Pump Components
- Replaces P-Channel High Side MOSFETs
- Compatible with Standard Logic Families
- Available in 8-Pin SO Package

**DESCRIPTION**

The LTC®1155 dual high side gate driver allows using low cost N-channel FETs for high side switching applications. An internal charge pump boosts the gate above the positive rail, fully enhancing an N-channel MOSFET with no external components. Micropower operation, with 8μA standby current and 85μA operating current, allows use in virtually all systems with maximum efficiency.

Included on-chip is overcurrent sensing to provide automatic shutdown in case of short circuits. A time delay can be added in series with the current sense to prevent false triggering on high in-rush loads such as capacitors and incandescent lamps.

The LTC1155 operates off of a 4.5V to 18V supply input and safely drives the gates of virtually all FETs. The LTC1155 is well suited for low voltage (battery-powered) applications, particularly where micropower “sleep” operation is required.

The LTC1155 is available in both 8-pin PDIP and 8-pin SO packages.

All registered trademarks and trademarks are the property of their respective owners.

**APPLICATIONS**

- Laptop Power Bus Switching
- SCSI Termination Power Switching
- Cellular Phone Power Management
- P-Channel Switch Replacement
- Relay and Solenoid Drivers
- Low Frequency Half H-Bridge
- Motor Speed and Torque Control

**TYPICAL APPLICATION**

Laptop Computer Power Bus Switch with Short-Circuit Protection
**LTC1155**

**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

Supply Voltage .......................................................... 22V
Input Voltage .......................................................... (VS +0.3V) to (GND – 0.3V)
Gate Voltage .......................................................... (VS +24V) to (GND – 0.3V)
Current (Any Pin) ................................................... 50mA
Storage Temperature Range ............... −65°C to 150°C

Operating Temperature Range

LTC1155C .......................................................... 0°C to 70°C
LTC1155I .......................................................... −40°C to 85°C
LTC1155M **(OBSOLETE)** ........................................ −55°C to 125°C

Lead Temperature Range (Soldering, 10 sec.) ...... 300°C

**PIN CONFIGURATION**

![J8 PACKAGE](diagram)

8-LEAD CERDIP

J8 PACKAGE

TJ(MAX) = 150°C, θ(JA) = 100°C/W (J8)

**OBSOLETE PACKAGE**

![N8 PACKAGE](diagram)

8-LEAD PDIP

N8 PACKAGE

TJ(MAX) = 100°C, θ(JA) = 130°C/W (N8)

![S8 PACKAGE](diagram)

8-LEAD PLASTIC SO

S8 PACKAGE

TJ(MAX) = 100°C, θ(JA) = 150°C/W

**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
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<td>8-Lead PDIP</td>
<td>−40°C to 85°C</td>
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**OBSOLETE PACKAGE**

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<td>1155</td>
<td>0°C to 70°C</td>
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<tr>
<td>LTC1155IS8#PBF</td>
<td>LTC1155IS8#TRPBF</td>
<td>1155I</td>
<td>−40°C to 85°C</td>
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</table>

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

**Tape and reel specifications.** Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.
**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$. $V_S = 4.5\text{V}$ to 18V, unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>LTC1155M (OBSCLETE)</th>
<th>LTC1155C/LTC1155I</th>
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<td></td>
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<td></td>
<td>MIN TYP MAX</td>
<td>MIN TYP MAX</td>
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<tr>
<td>$V_S$</td>
<td>Supply Voltage</td>
<td>●</td>
<td>4.5 18</td>
<td>4.5 18</td>
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<tr>
<td>$I_Q$</td>
<td>Quiescent Current OFF $V_{IN} = 0\text{V}, V_S = 5\text{V}$ (Note 2)</td>
<td>8 20</td>
<td>8 20</td>
<td>µA</td>
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<tr>
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<td>Quiescent Current ON $V_S = 5\text{V}, V_{IN} = 5\text{V}$ (Note 3)</td>
<td>85 120</td>
<td>85 120</td>
<td>µA</td>
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<tr>
<td></td>
<td>Quiescent Current ON $V_S = 12\text{V}, V_{IN} = 5\text{V}$ (Note 3)</td>
<td>180 400</td>
<td>180 400</td>
<td>µA</td>
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<tr>
<td>$V_{INH}$</td>
<td>Input High Voltage</td>
<td>●</td>
<td>2.0</td>
<td>2.0</td>
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<tr>
<td>$V_{INL}$</td>
<td>Input Low Voltage</td>
<td>●</td>
<td>0.8</td>
<td>0.8</td>
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<tr>
<td>$I_{IN}$</td>
<td>Input Current $0V &lt; V_{IN} &lt; V_S$</td>
<td>±1.0</td>
<td>±1.0</td>
<td>µA</td>
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<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>5</td>
<td>5</td>
<td>pF</td>
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<td>$V_{SEN}$</td>
<td>Drain Sense Threshold Voltage</td>
<td>75 100 125</td>
<td>75 100 125</td>
<td>mV</td>
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<td>$I_{SEN}$</td>
<td>Drain Sense Input Current $0V &lt; V_{SEN} &lt; V_S$</td>
<td>±0.1</td>
<td>±0.1</td>
<td>µA</td>
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<tr>
<td>$V_{GATE-V_S}$</td>
<td>Gate Voltage Above Supply $V_S = 5\text{V}$</td>
<td>6.0 6.8 9.0</td>
<td>6.0 6.8 9.0</td>
<td>V</td>
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<tr>
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<td>$V_S = 6\text{V}$</td>
<td>7.5 8.5 15</td>
<td>7.5 8.5 15</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_S = 12\text{V}$</td>
<td>15 18 25</td>
<td>15 18 25</td>
<td>V</td>
</tr>
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<td>$t_{ON}$</td>
<td>Turn ON Time $V_S = 5\text{V}, C_{GATE} = 1000\text{pF}$ Time for $V_{GATE} &gt; V_S + 2\text{V}$</td>
<td>50 250 750</td>
<td>50 250 750</td>
<td>µs</td>
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<tr>
<td></td>
<td>Time for $V_{GATE} &gt; V_S + 5\text{V}$</td>
<td>200 1100 2000</td>
<td>200 1100 2000</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$V_S = 12\text{V}, C_{GATE} = 1000\text{pF}$ Time for $V_{GATE} &gt; V_S + 5\text{V}$</td>
<td>50 180 500</td>
<td>50 180 500</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>Time for $V_{GATE} &gt; V_S + 10\text{V}$</td>
<td>120 450 1200</td>
<td>120 450 1200</td>
<td>µs</td>
</tr>
<tr>
<td>$t_{OFF}$</td>
<td>Turn OFF Time $V_S = 5\text{V}, C_{GATE} = 1000\text{pF}$ Time for $V_{GATE} &lt; 1\text{V}$</td>
<td>10 36 60</td>
<td>10 36 60</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$V_S = 12\text{V}, C_{GATE} = 1000\text{pF}$ Time for $V_{GATE} &lt; 1\text{V}$</td>
<td>10 26 60</td>
<td>10 26 60</td>
<td>µs</td>
</tr>
<tr>
<td>$I_{SC}$</td>
<td>Short-Circuit Turn OFF Time $V_S = 5\text{V}, C_{GATE} = 1000\text{pF}$ Time for $V_{GATE} &lt; 1\text{V}$</td>
<td>5 16 30</td>
<td>5 16 30</td>
<td>µs</td>
</tr>
<tr>
<td></td>
<td>$V_S = 12\text{V}, C_{GATE} = 1000\text{pF}$ Time for $V_{GATE} &lt; 1\text{V}$</td>
<td>5 16 30</td>
<td>5 16 30</td>
<td>µs</td>
</tr>
</tbody>
</table>

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** Quiescent current OFF is for both channels in OFF condition.

**Note 3:** Quiescent current ON is per driver and is measured independently.
TYPICAL PERFORMANCE CHARACTERISTICS

Standby Supply Current

Supply Current/Side (ON)

High Side Gate Voltage

Input Threshold Voltage

Drain Sense Threshold Voltage

Low Side Gate Voltage

Turn ON Time

Turn OFF Time

Short-Circuit Turn OFF Delay Time

For more information www.analog.com
TYPICAL PERFORMANCE CHARACTERISTICS

PIN FUNCTIONS

Input Pin
The LTC1155 logic input is a high impedance CMOS gate and should be grounded when not in use. These input pins have ESD protection diodes to ground and supply and, therefore, should not be forced beyond the power supply rails.

Gate Drive Pin
The gate drive pin is either driven to ground when the switch is turned OFF or driven above the supply rail when the switch is turned ON. This pin is a relatively high impedance when driven above the rail (the equivalent of a few hundred kΩ). Care should be taken to minimize any loading of this pin by parasitic resistance to ground or supply.

Supply Pin
The supply pin of the LTC1155 serves two vital purposes. The first is obvious: it powers the input, gate drive, regulation and protection circuitry. The second purpose is less obvious: it provides a Kelvin connection to the top of the two drain sense resistors for the internal 100mV reference. The supply pin should be connected directly to the power supply source as close as possible to the top of the two sense resistors.

The supply pin of the LTC1155 should not be forced below ground as this may result in permanent damage to the device. A 300Ω resistor should be inserted in series with the ground pin if negative supply voltages are anticipated.

Drain Sense Pin
As noted previously, the drain sense pin is compared against the supply pin voltage. If the voltage at this pin is more than 100mV below the supply pin, the input latch will be reset and the MOSFET gate will be quickly discharged. Cycle the input to reset the short-circuit latch and turn the MOSFET back on.

This pin is also a high impedance CMOS gate with ESD protection and, therefore, should not be forced beyond the power supply rails. To defeat the over current protection, short the drain sense to supply.

Some loads, such as large supply capacitors, lamps or motors require high inrush currents. An RC time delay must be added between the sense resistor and the drain sense pin to ensure that the drain sense circuitry does not false trigger during start-up. This time constant can be set from a few microseconds to many seconds. However, very long delays may put the MOSFET in risk of being destroyed by a short-circuit condition (see Applications Information section).
The LTC1155 contains two independent power MOSFET gate drivers and protection circuits (refer to the Block Diagram for details). Each half of the LTC1155 consists of the following functional blocks:

**TTL and CMOS Compatible Inputs**
Each driver input has been designed to accommodate a wide range of logic families. The input threshold is set at 1.3V with approximately 100mV of hysteresis.

A voltage regulator with low standby current provides continuous bias for the TTL to CMOS converters. The TTL to CMOS converter output enables the rest of the circuitry. In this way the power consumption is kept to a minimum in the standby mode.

**Internal Voltage Regulation**
The output of the TTL to CMOS converter drives two regulated supplies which power the low voltage CMOS logic and analog blocks. The regulator outputs are isolated from each other so that the noise generated by the charge pump logic is not coupled into the 100mV reference or the analog comparator.

**Gate Charge Pump**
Gate drive for the power MOSFET is produced by an adaptive charge pump circuit that generates a gate voltage substantially higher than the power supply voltage. The charge pump capacitors are included on-chip and, therefore, no external components are required to generate the gate drive.

**Drain Current Sense**
The LTC1155 is configured to sense the drain current of the power MOSFET in high side applications. An internal 100mV reference is compared to the drop across a sense resistor (typically 0.002Ω to 0.1Ω) in series with the drain lead. If the drop across this resistor exceeds the internal 100mV threshold, the input latch is reset and the gate is quickly discharged by a large N-channel transistor.

**Controlled Gate Rise and Fall Times**
When the input is switched ON and OFF, the gate is charged by the internal charge pump and discharged in a controlled manner. The charge and discharge rates have been set to minimize RFI and EMI emissions in normal operation. If a short circuit or current overload condition is encountered, the gate is discharged very quickly (typically a few microseconds) by a large N-channel transistor.
APPLICATIONS INFORMATION

Protecting the MOSFET

The MOSFET is protected against destruction by removing drive from the gate as soon as an overcurrent condition is detected. Resistive and inductive loads can be protected with no external time delay. Large capacitive or lamp loads, however, require that the overcurrent shutdown function be delayed long enough to start the load but short enough to ensure the safety of the MOSFET.

Example Calculations

Consider the circuit of Figure 1. A power MOSFET is driven by one side of an LTC1155 to switch a high inrush current load. The drain sense resistor is selected to limit the maximum DC current to 3.3A.

\[ R_{SEN} = \frac{V_{SEN}}{I_{TRIP}} = \frac{0.1}{3.3A} = 0.03\Omega \]

A time delay is introduced between \( R_{SEN} \) and the drain sense pin of the LTC1155 which provides sufficient delay to start a high inrush load such as large supply capacitors.

In this example circuit, we have selected the IRLZ34 because of its low \( R_{DS(ON)} \) (0.05Ω with \( V_{GS} = 5V \)). The FET drops 0.1V at 2A and, therefore, dissipates 200mW in normal operation (no heat sinking required).

If the output is shorted to ground, the current through the FET rises rapidly and is limited by the \( R_{DS(ON)} \) of the FET, the drain sense resistor and the series resistance between the power supply and the FET. Series resistance in the power supply can be substantial and attributed to many sources including harness wiring, PCB traces, supply capacitor ESR, transformer resistance or battery resistance.

For this example, we assume a worst-case scenario; i.e., that the power supply to the power MOSFET is “hard” and provides a constant 5V regardless of the current. In this case, the current is limited by the \( R_{DS(ON)} \) of the MOSFET and the drain sense resistance. Therefore:

\[ I_{PEAK} = \frac{V_{SUPPLY}}{0.08\Omega} = 62.5A \]

The drop across the drain sense resistor under these conditions is much larger than 100mV and is equal to the drain current times the sense resistance:

\[ V_{DROP} = (I_{PEAK})(R_{SEN}) = 1.88V \]

By consulting the power MOSFET data sheet SOA graph, we note that the IRLZ34 is capable of delivering 62.5A at a drain-to-source voltage of 3.12V for approximately 10ms. An RC time constant can now be calculated which satisfies this requirement:

\[ RC = -t \ln \left( 1 - \frac{V_{SEN}}{R_{SEN} \cdot I_{MAX}} \right) \]

\[ RC = \frac{-0.01}{\ln \left( 1 - \frac{0.10}{0.030 \cdot 62.5} \right)} \]

\[ = -0.01/0.054 \]

\[ = 182ms \]

This time constant should be viewed as a maximum safe delay time and should be reduced if the competing requirement of starting a high inrush current load is less stringent; i.e., if the inrush time period is calculated at 20ms, the RC time constant should be set at roughly two or three times this time period and not at the maximum of 182ms. A 60ms time constant would be produced with a 270k resistor and a 0.22µF capacitor (as shown in Figure 1).
APPLICATIONS INFORMATION

Graphical Approach to Selecting $R_{DLY}$ and $C_{DLY}$

Figure 2 is a graph of normalized overcurrent shutdown time versus normalized MOSFET current. This graph can be used instead of the above equation to calculate the RC time constant. The Y axis of the graph is normalized to one RC time constant. The X axis is normalized to the set current. (The set current is defined as the current required to develop 100mV across the drain sense resistor).

Note that the shutdown time is shorter for increasing levels of MOSFET current. This ensures that the total energy dissipated by the MOSFET is always within the bounds established by the MOSFET manufacturer for safe operation.

In the example presented above, we established that the power MOSFET should not be allowed to pass 62.5A for more than 10ms. 62.5A is roughly 18 times the set current of 3.3A. By drawing a line up from 18 and reflecting it off the curve, we establish that the RC time constant should be set at 10ms divided by 0.054, or 180ms. Both methods result in the same conclusion.

Using a Speed Up Diode

A way to further reduce the amount of time that the power MOSFET is in a short-circuit condition is to “bypass” the delay resistor with a small signal diode as shown in Figure 3. The diode will engage when the drop across the drain sense resistor exceeds 0.7V, providing a direct path to the sense pin and dramatically reducing the amount of time the MOSFET is in an overload condition. The drain sense resistor value is selected to limit the maximum DC current to 4A. Above 28A, the delay time drops to 10µs.

Switched Supply Applications

Large inductive loads, such as solenoids, relays and motors store energy which must be directed back to either the power supply or to ground when the supply voltage is interrupted (see Figure 4). In normal operation, when the switch is turned OFF, the energy stored in the inductor is harmlessly absorbed by the MOSFET; i.e., the current flows out of the supply through the MOSFET until the inductor current falls to zero.
APPLICATIONS INFORMATION

If the MOSFET is turned ON and the power supply (battery) removed, the inductor current is delivered by the supply capacitor. The supply capacitor must be large enough to deliver the energy demanded by the discharging inductor. **If the storage capacitor is too small, the supply lead of the LTC1155 may be pulled below ground, permanently destroying the device.**

Consider the case of a load inductance of 1mH which is supporting 3A when the 6V power supply connection is interrupted. A supply capacitor of at least 250µF is required to prevent the supply lead of the LTC1155 from being pulled below ground (along with any other circuitry tied to the supply).

Any wire between the power MOSFET source and the load will add a small amount of parasitic inductance in series with the load (approximately 0.4µH/foot). Bypass the power supply lead of the LTC1155 with a minimum of 10µF to ensure that this parasitic load inductance is discharged safely, even if the load is otherwise resistive.

### Large Inductive Loads

Large inductive loads (>0.1mH) may require diodes connected directly across the inductor to safely divert the stored energy to ground. Many inductive loads have these diodes included. If not, a diode of the proper current rating should be connected across the load to safely divert the stored energy.

### Reverse-Battery Protection

The LTC1155 can be protected against reverse-battery conditions by connecting a resistor in series with the ground lead as shown in Figure 5. The resistor limits the supply current to less than 50mA with −12V applied. Since the LTC1155 draws very little current while in normal operation, the drop across the ground resistor is minimal.

The TTL or CMOS driving logic is protected against reverse-battery conditions by the 100k input current limiting resistor. The addition of 100k resistance in series with the input pin will not affect the turn ON and turn OFF times which are dominated by the controlled gate charge and discharge periods.

**Overvoltage Protection**

The MOSFET and load can be protected against overvoltage conditions by using the circuit of Figure 6. The drain sense function is used to detect an overvoltage condition and quickly discharge the power MOSFET gate. The 18V zener diode conducts when the supply voltage exceeds 18.6V and pulls the drain sense pin 0.6V below the supply pin voltage.

The supply voltage is limited to 18.6V and the gate drive is immediately removed from the MOSFET to ensure that it cannot conduct during the overvoltage period. The gate of the MOSFET will be latched OFF until the supply transient is removed and the input turned OFF and ON again.

![Figure 5. Reverse Battery Protection](image1)

![Figure 6. Overvoltage Shutdown and Protection](image2)
TYPICAL APPLICATIONS

Dual 2A Autoreset Electronic Fuse

[Diagram of Dual 2A Autoreset Electronic Fuse with component values and connections]

High Side Driver with V_DS Sense Short-Circuit Shutdown

[Diagram of High Side Driver with 1N4148 and 1/2 SI9956DY MOSFET with component values and connections]

*ANY 74C OR 74HC LOGIC GATE, MOSFET SHUTS DOWN IF V_DS > 1V

ALL COMPONENTS SHOWN ARE SURFACE MOUNT
**TYPICAL APPLICATIONS**

**X-NOR Fault Detection**

```
+ 10µF
V_S 0.1Ω
IN1 10k
GND 74C266
100k
VS
LTC1155
G1
LOAD
FAULT

Truth Table

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<tr>
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<th>OUT</th>
<th>CONDITION</th>
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<td>0</td>
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<td>1</td>
<td>0</td>
<td>Short Circuit</td>
<td>0</td>
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<tr>
<td>0</td>
<td>1</td>
<td>Open Load</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Switch ON</td>
<td>1</td>
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```

**Low Side Driver with Drain End Current Sensing**

```
+ 10µF
VS 0.05Ω 5%
IN1 1/2 LTC1155
GND SMP25N05
LOAD

*DO NOT SUBSTITUTE. MUST BE A PRECISION, SINGLE SUPPLY, MICROPOWER OP AMP (I_O < 60µA)*
```

**Low Side Driver with Source End Current Sensing**

```
+ 10µF
5V 51Ω
IN1 1/2 LTC1155
GND LOAD
SMP25N05

*DO NOT SUBSTITUTE. MUST BE A PRECISION, SINGLE SUPPLY, MICROPOWER OP AMP (I_O < 60µA)*
```
TYPICAL APPLICATIONS

Automotive High Side Driver with Reverse-Battery and High Voltage Transient Protection

Using the Second Channel for Fault Detection

NOTE: DRAIN SENSE 2 IS USED TO DETECT A FAULT IN CHANNEL 1. GATE 2 PULLS DOWN ON DRAIN SENSE 1 TO DISCHARGE THE MOSFET AND REPORT THE FAULT TO THE µP.
*NOT REQUIRED FOR RESISTIVE OR INDUCTIVE LOADS
TYPICAL APPLICATIONS

5V/3A Extremely Low Voltage Drop Regulator with 10μA Standby Current and Short-Circuit Protection

Bootstrapped Gate Drive for (100Hz < F_0 < 10kHz)
TYPICAL APPLICATIONS

Logic Controlled Boost Mode Switching Regulator with Short-Circuit Protection and 8μA Standby Current

High Efficiency 60Hz Full-Wave Synchronous Rectifier

MOSFETs are synchronously enhanced when rectifier current exceeds 300mA
*No heatsink required. Cases (drains) can be tied together
**Internal body diode of MOSFET
TYPICAL APPLICATIONS

High Efficiency 60Hz Full-Wave Synchronous Rectifier

- MOSFETs are synchronously enhanced when rectifier current exceeds 300mA
- *No heatsink required
- **Internal body diode of MOSFET

Push-Pull Driver with Shoot-Through Current Lockout (f₀ < 100Hz)

- *Opposing gate must drop below 2V before the other is charged

For more information www.analog.com
LTC1155

TYPICAL APPLICATIONS

Full H-Bridge Driver with Shoot-Through Current Lockout and Stall Current Shutdown (f<sub>0</sub> < 100Hz)

DC Motor Speed and Torque Control for Cordless Tools and Appliances

SPEED IS PROPORTIONAL TO PULSE WIDTH. TORQUE IS PROPORTIONAL TO CURRENT
PACKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)

NOTE: LEAD DIMENSIONS APPLY TO SOLDER DIP/PLATE OR TIN PLATE LEADS

OBSOLETE PACKAGE
PACKAGE DESCRIPTION

N Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510 Rev I)

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)

NOTE:
1. DIMENSIONS ARE IN INCHES
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE
## REVISION HISTORY

(Revision history begins at Rev C)

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<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
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<td>Obsoleted CERDIP J8 package</td>
<td>2, 17</td>
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Isolated High Voltage High Side Switch with Circuit Breaker

Isolated Solid-State AC Relay with Circuit Breaker

RELATED PARTS

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<td>Quad Protected High Side MOSFET Driver</td>
<td>8V to 48V Supply Range, Individual Short-Circuit Protection</td>
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<td>Triple 1.8V to 6V High Side MOSFET Driver</td>
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<td>Low $R_{DS(ON)}$ 0.07Ω Switch, 2A Short-Circuit Protected</td>
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