FEATURES

- Ultralow RMS Noise: 0.8µVRMS (10Hz to 100kHz)
- Ultralow Spot Noise: 2.2nV/√Hz at 10kHz
- Ultrahigh PSRR: 74dB at 1MHz
- Output Current: 500mA
- Wide Input Voltage Range: –1.8V to –20V
- Single Capacitor Improves Noise and PSRR
- 100µA SET Pin Current: ±1% Initial Accuracy
- Single Resistor Programs Output Voltage
- Programmable Current Limit
- Low Dropout Voltage: 235mV
- Output Voltage Range: 0V to –19.5V
- Programmable Power Good and Fast Start-Up
- Bipolar Precision Enable/UVLO Pin
- VIOC Pin Controls Upstream Regulator to Minimize Power Dissipation and Optimize PSRR
- Minimum Output Capacitor: 10µF Ceramic
- 12-Lead MSOP and 3mm × 3mm DFN Packages

APPLICATIONS

- RF and Precision Power Supplies
- Very Low Noise Instrumentation
- High Speed/High Precision Data Converters
- Medical Applications: Diagnostics and Imaging
- Post-Regulator for Switching Supplies

DESCRIPTION

The LT®3094 is a high performance low dropout negative linear regulator featuring ADI’s ultralow noise and ultrahigh PSRR architecture for powering noise sensitive applications. The device can be easily paralleled to further reduce noise, increase output current and spread heat on a PCB.

The LT3094 supplies 500mA at a typical 235mV dropout voltage. Operating quiescent current is nominally 2.35mA and drops to 3µA in shutdown. The device’s wide output voltage range (0V to –19.5V) error amplifier operates in unity-gain and provides virtually constant output noise, PSRR, bandwidth, and load regulation independent of the programmed output voltage. Additional features are a bipolar enable pin, programmable current limit, fast start-up capability and programmable power good to indicate output voltage regulation. The regulator incorporates a tracking function to control an upstream supply to maintain a constant voltage across the LT3094 to minimize power dissipation and optimize PSRR.

The LT3094 is stable with a minimum 10µF ceramic output capacitor. Built-in protection includes internal current limit with foldback and thermal limit with hysteresis. The LT3094 is available in thermally enhanced 12-Lead MSOP and 3mm × 3mm DFN Packages.

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TYPICAL APPLICATION

[Diagram of LT3094 circuit with component values and connections]

Power Supply Ripple Rejection

[Graph showing Power Supply Ripple Rejection vs Frequency]
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**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

IN Pin Voltage
- with Respect to GND Pin ............... –22V, 0.3V

EN/UV Pin Voltage
- with Respect to IN Pin (Note 2) .... –0.3V, 30V
- with Respect to GND Pin .......... ±22V

PG Pin Voltage
- with Respect to IN Pin (Note 2) .... –0.3V, 30V
- with Respect to GND Pin .......... –0.3V, 22V

PGFB Pin Voltage
- with Respect to IN Pin (Note 2) .... –0.3V, 30V
- with Respect to GND Pin .......... ±22V

I_LIM Pin Voltage
- with Respect to IN Pin (Note 2) .... –0.3V, 22V

VIOC Pin Voltage
- with Respect to IN Pin (Note 2) .... –0.3V, 22V
- with Respect to GND Pin .......... –2V, 0.3V

SET Pin Voltage
- with Respect to IN Pin (Note 2) .... –0.3V, 22V
- with Respect to GND Pin .......... ±22V

SET Pin Current (Note 4) .................. ±10mA

OUTS Pin Voltage
- with Respect to IN Pin (Note 2) .... –0.3V, 22V
- with Respect to GND Pin .......... ±22V

OUTS Pin Current (Note 4) ............. ±10mA

SET-to-OUTS Differential (Note 5) ........ ±22V

OUT Pin Voltage
- with Respect to IN Pin (Note 2) .... –0.3V, 22V
- with Respect to GND Pin .......... ±22V

Output Short-Circuit Duration .......... Indefinite

Operating Junction Temperature Range (Note 3)
- E-, I-Grades .................. –40°C to 125°C
- H-Grade .......................... –40°C to 150°C
- MP-Grade (Note 17) ............. –55°C to 150°C

Storage Temperature Range ............. –65°C to 150°C

Lead Temperature (Soldering, 10 sec)
- MSE Package Only .................. 300°C
### LT3094

**ORDER INFORMATION**

<table>
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<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3094EDDD#PBF</td>
<td>LT3094EDDD#TRPBF</td>
<td>LHCC</td>
<td>12-Lead (3mm × 3mm) Plastic DFN</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3094IDD#PBF</td>
<td>LT3094IDD#TRPBF</td>
<td>LHCC</td>
<td>12-Lead (3mm × 3mm) Plastic DFN</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3094HDD#PBF</td>
<td>LT3094HDD#TRPBF</td>
<td>LHCC</td>
<td>12-Lead (3mm × 3mm) Plastic DFN</td>
<td>–40°C to 150°C</td>
</tr>
<tr>
<td>LT3094MPDD#PBF</td>
<td>LT3094MPDD#TRPBF</td>
<td>LHCC</td>
<td>12-Lead (3mm × 3mm) Plastic DFN</td>
<td>–55°C to 150°C</td>
</tr>
<tr>
<td>LT3094EMSE#PBF</td>
<td>LT3094EMSE#TRPBF</td>
<td>3094</td>
<td>12-Lead Plastic MSOP</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3094IMSE#PBF</td>
<td>LT3094IMSE#TRPBF</td>
<td>3094</td>
<td>12-Lead Plastic MSOP</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LT3094HMSE#PBF</td>
<td>LT3094HMSE#TRPBF</td>
<td>3094</td>
<td>12-Lead Plastic MSOP</td>
<td>–40°C to 125°C</td>
</tr>
</tbody>
</table>

Contact the factory for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

Tape and reel specifications. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
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<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>Input Voltage Range</td>
<td>ILOAD = 500mA</td>
<td>● −20</td>
<td>−1.8</td>
<td>130</td>
<td>V/Vm</td>
</tr>
<tr>
<td>Minimum IN Pin Voltage (Note 8)</td>
<td>ILOAD = 500mA, VIN UVLO Rising</td>
<td>● −2.3</td>
<td>−1.8</td>
<td>130</td>
<td>mV/mV</td>
</tr>
<tr>
<td></td>
<td>VIN UVLO Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SET Pin Current (ISET)</td>
<td>VIN = −2.3V, ILOAD = 1mA, VOUT = −1.5V</td>
<td>99</td>
<td>100</td>
<td>101</td>
<td>µA/µA</td>
</tr>
<tr>
<td></td>
<td>−20V &lt; VIN &lt; −2.3V, −19.5V &lt; VOUT &lt;0V, 1mA &lt; ILOAD &lt;500mA (Note 7)</td>
<td>98</td>
<td>100</td>
<td>102</td>
<td>µA/µA</td>
</tr>
<tr>
<td>Fast Start-Up SET Pin Current</td>
<td>VPGFB = −286mV, VIN = −2.3V, VSET = −1.5V</td>
<td>1.8</td>
<td></td>
<td></td>
<td>mA/mA</td>
</tr>
<tr>
<td>Output Offset Voltage (Note 9)</td>
<td>VIN = −2.3V, ILOAD = 1mA, VOUT = −1.5V</td>
<td>−1</td>
<td>1</td>
<td></td>
<td>mV/mA</td>
</tr>
<tr>
<td></td>
<td>−20V &lt; VIN &lt; −2.3V, −19.5V &lt; VOUT &lt;0V, 1mA &lt; ILOAD &lt;500mA (Note 7)</td>
<td>−2</td>
<td>2</td>
<td></td>
<td>mV/mA</td>
</tr>
<tr>
<td>Line Regulation: ΔISET</td>
<td>VIN = −2.3V to −20V, ILOAD = 1mA, VOUT = −1.5V (MP-Grade)</td>
<td>−5</td>
<td>0.5</td>
<td>5</td>
<td>nA/V</td>
</tr>
<tr>
<td></td>
<td>VIN = −2.3V to −20V, ILOAD = 1mA, VOUT = −1.5V (Note 9)</td>
<td>−10</td>
<td>0.5</td>
<td>10</td>
<td>nA/V</td>
</tr>
<tr>
<td></td>
<td>VOUT = −2.3V to −20V, ILOAD = 1mA, VOUT = −1.5V (Note 9)</td>
<td>−6</td>
<td>0.1</td>
<td>6</td>
<td>µA/µV</td>
</tr>
<tr>
<td>Load Regulation: ΔISET</td>
<td>ILOAD = 1mA to 500mA, VIN = −2.3V, VOUT = −1.5V</td>
<td>0.1</td>
<td></td>
<td></td>
<td>nA/V</td>
</tr>
<tr>
<td></td>
<td>ILOAD = 1mA to 500mA, VIN = −2.3V, VOUT = −1.5V (Note 9)</td>
<td>0.03</td>
<td>0.5</td>
<td></td>
<td>µA/µV</td>
</tr>
<tr>
<td>Change in ISET with VSET</td>
<td>VSET = −1.5V to −19.5V, VIN = −20V, ILOAD = 1mA</td>
<td>100</td>
<td>850</td>
<td></td>
<td>nA/V</td>
</tr>
<tr>
<td></td>
<td>VSET = −1.5V to −19.5V, VIN = −20V, ILOAD = 1mA (Note 9)</td>
<td>0.02</td>
<td>0.5</td>
<td></td>
<td>mV/V</td>
</tr>
<tr>
<td></td>
<td>VSET = 0V to −1.5V, VIN = −20V, ILOAD = 1mA</td>
<td>150</td>
<td>500</td>
<td></td>
<td>nA/V</td>
</tr>
<tr>
<td></td>
<td>VSET = 0V to −1.5V, VIN = −20V, ILOAD = 1mA (Note 9)</td>
<td>0.15</td>
<td>2</td>
<td></td>
<td>mV/V</td>
</tr>
<tr>
<td>Dropout Voltage (Note 10)</td>
<td>ILOAD = 1mA, 50mA</td>
<td>185</td>
<td>225</td>
<td>275</td>
<td>mV/mV</td>
</tr>
<tr>
<td></td>
<td>ILOAD = 100mA</td>
<td>185</td>
<td>230</td>
<td>280</td>
<td>mV/mV</td>
</tr>
<tr>
<td></td>
<td>ILOAD = 500mA</td>
<td>235</td>
<td>310</td>
<td>410</td>
<td>mV/mV</td>
</tr>
<tr>
<td>GND Pin Current (Note 11)</td>
<td>ILOAD = 10µA</td>
<td>2.35</td>
<td></td>
<td></td>
<td>mA/mA</td>
</tr>
<tr>
<td></td>
<td>ILOAD = 1mA</td>
<td>2.4</td>
<td></td>
<td></td>
<td>mA/mA</td>
</tr>
<tr>
<td></td>
<td>ILOAD = 50mA</td>
<td>3.1</td>
<td>5.5</td>
<td></td>
<td>mA/mA</td>
</tr>
<tr>
<td></td>
<td>ILOAD = 100mA</td>
<td>3.8</td>
<td>6.5</td>
<td></td>
<td>mA/mA</td>
</tr>
<tr>
<td></td>
<td>ILOAD = 500mA</td>
<td>12</td>
<td>23</td>
<td></td>
<td>mA/mA</td>
</tr>
</tbody>
</table>

For more information [www.analog.com](http://www.analog.com)
## Electrical Characteristics

The • denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Noise Spectral Density (Notes 9, 12)</td>
<td>$I_{LOAD} = 500\text{mA}$, Frequency = 10Hz, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$, $V_{OUT} = –3.3\text{V}$</td>
<td>700</td>
<td>70</td>
<td>2.2</td>
<td>nV/Hz</td>
</tr>
<tr>
<td></td>
<td>$I_{LOAD} = 500\text{mA}$, Frequency = 10Hz, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 4.7\mu\text{F}$, $–19.5\text{V} \leq V_{OUT} \leq –1.5\text{V}$</td>
<td>70</td>
<td>2.2</td>
<td>6</td>
<td>nV/Hz</td>
</tr>
<tr>
<td></td>
<td>$I_{LOAD} = 500\text{mA}$, Frequency = 10kHz, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$, $–19.5\text{V} \leq V_{OUT} \leq –1.5\text{V}$</td>
<td>2.2</td>
<td>6</td>
<td>1.8</td>
<td>nV/Hz</td>
</tr>
<tr>
<td>Output RMS Noise (Notes 9, 12)</td>
<td>$I_{LOAD} = 500\text{mA}$, $BW = 10\text{Hz}$ to $100\text{kHz}$, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$, $V_{OUT} = –3.3\text{V}$</td>
<td>3</td>
<td>0.8</td>
<td>1.8</td>
<td>µVRMS</td>
</tr>
<tr>
<td>Reference Current RMS</td>
<td>$BW = 10\text{Hz}$ to $100\text{kHz}$</td>
<td>8</td>
<td></td>
<td></td>
<td>nARMS</td>
</tr>
<tr>
<td>Output RMS Noise (Notes 9, 12)</td>
<td>$V_{RIPPLE} = 500\text{mVP-P}$, $f_{RIPPLE} = 120\text{Hz}$, $I_{LOAD} = 500\text{mA}$, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$</td>
<td>108</td>
<td>94</td>
<td>72</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$V_{RIPPLE} = 500\text{mVP-P}$, $f_{RIPPLE} = 10\text{kHz}$, $I_{LOAD} = 500\text{mA}$, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$</td>
<td>90</td>
<td>75</td>
<td>74</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$V_{RIPPLE} = 500\text{mVP-P}$, $f_{RIPPLE} = 1\text{MHz}$, $I_{LOAD} = 500\text{mA}$, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$</td>
<td>70</td>
<td>60</td>
<td>54</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td>$V_{RIPPLE} = 500\text{mVP-P}$, $f_{RIPPLE} = 10\text{MHz}$, $I_{LOAD} = 500\text{mA}$, $C_{OUT} = 10\mu\text{F}$, $C_{SET} = 0.47\mu\text{F}$</td>
<td>30</td>
<td>20</td>
<td>18</td>
<td>dB</td>
</tr>
</tbody>
</table>
# LT3094

## ELECTRICAL CHARACTERISTICS

The \*\* denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25°C \).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Minimum Load Current (Note 16)</strong></td>
<td>( V_{OUT} &gt; -1.5V )</td>
<td>*</td>
<td>10</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>Thermal Shutdown</strong></td>
<td>( T_J ) Rising</td>
<td>167</td>
<td>8</td>
<td></td>
<td>( °C )</td>
</tr>
<tr>
<td></td>
<td>Hysteresis</td>
<td>8</td>
<td></td>
<td></td>
<td>( °C )</td>
</tr>
<tr>
<td><strong>Start-Up Time</strong></td>
<td>( R_{SET} = 49.9k, V_{OUT(\text{NOM})} = -5V ), ( I_{LOAD} = 500mA ), ( C_{SET} = 0.47\mu F ), ( V_{IN} = -6V ), ( V_{PGFB} = -6V )</td>
<td>55</td>
<td>550</td>
<td>10</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>( R_{SET} = 49.9k, V_{OUT(\text{NOM})} = -5V ), ( I_{LOAD} = 500mA ), ( C_{SET} = 4.7\mu F ), ( V_{IN} = -6V ), ( V_{PGFB} = -6V )</td>
<td></td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td>( R_{SET} = 49.9k, V_{OUT(\text{NOM})} = -5V ), ( I_{LOAD} = 500mA ), ( C_{SET} = 4.7\mu F ), ( V_{IN} = -6V ), ( R_{PG1} = 50k\Omega ), ( R_{PG2} = 700k\Omega ) (with Fast Start-Up to 90% of ( V_{OUT} ))</td>
<td></td>
<td></td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td><strong>Thermal Regulation</strong></td>
<td>10ms Pulse</td>
<td></td>
<td></td>
<td>-0.01</td>
<td>%/W</td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** Parasitic diodes exist internally between the EN/UV, I\(_L\)IM, PG, PGFB, SET, GND, VIOC, OUTS and OUT pins and the IN pin. Do not drive these pins more than 0.3V below the IN pin during a fault condition. These pins must remain at a voltage more positive than IN during normal operation.

**Note 3:** The LT3094 is tested and specified under pulse load conditions such that \( T_J \approx T_A \). The LT3094E is tested at \( T_A = 25°C \) and performance is guaranteed from 0°C to 125°C. Performance of the LT3094E over the full –40°C and 125°C operating temperature range is assured by design, characterization, and correlation with statistical process controls. The LT3094I is 100% tested over the full –40°C to 125°C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

**Note 4:** SET and OUTS pins are clamped using diodes and two 400Ω series resistors. For less than 5ms transients, this clamp circuitry can carry more than the rated current.

**Note 5:** Maximum SET and OUTS pin current requirement must be satisfied.

**Note 6:** Maximum OUT-to-OUTS differential is guaranteed by design.

**Note 7:** Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current, especially due to the internal current limit foldback which starts to decrease current limit at \( V_{OUT} – V_{IN} > 7V \). If operating at maximum output current, limit the input voltage range. If operating at maximum input voltage, limit the output current range.

**Note 8:** The EN/UV pin threshold must be met to ensure device operation.

**Note 9:** OUTS ties directly to OUT.

**Note 10:** Dropout voltage is the minimum input-to-output differential voltage needed to maintain regulation at a specified output current. The dropout voltage is measured when output is 1% out of regulation. This definition results in a higher dropout voltage compared to hard dropout—which is measured when \( V_{IN} = V_{OUT(\text{NOMINAL})} \). For output voltages between 0V and –1.8V, dropout voltage is limited by the minimum input voltage specification.

**Note 11:** GND pin current is tested with \( V_{IN} = V_{OUT(\text{NOMINAL})} \) and a current source load. Therefore, the device is tested while operating in dropout. This is the worst-case GND pin current. GND pin current decreases at higher input voltages. Note that GND pin current does not include SET pin or I\(_L\)IM pin current, but they are included in quiescent current.

**Note 12:** Adding a capacitor across the SET pin resistor decreases output voltage noise. Adding this capacitor bypasses the SET pin resistor’s thermal noise as well as the reference current’s noise. The output noise then equals the error amplifier noise. Use of a SET pin bypass capacitor also increases start-up time.

**Note 13:** The current limit programming scale factor is specified while the internal backup current limit is not active. Note that the current limit has foldback protection for \( V_{OUT} – V_{IN} \) differentials greater than 7V.

**Note 14:** The internal backup current limit circuitry incorporates foldback protection that decreases current limit for \( V_{OUT} – V_{IN} > 7V \). Some level of output current is provided at all \( V_{OUT} – V_{IN} \) differentials. Consult the Typical Performance Characteristics graph for current limit vs \( V_{IN} – V_{OUT} \).

**Note 15:** The VIOC amplifier outputs a voltage equal to \( V_{IN} – V_{OUT} \) or \( V_{IN} + 1.5V \) (when \( V_{OUT} \) is between 0V and –1.5V). See Block Diagram and Applications Information for further information.

**Note 16:** For output voltages between 0V and –1.5V, the LT3094 requires a 10\( \mu A \) minimum load current for stability.

**Note 17:** MP-Grade is only offered in the DFN package.

For more information [www.analog.com](http://www.analog.com)
TYPICAL PERFORMANCE CHARACTERISTICS

TEMPERATURE (°C) = 33.2k
I_SET = –4.3V
QUIESCENT CURRENT (mA) = –300mA
I_L = –10µA
V_IN = –500mA
R_SET = 15k

QUIESCENT CURRENT (µA)

GND PIN CURRENT

R_SET = 33.2k

DROPOUT VOLTAGE (mV)

V_IN = –6V

R_SET = 11Ω
R_L = 11Ω
R_L = 330Ω

V_EN/UV

INPUT VOLTAGE (V)

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

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V_EN/UV = V_IN

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V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

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V_EN/UV = 0V

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V_EN/UV = V_IN

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V_EN/UV = 0V

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V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN

V_IN = –20V

V_EN/UV = 0V

V_IN = –2.3V

V_EN/UV = V_IN
**TYPICAL PERFORMANCE CHARACTERISTICS**

\[ T_A = 25^\circ\text{C}, \text{unless otherwise noted.} \]

### Minimum Input Voltage

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Input Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–75 –50 –25 0 25 50 75 100 125 150</td>
<td>–2.5 –2.2 –2.0 –1.75 –1.5 –1.25 –1.0 –0.75 –0.5 –0.25</td>
</tr>
</tbody>
</table>

### Negative EN/UV Turn-On Threshold

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Threshold (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–75 –50 –25 0 25 50 75 100 125 150</td>
<td>–1.36 –1.34 –1.32 –1.3 –1.28 –1.26 –1.24 –1.22 –1.2 –1.18</td>
</tr>
</tbody>
</table>

### Positive EN/UV Turn-On Threshold

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Threshold (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–75 –50 –25 0 25 50 75 100 125 150</td>
<td>1.36 1.34 1.32 1.3 1.28 1.26 1.24 1.22 1.2 1.18</td>
</tr>
</tbody>
</table>

### EN/UV Pin Hysteresis

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>EN/UV Pin Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–75 –50 –25 0 25 50 75 100 125 150</td>
<td>–1.25 –1.22 –1.2 –1.18 –1.16 –1.14 –1.12 –1.1 –1.08 –1.06 –1.04</td>
</tr>
</tbody>
</table>

### EN/UV Pin Current

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>EN/UV Pin Current (µA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–75 –50 –25 0 25 50 75 100 125 150</td>
<td>–20 –16 –12 –8 –4 0 4 8 12 16 20</td>
</tr>
</tbody>
</table>

### Internal Current Limit

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Current Limit (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–75 –50 –25 0 25 50 75 100 125 150</td>
<td>0 200 400 600 800 1000</td>
</tr>
</tbody>
</table>

### Programmable Current Limit

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>Current Limit (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–75 –50 –25 0 25 50 75 100 125 150</td>
<td>0 200 400 600 800 1000</td>
</tr>
</tbody>
</table>

For more information [www.analog.com](http://www.analog.com)
**LT3094**

**TYPICAL PERFORMANCE CHARACTERISTICS**  \( T_A = 25°C \), unless otherwise noted.

- **Programmable Current Limit**
  - \( R_{ILIM} = 37.5k \)
  - \( V_{OUT} = 0V \)

- **\( I_{LIM} \) Pin Voltage**
  - \( V_{IN} = -2.3V \)
  - \( V_{ILIM} = 0V \)

- **\( I_{LIM} \) Pin Current**
  - \( V_{IN} = -2.3V \)
  - \( V_{ILIM} = 0V \)

- **PGFB Rising Threshold**
  - \( V_{IN} = -2.3V \)

- **PGFB Hysteresis**

- **PG Output Low Voltage**
  - \( V_{IN} = -2.3V \)
  - \( V_{PGF} = -286mV \)
  - \( I_{PG} = 100µA \)

- **PG Pin Leakage Current**
  - \( V_{IN} = -2.3V \)
  - \( V_{PGFB} = -314mV \)
  - \( V_{PG} = 5V \)

- **\( I_{SET} \) During Start-Up with Fast Start-Up Enabled**
  - \( V_{IN} = -2.3V \)
  - \( V_{PGFB} = -286mV \)
  - \( V_{SET} = -1.9V \)

- **\( I_{SET} \) During Start-Up with Fast Start-Up Enabled**
  - \( V_{IN} = -2.3V \)
  - \( V_{PGFB} = -286mV \)
  - \( V_{OUT} = -1.3V \)

For more information [www.analog.com](http://www.analog.com)
TYPICAL PERFORMANCE CHARACTERISTICS

**Power Supply Ripple Rejection as a Function of Error Amplifier Input Pair**

![Graph showing power supply ripple rejection as a function of error amplifier input pair.]

**Integrated RMS Output Noise (10Hz to 100kHz)**

- **V\text{IN} = \text{VOUT} – 2.3V**
- **V\text{IN} = \text{VOUT} – 1.5V**
- **-0.8V > \text{VOUT} > -1.5V**
- **\text{VOUT} > -0.8V**
- **\text{VOUT} > -0.8V**

**Noise Spectral Density**

![Graph showing noise spectral density for various components.]

**TA = 25°C, unless otherwise noted.**
**Typical Performance Characteristics**  \( T_A = 25°C \), unless otherwise noted.

### Line Transient Response

- \( t_f = t_i = 1\mu s \)
- INPUT VOLTAGE: 1V/DIV
- OUTPUT VOLTAGE: 1mV/DIV
- \( R_{\text{SET}} = 33.2k \)
- \( C_{\text{OUT}} = 10\mu\text{F} \)
- \( C_{\text{SET}} = 4.7\mu\text{F} \)
- \( \Delta V_{\text{IN}} = -4.5\text{V} \) to \(-5.5\text{V} \)
- \( I_L = -500\text{mA} \)

### Start-Up Time with and without Fast Start-Up Circuitry for Large \( C_{\text{SET}} \)

- OUTPUT VOLTAGE: 500mV/DIV
- OUTPUT WITH FAST START–UP (SET TO 90%)
- Input Supply Ramp-Up and Ramp-Down

- OUTPUT WITH FAST START–UP
- OUTPUT WITHOUT FAST START–UP
- INPUT VOLTAGE: 2V/DIV
- PULSE EN/UV: 50ms/DIV

- \( V_{\text{IN}} = -5\text{V} \)
- \( R_{\text{SET}} = 33.2k \)
- \( C_{\text{OUT}} = 10\mu\text{F} \)
- \( C_{\text{SET}} = 4.7\mu\text{F} \)
- \( R_L = 6.6\Omega \)
PIN FUNCTIONS

IN (Pins 1, 2, Exposed Pad Pin 13): Input. These pins supply power to the regulator. The LT3094 requires a bypass capacitor at the IN pin. In general, a battery’s output impedance rises with frequency, so include a bypass capacitor in battery-powered applications. While a 10µF input bypass capacitor generally suffices, applications with large load transients may require higher input capacitance to prevent input supply droop. Consult the Applications Information section on the proper use of an input capacitor and its effect on circuit performance.

EN/UV (Pin 3): Enable/UVLO. Pulling the LT3094’s EN/UV pin low places the part in shutdown. Quiescent current in shutdown drops to 3µA and the output voltage turns off. Alternatively, the EN/UV pin can set an input supply undervoltage lockout (UVLO) threshold using a resistor divider between IN, EN/UV and GND. The EN/UV pin is bidirectional and can be switched with either a positive or negative voltage. The LT3094 typically turns on when the EN/UV voltage exceeds 1.26V above ground (with a 200mV hysteresis on its falling edge) or 1.26V below ground (with a 215mV hysteresis). If unused, tie EN/UV to IN. Do not float the EN/UV pin.

PG (Pin 4): Power Good. PG is an open-collector flag that indicates output voltage regulation. PG pulls low if PGFB is between OV and –300mV. If the power good functionality is not needed, float the PG pin. The PG flag status is valid even if the LT3094 is in shutdown, with the PG pin being pulled low.

PGFB (Pin 5): Power Good Feedback. The PG pin pulls high if PGFB is below ~300mV on its rising edge, with 7mV hysteresis on its falling edge. Connecting an external resistor divider between OUT, PGFB, and GND sets the programmable power good threshold with the following transfer function: \(-0.3V \times (1 + \frac{R_{PG1}}{R_{PG2}}) - I_{PGFB} \times R_{PG1}\). As discussed in the Applications Information section, PGFB also activates the fast start-up circuitry. If power good and fast start-up functionality are not needed, tie PGFB to IN.

\(I_{\text{LIM}}\) (Pin 6): Current Limit Programming Pin. Connecting a resistor between \(I_{\text{LIM}}\) and GND programs the current limit. For best accuracy, Kelvin connect this resistor directly to the LT3094’s GND pin. The programming scale factor is nominally 3.75A • kΩ. If the programmable current limit functionality is not needed, tie \(I_{\text{LIM}}\) to GND. Do not float the \(I_{\text{LIM}}\) pin.

VIQC (Pin 7): Voltage for Input-to-Output Control. The LT3094 incorporates a tracking feature to control a circuit supplying power to the LT3094 to maintain the differential voltage across the LT3094. This function maximizes efficiency and PSRR performance while minimizing power dissipation. See the Applications Information section for further information. If unused, float the VIQC pin.

SET (Pin 8): Set. This pin is the inverting input of the error amplifier and the regulation setpoint for the LT3094. The SET pin sinks a precision 100µA current that flows through an external resistor connected between SET and GND. The LT3094’s output voltage is determined by \(V_{\text{SET}} = I_{\text{SET}} \times R_{\text{SET}}\). Output voltage range is from zero to –19.5V. Adding a capacitor from SET to GND improves noise, PSRR, and transient response at the expense of increased start-up time unless the fast start-up capability is used via the PGFB pin. For optimum load regulation, Kelvin connect the ground side of the SET pin directly to the load.

GND (Pin 9): Ground.

OUTS (Pin 10): Output Sense. This pin is the noninverting input to the error amplifier. For optimal transient performance and load regulation, Kelvin connect OUTS directly to the output capacitor and the load. Also, tie the GND connections of the output capacitor and the SET pin capacitor directly together. Exercise care with regards to placement of input capacitors relative to output capacitors due to potential PSRR degradation from magnetic coupling effects; see the Applications Information section for further information on capacitor placement and board layout. A parasitic substrate diode exists between OUTS and IN pins of the LT3094; do not drive OUTS more than 0.3V below IN during normal operation or a fault condition.

OUT (Pins 11, 12): Output. This pin supplies power to the load. For stability, use a minimum 10µF output capacitor with an ESR below 30mΩ and an ESL below 1.5nH. Large load transients require larger output capacitance to limit peak voltage transients. Refer to the Applications Information section for more information on output capacitance. A parasitic substrate diode exists between OUT and IN pins of the LT3094; do not drive OUT more than 0.3V below IN during normal operation or during a fault condition.

For more information www.analog.com
The LT3094 is a high performance low dropout negative linear regulator featuring ADI’s ultralow noise (2.2nV/√Hz at 10kHz) and ultrahigh PSRR (74dB at 1MHz) architecture for powering noise sensitive applications. Designed as a precision current reference followed by a high performance rail-to-rail voltage buffer, the LT3094 can be easily paralleled to further reduce noise, increase output current and spread heat on the PCB. The device additionally features programmable current limit, fast start-up capability and programmable power good.

The LT3094 is easy to use and incorporates all of the protection features expected in high performance regulators. Included are short-circuit protection, safe operating area protection, and thermal shutdown with hysteresis.

**Output Voltage**

The LT3094 incorporates a precision 100µA current reference flowing into the SET pin, which also ties to the error amplifier’s inverting input. Figure 1 illustrates that connecting a resistor from SET to ground generates a reference voltage for the error amplifier. This reference voltage is simply the product of the SET pin current and the SET pin resistor. The error amplifier’s unity-gain configuration produces a low impedance version of this voltage on its noninverting input, i.e. the OUTS pin, which is externally tied to the OUT pin. The LT3094’s output voltage is determined by \( V_{SET} = I_{SET} \cdot R_{SET} \).

The LT3094’s rail-to-rail error amplifier and current reference architecture allows for a wide output voltage range from 0V (using a 0Ω resistor) to \( V_{IN} \) minus dropout. An NPN-based input pair is active for a 0V to –0.8V output and a PNP-based input pair is active for output voltages beyond –1.5V, with a smooth transition between the two input pairs from –0.8V to –1.5V output. The PNP-based input pair offers the best overall performance; refer to the Electrical Characteristics table for details on offset voltage, SET pin current, output noise and PSRR variation depending on the output voltage and corresponding active input pair(s). Table 1 lists common output voltages and their corresponding 1% \( R_{SET} \) resistors.

**Table 1. 1% Resistor for Common Output Voltages**

<table>
<thead>
<tr>
<th>( V_{OUT} ) (V)</th>
<th>( R_{SET} ) (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>–2.5</td>
<td>24.9</td>
</tr>
<tr>
<td>–3.3</td>
<td>33.2</td>
</tr>
<tr>
<td>–5</td>
<td>49.9</td>
</tr>
<tr>
<td>–12</td>
<td>121</td>
</tr>
<tr>
<td>–15</td>
<td>150</td>
</tr>
</tbody>
</table>

The benefit of using a current reference compared with a voltage reference as used in conventional regulators is that the regulator always operates in a unity-gain configuration, independent of the programmed output voltage. This allows the LT3094 to have loop gain, frequency response and bandwidth independent of the output voltage. As a result, noise, PSRR and transient performance do not change with output voltage. Moreover, since error amplifier gain is not needed to amplify the SET pin voltage to a higher output voltage, output load regulation is more tightly specified in the hundreds of microvolts range and not as a fixed percentage of the output voltage.

Since the zero TC current reference is highly accurate, the SET pin resistor can become the limiting factor in achieving high accuracy. Hence, it should be a precision resistor. Additionally, any leakage paths to or from the SET pin create errors in the output voltage. If necessary, use high quality insulation (e.g. Teflon, Kel-F); moreover, cleaning of all insulating surfaces to remove fluxes and other residues may be required. High humidity environments may require a surface coating at the SET pin to provide a moisture barrier.
APPLICATIONS INFORMATION

Minimize board leakage by encircling the SET pin with a guard ring operated at a similar potential—ideally tied to the OUT pin. Guarding both sides of the circuit board is recommended. Bulk leakage reduction depends on the guard ring width. Leakage of 100nA into or out of the SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over wide operating temperature range. Figure 2 illustrates a typical guard ring layout technique.

Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor at heavy load currents. Bypassing the SET pin with a small capacitance to ground resolves this issue—10nF is sufficient.

For applications requiring higher accuracy or an adjustable output voltage, the SET pin may be actively driven by an external voltage source capable of sourcing 100µA. Connecting a precision voltage reference to the SET pin eliminates any errors present in the output voltage due to the reference current and SET pin resistor tolerances.

Output Sensing and Stability

The LT3094’s OUTS pin provides a Kelvin sense connection to the output. The SET pin resistor’s GND side provides a Kelvin sense connection to the load’s GND side.

Additionally, for ultrahigh PSRR, the LT3094 bandwidth is made quite high (~1MHz), making it very close to a typical 10µF (1206 case size) ceramic output capacitor’s self-resonance frequency (~1.6MHz). It is very important to avoid adding extra impedance (ESR and ESL) outside the feedback loop. To that end, minimize the effects of PCB trace and solder inductance by tying the OUTS pin directly to C_OUT and the GND side of C_SET directly to the GND side of C_OUT, as well as keep the GND sides of C_IN and C_OUT reasonably close, as shown in Figure 3. Refer to the LT3094 demo board manual for more information on the recommended layout that meets these requirements. While the LT3094 is robust and will not oscillate if the recommended layout is not followed, depending on the actual layout, phase/gain margin, noise and PSRR performance may degrade.

Stability and Output Capacitance

The LT3094 requires an output capacitor for stability. Given its high bandwidth, ADI recommends low ESR and ESL ceramic capacitors. A minimum 10µF output capacitance with an ESR below 30mΩ and an ESL below 1.5nH is required for stability.

Given the high PSRR and low noise performance attained with using a single 10µF ceramic output capacitor, larger values of output capacitor only marginally improve the performance because the regulator bandwidth decreases with increasing output capacitance—hence, there is little to be gained by using larger than the minimum 10µF output capacitor. Nonetheless, larger values of output capacitance do decrease peak output deviations during a load transient.
Note that bypass capacitors used to decouple individual components powered by the LT3094 increase the effective output capacitance.

Give extra consideration to the type of ceramic capacitors used. They are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in small packages, but they tend to have stronger voltage and temperature coefficients as shown in Figure 4 and Figure 5. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied over the operating temperature range.

The X5R and X7R dielectrics result in more stable characteristics and are thus more suitable for use with the LT3094. The X7R dielectric has better stability across temperature, while the X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and the maximum capacitance change over temperature. While capacitance change due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance below sufficient levels. As shown in Figure 6, capacitor DC bias characteristics tend to improve as component case size increases, but verification of expected capacitance at the operating voltage is highly recommended. Due to its good voltage coefficient in small case sizes, ADI recommends using Murata’s GJ8 series ceramic capacitor.

**High Vibration Environments**

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates voltage across its terminals due to mechanical stress upon it, similar to how a piezoelectric microphone works. For a ceramic capacitor, this stress can be induced by mechanical vibrations within the system or due to thermal transients.

LT3094 applications in high vibration environments have three distinct piezoelectric noise generators: ceramic
output, input, and SET pin capacitors. However, due to the LT3094’s very low output impedance over a wide frequency range, negligible output noise is generated using a ceramic output capacitor. Similarly, due to the LT3094’s ultrahigh PSRR, negligible output noise is generated using a ceramic input capacitor. Given the high SET pin impedance, any piezoelectric response from a ceramic SET pin capacitor generates significant output noise; peak-to-peak excursions of hundreds of µVs are possible. However, due to the SET pin capacitor’s high ESR and ESL tolerance, any non-piezoelectrically responsive (tantalum, electrolytic, or film) capacitor can be used at the SET pin; do note that electrolytic capacitors tend to have high 1/f noise. In any case, use of surface mount capacitors is highly recommended.

Stability and Input Capacitance

The LT3094 is stable with a minimum 10µF IN pin capacitor. ADI recommends using low ESR ceramic capacitors. Applications using long wires to connect the power supply to the LT3094’s input and ground terminals together with low ESR ceramic input capacitors are prone to voltage spikes, reliability concerns and application-specific board oscillations. The wire inductance combined with the low ESR ceramic input capacitor forms a high Q resonant LC tank circuit. In some instances, this resonant frequency beats against the output current LDO bandwidth and interferes with stable operation. The resonant LC tank circuit formed by the wire inductance and input capacitor is the cause and not because of LT3094’s instability.

The self inductance, or isolated inductance, of a wire is directly proportional to its length. The wire diameter, however, has less influence on its self inductance. For example, the self inductance of a 2-AWG isolated wire with a diameter of 0.26” is about half the inductance of a 30-AWG wire with a diameter of 0.01”. One foot of 30-AWG wire has 465nH of self inductance.

Several methods exist to reduce a wire’s self inductance. One method divides the current flowing towards the LT3094 between two parallel conductors. In this case, placing wire further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed in close proximity to each other, their mutual inductance adds to the overall self inductance of the wires—therefore a 50% reduction is not possible in such cases. The second and more effective technique to reduce the overall inductance is to place the forward and return current conductors (the input and ground wires) in close proximity. Two 30-AWG wires separated by 0.02” reduce the overall inductance to about one-fifth of a single wire.

If a battery mounted in close proximity powers the LT3094, a 10µF input capacitor suffices for stability. If a distantly located supply powers the LT3094, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 10µF minimum) per 6” of wire length. The minimum input capacitance needed to stabilize the application also varies with the output capacitance as well as the load current. Placing additional capacitance on the LT3094’s output helps. However, this requires significantly more capacitance compared to additional input bypassing. Series resistance between the supply and the LT3094 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use a higher ESR tantalum or electrolytic capacitor at the LT3094 input in parallel with a 10µF ceramic capacitor.

PSRR and Input Capacitance

For applications utilizing the LT3094 for post-regulating switching converters, placing a capacitor directly at the LT3094 input results in AC current (at the switching frequency) to flow near the LT3094. This relatively high frequency switching current generates magnetic fields that couple to the LT3094 output, degrading the effective PSRR. While highly dependent on the PCB layout, the switching preregulator, the size of the input capacitor and other factors, the PSRR degradation can easily be over 30dB at 1MHz. This degradation is present even with the LT3094 desoldered from the board, it is a degradation in the PSRR of the PCB itself. While negligible for conventional low PSRR LDOs, the LT3094’s ultrahigh PSRR requires careful attention to higher order parasitics in order to realize the full performance offered by the regulator.

To mitigate the flow of high frequency switching current near the LT3094, the input capacitor can be entirely removed as long as the switching converter’s output capacitor is located more than an inch away from the
**APPLICATIONS INFORMATION**

LT3094. Magnetic coupling decreases rapidly with increasing distance. If the switching regulator is placed too far away (conservatively more than a couple inches) from the LT3094, the lack of an input capacitor presents a high impedance at the input of the LT3094 and oscillation may occur. It is generally a common (and preferred) practice to bypass regulator inputs with some capacitance, so this option is fairly limited in its scope and not the most palatable solution.

To that end, ADI recommends referencing the LT3094 demo board layout for achieving the best possible PSRR performance. Two main factors contribute to higher PSRR with a poor layout. Parasitic trace inductance coupled with the low ESR ceramic input capacitor can lead to higher ripple at the input of the LDO than at the output of the driving supply. Also, physical loops create magnetic fields that couple from the input to the output. The LT3094 demo board utilizes layout techniques to minimize both parasitic inductance in traces and coupling of magnetic loops, preventing PSRR degradation while keeping the input capacitor.

**Filtering High Frequency Spikes**

For applications where the LT3094 is used to post-regulate a switching converter, its high PSRR effectively suppresses any harmonic content present at the switching frequency (typically 100kHz to 4MHz). However, there are very high frequency (hundreds of MHz) spikes associated with the switcher’s power switch transition times that are beyond the LT3094’s bandwidth and will almost directly pass through to the output. While the output capacitor is partly intended to absorb these spikes, its ESL will limit its ability at these frequencies. A ferrite bead or even the inductance associated with a short (e.g. 0.5”) PCB trace coupled with a capacitor with a low impedance at the transition frequency can serve as an LC-filter to suppress these very high frequency spikes.

**Output Noise**

The LT3094 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for a traditional regulator are its voltage reference, error amplifier, noise from the resistor divider network used for setting output voltage and the noise gain created by this resistor divider. Many low noise regulators pin out their voltage reference to allow for noise reduction by bypassing the reference voltage.

Unlike most linear regulators, the LT3094 does not use a voltage reference; instead it uses a 100µA current reference. The current reference operates with typical noise current level of 27pA/√Hz (8nARMS over the 10Hz to 100kHz bandwidth). The resultant voltage noise equals the current noise multiplied by the resistor values, which is then RMS summed with the error amplifier’s noise and the resistor’s Johnson noise of √4kTR (k = Boltzmann’s constant, 1.38 • 10^-23 J/K, and T is absolute temperature) to give the net output noise.

One problem faced by conventional linear regulators is that the resistor divider setting the output voltage gains up the reference noise. In contrast, the LT3094’s unity-gain follower architecture presents no gain from the SET pin to the output. Therefore, using a capacitor to bypass the SET pin resistor allows output voltage noise to be independent of the programmed output voltage. The resultant output noise is then determined only by the error amplifier’s noise, typically 2nV/√Hz from 1kHz to 1MHz and 0.8µVRMS in the 10Hz to 100kHz bandwidth when using a 4.7µF SET pin capacitor. Paralleling multiple LT3094s further reduces noise by √N for N parallel regulators.

Refer to the Typical Performance Characteristics section for noise spectral density and RMS integrated noise performance over various load currents and SET pin capacitances.

**SET Pin (Bypass) Capacitance: Noise, PSRR, Transient Response and Soft-Start**

In addition to reducing output noise, using a SET pin bypass capacitor also improves PSRR and transient performance. Note that any bypass capacitor leakage deteriorates the LT3094’s DC regulation. Capacitor leakage of as little as 100nA causes a 0.1% DC error. ADI recommends the use of a good quality low leakage ceramic capacitor.

Using a SET pin bypass capacitor also soft starts the output and limits inrush current. The RC time constant formed by the SET pin resistor and capacitor determines soft-start
time. Without the use of fast start-up, the ramp-up rate from 0 to 90% of nominal $V_{OUT}$ is:

$$t_{SS} \approx 2.3 \cdot R_{SET} \cdot C_{SET} \text{ (Fast Start-Up Disabled)}$$

**Fast Start-Up**

For ultralow noise applications that require low 1/f noise (i.e., at frequencies below 100Hz) a larger value SET pin capacitor is required; up to 22µF may be used. While normally this would significantly increase the regulator’s start-up time, the LT3094 incorporates fast start-up circuitry that increases the SET pin current to about 1.8mA during start-up.

As shown in the Block Diagram, the 1.8mA current source remains engaged while PGFB is less than –300mV unless the regulator is in current limit, dropout, thermal shutdown, or input voltage is below the minimum $V_{IN}$.

If fast start-up capability is not used, tie PGFB to IN or to OUT (for output voltages more than –300mV). Note that doing so also disables power good functionality.

**ENABLE/UVLO**

The EN/UV pin is used to put the regulator into a micropower shutdown state. The LT3094 has an accurate –1.26V turn-on threshold on the EN/UV pin with 215mV of hysteresis. This threshold can be used in conjunction with a resistor divider from the input supply to define an accurate undervoltage lockout (UVLO) threshold for the regulator. The EN/UV pin current ($I_{EN}$) at the threshold needs to be considered when calculating the resistor divider network. See the Electrical Characteristics table and Typical Performance curves for EN/UV pin characteristics. The EN/UV pin current can be ignored if $R_{EN1}$ is less than 100k. Use the following formula to determine resistor divider values (See Programming Undervoltage Lockout in the Typical Applications section):

$$V_{IN(UVLO)} = -1.26V \cdot (1 + \frac{R_{EN2}}{R_{EN1}}) - I_{EN} \cdot R_{EN2}$$

Since the EN/UV pin is bidirectional, it can also be pulled above 1.26V to turn on the LT3094. In bipolar supply applications, the positive EN/UV threshold can be used to sequence the turn-on of the LT3094 after the positive regulator has turned on. If unused, tie the EN/UV pin to IN.

**High Efficiency Linear Regulator—Input-to-Output Voltage Control**

The VIOC pin is used to control an upstream switching converter and facilitate a design solution that maximizes system efficiency while providing good transient response, low noise, and high power supply ripple rejection (PSRR) by maintaining a constant voltage across the LT3094 regardless of the device’s output voltage. This works well in applications where the output voltage is varied for the application requirements. This regulation loop also minimizes total power dissipation in fault conditions; if the output is short-circuited and the LT3094 current limits, the VIOC amplifier lowers the switching regulator output voltage and limits the power dissipation in the LT3094.

The VIOC pin is the output of a fast unity-gain amplifier that measures the voltage differential between IN and OUTS or –1.5V, whichever is lower. It typically connects to the feedback node or into the resistor diver of most LTC® switching regulators or LTM® power modules and sinks at least 100µA of current. Targeting –1V differential from input-to-output provides an optimum tradeoff in terms of power dissipation and PSRR. If paralleling multiple LT3094’s, tie the VIOC pin of one of the devices to the upstream switching converter’s feedback pin and float the remaining VIOC pins.

The VIOC amplifier is designed to sink current, and only sources current through its internal impedance to ground. The VIOC pin has a typical impedance to ground of 40k±15%, this is important to consider if using a maximum input voltage configuration or if the LT3094 is disabled.

As the VIOC buffer operates with high bandwidth, the switching converter’s frequency compensation doesn’t need to be adjusted while the VIOC buffer is inside the switching converter’s feedback loop. Phase delay through the VIOC buffer is typically less than 4° for frequencies as high as 100kHz; within the switching converter’s bandwidth (usually well below 100kHz) the VIOC buffer is transparent and acts like an ideal wire. For example, with a switching converter with less than 100kHz bandwidth and a phase margin of 50°, using the VIOC buffer will degrade the phase margin by at most 4°. The net phase margin for the switching converter (using the VIOC pin)
APPLICATIONS INFORMATION

is at least 46°. With the VIOC buffer inside the switching converter’s feedback loop, keep the total capacitance on the VIOC pin to below 20pF.

For $0 \geq V_{\text{OUT}} \geq -1.5V$, $V_{\text{IN}} = V_{\text{VIQC(NOM)}} - 1.5V$. For $V_{\text{OUT}} \leq -1.5V$, $V_{\text{IN}} = V_{\text{OUT}} + V_{\text{VIQC(NOM)}}$. The VIOC pin voltage (and the input-to-output differential) is programmable to anywhere between $-0.41V$ (the dropout voltage of the regulator) and $-1.3V$. As shown in Figure 7, the input-to-output differential is easily programmed using the following equation:

$$V_{\text{LDOIN}} - V_{\text{LDOOUT}} = V_{\text{VIQC(NOM)}} = V_{\text{FBSWITCHER}} \times \frac{R1 + R2}{R1}$$

In the event that the SET pin has an open-circuit fault condition, the LT3094’s input voltage will increase to the switching converter’s maximum output voltage and may violate the LT3094’s absolute maximum rating for $V_{\text{IN}}$. To prevent this, adding an optional resistor (R3) between the VIOC and IN pins of the regulator gives a maximum voltage configuration based on the following equation:

$$V_{\text{LDOIN(MAX)}} = V_{\text{FBSWITCHER}} \times \frac{R1 + R2 + R3}{R1} + V_{\text{VIQC(NOM)}} \times \frac{R3}{40k}$$

**Typical VIOC Applications**

Figure 8 shows an application using the LT8330 configured as an inverting regulator powering the LT3094 to deliver a $-3.3V$ output. The resistors shown drive the FBX pin of the LT8330 to $-0.8V$ so that its output is $-4.3V$ (with $-1V$ on the VIOC pin) when the LT3094 is operating at $-3.3V$ output and is $-5V$ when the LT3094 is disabled.

Another inverting regulator configuration is shown in Figure 9, this time using the LT8580. The LT8580 FBX pin regulates at $3mV$ (typical) with $83.3\mu A$ flowing out of the pin ($I_{\text{FBX}}$). Because of this, only a single resistor is needed between the FBX pin and VIOC (from Figure 7, only R2 is

![Figure 7. Typical VIOC Application](image)

![Figure 8. VIOC Connection Using LT8330 Delivers $-4.3V$ When Operating, $-5V$ When LT3094 is Disabled](image)

![Figure 9. VIOC Connection Using LT8580](image)
APPLICATIONS INFORMATION

necessary, R1 is not needed). In this case, the resistor is calculated as follows:

\[ V_{\text{LDOIN}} - V_{\text{LDOOUT}} = V_{\text{VIOC (NOM)}} = V_{\text{FBX}} - R_2 \cdot I_{\text{FBX}} \]

For the optional maximum voltage configuration, R3 is added and the maximum input voltage to the LT3094 is calculated as follows:

\[ V_{\text{LDOIN (MAX)}} = V_{\text{VIOC (NOM)}} + V_{\text{VIOC (NOM)}} \frac{R_3}{40k} - R_3 \cdot I_{\text{FBX}} \]

Again, the resistors shown are configured to drive the output of the switcher to –4.3V when the LT3094 is operating at –3.3V output and –5V when disabled. Using the circuit from Figure 9, the LDO’s input and output is shown in Figure 10 when pulsing the LT3094’s EN/UV pin. As can be seen, when the LDO is disabled, the LDO input voltage goes to the maximum voltage set by the resistor divider on the VIOC pin. Figure 10 shows the load step response of the LT8580 using the VIOC buffer. Figure 11 shows the LDO’s input and output voltage response to stepping the SET pin voltage from –3V to –4V. Figure 12 shows the LDO’s input and output voltage while ramping the SET pin from 0V to –4.5V, and as can be seen, the LT8580’s output voltage tracks the LT3094’s output voltage when below –1.5V and limits at the maximum voltage set by the resistor divider set on the VIOC pin. Last, Figure 14 shows the noise spectral density at the LT3094’s input and output.
Programmable Power Good

As illustrated in the Block Diagram, power good threshold is user programmable using the ratio of two external resistors, \( R_{PG1} \) and \( R_{PG2} \):

\[
V_{OUT(PG\_THRESH)} = -0.3V(1 + R_{PG1}/R_{PG2}) - I_{PGFB} \cdot R_{PG1}
\]

If the PGFB pin becomes less than \(-300\text{mV}\), the open-collector PG pin deasserts and becomes high impedance. The power good comparator has 7mV hysteresis and 5\(\mu\)s of deglitching. The PGFB pin current \(I_{PGFB}\) can be ignored if \(R_{PG2}\) is less than 30k, otherwise it must be considered when determining the resistor divider network. If power good functionality is not used, float the PG pin. Please note that programmable power good and fast start-up capabilities are disabled for output voltages between OV and \(-300\text{mV}\).

Take care when laying out traces for PG and PGFB on a PCB. If the PG and PGFB pins are run close to each other for a distance (typically greater than two inches), stray capacitance from trace-to-trace couples the PG signal into the high impedance PGFB signal. Since PG is out of phase relative to PGFB, this results in oscillation. To avoid this, minimize the distance the two traces run close to each other; lowering the impedance seen at the PGFB pin by using lower value resistors for the PGFB divider also helps.

Externally Programmable Current Limit

The \(I_{ILIM}\) pin internally regulates to \(-300\text{mV}\). Connecting a resistor from ground to \(I_{ILIM}\) sets the current flowing into the \(I_{ILIM}\) pin, which in turn programs the LT3094’s current limit. With the 3.75k\(\Omega\) • A programming scale factor, the current limit can be calculated as follows:

\[
\text{Current Limit} = 3.75k\Omega \cdot A / R_{ILIM}
\]

For example, a 7.5k resistor programs the current limit to 500mA and a 15k resistor programs the current limit to 250mA. For good accuracy, Kelvin connect this resistor to the LT3094’s GND pin.

In cases where IN-to-OUT differential is greater than 7V, the LT3094’s foldback circuitry decreases the internal current limit. As a result, the internal current limit may override the externally programmed current limit to keep the LT3094 within its safe-operating-area (SOA). See the graph of Internal Current Limit vs Input-to-Output Differential in the Typical Performance Characteristics section. If not used, tie \(I_{ILIM}\) to GND.

Output Overshoot Recovery

During a load step from heavy load to very light or no load, the output voltage overshoots before the regulator responds to turn the power transistor off. With very light or no load, it takes a long time to discharge the output capacitor.

The LT3094 incorporates an overshoot recovery circuit that turns on a current source to discharge the capacitor in the event that OUTS is higher than SET. This current is typically 3.5mA.

If OUTS is externally held above SET, the current source turns on in an attempt to restore OUTS to its programmed voltage. The current source remains on until the external circuitry releases OUTS.

Direct Paralleling for Higher Current

Higher output current is obtained by paralleling multiple LT3094s. Tie all SET pins together and all IN pins together. Connect the OUT pins together using small pieces of PCB trace (used as a ballast resistor) to equalize currents in the LT3094s. PCB trace resistance in m\(\Omega\)/inch is shown in Table 2.

<table>
<thead>
<tr>
<th>WEIGHT (oz)</th>
<th>10mil WIDTH</th>
<th>20mil WIDTH</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>54.3</td>
<td>27.1</td>
</tr>
<tr>
<td>2</td>
<td>27.1</td>
<td>13.6</td>
</tr>
</tbody>
</table>

Trace resistance is measured in m\(\Omega\)/in.

The small worst-case offset of 2mV for each paralleled LT3094 minimizes the required ballast resistor value. Figure 15 illustrates that two LT3094s, each using a 20m\(\Omega\) PCB trace ballast resistor, provide better than 20% accurate output current sharing at full load. The two 20m\(\Omega\) external resistors only add 10mV of output regulation drop with a 1A maximum current. With a \(-3.3V\) output, this only adds 0.3% to the regulation accuracy. As has been discussed previously, tie the OUTS pins directly to the output capacitors.
More than two LT3094s can also be paralleled for even higher output current and lower output noise. Paralleling multiple LT3094s is also useful for distributing heat on the PCB. For applications with high input-to-output voltage differential, an input series resistor or a resistor in parallel with the LT3094 can also be used to spread heat.

**PCB Layout Considerations**

Given the LT3094’s high bandwidth and ultrahigh PSRR, careful PCB layout must be employed to achieve full device performance. Figure 16 shows a recommended layout that delivers full performance of the regulator. Refer to the LT3094’s DC2624A demo board manual for further details.

**Thermal Considerations**

The LT3094 has internal power and thermal limiting circuits that protect the device under overload conditions. The thermal shutdown temperature is nominally 165°C with about 8°C of hysteresis. For continuous normal load conditions, do not exceed the maximum junction temperature (125°C for E- and I-grades, 150°C for H- and MP-grades). It is important to consider all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Additionally, consider all heat sources in close proximity to the LT3094.

The undersides of the DFN and MSOP packages have exposed metal from the lead frame to the die attachment. Both packages allow heat to directly transfer from the die junction to the PCB metal to limit maximum operating junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of the PCB.
APPLICATIONS INFORMATION

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by the regulator.

Table 3 and Table 4 list thermal resistance as a function of copper area on a fixed board size. All measurements were taken in still air on a 4-layer FR-4 board with 1oz solid internal planes and 2oz top/bottom planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-7 and JESD51-12. Achieving low thermal resistance necessitates attention to detail and careful PCB layout.

Table 3. Measured Thermal Resistance for DFN Package

<table>
<thead>
<tr>
<th>COPPER AREA</th>
<th>BOARD AREA</th>
<th>THERMAL RESISTANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP SIDE*</td>
<td>BOTTOM SIDE</td>
<td></td>
</tr>
<tr>
<td>2500mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
</tr>
<tr>
<td>1000mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
</tr>
<tr>
<td>225mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
</tr>
<tr>
<td>100mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
</tr>
</tbody>
</table>

*Device is mounted on topside

Figure 16. Recommended DFN Layout
APPLICATIONS INFORMATION

Table 4. Measured Thermal Resistance for MSOP Package

<table>
<thead>
<tr>
<th>COPPER AREA</th>
<th>BOARD AREA</th>
<th>THERMAL RESISTANCE</th>
</tr>
</thead>
<tbody>
<tr>
<td>TOP SIDE*</td>
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<td>2500mm²</td>
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<tr>
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<tr>
<td>225mm²</td>
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</tr>
<tr>
<td>100mm²</td>
<td>2500mm²</td>
<td>2500mm²</td>
</tr>
</tbody>
</table>

*Device is mounted on topside

Calculating Junction Temperature

Example: Given an output voltage of –3.3V and input voltage of –5V ±5%, output current range from 1mA to 500mA, and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The LT3094’s power dissipation is:

\[ P_{\text{DISS}} = I_{\text{OUT(MAX)}} \cdot (V_{\text{IN(MAX)}} - V_{\text{OUT}}) + I_{\text{GND}} \cdot V_{\text{IN(MAX)}} \]

where:

\[ I_{\text{OUT(MAX)}} = -500mA \]
\[ V_{\text{IN(MAX)}} = -5.25V \]
\[ I_{\text{GND}} \text{ (at } I_{\text{OUT}} = 500mA \text{ and } V_{\text{IN}} = -5.25V) = -9mA \]

thus:

\[ P_{\text{DISS}} = -0.5A \cdot (-5.25V + 3.3V) + 9mA \cdot 5.25V = 1.02W \]

Using a DFN package, the thermal resistance is in the range of 34°C/W to 36°C/W depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals:

\[ 1.02W \cdot 35°C/W \approx 35.7°C \]

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

\[ T_{J(\text{MAX})} = 85°C + 35.8°C = 120.7°C \]

Overload Recovery

Like many IC power regulators, the LT3094 incorporates safe-operating-area (SOA) protection. The SOA protection activates at input-to-output differential voltages greater than 7V. The SOA protection decreases the current limit as the input-to-output differential increases and keeps the power transistor inside a safe operating region for all values of input-to-output voltages up to the LT3094’s absolute maximum ratings. The LT3094 provides some level of output current for all values of input-to-output differential voltage. Refer to the Current Limit curves in the Typical Performance Characteristics section. When power is first applied and input voltage rises, the output follows the input and keeps the input-to-output differential low to allow the regulator to supply large output current and start-up into high current loads.

Due to current limit foldback, however, at high input voltages a problem can occur if the output voltage is low and the load current is high. Such situations occur after the removal of a short-circuit or if the EN/UV pin is pulled high after the input voltage has already turned on. The load line in such cases intersects the output current profile at two points. The regulator now has two stable operating points. With this double intersection, the input power supply may need to be cycled down to zero and brought back up again to make the output recover. Other linear regulators with foldback current limit protection (such as the LT3090, LT1964 and LT1175) also exhibit this phenomenon, so it is not unique to the LT3094.

Protection Features

The LT3094 incorporates several protection features for sensitive applications. Precision current limit and thermal overload protection safeguard the LT3094 against overload and fault conditions at the device’s output. For normal operation, do not allow the junction temperature to exceed 125°C (E- and I-grades) or 150°C (H- and MP-grades).

Pulling the LT3094’s output above ground induces no damage to the part. If IN is left open circuit or grounded, OUT can be pulled 20V above GND. In this condition, a maximum current of 25mA flows into the OUT pin and out of the GND pin. If IN is powered by a voltage source, OUT sinks the LT3094’s (foldback) short circuit current and protects itself by thermal limiting. In this case, however, grounding the EN/UV pin turns off the device and stops OUT from sinking the short-circuit current.
TYPICAL APPLICATIONS

Programming Undervoltage Lookout

\[ V_{IN(UVLO)RISING} = \frac{-1.26 \times (1 + \frac{110k}{49.9k})}{10nF} \]

\[ V_{IN(TURN-ON)} = \approx -4V \]
\[ V_{IN(TURN-OFF)} = \approx -3.35V \]

PINS NOT USED IN THIS CIRCUIT: PG, VIOC
Positive and Negative Variable Supply

V\text{IN} \, 12V

L1A 2.2\mu F

10\mu F

10k

10k

PG1

SYNC1

CLKOUT1

CLKOUT2

SYNC2

PG2

SHDN2

VIN2

SWA2 SWB2

L1B 187k

47\mu F

47\mu F

100pF

47nF

0.1\mu F

2k

100pF

80.6k

80.6k

0.1\mu F

2k

14.7k

187k

L1: DRQ125-8R2
L2: DRQ125-4R7
D1, D2: DFLS230L

LT3045

V\text{IN}

14.7k

L2A 2.2\mu F

L2B 2.2\mu F

D2

187k

D1

V\text{POS}: VARIABLE
I\text{POS}\text{(MAX)}: 500mA

V\text{NEG}: VARIABLE
I\text{NEG}\text{(MAX)}: –500mA

LT3094

V\text{IN}

12V

100\mu A

100\mu A

4.7\mu F

10\mu F

10\mu F

249k

267k

150k

150k

4.7\mu F

4.7\mu F

100pF

100pF

100pF

100pF

47nF

47nF

80.6k

80.6k

100k

100k

100\mu A

100\mu A
PACKAGE DESCRIPTION

DD Package
12-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1725 Rev A)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

NOTE:
1. DRAWING IS NOT A JEDEC PACKAGE OUTLINE
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD AND TIE BARS SHALL BE SOLDER PLATED
6. SHADeD AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

For more information www.analog.com
**PACKAGE DESCRIPTION**

**MSE Package**
12-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1666 Rev G)

**NOTE:**
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

**BOTTOM VIEW OF EXPOSED PAD OPTION**

**RECOMMENDED SOLDER PAD LAYOUT**

**GAUGE PLANE**

**SEATING PLANE**

For more information www.analog.com
### REVISION HISTORY

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<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
<th>PAGE NUMBER</th>
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<tr>
<td>A</td>
<td>01/19</td>
<td>Added H temperature range, ( T_{J\text{MAX}} ) increased to 150°C.&lt;br&gt;Modified Note 3 for H temperature range.&lt;br&gt;Added Positive and Negative Supply application circuit.</td>
<td>3, 4, 26, 28, 6, 30</td>
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<tr>
<td>B</td>
<td>01/20</td>
<td>Added MP temperature range.&lt;br&gt;Updated Noise Spectral Density (0.1Hz to 10Hz) curve.</td>
<td>3, 4, 6, 26, 28, 13</td>
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LT3094

TYPICAL APPLICATION

Parallel Devices

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<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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<td>LT1185</td>
<td>3A, Negative Linear Regulator</td>
<td>750mV Dropout Voltage, $V_{IN} = -4.3V$ to $-35V$, DD-PAK and TO-220 Packages</td>
</tr>
<tr>
<td>LT1175</td>
<td>500mA, Negative Low Dropout Micropower Regulator</td>
<td>500mV Dropout Voltage, $V_{IN} = -4.5V$ to $-20V$, N8, S8, DD-PAK, TO-220 and SOT-223 Packages</td>
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<tr>
<td>LT1964</td>
<td>200mA, Negative Low Noise Low Dropout Regulator</td>
<td>340mV Dropout Voltage, Low Noise: $30\mu V_{RMS}$, $V_{IN} = -1.9V$ to $-20V$, DFN and SOT-23 Packages</td>
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<tr>
<td>LT3015</td>
<td>1.5A, Fast Transient Response, Negative LDO Regulator</td>
<td>310mV Dropout Voltage, Low Noise: $60\mu V_{RMS}$, $V_{IN} = -2.3V$ to $-30V$, DFN, MSOP, TO-220 and DD-PAK Packages</td>
</tr>
<tr>
<td>LT3080</td>
<td>1.1A, Parallelable, Low Noise, Low Dropout Linear Regulator</td>
<td>350mV Dropout Voltage (2-Supply Operation), Low Noise: $40\mu V_{RMS}$, $V_{IN}$ 1.2V to $36V$, Single Resistor Output, DFN, MSOP, TO-220, DD and SOT-223 Packages</td>
</tr>
<tr>
<td>LT3085</td>
<td>500mA, Parallelable, Low Noise, Low Dropout Linear Regulator</td>
<td>275mV Dropout Voltage (2-Supply Operation), Low Noise: $40\mu V_{RMS}$, $V_{IN}$ 1.2V to $36V$, Single Resistor Output, DFN and MSOP Packages</td>
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<td>LT3090</td>
<td>$-36V$, 600mA Negative Linear Regulator with Programmable Current Limit</td>
<td>300mV Dropout Voltage, Low Noise: $18\mu V_{RMS}$, $V_{IN}$ $-1.5V$ to $-36V$, Single Resistor Output, DFN and MSOP Packages</td>
</tr>
<tr>
<td>LT3091</td>
<td>$-36V$, 1.5A Negative Linear Regulator</td>
<td>300mV Dropout Voltage, Low Noise: $18\mu V_{RMS}$, $V_{IN}$ $-1.5V$ to $-36V$, Single Resistor Output, DFN, TSSOP, TO-220 and DD-Pak Packages</td>
</tr>
<tr>
<td>LT3045</td>
<td>20V, 500mA, Ultralow Noise Ultrahigh PSRR Linear Regulator</td>
<td>0.8$\mu V_{RMS}$ Noise and 75dB PSRR at 1MHz, $V_{IN}$ = 1.8V to 20V, 260mV Dropout Voltage, 3mm $\times$ 3mm DFN and MSOP Packages</td>
</tr>
<tr>
<td>LT3042</td>
<td>20V, 200mA, Ultralow Noise Ultrahigh PSRR Linear Regulator</td>
<td>0.8$\mu V_{RMS}$ Noise and 79dB PSRR at 1MHz, $V_{IN}$ = 1.8V to 20V, 350mV Dropout Voltage, Programmable Current Limit and Power Good, 3mm $\times$ 3mm DFN and MSOP Packages</td>
</tr>
</tbody>
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