20 GHz to 36 GHz, GaAs, MMIC, Double Balanced Mixer

HMC1106LG

FEATURES

- Passive: no dc bias required
- Wide IF frequency range: dc to 24 GHz
- Conversion loss up to TBD dB
- LO to RF isolation: 31 dB
- 12-terminal, 4.00 mm × 4.00 mm, RoHS compliant, LGA_CAV package

APPLICATIONS

- Microwave point to point radios
- Video satellite (VSAT) and satellite communications (SATCOM)
- Test equipment and sensors
- Military end use
- Automotive radars

FUNCTIONAL BLOCK DIAGRAM

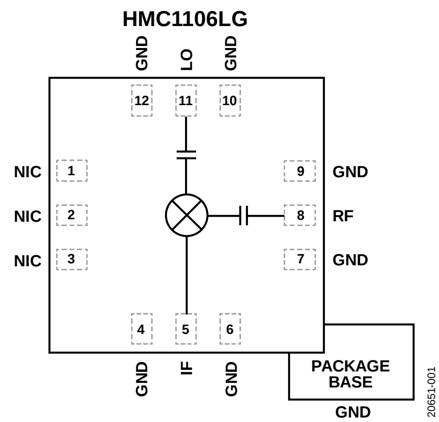

Figure 1.

GENERAL DESCRIPTION

The HMC1106LG is a general-purpose, double balanced, monolithic microwave integrated mixer (MMIC) that can be used as a downconverter or an upconverter with a dc to 24 GHz frequency range at the intermediate frequency (IF) port, a 20 GHz to 50 GHz frequency range at the local oscillator (LO) port, and a 20 GHz to 36 GHz frequency range at the RF port.

This MMIC mixer is fabricated with gallium arsenide (GaAs), Schottky diode technology and ideally suited for applications where small size, no dc bias, and consistent IC performance is required. The HMC1106LG is packaged in a 12-terminal, 4.00 mm × 4.00 mm, RoHS compliant, chip array small outline no lead cavity (LGA_CAV).

Rev. PrA
Document Feedback

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

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SPECIFICATIONS

T_A = 25°C, LO = 36.1 GHz at 15 dBm, lower sideband, and all measurements performed as a downconverter on the evaluation printed circuit board (PCB), unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
RF RANGE		20		36	GHz
LO INPUT FREQUENCY RANGE		20		50	GHz
IF FREQUENCY RANGE		DC		24	GHz
LO AMPLITUDE		13	15	19	dBm
20 GHz to 24 GHz PERFORMANCE					
Downconverter					
Conversion Loss			9.5	TBD	dB
Input Third-Order Intercept (IP3)	1 MHz separation between inputs	TBD	18		dBm
Input Second-Order Intercept (IP2)	1 MHz separation between inputs		TBD		dBm
Isolation					
RF to IF		TBD	TBD		dB
LO to RF			31		dB
LO to IF		TBD	TBD		dB
24 GHz to 27 GHz PERFORMANCE					
Downconverter					
Conversion Loss			11	TBD	dB
Input IP3	1 MHz separation between inputs	TBD	17		dBm
Input IP2	1 MHz separation between inputs		TBD		dBm
Isolation					
RF to IF		TBD	TBD		dB
LO to RF			31		dB
LO to IF		TBD	TBD		dB
27 GHz to 36 GHz PERFORMANCE					
Downconverter					
Conversion Loss			9	TBD	dB
Input IP3	1 MHz separation between inputs	TBD	22		dBm
Input IP2	1 MHz separation between inputs		TBD		dBm
Isolation					
RF to IF		TBD	TBD		dB
LO to RF			31		dB
LO to IF		TBD	TBD		dB

T_A = 25°C, IF = 100 MHz, LO = 15 dBm, lower sideband, and all measurements performed as a downconverter on the evaluation PCB, unless otherwise noted.

Table 2.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
LO AMPLITUDE			15		dBm
20 GHz to 24 GHz PERFORMANCE					
Downconverter					
Conversion Loss			6.5		dB
Single Sideband (SSB) Noise Figure	Taken with LO amplifier		TBD		dB
Input IP3	1 MHz separation between inputs		TBD		dBm
Input 1 dB Compression Point (P1dB)			TBD		dBm
Input IP2	1 MHz separation between inputs		TBD		dBm
Upconverter	IF input (IF_{IN}) = 100 MHz				
Conversion Loss			7		dB
Input IP3	1 MHz separation between inputs		TBD		dBm
Input P1dB			TBD		dBm
24 GHz to 27 GHz PERFORMANCE					
Downconverter					
Conversion Loss			6.5		dB
SSB Noise Figure	Taken with LO amplifier		TBD		dB
Input IP3	1 MHz separation between inputs		TBD		dBm
Input P1dB			TBD		dBm
Input IP2	1 MHz separation between inputs		TBD		dBm
Upconverter	IF_{IN} = 100 MHz				
Conversion Loss			6.5		dB
Input IP3	1 MHz separation between inputs		TBD		dBm
Input P1dB			TBD		dBm
27 GHz to 36 GHz PERFORMANCE					
Downconverter					
Conversion Loss			8		dB
SSB Noise Figure	Taken with LO amplifier		TBD		dB
Input IP3	1 MHz separation between inputs		TBD		dBm
Input P1dB			TBD		dBm
Input IP2	1 MHz separation between inputs		TBD		dBm
Upconverter	IF_{IN} = 100 MHz				
Conversion Loss			9		dB
Input IP3	1 MHz separation between inputs		TBD		dBm
Input P1dB			TBD		dBm

Absolute Maximum Ratings

Table 3.

Parameter	Rating
RF Input Power	17 dBm
LO Input Power	22 dBm
IF Input Power	10 dBm
IF Source and Sink Current	5 mA
Reflow Temperature	260°C
Junction Temperature (T_J)	175°C
Continuous Power Dissipation, P_{DISS} (T_A = 85°C, Derate 3.7 mW/°C Above 85°C)	183 mW
Temperature	
Operating Range	−40°C to +85°C
Storage Range	−65°C to +150°C
Lead (Soldering, 60 sec)	260°C
Peak Reflow, Moisture Sensitivity Level (MSL) 3[1]	260°C
Electrostatic Discharge (ESD) Sensitivity	
Human Body Model (HBM)	TBD
Field Induced Charged Device Model (FICDM)	TBD

[1] See the Ordering Guide.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to PCB design and operating environment. Careful attention to PCB thermal design is required.

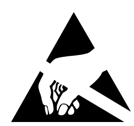
θ_{JA} is the junction to ambient temperature, and θ_{JC} is the junction to case temperature.

Table 4. Thermal Resistance

Package Type[1]	θ_{JA}	θ_{JC}	Unit
CE-12-4[1]	500	376	°C/W

[1] Test Condition 1: JEDEC standard JESD51-2.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

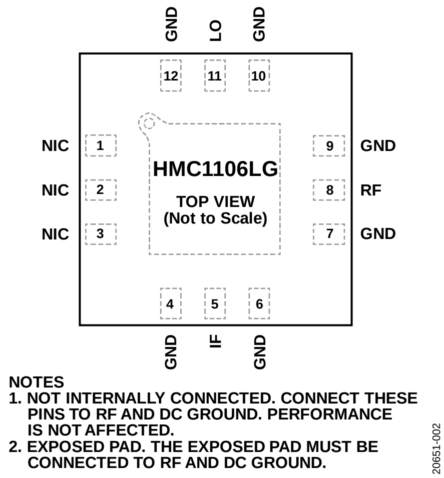


Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3	NIC	Not Internally Connected. Connect these pins to RF and dc ground. Performance is not affected.
4, 6, 7, 9, 10, and 12	GND	Ground. These pins and package bottom must be connected to RF and dc ground. See Figure 3 for the interface schematic.
5	IF	Intermediate Frequency Port. This pin is dc-coupled. See Figure 4 for the interface schematic.
		For applications not requiring operation to dc, dc block this port externally using a series capacitor of a value chosen to pass the necessary IF frequency range.
		For operation to dc, this pin must not source and/or sink more than 3 mA of current. Otherwise, die malfunction or die failure may result.
8	RF	Radio Frequency Port. This pin is ac-coupled and matched to 50 Ω. See Figure 5 for the interface schematic.
11	LO	Local Oscillator Port. This pin is ac-coupled and matched to 50 Ω. See Figure 6 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to RF and dc ground.

INTERFACE SCHEMATICS

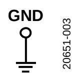


Figure 3. GND Interface Schematic

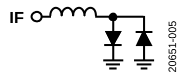


Figure 4. IF Interface Schematic

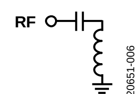


Figure 5. RF Interface Schematic

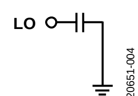


Figure 6. LO Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

DOWNCONVERTER PERFORMANCE

IF = 100 MHz, Lower Sideband (High-Side LO)

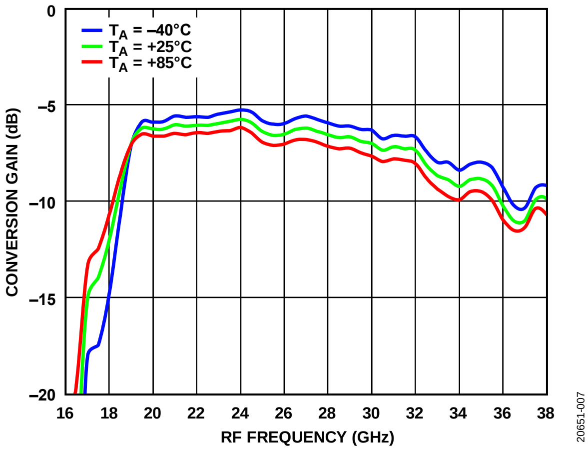


Figure 7. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 15 dBm

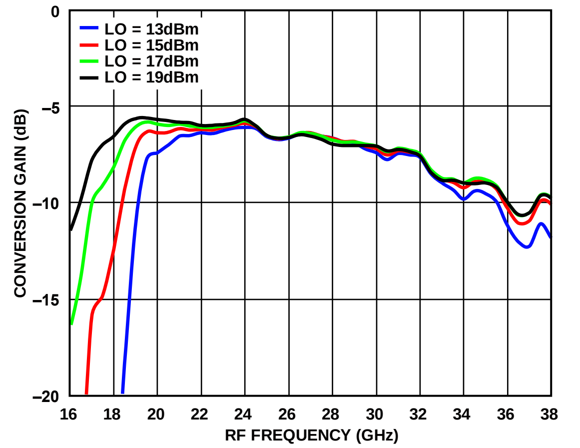


Figure 10. Conversion Gain vs. RF Frequency at Various LO Powers, T_A = 25°C

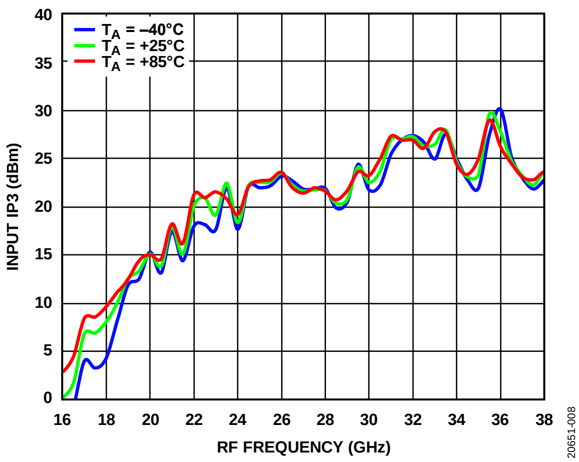


Figure 8. Input IP3 vs. RF Frequency at Various Temperatures, LO = 15 dBm

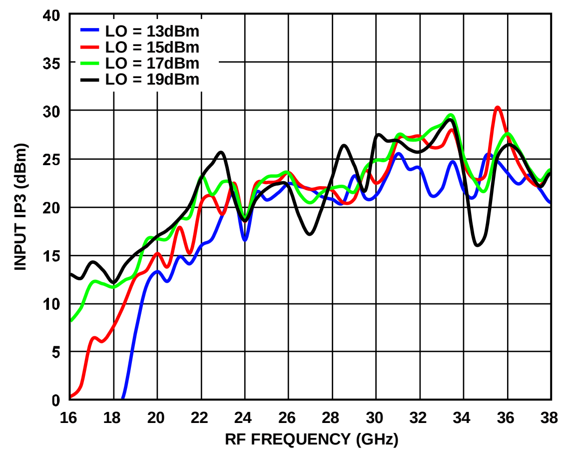


Figure 11. Input IP3 vs. RF Frequency at Various LO Powers, T_A = 25°C

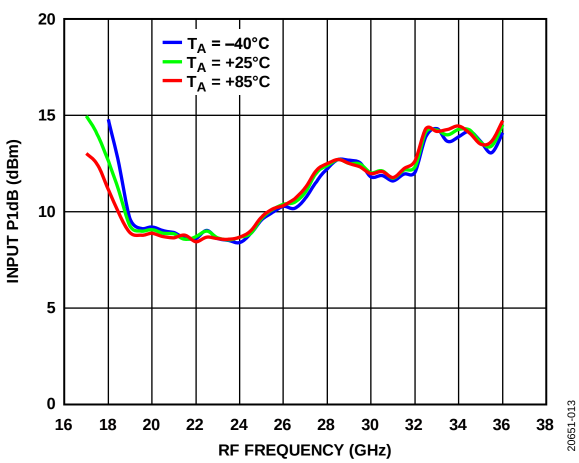


Figure 9. Input P1dB vs. RF Frequency at Various Temperatures, LO = 15 dBm

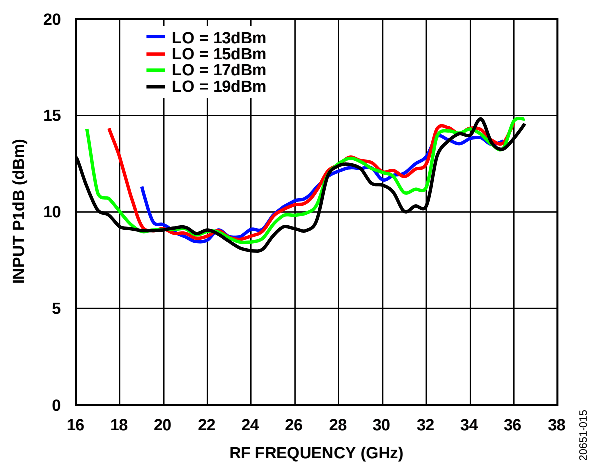


Figure 12. Input P1dB vs. RF Frequency at Various LO Powers, T_A = 25°C

SPURIOUS AND HARMONICS PERFORMANCE

LO Harmonics

LO = 15 dBm, and all values in dBc below input LO level and measured at RF port. N/A means not applicable.

Table 6. LO Harmonics at RF

	N_{LO} Spur at RF Port (dBc)			
LO Frequency (GHz)	**1**	**2**	**3**	**4**
20	TBD	TBD	TBD	TBD
21	TBD	TBD	TBD	TBD
22.5	TBD	TBD	TBD	TBD
23	TBD	TBD	TBD	TBD
24	TBD	TBD	TBD	TBD
25	TBD	TBD	TBD	TBD

LO = 13 dBm, and all values in dBc below input LO level and measured at IF port. N/A means not applicable.

Table 7. LO Harmonics at IF

	N_{LO} Spur at IF Port (dBc)			
LO Frequency (GHz)	**1**	**2**	**3**	**4**
20	TBD	TBD	TBD	TBD
21	TBD	TBD	TBD	TBD
22.5	TBD	TBD	TBD	TBD
23	TBD	TBD	TBD	TBD
24	TBD	TBD	TBD	TBD
25	TBD	TBD	TBD	TBD

M × N Spurious Outputs

Downconversion, Upper Sideband

Spur values are (M × RF) − (N × LO). RF = 37.1 GHz, LO = 20 GHz at +15 dBm, and RF power = −10 dBm. Mixer spurious products are measured in dBc from the IF output power level. N/A means not applicable.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × RF	**0**	TBD	TBD	TBD	TBD	TBD
	1	TBD	TBD	TBD	TBD	TBD
	2	TBD	TBD	TBD	TBD	TBD
	3	TBD	TBD	TBD	TBD	TBD
	4	TBD	TBD	TBD	TBD	TBD

Downconversion, Lower Sideband

Spur values are (M × RF) − (N × LO). RF = 20 GHz, LO = 35 GHz at 15 dBm, and RF power = −10 dBm. Mixer spurious products are measured in dBc from the IF output power level. N/A means not applicable.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × RF	**0**	TBD	TBD	TBD	TBD	TBD
	1	TBD	TBD	TBD	TBD	TBD
	2	TBD	TBD	TBD	TBD	TBD
	3	TBD	TBD	TBD	TBD	TBD
	4	TBD	TBD	TBD	TBD	TBD

Upconversion, Upper Sideband

Spur values are (M × IF_{IN}) + (N × LO). IF_{IN} = 12.1 GHz, LO = 25 GHz at +15 dBm, and IF_{IN} power = −10 dBm. Mixer spurious products are measured in dBc from the RF output power level. N/A means not applicable.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × IF_{IN}	**−5**	TBD	TBD	TBD	TBD	TBD
	−4	TBD	TBD	TBD	TBD	TBD
	−3	TBD	TBD	TBD	TBD	TBD
	−2	TBD	TBD	TBD	TBD	TBD
	−1	TBD	TBD	TBD	TBD	TBD
	0	TBD	TBD	TBD	TBD	TBD
	+1	TBD	TBD	TBD	TBD	TBD
	+2	TBD	TBD	TBD	TBD	TBD
	+3	TBD	TBD	TBD	TBD	TBD
	+4	TBD	TBD	TBD	TBD	TBD
	+5	TBD	TBD	TBD	TBD	TBD

Upconversion, Lower Sideband

Spur values are (M × IF_{IN}) + (N × LO). IF_{IN} = 15 GHz, LO = 35 GHz at +15 dBm, and IF_{IN} power = −10 dBm. Mixer spurious products are measured in dBc from the RF output power level. N/A means not applicable.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × IF_{IN}	**−5**	TBD	TBD	TBD	TBD	TBD
	−4	TBD	TBD	TBD	TBD	TBD
	−3	TBD	TBD	TBD	TBD	TBD
	−2	TBD	TBD	TBD	TBD	TBD
	−1	TBD	TBD	TBD	TBD	TBD
	0	TBD	TBD	TBD	TBD	TBD
	+1	TBD	TBD	TBD	TBD	TBD
	+2	TBD	TBD	TBD	TBD	TBD
	+3	TBD	TBD	TBD	TBD	TBD
	+4	TBD	TBD	TBD	TBD	TBD
	+5	TBD	TBD	TBD	TBD	TBD

THEORY OF OPERATION

The HMC1106LG is a MMIC, double balanced mixer that can operate as downconverter or a upconverter from 20 GHz to 36 GHz. When used as a downconverter, the HMC1106LG downconverts RF values between 20 GHz and 36 GHz to IF values between dc and 24 GHz. When used as an upconverter, the mixer upconverts IF values between dc and 24 GHz to RF values between 20 GHz and 36 GHz.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 13 shows the typical application circuit for the HMC1106LG. The HMC1106LG is a passive device and does not require any external components. The LO pin and the RF pin are internally ac-coupled. The IF pin is internally dc-coupled. For applications not requiring operation to dc, dc block this port externally using a series capacitor with a value chosen to pass the necessary IF frequency range. When IF operation to dc is required, do not exceed the IF source and sink current rating specified in the **Absolute Maximum Ratings** section.

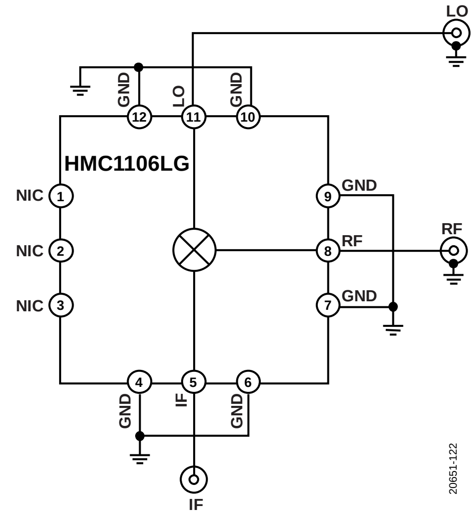


Figure 13. Typical Application Circuit

For information on the EV1HMC1106LG evaluation board, see the EV1HMC1106LG (UG-1651) user guide.

OUTLINE DIMENSIONS

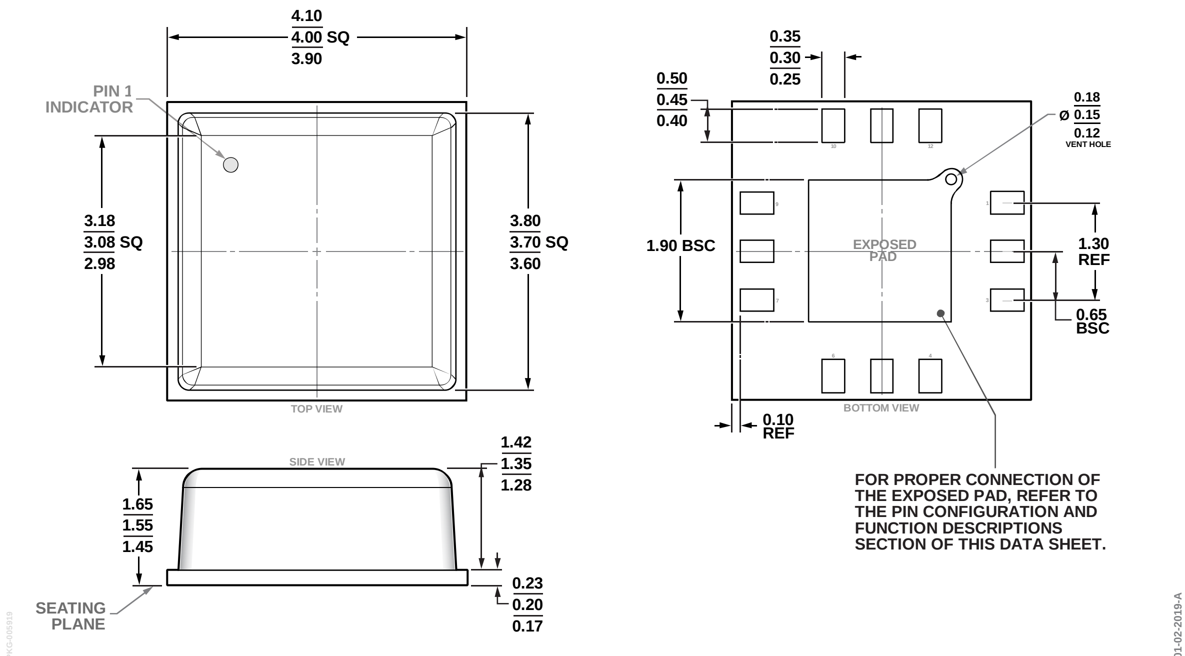


Figure 14. 12-Terminal Chip Array Small Outline No Lead Cavity [LGA_CAV]
4.00 mm × 4.00 mm Body and 1.65 mm Package Height
(CE-12-4)
Dimensions shown in millimeters