FEATURES
Small 20-lead QSOP
1000 V rms isolation rating
Safety and regulatory approvals (pending):
  UL recognition (pending)
  1000 V rms for 1 minute per UL 1577
Low power operation
  3.3 V operation
    1.6 mA per channel maximum at 0 Mbps to 1 Mbps
    7.8 mA per channel maximum at 25 Mbps
  5 V operation
    2.2 mA per channel maximum at 0 Mbps to 1 Mbps
    11.2 mA per channel maximum at 25 Mbps
Bidirectional communication
Up to 25 Mbps data rate (NRZ)
3 V/5 V level translation
High temperature operation: 105°C
High common-mode transient immunity: >15 kV/μs

APPLICATIONS
General-purpose, multichannel isolation
SPI interface/data converter isolation
RS-232/RS-422/RS-485 transceivers
Industrial field bus isolation

GENERAL DESCRIPTION
The ADuM7640/ADuM7641/ADuM7642/ADuM7643 are 6-channel digital isolators based on the Analog Devices, Inc., iCoupler® technology. These 1 kV digital isolation devices are packaged in a small 20-lead QSOP. They offer space savings and a lower price than 2.5 kV or 5 kV isolation solutions when only functional isolation is needed.

This family, like many Analog Devices isolators, offers very low power consumption, using one-tenth to one-sixth the power of other digital isolators, with the supply voltage on either side ranging from 3.0 V to 5.5 V. Despite their low power consumption, the ADuM7640/ADuM7641/ADuM7642/ADuM7643 provide low pulse width distortion (< 6 ns for C grade) and a channel-by-channel glitch filter to protect the device against extraneous noise disturbances. Four channel direction combinations are available with a maximum data rate of 1 Mbps or 25 Mbps. All products have a default output high logic state in the absence of input power.

1 Protected by U.S. Patents 5,952,849; 6,873,065; and 7,075,329. Other patents pending.

Rev. 0 Document Feedback
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Technical Support www.analog.com
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## Revision History

9/12—Revision 0: Initial Version
SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—5 V OPERATION
All typical specifications are at $T_A = 25^\circ C$, $V_{DD1} = V_{DD2} = 5$ V. Minimum/maximum specifications apply over the entire recommended operation range of $4.5$ V ≤ $V_{DD1}$ ≤ $5.5$ V, $4.5$ V ≤ $V_{DD2}$ ≤ $5.5$ V, and $-40^\circ C$ ≤ $T_A$ ≤ $+105^\circ C$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF and CMOS signal levels, unless otherwise noted.

Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>A Grade</th>
<th></th>
<th>C Grade</th>
<th></th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
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<tr>
<td></td>
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<td>Min Typ Max</td>
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<td>SWITCHING SPECIFICATIONS</td>
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<tr>
<td>Pulse Width</td>
<td>PW</td>
<td>250</td>
<td></td>
<td>40</td>
<td></td>
<td>ns</td>
<td>Within PWD limit</td>
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<tr>
<td>Data Rate</td>
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<td>25</td>
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<td>Mbps</td>
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<td>Propagation Delay tPHL, tPLH</td>
<td></td>
<td>75</td>
<td>28</td>
<td>40</td>
<td>50</td>
<td>ns</td>
<td>50% input to 50% output</td>
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<td>Propagation Delay Skew1 tPSK</td>
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<td></td>
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<td>ps/°C</td>
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<td>Channel Matching</td>
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<tr>
<td>Codirectional tPSKCD</td>
<td></td>
<td>20</td>
<td></td>
<td>14</td>
<td></td>
<td>ns</td>
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<td>Opposing Directional tPSKOD</td>
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<td>25</td>
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<td>Jitter</td>
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<td>7</td>
<td>12</td>
<td>ns</td>
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</table>

1 $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ or $t_{PLH}$ that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

2 Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

3 Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposite sides of the isolation barrier.

Table 2.

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<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>1 Mbps—A and C Grades</th>
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<td>ADuM7640</td>
<td>lDD1</td>
<td>5.7 7.0</td>
<td></td>
<td>44 54</td>
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<td>mA</td>
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<tr>
<td></td>
<td>lDD2</td>
<td>4.4 5.9</td>
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<td>11 13</td>
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<td>mA</td>
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<tr>
<td>ADuM7641</td>
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<td>38 46</td>
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<td>mA</td>
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<td></td>
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<td>15 19</td>
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<tr>
<td>ADuM7642</td>
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<td>5.2 6.3</td>
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<td>31 38</td>
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<td>mA</td>
<td></td>
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<td>lDD2</td>
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<td>ADuM7643</td>
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<td>mA</td>
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<td>lDD2</td>
<td>5.0 6.3</td>
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<td>22 29</td>
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<td>Input Voltage Threshold</td>
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<tr>
<td>Logic High</td>
<td>$V_{IH}$</td>
<td>0.7 $V_{DDx}$</td>
<td></td>
<td></td>
<td>V</td>
<td>$I_{Ox} = -20 \mu A, V_x = V_{WH}$</td>
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<tr>
<td>Logic Low</td>
<td>$V_{IL}$</td>
<td>0.3 $V_{DDx}$</td>
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<td></td>
<td>V</td>
<td>$I_{Ox} = -4 mA, V_x = V_{WH}$</td>
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<td>Output Voltages</td>
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<tr>
<td>Logic High</td>
<td>$V_{OH}$</td>
<td>$V_{DDx} - 0.1$</td>
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<td>V</td>
<td>$I_{Ox} = 20 \mu A, V_x = V_{HL}$</td>
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<td></td>
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<td>$V_{DDx} - 0.4$</td>
<td>4.8</td>
<td></td>
<td>V</td>
<td>$I_{Ox} = 4 mA, V_x = V_{HL}$</td>
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<tr>
<td>Logic Low</td>
<td>$V_{OL}$</td>
<td>0.0</td>
<td>0.1</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
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<td>0.2</td>
<td>0.4</td>
<td></td>
<td>V</td>
<td></td>
<td></td>
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<tr>
<td>Input Current per Channel</td>
<td>$I_i$</td>
<td>$-10$</td>
<td>+0.01</td>
<td>+10</td>
<td>$\mu A$</td>
<td>$0 V \leq V_x \leq V_{DDx}$</td>
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</tr>
<tr>
<td>Supply Current per Channel</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
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<tr>
<td>Quiescent Supply Current</td>
<td></td>
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<td></td>
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<td></td>
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<td></td>
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<tr>
<td>Input</td>
<td>$I_{DDI (Q)}$</td>
<td>0.95</td>
<td>1.16</td>
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<td>mA</td>
<td></td>
<td></td>
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<tr>
<td>Output</td>
<td>$I_{DDO (Q)}$</td>
<td>0.73</td>
<td>0.98</td>
<td></td>
<td>mA</td>
<td></td>
<td></td>
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<tr>
<td>Dynamic Supply Current</td>
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<tr>
<td>Input</td>
<td>$I_{DDI (D)}$</td>
<td>0.26</td>
<td></td>
<td></td>
<td>mA/Mbps</td>
<td></td>
<td></td>
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<tr>
<td>Output</td>
<td>$I_{DDO (D)}$</td>
<td>0.04</td>
<td></td>
<td></td>
<td>mA/Mbps</td>
<td></td>
<td></td>
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<td><strong>AC SPECIFICATIONS</strong></td>
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<tr>
<td>Output Rise/Fall Time</td>
<td>$t_{s}/t_{f}$</td>
<td>2.0</td>
<td></td>
<td></td>
<td>ns</td>
<td>10% to 90%</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Transient Immunity$^1$</td>
<td>$</td>
<td>CM</td>
<td>$</td>
<td>15</td>
<td>25</td>
<td></td>
<td>kV/µs</td>
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<tr>
<td>Refresh Rate</td>
<td>$f_r$</td>
<td>600</td>
<td></td>
<td></td>
<td>kHz</td>
<td>DC data inputs</td>
<td></td>
</tr>
</tbody>
</table>

$^1$ $|CM|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{CL} < 0.8 \times V_{DDx}$ or $V_{CH} > 0.7 \times V_{DDx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.
ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at \( T_A = 25°C \), \( V_{DD1} = V_{DD2} = 3.3 \) V. Minimum/maximum specifications apply over the entire recommended operation range of \( 3.0 \) V \( \leq V_{DD1} \leq 3.6 \) V, \( 3.0 \) V \( \leq V_{DD2} \leq 3.6 \) V, and \(-40°C \leq T_A \leq +105°C\), unless otherwise noted. Switching specifications are tested with \( C_L = 15 \) pF and CMOS signal levels, unless otherwise noted.

Table 4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>A Grade</th>
<th>C Grade</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
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<tr>
<td>SWITCHING SPECIFICATIONS</td>
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<tr>
<td>Pulse Width</td>
<td>PW</td>
<td>250</td>
<td>40</td>
<td>ns</td>
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<tr>
<td>Data Rate</td>
<td></td>
<td>1</td>
<td>25</td>
<td>Within PWD limit</td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>( t_{PHL}, t_{PLH} )</td>
<td>85</td>
<td>33</td>
<td>ns</td>
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<td>Pulse Width Distortion</td>
<td>PWD</td>
<td>25</td>
<td>2</td>
<td>6 ns</td>
</tr>
<tr>
<td>Change vs. Temperature</td>
<td></td>
<td>5</td>
<td>3</td>
<td>(</td>
</tr>
<tr>
<td>Propagation Delay Skew(^1)</td>
<td>( t_{PSK} )</td>
<td>20</td>
<td>14</td>
<td>ps/°C</td>
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<tr>
<td>Channel Matching</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Codirectional(^2)</td>
<td>( t_{PSKCD} )</td>
<td>25</td>
<td>6</td>
<td>12 ns</td>
</tr>
<tr>
<td>Opposing Directional(^3)</td>
<td>( t_{PSKOD} )</td>
<td>30</td>
<td>6</td>
<td>15 ns</td>
</tr>
<tr>
<td>Jitter</td>
<td></td>
<td>2</td>
<td>2</td>
<td>ns</td>
</tr>
</tbody>
</table>

1 \( t_{PSK} \) is the magnitude of the worst-case difference in \( t_{PHL} \) or \( t_{PLH} \) that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

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Table 5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>1 Mbps—A and C Grades</th>
<th>25 Mbps—C Grade</th>
<th>Test Conditions/Comments</th>
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<tr>
<td>ADuM7640</td>
<td>( I_{DD1} )</td>
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<td>( I_{DD2} )</td>
<td>3.3 4.3</td>
<td>7.2 8.7</td>
<td>mA</td>
</tr>
<tr>
<td>ADuM7641</td>
<td>( I_{DD1} )</td>
<td>3.9 4.9</td>
<td>27 33</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>( I_{DD2} )</td>
<td>3.4 4.2</td>
<td>11 13</td>
<td>mA</td>
</tr>
<tr>
<td>ADuM7642</td>
<td>( I_{DD1} )</td>
<td>3.7 4.7</td>
<td>23 27</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td>( I_{DD2} )</td>
<td>3.5 4.4</td>
<td>14 16</td>
<td>mA</td>
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<tr>
<td>ADuM7643</td>
<td>( I_{DD1} )</td>
<td>3.5 4.4</td>
<td>18 21</td>
<td>mA</td>
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<td></td>
<td>( I_{DD2} )</td>
<td>3.6 4.5</td>
<td>16 20</td>
<td>mA</td>
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### Table 6.

<table>
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<tr>
<th>Parameter</th>
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<tr>
<td>Input Voltage Threshold</td>
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</tr>
<tr>
<td>Logic High</td>
<td>$V_{IH}$</td>
<td>0.7 $V_{DDx}$</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic Low</td>
<td>$V_{IL}$</td>
<td>0.3 $V_{DDx}$</td>
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<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltages</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Logic High</td>
<td>$V_{OH}$</td>
<td>$V_{DDx} - 0.2$</td>
<td>3.3</td>
<td></td>
<td>V</td>
<td>$I_{Ox} = -20 \mu A, V_{Ix} = V_{IH}$</td>
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<td></td>
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<td>$V_{DDx} - 0.5$</td>
<td>3.1</td>
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<td>V</td>
<td>$I_{Ox} = -4 mA, V_{Ix} = V_{IH}$</td>
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<td>Logic Low</td>
<td>$V_{OL}$</td>
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<td>0.1</td>
<td>0.2</td>
<td>V</td>
<td>$I_{Ox} = 20 \mu A, V_{Ix} = V_{IL}$</td>
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<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>0.4</td>
<td>V</td>
<td>$I_{Ox} = 4 mA, V_{Ix} = V_{IL}$</td>
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<td>Input Current per Channel</td>
<td>$I_i$</td>
<td>-10</td>
<td>+0.01</td>
<td>+10</td>
<td>$\mu A$</td>
<td>0 V $\leq V_{Ix} \leq V_{DDx}$</td>
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<tr>
<td>Supply Current per Channel</td>
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<tr>
<td>Quiescent Supply Current</td>
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<tr>
<td>Output</td>
<td>$I_{DDO(Q)}$</td>
<td>0.55</td>
<td>0.72</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Dynamic Supply Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td>$I_{DDI(D)}$</td>
<td>0.19</td>
<td></td>
<td></td>
<td>mA/Mbps</td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td>$I_{DDO(D)}$</td>
<td>0.03</td>
<td></td>
<td></td>
<td>mA/Mbps</td>
<td></td>
</tr>
<tr>
<td><strong>AC SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Rise/Fall Time</td>
<td>$t_{Rs/Tr}$</td>
<td>2.8</td>
<td></td>
<td></td>
<td>ns</td>
<td>10% to 90%</td>
</tr>
<tr>
<td>Common-Mode Transient Immunity(^1)</td>
<td>$</td>
<td>CM</td>
<td>$</td>
<td>15</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>Refresh Rate</td>
<td>$f_r$</td>
<td>550</td>
<td></td>
<td></td>
<td>kHz</td>
<td>DC data inputs</td>
</tr>
</tbody>
</table>

\(^1\) $|CM|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{CL} < 0.8 V_{DDx}$ or $V_{CM} > 0.7 \times V_{DDx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.
### ELECTRICAL CHARACTERISTICS—MIXED 5 V/3.3 V OPERATION

All typical specifications are at \( T_A = 25°C \), \( \text{VDD1} = 5 \text{ V} \), \( \text{VDD2} = 3.3 \text{ V} \). Minimum/maximum specifications apply over the entire recommended operation range of \( 4.5 \text{ V} \leq \text{VDD1} \leq 5.5 \text{ V} \), \( 3.0 \text{ V} \leq \text{VDD2} \leq 3.6 \text{ V} \), and \( -40°C \leq T_A \leq +105°C \), unless otherwise noted. Switching specifications are tested with \( C_L = 15 \text{ pF} \) and CMOS signal levels, unless otherwise noted.

#### Table 7.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>A Grade</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SWITCHING SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width</td>
<td>PW</td>
<td></td>
<td>250</td>
<td>40</td>
<td></td>
<td>ns</td>
<td>Within PWD limit</td>
</tr>
<tr>
<td>Data Rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>( t_{PHL}, t_{PLH} )</td>
<td></td>
<td>80</td>
<td>30</td>
<td>58</td>
<td>ns</td>
<td>Within PWD limit</td>
</tr>
<tr>
<td>Pulse Width Distortion</td>
<td>PWD</td>
<td></td>
<td>25</td>
<td>2</td>
<td>6</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Change vs. Temperature</td>
<td>( t_{PSK} )</td>
<td></td>
<td>5</td>
<td>3</td>
<td></td>
<td>ps/°C</td>
<td></td>
</tr>
<tr>
<td>Propagation Delay Skew(^1)</td>
<td>( t_{PSKCD} )</td>
<td></td>
<td>25</td>
<td>5</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Channel Matching</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Codirectional(^2)</td>
<td>( t_{PSKCD} )</td>
<td></td>
<td>25</td>
<td>5</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Opposing Directional(^3)</td>
<td>( t_{PSKOD} )</td>
<td></td>
<td>30</td>
<td>8</td>
<td>15</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Jitter</td>
<td></td>
<td></td>
<td>2</td>
<td>2</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) \( t_{PSK} \) is the magnitude of the worst-case difference in \( t_{PHL} \) or \( t_{PLH} \) that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

\(^2\) Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

\(^3\) Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposite sides of the isolation barrier.

#### Table 8.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>1 Mbps—A, C Grades</th>
<th>25 Mbps—C Grade</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADuM7640</td>
<td>( I_{DD1} )</td>
<td>5.7</td>
<td>7.0</td>
<td>44</td>
<td>54</td>
</tr>
<tr>
<td></td>
<td>( I_{DD2} )</td>
<td>3.3</td>
<td>4.1</td>
<td>38</td>
<td>46</td>
</tr>
<tr>
<td>ADuM7641</td>
<td>( I_{DD1} )</td>
<td>5.4</td>
<td>6.8</td>
<td>38</td>
<td>46</td>
</tr>
<tr>
<td></td>
<td>( I_{DD2} )</td>
<td>3.4</td>
<td>4.0</td>
<td>11</td>
<td>13</td>
</tr>
<tr>
<td>ADuM7642</td>
<td>( I_{DD1} )</td>
<td>5.1</td>
<td>6.3</td>
<td>31</td>
<td>38</td>
</tr>
<tr>
<td></td>
<td>( I_{DD2} )</td>
<td>3.5</td>
<td>4.3</td>
<td>14</td>
<td>16</td>
</tr>
<tr>
<td>ADuM7643</td>
<td>( I_{DD1} )</td>
<td>4.8</td>
<td>6.0</td>
<td>24</td>
<td>30</td>
</tr>
<tr>
<td></td>
<td>( I_{DD2} )</td>
<td>3.6</td>
<td>4.3</td>
<td>16</td>
<td>20</td>
</tr>
</tbody>
</table>

#### Table 9.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic High</td>
<td>( V_{IH} )</td>
<td>0.7 ( V_{DDx} )</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic Low</td>
<td>( V_{IL} )</td>
<td>0.3 ( V_{DDx} )</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output Voltages</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic High</td>
<td>( V_{OH} )</td>
<td>( V_{DDx} − 0.1 ) ( V_{DDx} )</td>
<td></td>
<td></td>
<td>V</td>
<td>( I_{OH} = -20 \mu A, V_{OH} = V_{ILH} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_{DDx} − 0.5 ) ( V_{DDx} )</td>
<td></td>
<td></td>
<td>V</td>
<td>( I_{OH} = -4 \mu A, V_{OH} = V_{ILH} )</td>
</tr>
<tr>
<td>Logic Low</td>
<td>( V_{OL} )</td>
<td>0.0</td>
<td>0.1</td>
<td></td>
<td>V</td>
<td>( I_{OL} = 20 \mu A, V_{OL} = V_{IL} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>0.4</td>
<td></td>
<td>V</td>
<td>( I_{OL} = 4 \mu A, V_{OL} = V_{IL} )</td>
</tr>
<tr>
<td>Input Current per Channel</td>
<td>( I_i )</td>
<td>-10</td>
<td>+0.01</td>
<td>+10</td>
<td>\mu A</td>
<td>0 V ≤ ( V_i ) ≤ ( V_{DDx} )</td>
</tr>
</tbody>
</table>

#### AC SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Rise/Fall Time</td>
<td>( t_{r} )/( t_{f} )</td>
<td>2.5</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Common-Mode Transient Immunity(^1)</td>
<td>(</td>
<td>CM</td>
<td>)</td>
<td>15</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>Refresh Rate</td>
<td>( f_r )</td>
<td>600</td>
<td></td>
<td></td>
<td>kHz</td>
<td>DC data inputs</td>
</tr>
</tbody>
</table>

\(^1\) \( |CM| \) is the maximum common-mode voltage slew rate that can be sustained while maintaining \( V_{OL} < 0.8 V_{DDx} \) or \( V_{OL} > 0.7 \times V_{DDx} \). The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.
**ADuM7640/ADuM7641/ADuM7642/ADuM7643 Data Sheet**

**ELECTRICAL CHARACTERISTICS—MIXED 3.3 V/5 V OPERATION**

All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{DD1} = 3.3$ V, $V_{DD2} = 5$ V. Minimum/maximum specifications apply over the entire recommended operation range of $3.0$ V $\leq V_{DD1} \leq 3.6$ V, $4.5$ V $\leq V_{DD2} \leq 5.5$ V, and $-40^\circ\text{C} \leq T_A \leq +105^\circ\text{C}$, unless otherwise noted. Switching specifications are tested with $C_L = 15$ pF and CMOS signal levels, unless otherwise noted.

**Table 10.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>A Grade</th>
<th>C Grade</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SWITCHING SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width</td>
<td>PW</td>
<td>250</td>
<td>40</td>
<td>ns</td>
<td>Within PWD limit</td>
</tr>
<tr>
<td>Data Rate</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Propagation Delay</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Change vs. Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Propagation Delay Skew1</td>
<td>tPSK</td>
<td>20</td>
<td>14</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Channel Matching</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Codirectional2</td>
<td>tPSKCD</td>
<td>25</td>
<td>6</td>
<td>13</td>
<td>ns</td>
</tr>
<tr>
<td>Opposing Directional3</td>
<td>tPSKOD</td>
<td>30</td>
<td>9</td>
<td>18</td>
<td>ns</td>
</tr>
<tr>
<td>Jitter</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 $t_{PSK}$ is the magnitude of the worst-case difference in $t_{PHL}$ or $t_{PLH}$ that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

2 Codirectional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on the same side of the isolation barrier.

3 Opposing directional channel matching is the absolute value of the difference in propagation delays between any two channels with inputs on opposite sides of the isolation barrier.

**Table 11.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>1 Mbps—A, C Grades</th>
<th>25 Mbps—C Grade</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUPPLY CURRENT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADuM7640</td>
<td>$I_{DD1}$</td>
<td>4.1</td>
<td>4.9</td>
<td>32</td>
<td>38 mA</td>
</tr>
<tr>
<td></td>
<td>$I_{DD2}$</td>
<td>4.5</td>
<td>5.9</td>
<td>11</td>
<td>13 mA</td>
</tr>
<tr>
<td>ADuM7641</td>
<td>$I_{DD1}$</td>
<td>3.9</td>
<td>4.7</td>
<td>27</td>
<td>33 mA</td>
</tr>
<tr>
<td></td>
<td>$I_{DD2}$</td>
<td>4.6</td>
<td>5.7</td>
<td>15</td>
<td>19 mA</td>
</tr>
<tr>
<td>ADuM7642</td>
<td>$I_{DD1}$</td>
<td>3.7</td>
<td>4.4</td>
<td>23</td>
<td>27 mA</td>
</tr>
<tr>
<td></td>
<td>$I_{DD2}$</td>
<td>4.8</td>
<td>6.0</td>
<td>19</td>
<td>24 mA</td>
</tr>
<tr>
<td>ADuM7643</td>
<td>$I_{DD1}$</td>
<td>3.5</td>
<td>4.2</td>
<td>18</td>
<td>21 mA</td>
</tr>
<tr>
<td></td>
<td>$I_{DD2}$</td>
<td>5.0</td>
<td>6.2</td>
<td>22</td>
<td>29 mA</td>
</tr>
</tbody>
</table>

**Table 12.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC SPECIFICATIONS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic High</td>
<td>$V_{IH}$</td>
<td>0.7 $V_{DDx}$</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Logic Low</td>
<td>$V_{IL}$</td>
<td></td>
<td></td>
<td>0.3 $V_{DDx}$</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Voltages</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic High</td>
<td>$V_{OH}$</td>
<td>$V_{DDx} - 0.1$</td>
<td>$V_{DDx}$</td>
<td></td>
<td>V</td>
<td>$I_{OH} = -20 \mu A, V_{Ix} = V_{IH}$</td>
</tr>
<tr>
<td></td>
<td>$V_{OL}$</td>
<td>$V_{DDx} - 0.5$</td>
<td>$V_{DDx} - 0.2$</td>
<td></td>
<td>V</td>
<td>$I_{OL} = -4 mA, V_{Ix} = V_{IL}$</td>
</tr>
<tr>
<td>Logic Low</td>
<td>$V_{OL}$</td>
<td>0.0</td>
<td>0.1</td>
<td></td>
<td>V</td>
<td>$I_{OL} = 20 \mu A, V_{Ix} = V_{OL}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.2</td>
<td>0.4</td>
<td></td>
<td>V</td>
<td>$I_{OL} = 4 mA, V_{Ix} = V_{OL}$</td>
</tr>
<tr>
<td>Input Current per Channel</td>
<td>$I_i$</td>
<td>-10</td>
<td>+0.01</td>
<td>+10</td>
<td>$\mu A$</td>
<td>0 V $\leq V_{Ix} \leq V_{DDx}$</td>
</tr>
</tbody>
</table>

**AC SPECIFICATIONS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Rise/Fall Time</td>
<td>$t_{r/f}$</td>
<td>2.5</td>
<td></td>
<td></td>
<td>ns</td>
<td>10% to 90%</td>
</tr>
<tr>
<td>Common-Mode Transient Immunity1</td>
<td>$</td>
<td>CM</td>
<td>$</td>
<td>15</td>
<td>20</td>
<td></td>
</tr>
<tr>
<td>Refresh Rate</td>
<td>$f_r$</td>
<td>550</td>
<td></td>
<td></td>
<td>kHz</td>
<td>DC data inputs</td>
</tr>
</tbody>
</table>

1 $|CM|$ is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OL} < 0.8 V_{DDLx}$ or $V_{OH} > 0.7 \times V_{DDIx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.
Table 13.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance (Input to Output)¹</td>
<td>R&lt;sub&gt;I-O&lt;/sub&gt;</td>
<td>10&lt;sup&gt;13&lt;/sup&gt;</td>
<td>11</td>
<td>13</td>
<td>Ω</td>
<td>f = 1 MHz</td>
</tr>
<tr>
<td>Capacitance (Input to Output)¹</td>
<td>C&lt;sub&gt;I-O&lt;/sub&gt;</td>
<td>2</td>
<td>2</td>
<td>4.0</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Input Capacitance²</td>
<td>C&lt;sub&gt;I&lt;/sub&gt;</td>
<td>4.0</td>
<td>4.0</td>
<td>6.0</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>IC Junction-to-Ambient Thermal Resistance</td>
<td>θ&lt;sub&gt;JA&lt;/sub&gt;</td>
<td>76</td>
<td>76</td>
<td>76</td>
<td>°C/W</td>
<td>Thermocouple located at center of package underside</td>
</tr>
</tbody>
</table>

¹ The device is considered a 2-terminal device: Pin 1 through Pin 10 are shorted together, and Pin 11 through Pin 20 are shorted together.
² Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM7640/ADuM7641/ADuM7642/ADuM7643 are approved by the organizations listed in Table 14. See Table 18 and the Insulation Lifetime section for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 14.

UL (Pending)

Recognized Under UL 1577 Component Recognition Program¹
Single Protection, 1000 V rms Isolation Voltage
File E274400

¹ In accordance with UL 1577, each ADuM7640/ADuM7641/ADuM7642/ADuM7643 is proof tested by applying an insulation test voltage ≥ 1200 V rms for 1 sec (current leakage detection limit = 5 µA).

INSULATION AND SAFETY RELATED SPECIFICATIONS

Table 15.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Dielectric Insulation Voltage</td>
<td>L(I01)</td>
<td>1000</td>
<td>V rms</td>
<td>1 minute duration</td>
</tr>
<tr>
<td>Minimum External Air Gap (Clearance)</td>
<td>L(I01)</td>
<td>3.8</td>
<td>mm min</td>
<td>Measured from input terminals to output terminals, shortest distance through air</td>
</tr>
<tr>
<td>Minimum External Tracking (Creepage)</td>
<td>L(I02)</td>
<td>2.8</td>
<td>mm min</td>
<td>Measured from input terminals to output terminals, shortest distance path along body</td>
</tr>
<tr>
<td>Minimum Internal Gap (Internal Clearance)</td>
<td>CTI</td>
<td>&gt;400</td>
<td>µm min</td>
<td>Insulation distance through insulation</td>
</tr>
<tr>
<td>Tracking Resistance (Comparative Tracking Index)</td>
<td>CTI</td>
<td>400</td>
<td>V</td>
<td>DIN IEC 112/VDE 0303 Part 1</td>
</tr>
<tr>
<td>Isolation Group</td>
<td></td>
<td>II</td>
<td></td>
<td>Material Group (DIN VDE 0110, 1/89, Table 1)</td>
</tr>
</tbody>
</table>

Figure 5. Thermal Derating Curve, Dependence of Safety-Limiting Values on Case Temperature per DIN V VDE V 0884-10

Figure 6. Power Dissipation due to Safety-Limiting Values for Specific Case Temperature Values

RECOMMENDED OPERATING CONDITIONS

Table 16.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature</td>
<td>T&lt;sub&gt;A&lt;/sub&gt;</td>
<td>−40</td>
<td>+105</td>
<td>°C</td>
</tr>
<tr>
<td>Supply Voltages¹</td>
<td>V&lt;sub&gt;DD1&lt;/sub&gt;, V&lt;sub&gt;DD2&lt;/sub&gt;</td>
<td>3.0</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Input Signal Rise and Fall Times</td>
<td></td>
<td></td>
<td>1.0</td>
<td>ms</td>
</tr>
</tbody>
</table>

¹ All voltages are relative to their respective grounds. See the DC Correctness section for information about immunity to external magnetic fields.
ABSOLUTE MAXIMUM RATINGS

TA = 25°C, unless otherwise noted.

Table 17.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature (TST) Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Ambient Operating Temperature (TA)</td>
<td>−40°C to +105°C</td>
</tr>
<tr>
<td>Supply Voltages (VDD1, VDD2)</td>
<td>−0.5 V to +7.0 V</td>
</tr>
<tr>
<td>Input Voltages (VIA, VIB, VIC, VID, VIE, VIF)</td>
<td>−0.5 V to VDDI + 0.5 V</td>
</tr>
<tr>
<td>Output Voltages (VOA, VOB, VOC, VOD, VIE, VIF)</td>
<td>−0.5 V to VDDO + 0.5 V</td>
</tr>
<tr>
<td>Average Output Current per Pin1</td>
<td>−10 mA to +10 mA</td>
</tr>
<tr>
<td>Side 1 (IO1)</td>
<td>−10 mA to +10 mA</td>
</tr>
<tr>
<td>Common-Mode Transients3</td>
<td>−100 kV/µs to +100 kV/µs</td>
</tr>
</tbody>
</table>

1 VDDI and VDDO refer to the supply voltages on the input and output sides of a given channel, respectively. See the Printed Circuit Board Layout section.
2 See Figure 5 for maximum rated current values for various temperatures.
3 Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

Table 18. Maximum Continuous Working Voltage1

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max</th>
<th>Unit</th>
<th>Constraint</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Voltage, Bipolar Waveform</td>
<td>420</td>
<td>V peak</td>
<td>50-year minimum lifetime</td>
</tr>
<tr>
<td>AC Voltage, Unipolar Waveform Basic Insulation</td>
<td>420</td>
<td>V peak</td>
<td>50-year minimum lifetime</td>
</tr>
<tr>
<td>DC Voltage Basic Insulation</td>
<td>420</td>
<td>V peak</td>
<td>50-year minimum lifetime</td>
</tr>
</tbody>
</table>

1 Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.

Table 19. Truth Table (Positive Logic)

<table>
<thead>
<tr>
<th>Vx, Input1</th>
<th>VDDO State2</th>
<th>VDDO State3</th>
<th>Vx Output4</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>H</td>
<td>Powered</td>
<td>Powered</td>
<td>H</td>
<td>Normal operation; data is high.</td>
</tr>
<tr>
<td>L</td>
<td>Powered</td>
<td>Powered</td>
<td>L</td>
<td>Normal operation; data is low.</td>
</tr>
<tr>
<td>X</td>
<td>Unpowered</td>
<td>Powered</td>
<td>H</td>
<td>Input unpowered. Output pins are in the default high state. Outputs return to input state within 1.6 µs of VDDO power restoration. See the pin function descriptions (Table 20 through Table 23) for more information.</td>
</tr>
<tr>
<td>X</td>
<td>Powered</td>
<td>Unpowered</td>
<td>Z</td>
<td>Output unpowered. Output pins are in high impedance state. Outputs return to input state within 1.6 µs of VDDO power restoration. See the pin function descriptions (Table 20 through Table 23) for more information.</td>
</tr>
</tbody>
</table>

1 Vx and VDDO refer to the input and output signals of a given channel (A, B, C, D, E or F).
2 VDDO refers to the supply voltage on the input side of a given channel (A, B, C, D, E or F).
3 VDDO refers to the supply voltage on the output side of a given channel (A, B, C, D, E or F).
**PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS**

**Table 20. ADuM7640 Pin Function Descriptions**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD1A</td>
<td>Supply Voltage A for Isolator Side 1 (3.0 V to 5.5 V). Pin 1 must be connected externally to Pin 7. Connect a 0.01 µF to 0.1 µF between VDD1A (Pin 1) and GND1 (Pin 2).</td>
</tr>
<tr>
<td>2</td>
<td>GND1*</td>
<td>Ground Reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>3</td>
<td>VA</td>
<td>Logic Input A.</td>
</tr>
<tr>
<td>4</td>
<td>VB</td>
<td>Logic Input B.</td>
</tr>
<tr>
<td>5</td>
<td>VC</td>
<td>Logic Input C.</td>
</tr>
<tr>
<td>6</td>
<td>VD</td>
<td>Logic Input D.</td>
</tr>
<tr>
<td>7</td>
<td>VDD1B</td>
<td>Supply Voltage B for Isolator Side 1 (3.0 V to 5.5 V). Pin 7 must be connected externally to Pin 1. Connect a 0.01 µF to 0.1 µF between VDD1B (Pin 7) and GND1 (Pin 10).</td>
</tr>
<tr>
<td>8</td>
<td>VE</td>
<td>Logic Input E.</td>
</tr>
<tr>
<td>9</td>
<td>VF</td>
<td>Logic Input F.</td>
</tr>
<tr>
<td>10</td>
<td>GND1*</td>
<td>Ground Reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>11</td>
<td>GND2*</td>
<td>Ground Reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>12</td>
<td>VO</td>
<td>Logic Output F.</td>
</tr>
<tr>
<td>13</td>
<td>VE</td>
<td>Logic Output E.</td>
</tr>
<tr>
<td>14</td>
<td>VDD2B</td>
<td>Supply Voltage B for Isolator Side 2 (3.0 V to 5.5 V). Pin 14 must be connected externally to Pin 20. Connect a 0.01 µF to 0.1 µF between VDD2B (Pin 14) and GND2 (Pin 11).</td>
</tr>
<tr>
<td>15</td>
<td>VD</td>
<td>Logic Output D.</td>
</tr>
<tr>
<td>16</td>
<td>VC</td>
<td>Logic Output C.</td>
</tr>
<tr>
<td>17</td>
<td>VB</td>
<td>Logic Output B.</td>
</tr>
<tr>
<td>18</td>
<td>VO</td>
<td>Logic Output A.</td>
</tr>
<tr>
<td>19</td>
<td>GND2*</td>
<td>Ground Reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>20</td>
<td>VDD2A</td>
<td>Supply Voltage A for Isolator Side 2 (3.0 V to 5.5 V). Pin 20 must be connected externally to Pin 14. Connect a 0.01 µF to 0.1 µF between VDD2A (Pin 20) and GND2 (Pin 19).</td>
</tr>
</tbody>
</table>

Reference the AN-1109 Application Note for specific layout guidelines.
*PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED. CONNECTING BOTH PINS TO PCB SIDE 1 GROUND IS RECOMMENDED. PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED. CONNECTING BOTH PINS TO PCB SIDE 2 GROUND IS RECOMMENDED.

**Figure 7. ADuM7641 Pin Configuration**

**Table 21. ADuM7641 Pin Function Descriptions**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD1A</td>
<td>Supply Voltage A for Isolator Side 1 (3.0 V to 5.5 V). Pin 1 must be connected externally to Pin 7. Connect a 0.01 µF to 0.1 µF between VDD1A (Pin 1) and GND1 (Pin 2).</td>
</tr>
<tr>
<td>2</td>
<td>GND1</td>
<td>Ground Reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>3</td>
<td>VA</td>
<td>Logic Input A.</td>
</tr>
<tr>
<td>4</td>
<td>VB</td>
<td>Logic Input B.</td>
</tr>
<tr>
<td>5</td>
<td>VC</td>
<td>Logic Input C.</td>
</tr>
<tr>
<td>6</td>
<td>VG</td>
<td>Logic Input D.</td>
</tr>
<tr>
<td>7</td>
<td>VDD1B</td>
<td>Supply Voltage B for Isolator Side 1 (3.0 V to 5.5 V). Pin 7 must be connected externally to Pin 1. Connect a 0.01 µF to 0.1 µF between VDD1B (Pin 7) and GND1 (Pin 10).</td>
</tr>
<tr>
<td>8</td>
<td>VOE</td>
<td>Logic Output E.</td>
</tr>
<tr>
<td>9</td>
<td>VF</td>
<td>Logic Input F.</td>
</tr>
<tr>
<td>10</td>
<td>GND1</td>
<td>Ground Reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>11</td>
<td>GND2</td>
<td>Ground Reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>12</td>
<td>VOF</td>
<td>Logic Output F.</td>
</tr>
<tr>
<td>13</td>
<td>VE</td>
<td>Logic Input E.</td>
</tr>
<tr>
<td>14</td>
<td>VDD2B</td>
<td>Supply Voltage B for Isolator Side 2 (3.0 V to 5.5 V). Pin 14 must be connected externally to Pin 20. Connect a 0.01 µF to 0.1 µF between VDD2B (Pin 14) and GND2 (Pin 11).</td>
</tr>
<tr>
<td>15</td>
<td>VOD</td>
<td>Logic Output D.</td>
</tr>
<tr>
<td>16</td>
<td>VOC</td>
<td>Logic Output C.</td>
</tr>
<tr>
<td>17</td>
<td>VOB</td>
<td>Logic Output B.</td>
</tr>
<tr>
<td>18</td>
<td>VOA</td>
<td>Logic Output A.</td>
</tr>
<tr>
<td>19</td>
<td>GND2</td>
<td>Ground Reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>20</td>
<td>VDD2A</td>
<td>Supply Voltage A for Isolator Side 2 (3.0 V to 5.5 V). Pin 20 must be connected externally to Pin 14. Connect a 0.01 µF to 0.1 µF between VDD2A (Pin 20) and GND2 (Pin 19).</td>
</tr>
</tbody>
</table>

Reference the AN-1109 Application Note for specific layout guidelines.
*PIN 2 AND PIN 10 ARE INTERNALLY CONNECTED. CONNECTING BOTH PINS TO PCB SIDE 1 GROUND IS RECOMMENDED. PIN 11 AND PIN 19 ARE INTERNALLY CONNECTED. CONNECTING BOTH PINS TO PCB SIDE 2 GROUND IS RECOMMENDED.

Figure 8. ADuM7642 Pin Configuration

Table 22. ADuM7642 Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD1A</td>
<td>Supply Voltage A for Isolator Side 1 (3.0 V to 5.5 V). Pin 1 must be connected externally to Pin 7. Connect a 0.01 µF to 0.1 µF between VDD1A (Pin 1) and GND1 (Pin 2).</td>
</tr>
<tr>
<td>2</td>
<td>GND1</td>
<td>Ground Reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>3</td>
<td>VA</td>
<td>Logic Input A.</td>
</tr>
<tr>
<td>4</td>
<td>VB</td>
<td>Logic Input B.</td>
</tr>
<tr>
<td>5</td>
<td>VC</td>
<td>Logic Input C.</td>
</tr>
<tr>
<td>6</td>
<td>VD</td>
<td>Logic Output D.</td>
</tr>
<tr>
<td>7</td>
<td>VDD1B</td>
<td>Supply Voltage B for Isolator Side 1 (3.0 V to 5.5 V). Pin 7 must be connected externally to Pin 1. Connect a 0.01 µF to 0.1 µF between VDD1B (Pin 7) and GND1 (Pin 10).</td>
</tr>
<tr>
<td>8</td>
<td>VE</td>
<td>Logic Output E.</td>
</tr>
<tr>
<td>9</td>
<td>VF</td>
<td>Logic Input F.</td>
</tr>
<tr>
<td>10</td>
<td>GND1</td>
<td>Ground Reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>11</td>
<td>GND2</td>
<td>Ground Reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>12</td>
<td>VO</td>
<td>Logic Output F.</td>
</tr>
<tr>
<td>13</td>
<td>VE</td>
<td>Logic Input E.</td>
</tr>
<tr>
<td>14</td>
<td>VDD2B</td>
<td>Supply Voltage B for Isolator Side 2 (3.0 V to 5.5 V). Pin 14 must be connected externally to Pin 20. Connect a 0.01 µF to 0.1 µF between VDD2B (Pin 14) and GND2 (Pin 11).</td>
</tr>
<tr>
<td>15</td>
<td>VD</td>
<td>Logic Input D.</td>
</tr>
<tr>
<td>16</td>
<td>VC</td>
<td>Logic Output C.</td>
</tr>
<tr>
<td>17</td>
<td>VB</td>
<td>Logic Output B.</td>
</tr>
<tr>
<td>18</td>
<td>VO</td>
<td>Logic Output A.</td>
</tr>
<tr>
<td>19</td>
<td>GND2</td>
<td>Ground Reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>20</td>
<td>VDD2A</td>
<td>Supply Voltage A for Isolator Side 2 (3.0 V to 5.5 V). Pin 20 must be connected externally to Pin 14. Connect a 0.01 µF to 0.1 µF between VDD2A (Pin 20) and GND2 (Pin 19).</td>
</tr>
</tbody>
</table>

Reference the AN-1109 Application Note for specific layout guidelines.
**Table 23. ADuM7643 Pin Function Descriptions**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD1A</td>
<td>Supply Voltage A for Isolator Side 1 (3.0 V to 5.5 V). Pin 1 must be connected externally to Pin 7. Connect a 0.01 μF to 0.1 μF between VDD1A (Pin 1) and GND1 (Pin 2).</td>
</tr>
<tr>
<td>2</td>
<td>GND1</td>
<td>Ground Reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>3</td>
<td>VA</td>
<td>Logic Input A.</td>
</tr>
<tr>
<td>4</td>
<td>VB</td>
<td>Logic Input B.</td>
</tr>
<tr>
<td>5</td>
<td>VC</td>
<td>Logic Output C.</td>
</tr>
<tr>
<td>6</td>
<td>VOD</td>
<td>Logic Output D.</td>
</tr>
<tr>
<td>7</td>
<td>VDD1B</td>
<td>Supply Voltage B for Isolator Side 1 (3.0 V to 5.5 V). Pin 7 must be connected externally to Pin 1. Connect a 0.01 μF to 0.1 μF between VDD1B (Pin 7) and GND1 (Pin 10).</td>
</tr>
<tr>
<td>8</td>
<td>VOE</td>
<td>Logic Output E.</td>
</tr>
<tr>
<td>9</td>
<td>VIF</td>
<td>Logic Input F.</td>
</tr>
<tr>
<td>10</td>
<td>GND1</td>
<td>Ground Reference for Isolator Side 1. Pin 2 and Pin 10 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>11</td>
<td>GND2</td>
<td>Ground Reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>12</td>
<td>VOF</td>
<td>Logic Output F.</td>
</tr>
<tr>
<td>13</td>
<td>VIE</td>
<td>Logic Input E.</td>
</tr>
<tr>
<td>14</td>
<td>VDD2A</td>
<td>Supply Voltage A for Isolator Side 2 (3.0 V to 5.5 V). Pin 20 must be connected externally to Pin 14. Connect a 0.01 μF to 0.1 μF between VDD2A (Pin 20) and GND2 (Pin 19).</td>
</tr>
<tr>
<td>15</td>
<td>VD</td>
<td>Logic Input D.</td>
</tr>
<tr>
<td>16</td>
<td>VC</td>
<td>Logic Input C.</td>
</tr>
<tr>
<td>17</td>
<td>VOB</td>
<td>Logic Output B.</td>
</tr>
<tr>
<td>18</td>
<td>VOA</td>
<td>Logic Output A.</td>
</tr>
<tr>
<td>19</td>
<td>GND2</td>
<td>Ground Reference for Isolator Side 2. Pin 11 and Pin 19 are internally connected, and connecting both pins to the PCB ground plane is recommended.</td>
</tr>
<tr>
<td>20</td>
<td>VDD2B</td>
<td>Supply Voltage B for Isolator Side 2 (3.0 V to 5.5 V). Pin 14 must be connected externally to Pin 20. Connect a 0.01 μF to 0.1 μF between VDD2B (Pin 14) and GND2 (Pin 11).</td>
</tr>
</tbody>
</table>

Reference the AN-1109 Application Note for specific layout guidelines.
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 10. Typical Supply Current per Input Channel vs. Data Rate for 5 V and 3.3 V Operation

Figure 11. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (No Output Load)

Figure 12. Typical Supply Current per Output Channel vs. Data Rate for 5 V and 3.3 V Operation (15 pF Output Load)

Figure 13. Typical ADuM7640 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation

Figure 14. Typical ADuM7640 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation

Figure 15. Typical ADuM7641 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation
Figure 16. Typical ADuM7641 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation

Figure 17. Typical ADuM7642 $V_{DD1}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation

Figure 18. Typical ADuM7642 $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation

Figure 19. Typical ADuM7643 $V_{DD1}$ or $V_{DD2}$ Supply Current vs. Data Rate for 5 V and 3.3 V Operation
APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD LAYOUT

The ADuM7640/ADuM7641/ADuM7642/ADuM7643 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at the input and output supply pins (see Figure 20). Connect four bypass capacitors between Pin 1 and Pin 2 for VDD1A, between Pin 7 and Pin 10 for VDD1B, between Pin 11 and Pin 14 for VDD2B, and between Pin 19 and Pin 20 for VDD2A. Connect the VDD1A supply pin and the VDD2B supply pin together, and connect the VDD2A supply pin and the VDD1A supply pin together. The capacitor values should be from 0.01 µF to 0.1 µF. The total lead length between both ends of the capacitor and the power supply pin should not exceed 20 mm.

In applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, users should design the board layout so that any coupling that occurs affects all pins equally on a given component side. Failure to follow this design guideline can cause voltage differentials between pins that exceed the absolute maximum ratings of the device, which can lead to latch-up or permanent damage.

With proper PCB design choices, the ADuM7640/ADuM7641/ADuM7642/ADuM7643 can readily meet CISPR 22 Class A (and FCC Class A) emissions standards, as well as the more stringent CISPR 22 Class B (and FCC Class B) standards in an unshielded environment. For PCB-related EMI mitigation techniques, including board layout and stack-up issues, see the AN-1109 Application Note.

PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition may differ from the propagation delay time for a low-to-high transition.

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount of time that the propagation delay differs between channels within a single ADuM7640/ADuM7641/ADuM7642/ADuM7643 component.

Propagation delay skew refers to the maximum amount of time that the propagation delay differs between multiple ADuM7640/ADuM7641/ADuM7642/ADuM7643 components operating under the same conditions.

DC CORRECTNESS

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder using the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. In the absence of logic transitions at the input for more than ~1 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses for more than approximately 5 µs, the input side is assumed to be unpowered or nonfunctional, in which case the isolator output is forced to a default high state by the watchdog timer circuit.
MAGNETIC FIELD IMMUNITY

The magnetic field immunity of the ADuM7640/ADuM7641/ADuM7642/ADuM7643 is determined by the changing magnetic field, which induces a voltage in the transformer receiving coil large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3 V operating condition of the ADuM7640/ADuM7641/ADuM7642/ADuM7643 is examined because it represents the most susceptible mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

\[ V = (-\frac{d\beta}{dt}) \sum \pi r_n^2; \quad n = 1, 2, \ldots, N \]

where:
- \( \beta \) is magnetic flux density (gauss).
- \( r_n \) is the radius of the \( n \)th turn in the receiving coil (cm).
- \( N \) is the total number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM7640/ADuM7641/ADuM7642/ADuM7643 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 22.

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is of the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM7640/ADuM7641/ADuM7642/ADuM7643 transformers. Figure 23 shows these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 23, the ADuM7640/ADuM7641/ADuM7642/ADuM7643 are extremely immune and can be affected only by extremely large currents operated at high frequency very close to the component. For the 1 MHz example noted previously, a 1.2 kA current would have to be placed 5 mm away from the ADuM7640/ADuM7641/ADuM7642/ADuM7643 to affect the operation of the component.

Note that at combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces can induce error voltages sufficiently large to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.
POWER CONSUMPTION

The supply current at a given channel of the ADuM7640/ADuM7641/ADuM7642/ADuM7643 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

\[ I_{DDI} = I_{DDI(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO} \times (2f - f_i) + I_{DDI(Q)} \]

where:
- \( I_{DDI(D)} \) and \( I_{DDO(D)} \) are the input and output dynamic supply currents per channel (mA/Mbps).
- \( I_{DDI(Q)} \) and \( I_{DDO(Q)} \) are the specified input and output quiescent supply currents (mA).
- \( f \) is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.
- \( f_i \) is the input stage refresh rate (Mbps).
- \( C_L \) is the output load capacitance (pF).
- \( V_{DDO} \) is the output supply voltage (V).

To calculate the total supply current, the supply currents for each input and output channel corresponding to \( V_{DDI} \) and \( V_{DDO} \) are calculated and totaled. Figure 10 and Figure 11 show per-channel supply currents as a function of data rate for an unloaded output condition. Figure 12 shows the per-channel supply current as a function of data rate for a 15 pF output condition. Figure 13 through Figure 17 show the total supply current as a function of data rate for ADuM7640/ADuM7641/ADuM7642/ADuM7643 channel configurations.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM7640/ADuM7641/ADuM7642/ADuM7643 components.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 18 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.
OUTLINE DIMENSIONS

Figure 27. 20-Lead Shrink Small Outline Package [QSOP] (RQ-20)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Number of Inputs, V_{DD} Side</th>
<th>Number of Inputs, V_{SS} Side</th>
<th>Maximum Data Rate</th>
<th>Maximum Propagation Delay, 5 V</th>
<th>Maximum Pulse Width Distortion</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
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<tbody>
<tr>
<td>ADuM7640ARQZ/ADuM7640ARQZ-RL7</td>
<td>6</td>
<td>0</td>
<td>1 Mbps</td>
<td>20 ns</td>
<td>75 ns</td>
<td>−40°C to +105°C</td>
<td>20-Lead QSOP</td>
<td>RQ-20</td>
</tr>
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<td>14 ns</td>
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<td>RQ-20</td>
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<td>20 ns</td>
<td>75 ns</td>
<td>−40°C to +105°C</td>
<td>20-Lead QSOP</td>
<td>RQ-20</td>
</tr>
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<td>25 Mbps</td>
<td>14 ns</td>
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<td>−40°C to +105°C</td>
<td>20-Lead QSOP</td>
<td>RQ-20</td>
</tr>
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<td>2</td>
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<td>75 ns</td>
<td>−40°C to +105°C</td>
<td>20-Lead QSOP</td>
<td>RQ-20</td>
</tr>
<tr>
<td>ADuM7642CRQZ/ADuM7642CRQZ-RL7</td>
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<td>2</td>
<td>25 Mbps</td>
<td>14 ns</td>
<td>50 ns</td>
<td>−40°C to +105°C</td>
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<td>RQ-20</td>
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<td>3</td>
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<td>20 ns</td>
<td>75 ns</td>
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<td>20-Lead QSOP</td>
<td>RQ-20</td>
</tr>
<tr>
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<td>3</td>
<td>25 Mbps</td>
<td>14 ns</td>
<td>50 ns</td>
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<td>20-Lead QSOP</td>
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1 Z = RoHS Compliant Part.