FEATURES
isoPower integrated isolated high-side supply
275 mW isolated dc-to-dc converter
200 mA output sink current, 200 mA output source current
High common-mode transient immunity: >50 kV/µs
Wide-body 16-lead SOIC package
Safety and regulatory approvals
UL recognition
3750 V rms for 1 minute per UL 1577
CSA Component Acceptance Notice #5A
CSA/IEC 60950-1, 400 V rms
VDE certificate of conformity (pending)
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
$V_{	ext{FORM}} = 560$ V peak

APPLICATIONS
MOSFET/IGBT gate drivers
Motor drives
Solar panel inverters
Power supplies

GENERAL DESCRIPTION
The ADuM6132 is an isolated half-bridge gate driver that employs the Analog Devices, Inc., iCoupler technology to provide an isolated high-side driver with an integrated 275 mW high-side supply. This supply, provided by an internal isolated dc-to-dc converter, powers not only the ADuM6132 high-side output but also any external buffer circuitry that is commonly used with the ADuM6132. This functionality eliminates the cost, space, and performance issues associated with external supply configurations such as a bootstrap circuit.

The architecture of the ADuM6132 isolates the high-side channel and the high-side power from the control and low-side interface circuitry. Care has been taken to ensure close matching between the high-side and low-side driver timing characteristics to reduce the need for a dead time margin.

In comparison to gate drivers that employ high voltage level translation methodologies, the ADuM6132 offers the benefit of true, galvanic isolation. The differential voltage between high-side and low-side channels can be as high as 800 V with good insulation lifetime (see Table 12).

isoPower uses high frequency switching elements to transfer power through its transformer. Special care must be taken during printed circuit board (PCB) layout to meet emissions standards. Refer to the AN-0971 Application Note for information about board layout considerations.

1 Protected by U.S. Patents 5,952,849; 6,873,065; 6,903,578; 7,075,329; and other pending patents.
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### SPECIFICATIONS

#### ELECTRICAL CHARACTERISTICS

All voltages are relative to their respective ground; \(4.5 \text{ V} \leq V_{DD} = V_{DDB} \leq 5.5 \text{ V}; 12.5 \text{ V} \leq V_{DDA} = V_{ISO} \leq 17.0 \text{ V}\). All minimum/maximum specifications apply over the entire recommended operating range, unless otherwise noted. All typical specifications are at \(T_A = 25^\circ\text{C}\), \(V_{DD} = V_{DDB} = 5.0 \text{ V}, V_{DDA} = V_{ISO} = 15 \text{ V}\).

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>DC SPECIFICATIONS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isolated Power Supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current, Quiescent</td>
<td>(I_{DDQ})</td>
<td>280</td>
<td>mA</td>
<td></td>
<td></td>
<td>(I_{ISO} = 0 \text{ mA}, \text{dc signal inputs})</td>
</tr>
<tr>
<td>Input Current, Loaded</td>
<td>(I_{DL})</td>
<td>350</td>
<td>mA</td>
<td></td>
<td></td>
<td>(I_{ISO} = I_{ISO(MAX)})</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>(I_{ISO(MAX)})</td>
<td>22</td>
<td>mA</td>
<td></td>
<td></td>
<td>(12.5 \text{ V} \leq V_{ISO} \leq 17.0 \text{ V})</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>(V_{ISO})</td>
<td>12.5</td>
<td>15</td>
<td>17</td>
<td>V</td>
<td>0 mA (\leq I_{ISO} \leq 22 \text{ mA})</td>
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<tr>
<td>Logic Supply</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current</td>
<td>(I_{DDL})</td>
<td>1.8</td>
<td>3.0</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Supplies, Channel A or Channel B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current, Quiescent</td>
<td>(I_{DDA(0)}, I_{DDB(0)})</td>
<td>1.0</td>
<td>2.0</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current, (f_{IN} = 20 \text{ kHz})</td>
<td>(I_{DDA(20)}, I_{DDB(20)})</td>
<td>1.1</td>
<td>2.1</td>
<td>mA</td>
<td>(C_{L} = 200 \text{ pF})</td>
<td></td>
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<tr>
<td>Supply Current, (f_{IN} = 100 \text{ kHz})</td>
<td>(I_{DDA(100)}, I_{DDB(100)})</td>
<td>1.3</td>
<td>2.3</td>
<td>mA</td>
<td>(C_{L} = 200 \text{ pF})</td>
<td></td>
</tr>
<tr>
<td>Supply Current, (f_{IN} = 1000 \text{ kHz})</td>
<td>(I_{DDA(1000)}, I_{DDB(1000)})</td>
<td>4.5</td>
<td>5.5</td>
<td>mA</td>
<td>(C_{L} = 200 \text{ pF})</td>
<td></td>
</tr>
<tr>
<td>Logic Inputs, Channel A or Channel B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Current</td>
<td>(I_{IA}, I_{IB})</td>
<td>(-10)</td>
<td>+0.01</td>
<td>+10</td>
<td>(\mu\text{A})</td>
<td>(0 \text{ V} \leq V_{IA}, V_{IB} \leq 5.5 \text{ V})</td>
</tr>
<tr>
<td>Logic High Input Voltage</td>
<td>(V_{IAH}, V_{IBH})</td>
<td>(0.7 \times V_{DDL})</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Logic Low Input Voltage</td>
<td>(V_{IAL}, V_{IBL})</td>
<td>(0.3 \times V_{DDL})</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Outputs, Channel A or Channel B</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel A High Level Output Voltage</td>
<td>(V_{DAH})</td>
<td>(V_{DDA} - 0.1)</td>
<td>V</td>
<td>(I_{OAH} = -1 \text{ mA})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel B High Level Output Voltage</td>
<td>(V_{DBH})</td>
<td>(V_{DDB} - 0.1)</td>
<td>V</td>
<td>(I_{OBH} = -1 \text{ mA})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Level Output Voltages</td>
<td>(V_{DAL}, V_{DBL})</td>
<td>0.1</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Level Output Current, Peak</td>
<td>(I_{OAH}, I_{OBH})</td>
<td>200</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low Level Output Current, Peak</td>
<td>(I_{OAL}, I_{OBL})</td>
<td>200</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lockout, (V_{DDA}) or (V_{DDB}) Supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive Going Threshold</td>
<td>(V_{DDAUV+}, V_{DDBUV+})</td>
<td>11.0</td>
<td>11.7</td>
<td>12.3</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Negative Going Threshold</td>
<td>(V_{DDAUV-}, V_{DDBUV-})</td>
<td>10.0</td>
<td>10.7</td>
<td>11.2</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Hysteresis</td>
<td>(V_{DDAUVH}, V_{DDBUVH})</td>
<td>1.0</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lockout, (V_{DDB}) Supply</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive Going Threshold</td>
<td>(V_{DDBHV+})</td>
<td>3.5</td>
<td>4.2</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Negative Going Threshold</td>
<td>(V_{DDBHV-})</td>
<td>3.1</td>
<td>3.8</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Hysteresis</td>
<td>(V_{DDBHVH})</td>
<td>0.5</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### SWITCHING SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
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<tbody>
<tr>
<td>Minimum Pulse Width</td>
<td>(PW)</td>
<td>50</td>
<td>ns</td>
<td></td>
<td>(C_{L} = 200 \text{ pF})</td>
<td></td>
</tr>
<tr>
<td>Maximum Switching Frequency</td>
<td>(f_{IN})</td>
<td>1000</td>
<td>kHz</td>
<td></td>
<td>(C_{L} = 200 \text{ pF})</td>
<td></td>
</tr>
<tr>
<td>Propagation Delay</td>
<td>(t_{PHL}, t_{PLH})</td>
<td>40</td>
<td>60</td>
<td>100</td>
<td>ns</td>
<td>(C_{L} = 200 \text{ pF})</td>
</tr>
<tr>
<td>Change vs. Temperature</td>
<td></td>
<td></td>
<td>100</td>
<td>ps/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pulse Width Distortion, (</td>
<td>t_{PLH} - t_{PHL}</td>
<td>)</td>
<td>(PWD)</td>
<td>10</td>
<td>ns</td>
<td>(C_{L} = 200 \text{ pF})</td>
</tr>
<tr>
<td>Channel-to-Channel Matching, Rising or Falling Matching Edge Polarity</td>
<td>(t_{MQ})</td>
<td>20</td>
<td>ns</td>
<td>(C_{L} = 200 \text{ pF})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Channel-to-Channel Matching, Rising vs. Falling Opposite Edge Polarity</td>
<td>(t_{MT})</td>
<td>20</td>
<td>ns</td>
<td>(C_{L} = 200 \text{ pF})</td>
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</table>
### PACKAGE CHARACTERISTICS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistance (Input Side to High-Side Output)¹</td>
<td>R\textsubscript{i-o}</td>
<td>10\textsuperscript{12}</td>
<td>Ω</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Capacitance (Input Side to High-Side Output)¹</td>
<td>C\textsubscript{i-o}</td>
<td>2.0</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>C\textsubscript{i}</td>
<td>4.0</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Junction-to-Ambient Thermal Resistance</td>
<td>θ\textsubscript{JA}</td>
<td>45</td>
<td>°C/W</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

¹ The device is considered a two-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.

### REGULATORY INFORMATION

<table>
<thead>
<tr>
<th>UL Recognized under UL 1577</th>
<th>CSA Approved under CSA Component Acceptance Notice #5A</th>
<th>VDE (Pending)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Single protection, 3750 V rms isolation voltage</td>
<td>Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V peak) maximum working voltage</td>
<td>Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12²</td>
</tr>
<tr>
<td></td>
<td>Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 250 V rms (354 V peak) maximum working voltage</td>
<td>Reinforced insulation, 560 V peak</td>
</tr>
<tr>
<td>File E214100</td>
<td>File 205078</td>
<td>File 2471900-4880-0001</td>
</tr>
</tbody>
</table>

¹ In accordance with UL 1577, each ADuM6132 is proof-tested by applying an insulation test voltage ≥ 4500 V rms for 1 second (current leakage detection limit = 10 µA).

² In accordance with DIN V VDE V 0884-10, each ADuM6132 is proof-tested by applying an insulation test voltage ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 approval.

### INSULATION AND SAFETY-RELATED SPECIFICATIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Dielectric Insulation Voltage</td>
<td>L(01)</td>
<td>3750</td>
<td>V rms</td>
<td>1 minute duration</td>
</tr>
<tr>
<td>Minimum External Air Gap (Clearance)</td>
<td>L(02)</td>
<td>&gt;8.0</td>
<td>mm</td>
<td>Measured from input terminals to output terminals, shortest distance through air</td>
</tr>
<tr>
<td>Minimum External Tracking (Creepage)</td>
<td>L(02)</td>
<td>&gt;8.0</td>
<td>mm</td>
<td>Measured from input terminals to output terminals, shortest distance path along body</td>
</tr>
<tr>
<td>Minimum Internal Gap (Internal Clearance)</td>
<td>CTI</td>
<td>0.017 min</td>
<td>mm</td>
<td>Insulation distance through insulation</td>
</tr>
<tr>
<td>Tracking Resistance (Comparative Tracking Index)</td>
<td>CTI</td>
<td>&gt;175</td>
<td>V</td>
<td>DIN IEC 112/VDE 0303 Part 1</td>
</tr>
<tr>
<td>Isolation Group</td>
<td></td>
<td>IIIa</td>
<td></td>
<td>Material Group (DIN VDE 0110, 1/89, Table 1)</td>
</tr>
</tbody>
</table>
DIN V VDE V 0884-10 (VDE V 0884-10) INSULATION CHARACTERISTICS

The ADuM6132 is suitable for reinforced electrical isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking on the package denotes DIN V VDE V 0884-10 approval.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions/Comments</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Installation Classification per DIN VDE 0110</td>
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<tr>
<td>For Rated Mains Voltage ≤ 150 V rms</td>
<td>I to IV</td>
<td></td>
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<tr>
<td>For Rated Mains Voltage ≤ 300 V rms</td>
<td>I to III</td>
<td></td>
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<tr>
<td>For Rated Mains Voltage ≤ 400 V rms</td>
<td>I to II</td>
<td>40/105/21</td>
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<tr>
<td>Climatic Classification</td>
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<tr>
<td>Pollution Degree (DIN VDE 0110, Table 1)</td>
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<tr>
<td>Maximum Working Insulation Voltage</td>
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<td>$V_{ORM} = 560$ V peak</td>
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<tr>
<td>Input-to-Output Test Voltage, Method B1</td>
<td>$V_{PR} = 1050$ V peak</td>
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<tr>
<td>Input-to-Output Test Voltage, Method A</td>
<td>After Environmental Tests Subgroup 1</td>
<td>$V_{IORM} = 896$ V peak</td>
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<tr>
<td>After Input and/or Safety Test Subgroup 2</td>
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<td>$V_{IORM} = 672$ V peak</td>
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<tr>
<td>and Subgroup 3</td>
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<tr>
<td>Highest Allowable Overvoltage</td>
<td>Transient overvoltage, $t_{TR} = 10$ sec</td>
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<tr>
<td>Safety-Limiting Values</td>
<td>Maximum value allowed in the event of a failure (see Figure 2)</td>
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<tr>
<td>Case Temperature</td>
<td>$T_s = 150$ °C</td>
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</tr>
<tr>
<td>Side 1 Current</td>
<td>$I_{S1} = 555$ mA</td>
<td></td>
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<tr>
<td>Insulation Resistance at $T_s$</td>
<td>$R_s &gt; 109$ Ω</td>
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</table>

RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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<tbody>
<tr>
<td>Operating Temperature Range, $T_A$</td>
<td>$-40^\circ$C to $+85^\circ$C</td>
</tr>
<tr>
<td>Input Supply Voltage, $V_{DD}$ and $V_{DDL}$</td>
<td>$4.5$ V to $5.5$ V</td>
</tr>
<tr>
<td>Channel A, Channel B Supply Voltage, $V_{DDA}$ and $V_{DDB}$</td>
<td>$12.5$ V to $17$ V</td>
</tr>
<tr>
<td>Input Signal Rise and Fall Times</td>
<td>$1$ ms</td>
</tr>
<tr>
<td>Common-Mode Transient Immunity, Input to Output</td>
<td>$-50$ kV/μs to $+50$ kV/μs</td>
</tr>
<tr>
<td>Minimum Power-On Slew Rate ($P_{SLEW}$), $V_{DD}$ and $V_{DDL}$</td>
<td>$1$ V/ms</td>
</tr>
</tbody>
</table>

1 All voltages are relative to their respective ground.
2 The ADuM6132 power supply may fail to properly initialize if $V_{CC}$ and $V_{CCX}$ are applied too slowly. The power supply slew rate must be faster than specified over the entire turn-on ramp. Power-on should start from a completely discharged state.
### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ$C, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
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<tbody>
<tr>
<td>Storage Temperature Range, $T_{ST}$</td>
<td>$-55^\circ$C to $+150^\circ$C</td>
</tr>
<tr>
<td>Ambient Operating Temperature Range, $T_A$</td>
<td>$-40^\circ$C to $+85^\circ$C</td>
</tr>
<tr>
<td>Input Supply Voltage, $V_{DDL}$, $V_{DD}$</td>
<td>$-0.5$ V to $+7.0$ V</td>
</tr>
<tr>
<td>Channel A, Channel B Supply Voltage, $V_{DDA}$, $V_{DDB}$</td>
<td>$-0.5$ V to $+27$ V</td>
</tr>
<tr>
<td>Input Voltage, $V_{IA}$, $V_{IB}$</td>
<td>$-0.5$ V to $V_{DDL} + 0.5$ V</td>
</tr>
<tr>
<td>Output Voltage, $V_{OA}$</td>
<td>$-0.5$ V to $V_{DD} + 0.5$ V</td>
</tr>
<tr>
<td>Output Voltage, $V_{OB}$</td>
<td>$-0.5$ V to $V_{DDB} + 0.5$ V</td>
</tr>
<tr>
<td>Average DC Output Current, $I_{OA}$, $I_{OB}$</td>
<td>$-10$ mA to $+10$ mA</td>
</tr>
<tr>
<td>Peak Output Current, $I_{OA}$, $I_{OB}$</td>
<td>$-200$ mA to $+200$ mA</td>
</tr>
<tr>
<td>Common-Mode Transients$^2$</td>
<td>$-100$ kV/µs to $+100$ kV/µs</td>
</tr>
</tbody>
</table>

$^1$ All voltages are relative to their respective ground.

$^2$ Refers to common-mode transients across any insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**ESD CAUTION**

*ESD (electrostatic discharge) sensitive device.* Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
Table 8. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VDD</td>
<td>Input Supply Voltage for Isolated Power Supply, 4.5 V to 5.5 V.</td>
</tr>
<tr>
<td>2, 8</td>
<td>GND</td>
<td>Ground Reference for Isolated Power Supply Input and Logic Inputs.</td>
</tr>
<tr>
<td>3</td>
<td>VDDL</td>
<td>Input Supply Voltage for Logic, 4.5 V to 5.5 V.</td>
</tr>
<tr>
<td>4</td>
<td>VIA</td>
<td>Logic Input A.</td>
</tr>
<tr>
<td>5</td>
<td>VIB</td>
<td>Logic Input B.</td>
</tr>
<tr>
<td>6</td>
<td>VOB</td>
<td>Output B (Nonisolated).</td>
</tr>
<tr>
<td>7</td>
<td>VDB</td>
<td>Output B Supply Voltage Input (Nonisolated), 12.5 V to 17 V.</td>
</tr>
<tr>
<td>9, 15</td>
<td>GNDISO</td>
<td>Ground Reference for Isolated Power Supply Output.</td>
</tr>
<tr>
<td>10, 11</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>12</td>
<td>VOA</td>
<td>Output A (Isolated).</td>
</tr>
<tr>
<td>13</td>
<td>VDDA</td>
<td>Output A Supply Voltage Input. Must be connected externally to VISO (Pin 16).</td>
</tr>
<tr>
<td>14</td>
<td>GND_A</td>
<td>Output A Ground Reference. Must be connected externally to GND_ISO (Pin 15).</td>
</tr>
<tr>
<td>16</td>
<td>VISO</td>
<td>Isolated Power Supply Voltage Output.</td>
</tr>
</tbody>
</table>

Table 9. Truth Table (Positive Logic)\(^1\)

<table>
<thead>
<tr>
<th>VIA Input</th>
<th>VIB Input</th>
<th>VDDL State</th>
<th>VDDL State</th>
<th>VOA Output</th>
<th>VOB Output</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>L</td>
<td>L</td>
<td>Powered</td>
<td>Powered</td>
<td>L</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>L</td>
<td>H</td>
<td>Powered</td>
<td>Powered</td>
<td>L</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>L</td>
<td>Powered</td>
<td>Powered</td>
<td>H</td>
<td>L</td>
<td></td>
</tr>
<tr>
<td>H</td>
<td>H</td>
<td>Powered</td>
<td>Powered</td>
<td>H</td>
<td>H</td>
<td></td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>Unpowered</td>
<td>Powered</td>
<td>L</td>
<td>L</td>
<td>VOA returns to input state within 1 μs of VDDL power restoration</td>
</tr>
<tr>
<td>X</td>
<td>X</td>
<td>Powered</td>
<td>Unpowered</td>
<td>L</td>
<td>L</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) L = low; H = high; X = high or low.
TYPICAL PERFORMANCE CHARACTERISTICS

All typical performance curves are based on operation at $T_A = 25^\circ C$, unless otherwise noted.

![Figure 4. Typical $V_{ISO}$ Supply Voltage vs. $I_{ISO}$ External Load](image)

![Figure 7. Typical Total Power Dissipation vs. $I_{ISO}$ External Load](image)

![Figure 5. Typical $I_{ISO}$ Supply Current vs. $I_{ISO}$ External Load](image)

![Figure 8. Typical $V_{ISO}$ Output Voltage at Maximum Combined Load over Temperature](image)

![Figure 6. Typical $V_{ISO}$ Supply Efficiency vs. $I_{ISO}$ External Load](image)

![Figure 9. Power Dissipation vs. Load Impedance for Fault Conditions](image)
Figure 10. Typical $I_{D\text{DA}}$ Supply Current, $C_L = 200\, \text{pF}$

Figure 11. Typical $I_{D\text{DB}}$ Supply Current, $C_L = 200\, \text{pF}$

Figure 12. Typical $V_{\text{OH}}$ Voltage Drop vs. $I_{\text{OL}}$ ($V_{\text{DDA}} = V_{\text{DDB}} = 5\, \text{V}, V_{\text{DDA}} = V_{\text{DDB}} = 12\, \text{V to 17 V}$)

Figure 13. Typical $V_{\text{OL}}$ vs. $I_{\text{OL}}$ ($V_{\text{DDA}} = V_{\text{DDB}} = 12\, \text{V to 17 V}$)

Figure 14. Typical Channel A Propagation Delay vs. Temperature

Figure 15. Typical Channel B Propagation Delay vs. Temperature
**TERMINOLOGY**

**Channel-to-Channel Matching**
Channel-to-channel matching with rising or falling matching edge polarity is the magnitude of the propagation delay difference between two channels of the same part when the inputs are both rising edges or both falling edges. The loads on each channel are equal.

Channel-to-channel matching with rising vs. falling opposite edge polarity is the magnitude of the propagation delay difference between two channels of the same part when one input is a rising edge and one input is a falling edge. The loads on each channel are equal.

**Maximum Output Current**
The maximum output current is the maximum isolated supply current that the ADuM6132 can provide. This current supports external loads as well as the needs of the ADuM6132 Channel A output circuitry. This is achieved via external connection of the $V_{ISO}$ pin to the $V_{DDA}$ pin and of the $GND_{ISO}$ pin to the $GND_{A}$ pin (see Figure 16). The net current available to power external loads is the ADuM6132 output current, $I_{ISO}$, minus the Channel A supply current, $I_{DDA}$.

**Maximum Switching Frequency**
The maximum switching frequency is the maximum signal frequency at which the specified timing parameters are guaranteed. Operation beyond the maximum switching frequency is not recommended, because high switching rates can cause droop in the output supply voltage.

**Minimum Pulse Width**
The minimum pulse width is the shortest pulse width at which the specified pulse width distortion is guaranteed. Operation below the minimum pulse width is not recommended.

**Part-to-Part Matching**
Part-to-part matching is the magnitude of the propagation delay difference between the same channels of two different parts. This includes rising vs. rising edges, falling vs. falling edges, or rising vs. falling edges. The supply voltages, temperatures, and loads of each part are equal.

**Propagation Delay**
The propagation delay is the time that it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high output.

The $t_{PHL}$ propagation delay is measured from the 50% level of the falling edge of the $V_{IA}$ or $V_{IB}$ signal to the 50% level of the falling edge of the $V_{OA}$ or $V_{OB}$ signal. The $t_{PLH}$ propagation delay is measured from the 50% level of the rising edge of the $V_{IA}$ or $V_{IB}$ signal to the 50% level of the rising edge of the $V_{OA}$ or $V_{OB}$ signal.

**Capacitive Load ($C_L$)**
The output capacitive load simulates a typical FET, IGBT, or buffer for timing or current measurements. This load includes all discrete and parasitic capacitive loads on the output.
APPLICATIONS INFORMATION

TYPICAL APPLICATION USAGE

The architecture of the ADuM6132 is ideal for motor drive and inverter applications where the low-side channels are common to the controller. This arrangement requires only two isolation regions in a package. All the isolated signals and the isolated power are grouped on one side of the package to maintain full package creepage and clearance. The low-side driver, as well as the control signals, share a common reference and are also grouped. To maximize the effectiveness of external bypass capacitors, the IsoPower dc-to-dc converter is not internally tied to the data channels, and should be treated as a completely independent subsystem, except for a UVLO function (see the Undervoltage Lockout section). This means that power must be applied to VDD to operate the dc-to-dc converter. Power must also be applied to VDDL and VDDB to operate the data input and the Channel B driver output. On the secondary side, the power generated at the VISO pin must be applied as an input power supply to the VDDA pin. GNDISO and GNDA must also be connected.

The ADuM6132 is intended for use in driving low gate capacitance transistors (200 pF typically). Most high voltage applications involve larger transistors than this. To accommodate these applications, users can implement a buffer configuration with the ADuM6132, as shown in Figure 16. In many cases, this buffer configuration is the least expensive option to drive high capacitance devices and provides the greatest amount of design flexibility. The precise buffer/high voltage transistor combination can be selected to suit the requirements of the application.

PCB LAYOUT

The ADuM6132 digital isolator with integrated 275 mW IsoPower dc-to-dc converter requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 17). The power supply section of the ADuM6132 uses a very high oscillator frequency to efficiently pass power through its chip scale transformers. In addition, the normal operation of the data section of the iCoupler introduces switching transients on the power supply pins. Bypass capacitors are required for several operating frequencies. Noise suppression requires a low ESR, high frequency capacitor; ripple suppression and proper regulation require a large value capacitor in parallel (see Table 10). The total lead length between both ends of the capacitor and the input power supply pin should not exceed 20 mm.

<table>
<thead>
<tr>
<th>Supply</th>
<th>Pins</th>
<th>Bypass Capacitors</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD</td>
<td>1, 2</td>
<td>0.1 μF, 10 μF</td>
</tr>
<tr>
<td>VDBB</td>
<td>7, 8</td>
<td>0.1 μF</td>
</tr>
<tr>
<td>VDDL</td>
<td>2, 3</td>
<td>0.1 μF</td>
</tr>
<tr>
<td>VDDA</td>
<td>13, 14</td>
<td>0.1 μF</td>
</tr>
<tr>
<td>VISO</td>
<td>15, 16</td>
<td>0.1 μF, 10 μF</td>
</tr>
</tbody>
</table>

Table 10. Recommended Bypass Capacitors

Figure 16. Typical Application Circuit
In applications involving high common-mode transients, care should be taken to ensure that board capacitive coupling across the isolation barrier is minimized. Furthermore, the board layout should be designed so that any coupling that does occur affects all pins on a given component side equally. Failure to ensure this may cause voltage differentials between pins that exceed the absolute maximum ratings of the device (see Table 7), leading to latch-up or permanent damage.

The ADuM6132 is a power device that dissipates approximately 1 W of power when fully loaded and running at maximum speed. Because it is not possible to apply a heat sink to an isolation device, the device depends primarily on heat dissipation into the PCB through the GND pins. If the device will be used at high ambient temperatures, provide a thermal path from the GND pins to the PCB ground plane.

The board layout in Figure 17 shows enlarged pads for Pin 8 (GND) and Pin 9 (GNDISO). Multiple vias should be implemented from the pad to the ground plane. This layout significantly reduces the temperatures inside the chip. The dimensions of the expanded pads are left to the discretion of the designer and the available board space. See the AN-0971 Application Note for board layout recommendations.

**THERMAL ANALYSIS**

The ADuM6132 consists of several internal die attached to two lead frame paddles. For the purposes of thermal analysis, the part is treated as a thermal unit with the highest junction temperature determining $\theta_{JA}$, as shown in Table 2. The value of $\theta_{JA}$ is based on measurements taken with the part mounted on a JEDEC standard 4-layer board with fine width traces and still air. Under normal operating conditions, the ADuM6132 operates at full load across the full temperature range without derating the output current. However, following the recommendations in the PCB Layout section decreases the thermal resistance to the PCB, allowing increased thermal margin at high ambient temperatures.

Under $V_{ISO}$ output short-circuit conditions, as shown in Figure 9, the package power dissipation quickly exceeds the safe operating limit of 1.44 W for ambient temperatures up to 85°C. At low input voltage, the power dissipation can approach 2 W. Because internal compensation of the PWM makes low $V_{DD}$ a worst-case condition, input voltage limiting is not an effective strategy for protecting the ADuM6132 from output load fault conditions. Therefore, the preferred protection methods, where required, are either limiting ambient temperature to 60°C or the use of a fuse.
PROPAGATION DELAY-RELATED PARAMETERS

Propagation delay is a parameter that describes the time it takes a logic signal to propagate through a component. The propagation delay to a logic low output may differ from the propagation delay to a logic high output.

<table>
<thead>
<tr>
<th>INPUT (VIX)</th>
<th>OUTPUT (VOX)</th>
</tr>
</thead>
<tbody>
<tr>
<td>tPLH</td>
<td>tPHL</td>
</tr>
<tr>
<td>50%</td>
<td>50%</td>
</tr>
</tbody>
</table>

Figure 18. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and is an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching refers to the maximum amount that the propagation delay differs between channels within a single ADuM6132 component.

MAGNETIC FIELD IMMUNITY

The ADuM6132 is extremely immune to external magnetic fields. The limitation on the ADuM6132 magnetic field immunity is set by the condition in which induced voltage in the receiving coil of the transformer is sufficiently large to falsely set or reset the decoder. The following analysis defines the conditions under which this may occur.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at approximately 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

\[ V = (-\frac{d\beta}{dt}) \Sigma \pi r_n^2 ; n = 1, 2, \ldots, N \]

where:
- \( \beta \) is the magnetic flux density (gauss).
- \( r_n \) is the radius of the nth turn in the receiving coil (cm).
- \( N \) is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM6132 and an imposed requirement that the induced voltage be at most 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic flux density is calculated, as shown in Figure 19.

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic flux density of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This voltage is approximately 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse (with the worst-case polarity), the received pulse is reduced from >1.0 V to 0.75 V—still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM6132 transformers. Figure 20 expresses these allowable current magnitudes as a function of frequency for selected distances. As shown in Figure 20, the ADuM6132 is extremely immune and can be affected only by extremely large currents operated at high frequency and very close to the component. For example, at a magnetic field frequency of 1 MHz, a 0.5 kA current would need to be placed 5 mm away from the ADuM6132 to affect the operation of the component.

Figure 19. Maximum Allowable External Magnetic Flux Density

Figure 20. Maximum Allowable Current for Various Current-to-ADuM6132 Spacings
Note that in the presence of strong magnetic fields and high frequencies, any loops formed by PCB traces may induce sufficiently large error voltages to trigger the threshold of succeeding circuitry. Care should be taken in the layout of such traces to avoid this possibility.

**INSULATION LIFETIME**

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation depends on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices conducts an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM6132.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. Table 12 summarizes the recommended peak working voltages for 50 years and 15 years of service life for various operating conditions evaluated by Analog Devices. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life in some cases.

The insulation lifetime of the ADuM6132 depends on the voltage waveform type imposed across the isolation barrier. The iCoupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 21, Figure 22, and Figure 23 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the bipolar ac condition determines the maximum working voltage recommended by Analog Devices.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower, which allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 12 can be applied while maintaining the 50-year minimum lifetime, provided that the voltage conforms to either the unipolar ac or dc voltage cases.

Any cross-insulation voltage waveform that does not conform to Figure 22 or Figure 23 should be treated as a bipolar ac waveform, and its peak voltage should be limited to the 50-year lifetime voltage value listed in Table 12. Note that the voltage shown in Figure 22 is sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

### Table 12. Maximum Continuous Working Voltage

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Peak Voltage</th>
<th>Lifetime</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Voltage, Bipolar Waveform</td>
<td>424 V peak</td>
<td>50-year minimum lifetime</td>
</tr>
<tr>
<td>AC Voltage, Unipolar Waveform</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Basic Insulation</td>
<td>800 V peak</td>
<td>15-year minimum lifetime</td>
</tr>
<tr>
<td>Basic Insulation</td>
<td>660 V peak</td>
<td>50-year minimum lifetime</td>
</tr>
<tr>
<td>DC Voltage Waveform</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Basic Insulation</td>
<td>800 V peak</td>
<td>15-year minimum lifetime</td>
</tr>
<tr>
<td>Basic Insulation</td>
<td>660 V peak</td>
<td>50-year minimum lifetime</td>
</tr>
</tbody>
</table>

1 Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more information.
OUTLINE DIMENSIONS

Figure 24. 16-Lead Standard Small Outline Package [SOIC_W]
Wide Body
(RW-16)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>No. of Channels</th>
<th>Output Peak Current (A)</th>
<th>Output Voltage (V)</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADuM6132ARWZ</td>
<td>2</td>
<td>0.2</td>
<td>15</td>
<td>−40°C to +85°C</td>
<td>16-Lead SOIC_W</td>
<td>RW-16</td>
</tr>
<tr>
<td>ADuM6132ARWZ-RL</td>
<td>2</td>
<td>0.2</td>
<td>15</td>
<td>−40°C to +85°C</td>
<td>16-Lead SOIC_W, 13-inch Tape and Reel Option (1,000 Units)</td>
<td>RW-16</td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.