FEATUERS
Stable over time and temperature
  0.5% initial error accuracy
  1% accuracy error over the full temperature range
Compatible with Type II or Type III compensation networks
Reference output voltage: 1.225 V
Compatible with Distributed-power Open Standards Alliance (DOSA)
Low power operation: <7 mA total
Wide voltage supply range: 3.0 V to 20 V (VDD1 and VDD2)
Output −3 dB bandwidth: 400 kHz typical
Isolation voltage: 5000 V rms reinforced

SAFETY AND REGULATORY APPROVALS
  UL recognition: 5000 V rms for 1 minute per UL 1577
  CSA Component Acceptance Notice 5A
  VDE certificate of conformity
  DIN V VDE V 0884-10 (VDE V 0884-10):2006-12
  \( V_{\text{FORM}} = 849 \text{ V peak} \)

ENHANCED FEATURES
Supports defense and aerospace applications (AQEC standard)
Military temperature range (−55°C to +125°C)
Controlled manufacturing baseline
One assembly/test site
One fabrication site
Enhanced product change notification
Qualification data available on request

APPLICATIONS
Linear feedback power supplies
Inverters
Uninterruptible power supplies (UPS)
DOSA-compatible modules
Voltage monitors

GENERAL DESCRIPTION
The ADuM4190-EP\(^1\) is an isolated error amplifier based on Analog Devices, Inc., iCoupler\(^\text{®}\) technology. The ADuM4190-EP is ideal for linear feedback power supplies. The primary side controllers of the ADuM4190-EP enable improvements in transient response, power density, and stability as compared to commonly used optocoupler and shunt regulator solutions.

Unlike optocoupler-based solutions, which have an uncertain current transfer ratio over lifetime and at high temperatures, the ADuM4190-EP transfer function does not change over its lifetime and is stable over a wide temperature range of −55°C to +125°C.

Included in the ADuM4190-EP is a wideband operational amplifier for a variety of commonly used power supply loop compensation techniques. The ADuM4190-EP is fast enough to allow a feedback loop to react to fast transient conditions and overcurrent conditions. Also included is a high accuracy 1.225 V reference to compare with the supply output setpoint.

The ADuM4190-EP is packaged in a wide body, 16-lead SOIC package for a reinforced 5000 V rms isolation voltage rating. Additional application and technical information can be found in the ADuM4190 data sheet.

\( ^1 \)Protected by U.S. Patents 5,952,849; 6,873,065; 7,075,329; and 9,293,997.
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## REVISION HISTORY

7/2016—Revision 0: Initial Version

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**SPECIFICATIONS**

\( V_{DD1} = V_{DD2} = 3 \) V to 20 V for \( T_A = T_{MIN} \) to \( T_{MAX} \). All typical specifications are at \( T_A = 25^\circ C \) and \( V_{DD1} = V_{DD2} = 5 \) V, unless otherwise noted.

**Table 1.**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>ACCURACY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Initial Error</td>
<td>( (1.225 V - EA_{OUT})/1.225 V \times 100% ); see Figure 27</td>
<td>0.25</td>
<td>0.5</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Total Error</td>
<td>( T_A = 25^\circ C )</td>
<td>0.5</td>
<td>1</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td><strong>OP AMP</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Error</td>
<td></td>
<td>-5</td>
<td>±2.5</td>
<td>+5</td>
<td>mV</td>
</tr>
<tr>
<td>Open-Loop Gain</td>
<td></td>
<td>66</td>
<td>80</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Common-Mode Range</td>
<td></td>
<td>0.35</td>
<td>1.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Common-Mode Rejection</td>
<td></td>
<td>72</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>Output Voltage Range</td>
<td>COMP pin</td>
<td>0.2</td>
<td></td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td></td>
<td>0.01</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td><strong>REFERENCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>0 mA to 1 mA load, ( C_{REFOUT} = 15 ) pF</td>
<td>1.215</td>
<td>1.225</td>
<td>1.235</td>
<td>V</td>
</tr>
<tr>
<td>( T_A = 25^\circ C )</td>
<td></td>
<td>1.213</td>
<td>1.225</td>
<td>1.237</td>
<td>V</td>
</tr>
<tr>
<td>( T_A = T_{MIN} ) to ( T_{MAX} )</td>
<td>( C_{REFOUT} = 15 ) pF</td>
<td>2.0</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>UNDERVOLTATE LOCK OUT (UVLO)</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Positive Going Threshold</td>
<td></td>
<td>2.8</td>
<td>2.96</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Negative Going Threshold</td>
<td></td>
<td>2.4</td>
<td>2.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( EA_{OUT} ) Impedance</td>
<td>( V_{DD2} ) or ( V_{DD1} &lt; UVLO ) threshold</td>
<td>High-Z</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td><strong>OUTPUT CHARACTERISTICS</strong></td>
<td>See Figure 29</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Gain (^1)</td>
<td>From ( EA_{OUT} ), 0.4 V to 2.1 V, ±3 mA</td>
<td>0.83</td>
<td>1.0</td>
<td>1.17</td>
<td>V/V</td>
</tr>
<tr>
<td>Output Offset Voltage</td>
<td>From ( EA_{OUT} ) to ( EA_{OUT2} ), 0.4 V to 2.1 V, ±1 mA, ( V_{DD1} = 20 ) V</td>
<td>2.5</td>
<td>2.6</td>
<td>2.7</td>
<td>V/V</td>
</tr>
<tr>
<td>Output Linearity (^2)</td>
<td>From ( EA_{OUT} ) to ( EA_{OUT2} ), 0.4 V to 2.1 V, ±3 mA</td>
<td>-0.4</td>
<td>+0.05</td>
<td>+0.4</td>
<td>V</td>
</tr>
<tr>
<td>Output (-3\ dB Bandwidth)</td>
<td>From ( EA_{OUT} ) to ( EA_{OUT2} ), 0.4 V to 2.1 V, ±1 mA, ( V_{DD1} = 20 ) V</td>
<td>-0.1</td>
<td>+0.01</td>
<td>+0.1</td>
<td>V</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>From ( EA_{OUT} ) to ( EA_{OUT2} ), 0.4 V to 2.1 V, ±3 mA</td>
<td>-1.0</td>
<td>+0.15</td>
<td>+1.0</td>
<td>%</td>
</tr>
<tr>
<td>( EA_{OUT} ) Low Voltage</td>
<td>( V_{DD1} = 4.5 ) V to 5.5 V</td>
<td>0.3</td>
<td>0.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{DD1} = 10 ) V to 20 V</td>
<td>0.3</td>
<td>0.6</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( EA_{OUT2} ) High Voltage</td>
<td>( V_{DD1} = 4.5 ) V to 5.5 V</td>
<td>4.8</td>
<td>4.9</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( V_{DD1} = 10 ) V to 20 V</td>
<td>5.0</td>
<td>5.4</td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td><strong>Noise</strong></td>
<td>See Figure 15</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( EA_{OUT} )</td>
<td></td>
<td>1.7</td>
<td></td>
<td></td>
<td>mV rms</td>
</tr>
<tr>
<td>( EA_{OUT2} )</td>
<td></td>
<td>4.8</td>
<td></td>
<td></td>
<td>mV rms</td>
</tr>
<tr>
<td><strong>POWER SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Operating Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Side 1</td>
<td>( V_{DD1} )</td>
<td>3.0</td>
<td>20</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Side 2</td>
<td>( V_{DD2} )</td>
<td>3.0</td>
<td>20</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>
ADuM4190-EP
Enhanced Product

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Supply Rejection</td>
<td>DC, ( V_{DD1} = V_{DD2} = 3.0 ) V to 20 V</td>
<td>60</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Supply Current ( I_{DD1} )</td>
<td>See Figure 4</td>
<td>1.4</td>
<td>2.0</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Supply Current ( I_{DD2} )</td>
<td>See Figure 5</td>
<td>2.9</td>
<td>5.0</td>
<td></td>
<td>mA</td>
</tr>
</tbody>
</table>

1. Output gain is defined as the slope of the best-fit line of the output voltage vs. the input voltage over the specified input range, with the offset error adjusted out.
2. Output linearity is defined as the peak-to-peak output deviation from the best-fit line of the output gain, expressed as a percentage of the full-scale output voltage.

**PACKAGE CHARACTERISTICS**

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESISTANCE Input to Output(^1)</td>
<td>( R_{I-O} )</td>
<td>10(^13)</td>
<td></td>
<td></td>
<td>Ω</td>
<td></td>
</tr>
<tr>
<td>CAPACITANCE Input to Output(^1)</td>
<td>( C_{I-O} )</td>
<td>2.2</td>
<td></td>
<td></td>
<td>pF</td>
<td>( f = 1 ) MHz</td>
</tr>
<tr>
<td>Input Capacitance(^2)</td>
<td>( C_{I} )</td>
<td>4.0</td>
<td></td>
<td></td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>IC JUNCTION-TO-AMBIENT THERMAL RESISTANCE</td>
<td>( \theta_{JA} )</td>
<td>45</td>
<td></td>
<td></td>
<td>°/W</td>
<td>Thermocouple located at center of package underside</td>
</tr>
</tbody>
</table>

\(^1\) The device is considered a 2-terminal device; Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
\(^2\) Input capacitance is from any input pin to ground.

**REGULATORY INFORMATION**

The ADuM4190-EP is pending approval by the organizations listed in Table 3. See Table 8 for recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 3.

<table>
<thead>
<tr>
<th>UL (Pending)</th>
<th>CSA (Pending)</th>
<th>VDE (Pending)</th>
<th>CQC (Pending)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Recognized under UL 1577 Component Recognition Program(^1)</td>
<td>Approved under CSA Component Acceptance Notice 5A</td>
<td>Certified according to DIN V VDE V 0884-10 (VDEV 0884-10):2006-12(^2)</td>
<td>Certified by CQC11-471543-2015, GB4943.1-2011</td>
</tr>
<tr>
<td>Single Protection, 5000 V rms Isolation Voltage, 16-Lead SOIC</td>
<td>Reinforced insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (565 V peak) maximum working voltage Basic insulation per CSA 60950-1-03 and IEC 60950-1, 800 V rms (1131 V peak) maximum working voltage</td>
<td>Reinforced insulation, 849 V peak</td>
<td>Reinforced insulation at 400 V rms (565 V peak), tropical climate, altitude ≤ 5000 meters</td>
</tr>
<tr>
<td>Certified temperature range: (-40°C) to (+125°C)</td>
<td>Certified temperature range: (-40°C) to (+125°C)</td>
<td>Certified temperature range: (-40°C) to (+125°C)</td>
<td>Certified temperature range: (-40°C) to (+125°C)</td>
</tr>
<tr>
<td>File E214100</td>
<td>File 205078</td>
<td>File 2471900-4880-0001</td>
<td>File CQC15001129480</td>
</tr>
</tbody>
</table>

\(^1\) In accordance with UL 1577, each ADuM4190-EP is proof tested by applying an insulation test voltage ≥ 6000 V rms for 1 sec (current leakage detection limit = 10 µA).
\(^2\) In accordance with DIN V VDE V 0884-10 (VDEV 0884-10):2006-12, each ADuM4190-EP is proof tested by applying an insulation test voltage ≥ 1590 V peak for 1 sec (partial discharge detection limit = 5 pC). The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDEV 0884-10):2006-12 approval.
## INSULATION AND SAFETY RELATED SPECIFICATIONS

### Table 4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated Dielectric Insulation Voltage</td>
<td></td>
<td>5000</td>
<td>V rms</td>
<td>1-minute duration</td>
</tr>
<tr>
<td>Minimum External Air Gap (Clearance)</td>
<td>L(i01)</td>
<td>8.0 min</td>
<td>mm</td>
<td>Measured from input terminals to output terminals, shortest distance through air along the PCB mounting plane, as an aid to PCB layout</td>
</tr>
<tr>
<td>Minimum External Tracking (Creepage)</td>
<td>L(i02)</td>
<td>8.3 min</td>
<td>mm</td>
<td>Measured from input terminals to output terminals, shortest distance path along body</td>
</tr>
<tr>
<td>Minimum Internal Gap (Internal Clearance)</td>
<td></td>
<td>0.017 min</td>
<td>mm</td>
<td>Insulation distance through insulation</td>
</tr>
<tr>
<td>Tracking Resistance (Comparative Tracking Index)</td>
<td>CTI</td>
<td>&gt;400</td>
<td>V</td>
<td>DIN IEC 112/VDE 0303, Part 1</td>
</tr>
<tr>
<td>Isolation Group</td>
<td></td>
<td>II</td>
<td></td>
<td>Material Group DIN VDE 0110, 1/89, Table 1</td>
</tr>
</tbody>
</table>

### RECOMMENDED OPERATING CONDITIONS

### Table 5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>OPERATING TEMPERATURE</td>
<td>$T_a$</td>
<td>−55</td>
<td>+125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>SUPPLY VOLTAGES$^1$</td>
<td>$V_{DD1}, V_{DD2}$</td>
<td>3.0</td>
<td>20</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>INPUT SIGNAL RISE AND FALL TIMES</td>
<td>$t_{rp}, t_r$</td>
<td>1.0</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
</tbody>
</table>

$^1$ All voltages are relative to their respective grounds.
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

This isolator is suitable for reinforced isolation only within the safety limit data. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marking branded on the component designates DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 approval for an 849 V peak working voltage.

Table 6.

<table>
<thead>
<tr>
<th>Description</th>
<th>Test Conditions/Comments</th>
<th>Symbol</th>
<th>Characteristic</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Installation Classification per DIN VDE 0110</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>For Rated Mains Voltage ≤ 150 V rms</td>
<td></td>
<td>I to IV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>For Rated Mains Voltage ≤ 300 V rms</td>
<td></td>
<td>I to IV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>For Rated Mains Voltage ≤ 400 V rms</td>
<td></td>
<td>I to III</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Climatic Classification</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pollution Degree per DIN VDE 0110, Table 1</td>
<td></td>
<td>40/105/21</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Working Insulation Voltage</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input-to-Output Test Voltage, Method B1</td>
<td>$V_{ORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = 60$ sec, $t_{m} = 10$ sec, partial discharge &lt; 5 pC</td>
<td>$V_{ORM}$</td>
<td>849</td>
<td>V peak</td>
</tr>
<tr>
<td>Input-to-Output Test Voltage, Method A</td>
<td>$V_{ORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_{m} = 10$ sec, partial discharge &lt; 5 pC</td>
<td>$V_{pd(m)}$</td>
<td>1592</td>
<td>V peak</td>
</tr>
<tr>
<td>After Environmental Tests Subgroup 1</td>
<td>$V_{ORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_{m} = 10$ sec, partial discharge &lt; 5 pC</td>
<td>$V_{pd(m)}$</td>
<td>1273</td>
<td>V peak</td>
</tr>
<tr>
<td>After Input and/or Safety Tests Subgroup 2</td>
<td>$V_{ORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_{m} = 10$ sec, partial discharge &lt; 5 pC</td>
<td>$V_{pd(m)}$</td>
<td>1018</td>
<td>V peak</td>
</tr>
<tr>
<td>Highest Allowable Overvoltage</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Surge Isolation Voltage</td>
<td>$V = 10$ kV; 1.2 $\mu$s rise time; 50 $\mu$s, 50% fall time</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Safety Limiting Values</td>
<td>Maximum value allowed in the event of a failure (see Figure 2)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Maximum Junction Temperature</td>
<td>$T_s$</td>
<td>150</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Safety Total Dissipated Power</td>
<td>$P_S$</td>
<td>2.78</td>
<td>W</td>
<td></td>
</tr>
<tr>
<td>Insulation Resistance at $T_s$</td>
<td>$V_{ID} = 500$ V</td>
<td>$R_s$</td>
<td>&gt;10$^9$</td>
<td>Ω</td>
</tr>
</tbody>
</table>

Figure 2. Thermal Derating Curve, Dependence of Safety Limiting Values on Case Temperature, per DIN V VDE V 0884-10
ABSOLUTE MAXIMUM RATINGS

$T_A = 25°C$, unless otherwise noted.

### Table 7.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Storage Temperature ($T_{ST}$) Range</td>
<td>$-65°C$ to $+150°C$</td>
</tr>
<tr>
<td>Ambient Operating Temperature ($T_J$) Range</td>
<td>$-55°C$ to $+125°C$</td>
</tr>
<tr>
<td>Junction Temperature Range</td>
<td>$-55°C$ to $+150°C$</td>
</tr>
<tr>
<td>Supply Voltage Range $V_{DD1}, V_{DD2}$</td>
<td>$-0.5$ V to $+24$ V</td>
</tr>
<tr>
<td>$V_{REG1}, V_{REG2}$</td>
<td>$-0.5$ V to $+3.6$ V</td>
</tr>
<tr>
<td>Input Voltage Range $V(+IN, −IN)$</td>
<td>$-0.5$ V to $+3.6$ V</td>
</tr>
<tr>
<td>Output Voltage Range $REF_{OUT}, REF_{OUT1}$</td>
<td>$-0.5$ V to $+3.6$ V</td>
</tr>
<tr>
<td>$COMP, EA_{OUT}$</td>
<td>$-11$ mA to $+11$ mA</td>
</tr>
<tr>
<td>Common-Mode Transients Range $2$</td>
<td>$-100$ kV/μs to $+100$ kV/μs</td>
</tr>
</tbody>
</table>

1 All voltages are relative to their respective grounds.

2 Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings may cause latch-up or permanent damage.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### Table 8. Maximum Continuous Working Voltage

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Max</th>
<th>Unit</th>
<th>Constraint</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Voltage</td>
<td></td>
<td></td>
<td>50-year minimum lifetime</td>
</tr>
<tr>
<td>Bipolar Waveform</td>
<td>560</td>
<td>V peak</td>
<td></td>
</tr>
<tr>
<td>Unipolar Waveform</td>
<td>1131</td>
<td>V peak</td>
<td></td>
</tr>
<tr>
<td>DC Voltage</td>
<td>1131</td>
<td>V peak</td>
<td></td>
</tr>
</tbody>
</table>

1 Refers to the continuous voltage magnitude imposed across the isolation barrier.

**ESD CAUTION**

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
Table 9. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>$\text{V}_\text{DD1}$</td>
<td>Supply Voltage for Side 1 (3.0 V to 20 V). Connect a 1 μF capacitor between $\text{V}_\text{DD1}$ and GND1.</td>
</tr>
<tr>
<td>2, 8</td>
<td>GND1</td>
<td>Ground Reference for Side 1.</td>
</tr>
<tr>
<td>3</td>
<td>$\text{V}_\text{REG1}$</td>
<td>Internal Supply Voltage for Side 1. Connect a 1 μF capacitor between $\text{V}_\text{REG1}$ and GND1.</td>
</tr>
<tr>
<td>4</td>
<td>REFOUT1</td>
<td>Reference Output Voltage for Side 1. The maximum recommended capacitance for this pin ($C_{\text{REFOUT1}}$) is 15 pF.</td>
</tr>
<tr>
<td>5</td>
<td>NC</td>
<td>No Connection. Connect Pin 5 to GND1; do not leave this pin floating.</td>
</tr>
<tr>
<td>6</td>
<td>EAOUT2</td>
<td>Isolated Output Voltage 2, Open-Drain Output. Connect a pull-up resistor between EAOUT2 and $\text{V}_{\text{DD1}}$ for current up to 1 mA.</td>
</tr>
<tr>
<td>7</td>
<td>EAOUT</td>
<td>Isolated Output Voltage.</td>
</tr>
<tr>
<td>9, 15</td>
<td>GND2</td>
<td>Ground Reference for Side 2.</td>
</tr>
<tr>
<td>10</td>
<td>COMP</td>
<td>Output of the Op Amp. A loop compensation network can be connected between the COMP pin and the $-\text{IN}$ pin.</td>
</tr>
<tr>
<td>11</td>
<td>$-\text{IN}$</td>
<td>Inverting Op Amp Input. Pin 11 is the connection for the power supply setpoint and compensation network.</td>
</tr>
<tr>
<td>12</td>
<td>$+\text{IN}$</td>
<td>Noninverting Op Amp Input. Pin 12 can be used as a reference input.</td>
</tr>
<tr>
<td>13</td>
<td>REFOUT</td>
<td>Reference Output Voltage for Side 2. The maximum recommended capacitance for this pin ($C_{\text{REFOUT}}$) is 15 pF.</td>
</tr>
<tr>
<td>14</td>
<td>$\text{V}_\text{REG2}$</td>
<td>Internal Supply Voltage for Side 2. Connect a 1 μF capacitor between $\text{V}_\text{REG2}$ and GND2.</td>
</tr>
<tr>
<td>16</td>
<td>$\text{V}_\text{DD2}$</td>
<td>Supply Voltage for Side 2 (3.0 V to 20 V). Connect a 1 μF capacitor between $\text{V}_\text{DD2}$ and GND2.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. Typical $I_{DD1}$ Supply Current vs. Junction Temperature for $V_{DD} = 20$ V and $V_{DD} = 5$ V

Figure 5. Typical $I_{DD2}$ Supply Current vs. Junction Temperature for $V_{DD} = 20$ V and $V_{DD} = 5$ V

Figure 6. $+\text{IN}, -\text{IN}$ Input Bias Current vs. Junction Temperature

Figure 7. $\text{REFOUT}$ Accuracy vs. Junction Temperature

Figure 8. $\text{EAOUT}$ Accuracy vs. Junction Temperature

Figure 9. Op Amp Offset Voltage vs. Junction Temperature
Figure 10. Op Amp Open-Loop Gain vs. Junction Temperature

Figure 11. EA_{OUT} Gain vs. Junction Temperature

Figure 12. EA_{OUT2} Gain vs. Junction Temperature

Figure 13. EA_{OUT} Offset Voltage vs. Junction Temperature

Figure 14. EA_{OUT2} Offset Voltage vs. Junction Temperature

Figure 15. Output Noise with Test Circuit 1 (10 mV/DIV), Channel 1 = EA_{OUT}, Channel 2 = EA_{OUT2}
Figure 16. COMP to EA\textsubscript{OUT} Gain Distribution at 25°C

Figure 17. COMP to EA\textsubscript{OUT} Gain Distribution at 125°C

Figure 18. COMP to EA\textsubscript{OUT} Gain Distribution at −55°C

Figure 19. COMP to EA\textsubscript{OUT} Offset Distribution at 25°C

Figure 20. COMP to EA\textsubscript{OUT} Offset Distribution at 125°C

Figure 21. COMP to EA\textsubscript{OUT} Offset Distribution at −55°C
Figure 22. \( E_{A\text{OUT}} \) Accuracy Distribution at 25°C

Figure 23. \( E_{A\text{OUT}} \) Accuracy Distribution at 125°C

Figure 24. \( E_{A\text{OUT}} \) Accuracy Distribution at −55°C

Figure 25. Output 100 kHz Signal with Test Circuit 3, Channel 1 = +IN, Channel 2 = \( E_{A\text{OUT}} \), Channel 3 = \( E_{A\text{OUT}} \)

Figure 26. Output Square Wave Response with Test Circuit 3, Channel 1 = +IN, Channel 2 = \( E_{A\text{OUT}} \), Channel 3 = \( E_{A\text{OUT}} \)
TEST CIRCUITS

Figure 27. Accuracy Circuit Using EA_OUT

Figure 28. Accuracy Circuit Using EA_OUT2

Figure 29. Isolated Amplifier Circuit
OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MS-013-AC

Figure 30. 16-Lead Standard Small Outline Package, with Increased Creepage [SOIC_IC] Wide Body (RI-16-2)

Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Typical Bandwidth (kHz)</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
</table>

1 Z = RoHS Compliant Part.