MicroConverter® Multichannel 24-/16-Bit ADCs with Embedded 62 kB Flash and Single-Cycle MCU

Anomaly Sheet for Silicon Rev. C ADuC845/ADuC847/ADuC848

This anomaly list represents the known bugs, anomalies, and workarounds for the ADuC845, ADuC847, and ADuC848 MicroConverter products. The anomalies listed apply to all ADuC845/ADuC847/ADuC848 packaged material branded as follows:

First (CSP) / Second (PQFP) Line ADuC845 or ADuC847 or ADuC848
Third (CSP) / Fourth Line (PQFP) C20

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ADuC845/ADuC847/ADuC848 SILICON REVISION HISTORY

Silicon Revision Identifier	Kernel Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Anomalies
C	0	All silicon branded ADUC845BS or ADuC845BCP ADuC847BS or ADuC847BCP ADuC8484BS or ADuC848BCP Third/Fourth Line: C20	Release	Rev. B	7

ANOMALIES

1. Interrupts During Reading/Writing to DATAFLASH/EE [er001]

Background:	There are 4 kB of DATAFLASH/EE that can be used for nonvolatile data storage.
Issue:	If an interrupt occurs during a DATAFLASH/EE read or write operation, code execution following the ISR may resume at a random program memory address.
Workaround:	Disable all interrupts prior to a read or write operation. This can be done by setting the EA bit to 0.
Related Issues:	None.

2. PWM Operation [er002]

Background:	The PWM output rate is determined by the PWMxH and PWMxL registers for the PWM0 and PWM1 outputs.	
Issue:	Modifying RAM address 2EH causes the PWM timer to be reset.	
Workaround:	For Assembly code:	Do not use memory location 2EH.
	For C code:	Assign a dummy variable to location 0x2E using the following code: `idata unsigned int ui32Dummy[2] _at_ 0x2E;`
Related Issues:	None.	

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3. I²C® Operation [er003]

Background:	The I2CDAT register is used to read or write data to the I²C bus. The I2CDAT register has an SFR address of 9AH.	
Issue:	During an I²C transfer, if a user accesses the RAM address 9AH, the contents of the I2CDAT SFR can be modified.	
Workaround A:	For Assembly code:	Do not use memory location 9AH.
	For C code:	Assign a dummy variable to location 0x9A by using the following code, thereby preventing C from using it.
		`idata unsigned int ui32Dummy[2] _at_ 0x9A;`
Related Issues:	None.	

4. ADC Noise [er004]

Background:	The ADuC845 incorporates two 24-bit Σ-Δ ADCs, and the ADuC847 and ADuC848 incorporate a 24-bit and 16-bit Σ-Δ ADC, respectively. These ADCs are specified for typical noise performance as described in the relevant noise tables of the data sheet.
Issue:	ADC noise performance degrades when operating at maximum MCU clock frequency as determined via the CD bits in the PLLCON SFR.
Workaround:	For the duration of an ADC conversion, the CD bits should be set to 3 or greater. Note that the default CD setting is 3.
Related Issues:	None.

5. Watchdog Timer [er005]

Background: The ADuC845, ADuC847, and ADuC848 incorporate a watchdog timer. The purpose of the WDT is to ensure that the part is never stuck in an endless loop by generating either a hardware reset or an interrupt event that vectors to the WDT ISR.

Issue: If the WDT generates an interrupt as opposed to a hardware reset, and if the ISR subsequently sets up the WDT to time out to a hardware reset, the reset is ignored.

Workaround: Ensure that a double write to the WDCON is executed inside the ISR, with the first write being a reset of the WDT. For example:

```
void isr_wdt( void ) interrupt 11
{
     WDWR = 1;       // This first WDT write is required to get the WDT to work inside the ISR.
     WDCON  = 0x60; // Reset WDT.
     WDWR = 1;       // Now set the WDT to the required 1s timeout
     WDCON  = 0x62; // select reset after 1000mS
     while(1);
}
void main(void)
{
     EA = 0;
     WDWR = 1;     // Allow write to WDCON
     WDCON = 0x6A; // timeout=1000mS, WDT enable, WDT ISR Interrupt
     while (1);
}
```

Related Issues: None.

6. Stack Pointer in ULOAD Mode [er006]

Background: When starting user code, the stack pointer should, by default, be initialized to Address 07H.

Issue: In ULOAD mode, the stack pointer defaults to 03H causing conflict between RAM locations R4 to R7 and the stack.

Workaround: Manually change in code the stack pointer address to 07H or to the address that is required upon entry to ULOAD mode, that is,

```
MOV SP, #07H
```

or

```
SP = 0x07;
```

Related Issues: None.

7. Level-Triggered Interrupt Operation [er007]

Background:	The ADuC845/ADuC847/ADuC848 incorporate two external interrupt sources (INT0 and INT1) that can be configured to respond to either an edge event or a level event.
Issue:	If an interrupt occurs on the INT0 or INT1 pins and is then removed within one core instruction cycle, the interrupt vector address that is generated may be incorrect, resulting in a vector to 0000H. This effectively restarts code execution.
Workaround:	To ensure that this does not occur, the level-triggered interrupt source must be kept low for a minimum of nine core clock cycles.
Related Issues:	None.

ADuC845/ADuC847/ADuC848 SILICON ANOMALIES

Anomaly No.	Description	Status
er001	Interrupts During Reading/Writing to DATAFLASH/EE	Pending
er002	PWM Operation	Pending
er003	I^2C Operation	Pending
er004	ADC Noise	Pending
er005	Watchdog Timer	Pending
er006	Stack Pointer in ULOAD Mode	Pending
er007	Level Triggered Interrupt Operation	Pending

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