



A. This Errata sheet represents the known bugs, anomalies and work-arounds for the ADuC812 MicroConverter.

B. The Errata listed, apply to all ADuC812 packaged material branded as follows :

**(Production Material)**

ADUC812BS

Date Stamp AD Logo C

Lot Number

(Note : The identifier 'C' after the ADLogo on the second line of the brand)

C. Errata Sheets referring to previous silicon revisions are available on our web-site at

<http://www.analog.com/microconverter/erratasheets.html>

D. Because of silicon revisions and improved work-arounds, this Errata Sheet will be updated periodically. Please find the latest Errata Sheet listed on the World Wide Web at :

<http://www.analog.com/microconverter/erratasheets.html>

E. Analog Devices Inc. is committed, through future silicon revisions to continuously improve silicon functionality. Analog Devices Inc. will use its best endeavors to ensure that these future silicon revisions remain compatible with your present software/systems that implement the recommended work-arounds outlined in this document.

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REV. F.2 FEB/02

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**812\_S01. ADC FUNCTION - ADC CONVERSION IN DMA MODE :**

- Background:** The ADC can be triggered by 1 of 4 trigger events in Normal and DMA operating modes, namely: Single Software Conversion, Continuous Software Conversions, External Pin Triggered Conversions and Timer2 triggered Conversions. DMA mode is initiated by setting the DMA bit in the ADCCON2 SFR and the DMA controller proceeds starting from the external data memory address indicated by the DMA address SFRs DMAL/H/P. Once a DMA conversion sequence is complete, both the DMA bit and the bit controlling the conversion mode are reset by the DMA controller.
- Issue A:** DMA operation will not execute when triggered from Timer2 driven conversions unless when configuring the ADC, ADCCON2 is written prior to ADCCON1.
- Work-Around A:** For Timer2 triggered DMA conversions, ensure that the correct configuration sequence is used for the ADC, i.e. configure ADCCON2 then ADCCON1.
- Issue B:** DMA operation will not execute when triggered from Timer2 driven conversions unless DMA Address (DMAL/H/P) is initially set to 000000H.
- Work-Around B:** For Timer2 triggered DMA conversions, ensure that the DMA start address is set to 000000H.
- Related Issues :** None.
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**812\_S02. UART FUNCTION - MULTIPROCESSOR COMMUNICATIONS MODE :**

- Background:** UART Modes 2 and 3 (programmed via SCON) have a special provision for multiprocessor communications. In these modes, nine data bits are received and the ninth bit goes into RB8. In this mode the port can be programmed so that when the stop bit is received, the serial port interrupt is activated only if RB8(SCON) = 1. This feature is enabled by setting the SM2 bit in SCON.
- Issue:** With SM2 set, the serial port interrupt is set each time a stop bit is received, regardless of the state of the RB8 bit.
- Work-Around :** Implement a software polling scheme in the Serial Port ISR so that the state of the RB8 bit is checked on entering the ISR. If RB8 is '0' then a 'RETI' is executed to exit the ISR immediately, and only if RB8 is set will the ISR function be executed.
- Related Issues :** None.

**812\_S03. UART FUNCTIONALITY - BAUD RATE GENERATION IN SPLIT TIMER MODE:**

|                         |  |
|-------------------------|--|
| <b>Background :</b>     | Timer 0 can be enabled as two 8-bit timers (Mode 3). Since the overflow flag for timer 1 is used by timer 0 in split timer mode, timer 1 can only be used as either a baud rate generator or as a timer as long as it does not require interrupts. |
| <b>Issue :</b>          | When the timers are configured as above with timer 1 as a baud rate generator the reload value in TH1 fails to be loaded into TH0, generating the incorrect baud rate.   |
| <b>Work-Around :</b>    | Pending  |
| <b>Related Issues :</b> | All other Timer and Baud Rate generation modes operate correctly.  |

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**812\_S04. PORT 2 INTERNAL ACTIVE PULL-UP FUNCTIONALITY :**

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|-------------------------|--|
| <b>Background :</b>     | As with standard 8051 compatible Port functionality, Port 2 (P2.0 - P2.7) feature weak internal pull-up resistors and will source current (Logic 0 input current, datasheet) when pulled low externally. On a 0-to-1 transition, an additional pullup is turned on for 2 master clock periods to help increase transition speed. |
| <b>Issue :</b>          | On Port 2 pins, the additional pullup resistor does not come on during the required 2 clock periods when these pins are being driven as digital outputs.   |
| <b>Work-Around :</b>    | Pending  |
| <b>Related Issues :</b> | Port 2 pins operate correctly when operating as part of the external memory interface on the device.   |

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**812\_S05. FLASH/EE MEMORY - 3V PROGRAMMING :**

|                         |   |
|-------------------------|---|
| <b>Background :</b>     | The ADuC812 contains 2 separate arrays of Flash/EE memory, namely :<br>- 8 KBytes Internal Code Space and 640 Bytes Flash/EE Data Memory.<br>The 8 KBytes code space can be programmed in serial download or parallel programming modes, while the 640 Byte data space can be written by user software via a specified SFR interface. |
| <b>Issue :</b>          | In the temperature range -40°C to 0°C, this revision of silicon will not support programming below $DV_{DD}=3V$ supplies.   |
| <b>Work-Around :</b>    | In the temperature range 0°C to 85°C, the device can be programmed at $DV_{DD}= 3.0V \pm 10\%$ .<br>The device can be programmed at $DV_{DD}=3.3V\pm 10\%$ over the full temperature range -40°C to 85°C.   |
| <b>Related Issues :</b> | The device can be programmed at $DV_{DD}=5V\pm 10\%$ over the full temperature range -40°C to 85°C.   |

**812\_S06. FUNCTIONALITY OF PSMCON.1 BIT IN THE PSMCON SFR :**

- Background :** The PSMCON.1 bit in the PSMCON SFR can be used to indicate which supply caused the active power supply trip condition. PSMCON.1=0 indicates a DV<sub>DD</sub> fault while PSMCON.1=1 indicates an AV<sub>DD</sub> fault.
- Issue :** If the power supply trip point selection bits are set to select the 4.63V or 4.37V supply trip points, the PSMCON.1 (AV<sub>DD</sub>/DV<sub>DD</sub> power supply trip indicator) bit may not correctly indicate which supply has caused the fault. The supply trip indicator bit will function correctly at all other trip point voltage levels.
- Work-Around :** Pending.
- Related Issues :** It should be noted that while the trip indicator bit function is suspect at these trip levels, the PSM function itself is still 100% operational (even at 4.63V and 4.37V trip levels) generating an interrupt as soon as any one of the supply pins falls below the specified supply voltage trip point selection.
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**812\_S07. EXTERNAL POWER-ON RESET (POR) OPERATION - DOCUMENTATION UPDATE :**

All ADuC812 documentation has been updated to include a detailed recommendation on how the external RESET pin (#15) should be driven with external POR circuitry during power-on, power-down and brown-out conditions. These recommendations can be found in the ADuC812 technical datasheet (REVA) and the ADuC812 User's Manual (Draft 0.5) available at <http://www.analog.com/microconverter>

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**812\_S08 RESET FUNCTIONALITY WHEN EXECUTING FROM EXTERNAL MEMORY ONLY:**

- Background :** The ADuC812 can be reset using in three ways, namely a. Power cycling the part, b. Toggling the reset pin and c. A watchdog Timeout
- Issue :**
- When executing from external memory only i.e.  $\overline{EA}$  tied low, resetting the ADuC812 by toggling the RESET pin can cause the part to enter an internal emulation mode.
  - When executing from external memory only i.e.  $\overline{EA}$  tied low, a watchdog reset can cause the part to enter an internal emulation mode.
- Work-Around :**
- A subsequent toggle of the reset pin will reset the part.
  - Tying the  $\overline{PSEN}$  pin low through an external pull-down resistor (maximum value = 4KOhm) prevents entry to the emulation mode and correctly resets the ADuC812.
- Related Issues :**
- This issue does not occur when executing code from **internal** memory only.
  - This issue does not occur when executing code from both **internal and external** code memory.
  - This issue does not occur when power cycling the ADuC812.