DC to 12GHz, Differential, Nonreflective, Silicon SPDT Switch

FEATURES

- Frequency range: DC to 12GHz
- DC voltage range: ±8V
- DC R_{ON}: <2.5Ω
- Fully differential 100Ω design
- Low insertion loss
  - 0.65dB typical to 6GHz
  - 0.9dB typical to 10GHz
  - 1.1dB typical to 12GHz
- High isolation (terminated mode)
  - >48 dB typical to 6GHz
  - >41 dB typical to 10GHz
  - >37 dB typical to 12GHz
- High input linearity
  - P0.1dB: 33dBm typical
  - IP3: 51dBm typical
- High power handling
  - 31dBm through path
  - 24dBm terminated path
- On time: 1.9µs
- 0.1dB settling time: 3.2µs
- All off state control
- Termination control: 100Ω differential or high-Z (reflective)
- 22-terminal, 3mm × 3mm, RoHS-compliant, land grid array (LGA) package

APPLICATIONS

- Test instrumentation
- Data converter interfaces
- High data rate interfaces

FUNCTIONAL BLOCK DIAGRAM

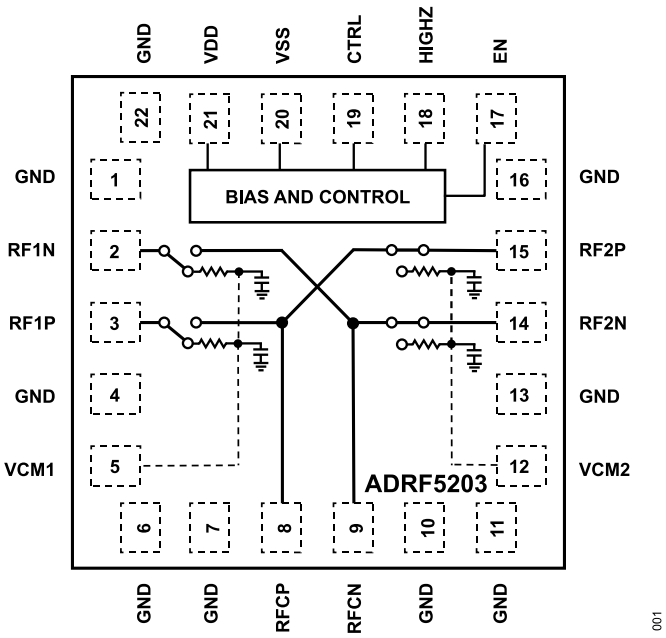

Figure 1. Functional Block Diagram

GENERAL DESCRIPTION

The ADRF5203 is a silicon, differential, SPDT switch. The ADRF5203 operates from DC to 12GHz with an insertion loss of better than 1.1dB and an isolation higher than 37dB. The device has a DC input voltage range of ±8 V and RF input power handling of differential 31dBm for through paths and 24dBm for terminated paths.

The ADRF5203 operates with dual-supply voltages of ±12V. The ADRF5203 employs complementary metal-oxide semiconductor (CMOS)- and low voltage transistor logic (LVTTL)-compatible controls. The ADRF5203 has an enable control to feature its all off state function. The high-Z control selects the termination (100Ω or high-Z) on the unselected RF channel.

The ADRF5203 comes in a 22-terminal, 3mm × 3mm, RoHS compliant, land grid array (LGA) package and can operate from −40°C to +105°C.

One Analog Way, Wilmington, MA 01887-2356, U.S.A.

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REVISION HISTORY

5/2026—Rev. 0 to Rev. A

Change to Figure 25.... 12

10/2025—Revision 0: Initial Version

SPECIFICATIONS

VDD = 12V, VSS = −12V, CTRL, EN, and HIGHZ = 0V or 3.3V, and T_{CASE} = 25°C, with a 100Ω differential system, unless otherwise noted. RFC refers to the RFCP and RFCN differential pair, RF1 refers to the RF1P and RF1N differential pair, RF2 refers to the RF2P and RF2N differential pair, and RFx refers the RF1 and RF2 differential pairs.

Table 1. Electrical Specifications

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
FREQUENCY RANGE	f		0		12	GHz
INSERTION LOSS						
RFC and RFx (On)		DC to 6GHz		0.65		dB
		6GHz to 10GHz		0.9		dB
		10GHz to 12GHz		1.1		dB
RETURN LOSS						
RFC (On)		DC to 6GHz		18		dB
		6GHz to 10GHz		15		dB
		10GHz to 12GHz		13		dB
RFx (On)		DC to 6GHz		19		dB
		6GHz to 10GHz		16		dB
		10GHz to 12GHz		13		dB
RFx (Terminated)		DC to 6GHz		16		dB
		6GHz to 10GHz		14		dB
		10GHz to 12GHz		13		dB
ISOLATION						
RFC to RFx (Terminated)		DC to 6GHz		48		dB
		6GHz to 10GHz		41		dB
		10GHz to 12GHz		37		dB
RFC to RFx (HIGHZ)		DC to 6GHz		45		dB
		6GHz to 10GHz		36		dB
		10GHz to 12GHz		32		dB
RFx to RFx (Terminated)		DC to 6GHz		49		dB
		6GHz to 10GHz		42		dB
		10GHz to 12GHz		37		dB
RFx to RFx (HIGHZ)		DC to 6GHz		55		dB
		6GHz to 10GHz		43		dB
		10 GHz to 12GHz		35		dB
DC CHARACTERISTICS		Single ended				
RFC to RFx On Resistance	R_{ON}	RFCP to RF1P and RFCN to RF1N		2.5		Ω
RFC to RFx Off Resistance	R_{OFF}	RFCP to RF1P and RFCN to RF1N		1.2		MΩ
RFC to GND	R_{CG}	RFCP to GND and RFCN to GND		>30		MΩ
RFx to GND	R_{XG}	RF1P to GND and RF1N to GND		>30		MΩ
SWITCHING CHARACTERISTICS						
Rise and Fall Time	t_{RISE}, t_{FALL}	10% to 90% of RF output		400		ns
On Time	t_{ON}	50% CTRL voltage (V_{CTRL}) to 90% of RF output		1.9		µs
Off Time	t_{OFF}	50% V_{CTRL} to 10% of RF output		1.1		µs
0.1dB Settling Time	$t_{SETTLING}$	50% V_{CTL} to 0.1 dB of final RF output		3.2		µs
INPUT LINEARITY [1]						
0.1dB Power Compression	P0.1dB	100MHz to 10GHz		34		dBm
		10GHz to 12GHz		33		dBm

SPECIFICATIONS

Table 1. Electrical Specifications (Continued)

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Third-Order Intercept	IP3	100MHz to 10GHz, two-tone Input power = 15dBm each tone, Δf = 1MHz		53		dBm
		10GHz to 12GHz , two-tone input power = 15dBm each tone, Δf = 1MHz		51		dBm
RF IMBALANCE						
Amplitude		DC to 12GHz		<0.3		dB
Phase		DC to 12GHz		<8		Degrees
POWER SUPPLY REJECTION	PSRR	1MHz				
Unfiltered		Without supply decoupling capacitors		>80		dB
Filtered		With supply decoupling capacitors, C1 = 10µF, C2 = 0.01µF, C3 = 100pF		>140		dB
GROUP DELAY	t_{GD}	100Ω differential, f = 12GHz		45		ps
SUPPLY CURRENTS						
Positive	I_{DD}			19		mA
Negative	I_{SS}			18		mA
DIGITAL CONTROL INPUTS		CTRL, EN, and HIGHZ pins				
Voltage						
Low	V_{INL}		0		0.8	V
High	V_{INH}		1.2		3.3	V
Current						
Low	I_{INL}			<1		µA
High	I_{INH}			<1		µA
RECOMMENDED OPERATING CONDITIONS		f = 100MHz to 10GHz, T_{CASE} = 85°C, −8V < common-mode voltage (V_{CM}) < +8V				
Supply Voltage						
Positive	V_{DD}		11.4		12.6	V
Negative	V_{SS}		−12.6		−11.4	V
DC Input						
Voltage Range	V_{DC}	RFCP, RFCN, RF1P, RF1N, RF2P, and RF2N	−8		+8	V
Current Range	I_{DC}		−160		+160	mA
Common-Mode Voltage Range	V_{CM}	VCM1 and VCM2	−8		+8	V
RF Input Power [1,2,3,4]	P_{IN}	f = 100MHz to 10GHz, T_{CASE} = 85°C, −8V < V_{CM} < +8V				
Through Path		RF signal is applied to RFC or through connected RFx			31	dBm
Terminated Path		RF signal is applied to unselected RFx (terminated within an internal resistor)				
Average					24	dBm
Peak[5]					31	dBm
Hot Switching		RF signal is applied to RFC or RFx while switching in between RF1 and RF2.			24	dBm
Case Temperature	T_{CASE}		−40		+105	°C

[1] For power derating over frequency, see Figure 2 and Figure 3.

[2] For power derating where a different DC voltage is applied for the selected and unselected RF channels, see Figure 4.

[3] For the case where different DC voltages are applied at the positive and negative pins of the RF pair, see Figure 5.

[4] For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3dB.

[5] Peak is ≤100ns pulse duration and 5% duty cycle.

ABSOLUTE MAXIMUM RATINGS

For recommended operating conditions, see Table 1.

Table 2. Absolute Maximum Ratings

Parameter	Rating
Supply Voltage	
Positive	−0.3V to +13.2V
Negative	−13.2V to +0.3V
Digital Control Inputs [1]	
Voltage	−0.3V to +3.6V
Current	3mA
RF Input Power [2, 3] (VDD = 12V, VSS = −12V, f = 100MHz to 10GHz, T_{CASE} = 85°C[4])	
Through Path	31.5dBm
Terminated Path	
Average	24.5dBm
Peak[5]	31.5dBm
Hot Switching	24.5dBm
RF Input Power, Unbiased (VDD and VSS = 0V)	30.5dBm
Temperature	
Junction, T_J	135°C
Storage Range	−65°C to +150°C
Reflow	260°C

1 Overvoltages at digital control inputs are clamped by internal diodes. Current must be limited to the maximum rating given.

2 For power derating over frequency, see Figure 2 and Figure 3.

3 For power derating over DC voltages, see Figure 4 and Figure 5.

4 For 105°C operation, the power handling degrades from the T_{CASE} = 85°C specification by 3dB.

5 Peak is ≤100ns pulse duration and 5% duty cycle.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case bottom (channel to package bottom) thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}[1]	Unit
CC-22-5		
Through Path	49	°C/W
Terminated Path	72	°C/W

1 θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel through the round pad to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

POWER DERATING CURVES

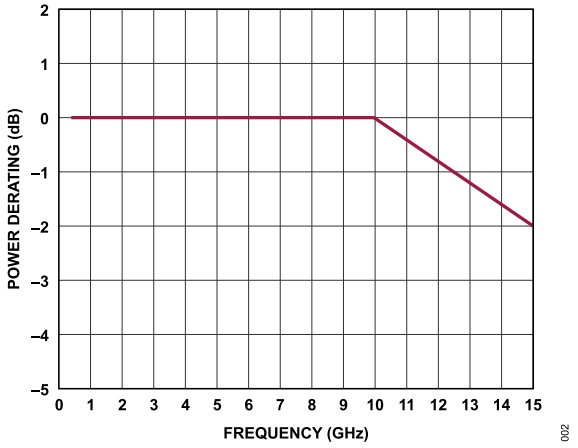

Figure 2. Maximum RF Power Derating vs. Frequency, T_{CASE} = 85°C

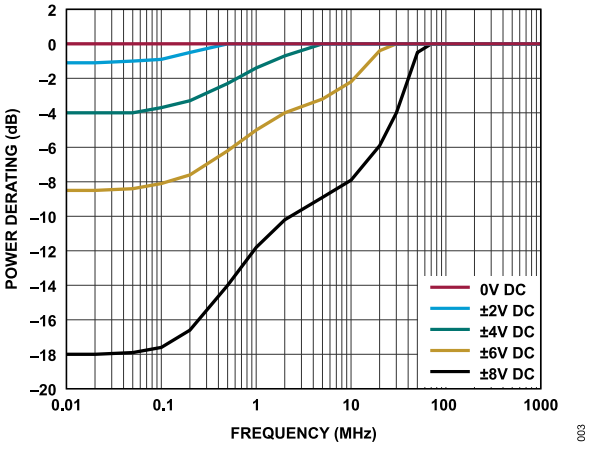

Figure 3. Maximum RF Power Derating vs. Frequency over V_{DC}, T_{CASE} = 85°C (Low Frequency)

ABSOLUTE MAXIMUM RATINGS

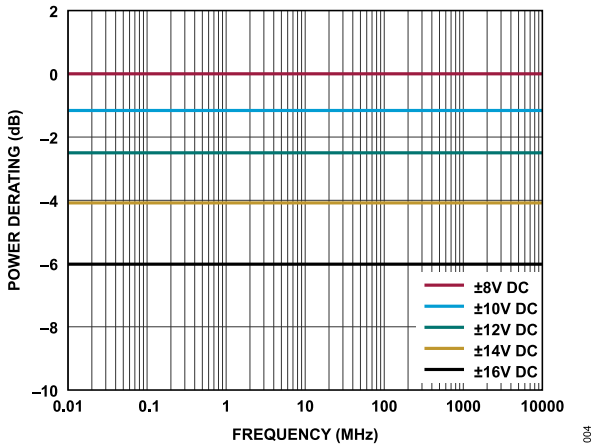

Figure 4. Maximum RF Power Derating vs. Frequency over V_{DC} (Selected Channel) − V_{DC} (Unselected Channel), T_{CASE} = 85°C

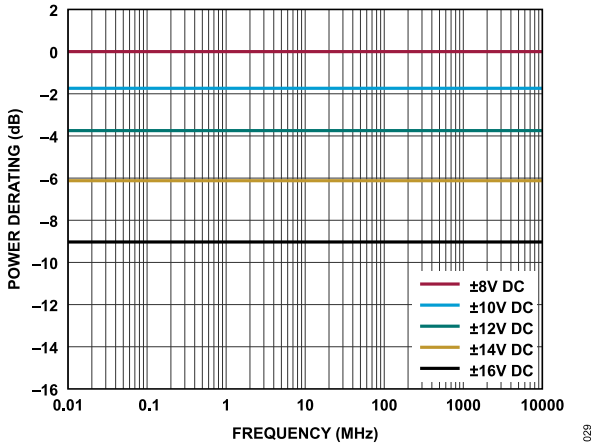

Figure 5. Maximum RF Power Derating vs. Frequency over Differential V_{DC} ($V_{DC\_DIFFERENTIAL}$) = (RFxP Pins VDC (V_{DC_RFxP}) − RFxN Pins VDC (V_{DC_RFxN}), T_{CASE} = 85°C, Where x Refers to Each RF Pair

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDEC JS-001.

Charged device model (CDM) ratings are per ANSI/ESDA/JEDEC JS-002.

ESD Ratings for the ADRF5203

Table 4. ADRF5203, 22-Terminal LGA

ESD Model	Withstand Threshold (V)	Class
HBM	±500 for the RFCN, RFCP, RF1P, RF1N, RF2P, and RF2N pins	1A
	±1500 for the supply and digital control pins	1C
CDM	±500 for all pins	C2A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

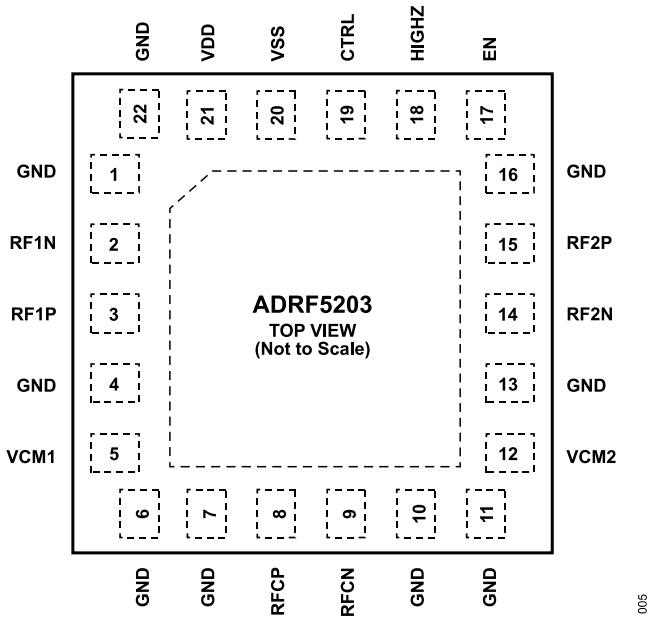

Figure 6. Pin Configuration (Top View)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 6, 7, 10, 11, 13, 16, 22	GND	Ground. The GND pins must be connected to the RF and DC ground of the PCB.
2, 3, 8, 9, 14, 15	RF1N, RF1P, RFCP, RFCN, RF2N, RF2P	Negative and Positive RF Pins. These pins are DC-coupled and AC matched to differential 100Ω. See Figure 7 for the interface schematic.
5, 12	VCM1, VCM2	DC Common-Mode Monitoring Pins. See Figure 11 for the interface schematic
17	EN	Enable Input. See Table 6 for the truth table and Figure 9 for the interface schematic.
18	HIGHZ	The HIGHZ pin sets the termination type of the unselected channel. See Table 6 for the truth table and Figure 9 for the interface schematic.
19	CTRL	Digital Input to Control the RF Path State. See Table 6 for the truth table and Figure 9 for the interface schematic.
20	VSS	Negative Supply Voltage. See Figure 10 for the interface schematic .
21	VDD	Positive Supply Voltage. See Figure 8 for the interface schematic.
	EPAD	Exposed Pad. The exposed pad must be connected to the RF and DC ground.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

INTERFACE SCHEMATICS

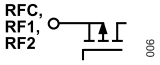

Figure 7. RFC, RF1, and RF2 Interface Schematic

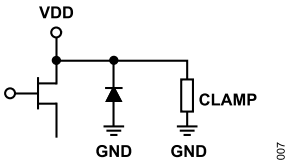

Figure 8. VDD Interface Schematic

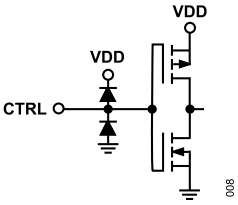

Figure 9. CTRL, EN, and HIGHZ Interface Schematic

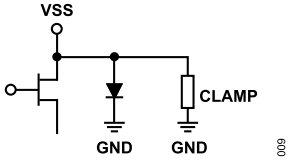

Figure 10. VSS Interface Schematic

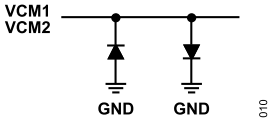

Figure 11. VCM1 and VCM2 Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

INSERTION LOSS, RETURN LOSS, AND ISOLATION

VDD = 12V, VSS = −12V, CTRL, EN, and HIGHZ = 0V or 3.3V, and T_{CASE} = 25°C, with a 100Ω differential system, unless otherwise noted.

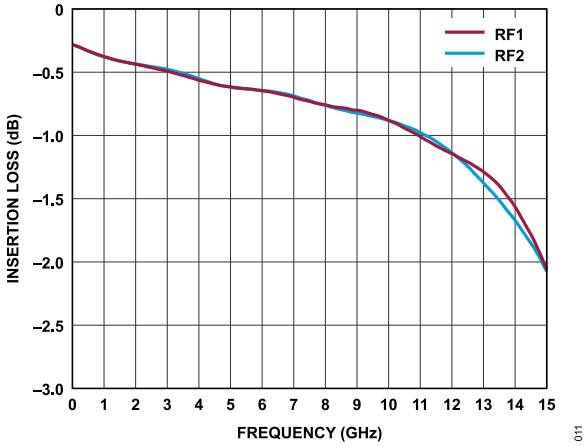

Figure 12. Insertion Loss vs. Frequency

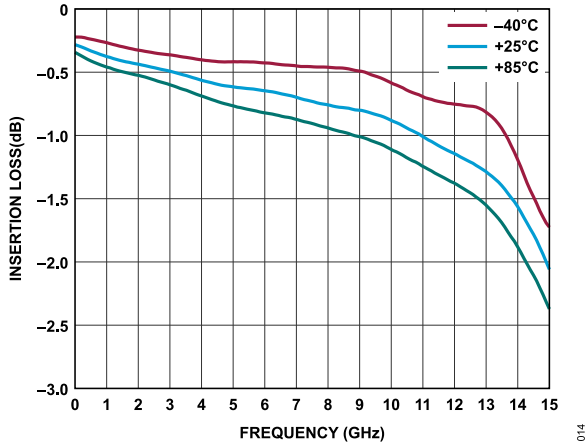

Figure 15. Insertion Loss vs. Frequency over Temperature

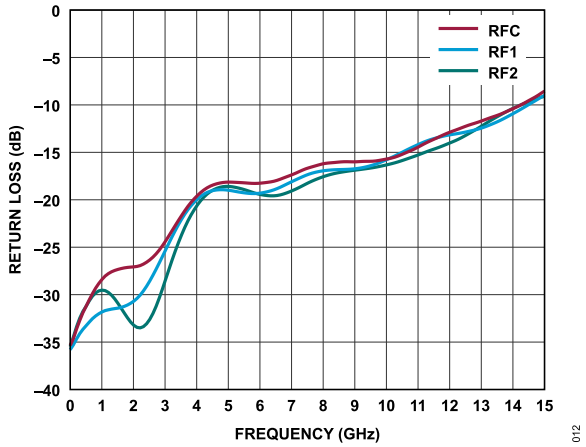

Figure 13. Return Loss vs. Frequency (On Channel)

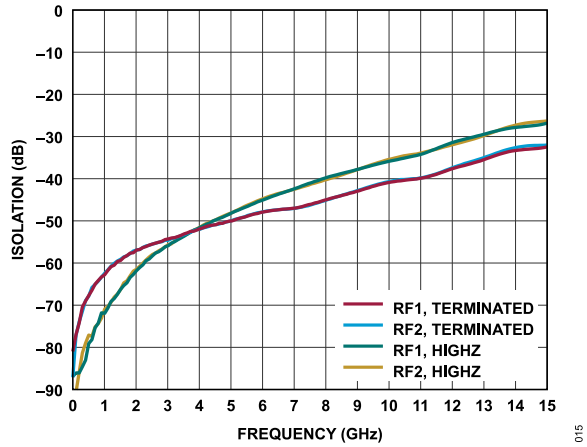

Figure 16. Isolation vs. Frequency (RFC to RF1 and RF2)

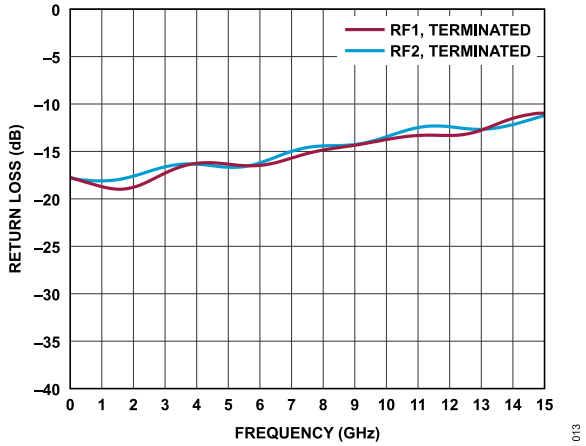

Figure 14. Return Loss vs. Frequency (Off Channel, Terminated)

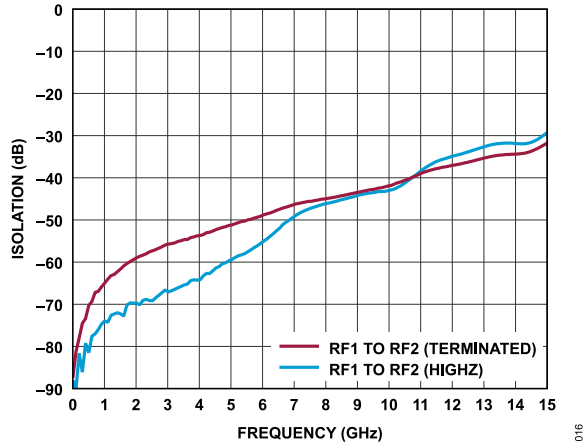

Figure 17. Isolation vs. Frequency (RF1 to RF2)

TYPICAL PERFORMANCE CHARACTERISTICS

AMPLITUDE IMBALANCE, PHASE IMBALANCE, GROUP DELAY, EYE DIAGRAM, AND PSRR

VDD = 12V, VSS = −12V, CTRL, EN, and HIGHZ = 0V or 3.3V, and T_{CASE} = 25°C, with a 100Ω differential system, unless otherwise noted.

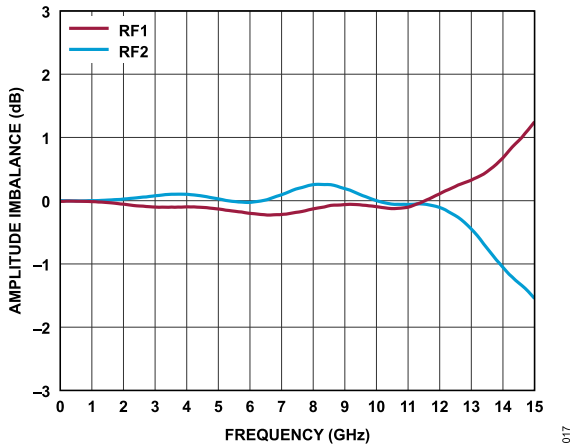

Figure 18. Amplitude Imbalance vs. Frequency

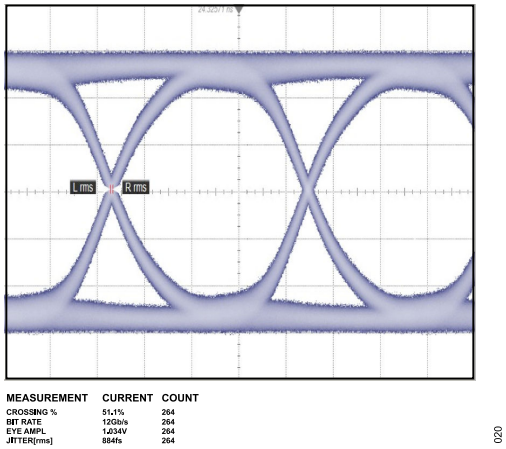

Figure 21. Eye Diagram, PRBS23, 12Gbps

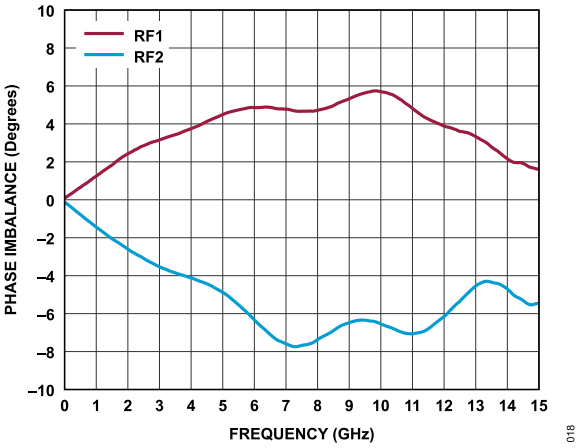

Figure 19. Phase Imbalance vs. Frequency

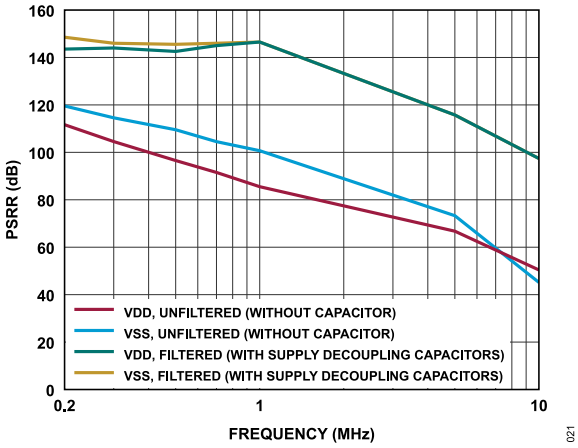

Figure 22. PSRR vs. Frequency

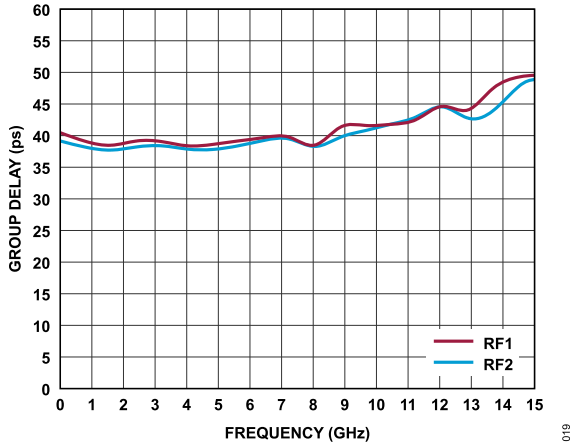

Figure 20. Group Delay vs. Frequency

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT POWER COMPRESSION AND THIRD-ORDER INTERCEPT

VDD = 12V, VSS = −12V, CTRL, EN, and HIGHZ = 0V or 3.3V, and T_{CASE} = 25°C, with a 100Ω differential system, unless otherwise noted.

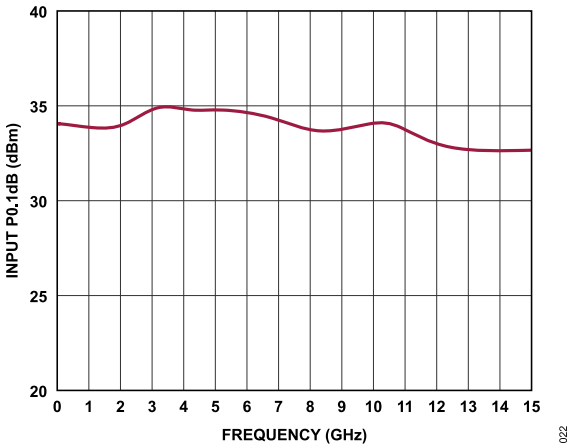

Figure 23. Input P0.1dB vs. Frequency

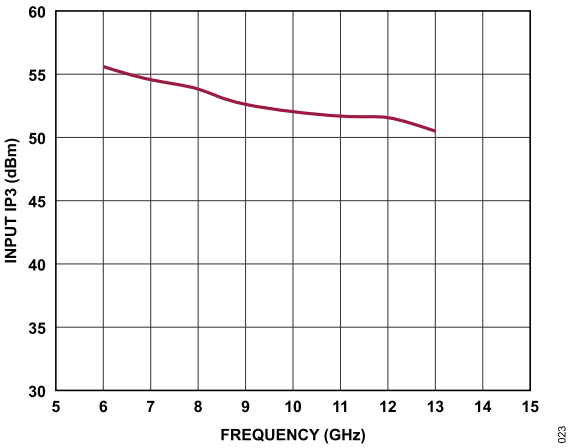

Figure 24. Input IP3 vs. Frequency

THEORY OF OPERATION

The ADRF5203 integrates a driver to perform logic functions internally to provide the advantage of a simplified CMOS-/LVTTL-compatible control interfaces. The CTRL pin determines which RF port is in the insertion loss state and in the isolation state. The EN pin selects the all off state of the ADRF5203 . When the EN pin is at logic high, both the RFC to RF1 and RFC to RF2 paths are in the isolation state. The HIGHZ pin allows the user to choose between 100Ω or high-Z termination for the unselected channel. See Table 6 for the control voltage truth table.

DIFFERENTIAL RF INPUTS AND OUTPUTS

The ADRF5203 is a fully differential 100Ω design. The RF pins are DC coupled. DC levels of all the RF lines are 0V when there is no input. When RF1 is selected, RFCN is connected to RF1N, and RFCP is connected to RF1P. When RF2 is selected, RFCN is connected to RF2N and RFCP is connected to RF2P.

DC OPERATION

The RF ports are DC-coupled and can support a DC voltage range of ±8V. Figure 25 shows the DC equivalent circuit for the selected and unselected channels.

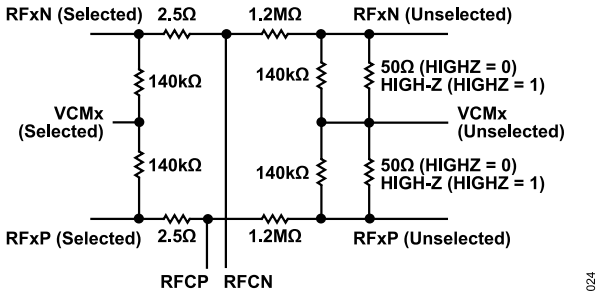

Figure 25. DC Equivalent Circuit

The VCM1 and VCM2 pins can be used to set or monitor the DC common-mode voltage on the RF ports. The VCMx pins can be left floating or can be decoupled to ensure a low impedance common-mode AC ground.

The VCMx pins are internally connected to the RF ports via high impedance, see Figure 25. When the input signal is driven DC-coupled from the RFC port or the RFx port, the selected RFx port follows the input signal;therefore, V_{CM} is set by the input signal.

The V_{CM} on the unselected channel can be set via the VCMx pins. This feature can be used to match the DC level of connected circuitry. The V_{CM} on the selected channel can also be set at the VCMx pins if the input signal is AC-coupled.

Power derating must be applied in applications where the common-mode voltage of selected and unselected channels differ by more than 8V, see Figure 4.

RF POWER HANDLING

The RF power handling of the ADRF5203 derates over frequencies below 100 MHz and derating is dependent on the applied DC voltage . See Figure 3 for power derating towards lower frequencies for different DC input voltages. For low frequency operation, the device ensures a constant R_{ON} on the selected channel.

For frequencies higher than 100MHz, both the maximum DC voltage and maximum RF power can be applied at the same time. See Figure 2 for power derating frequencies higher than 10GHz.

For use cases where different common-mode DC voltages are applied at the selected and unselected RF channels, apply the power derating shown in Figure 4.

The ADRF5203 is designed as bidirectional with equal power handling capabilities on RFC and RFx ports. Either port can be used as an input or as output.

THEORY OF OPERATION

POWER SUPPLY

The ADRF5203 requires a positive supply voltage applied to the VDD pin, and a negative supply voltage applied to the VSS pin. Bypassing capacitors are recommended on the supply lines to filter high frequency noise.

The ideal power-up sequence is as follows:

1. Connect GND.
2. Power up VDD and VSS. Power up VSS after VDD to avoid current transients on VDD during ramp up.
3. Power up the digital control inputs. The relative order of the logic control inputs is not important. However, powering the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures.
4. Apply digital control inputs. The relative order of the control inputs is not important. However, powering the digital control inputs before the V_{DD} supply can inadvertently forward bias and damage the internal ESD protection structures. To avoid this damage, use series 1kΩ resistors to limit the current flowing into the control pins. Use pull-up or pull-down resistors if the controllers are in a high impedance state after VDD is powered up, and the control pins are not driven to a valid logic state.

The ideal power-down sequence is the reverse order of the power-up sequence.

Table 6. Control Voltages Truth Table

Digital Control Inputs			RF Paths	
EN	**HIGHZ**	**CTRL**	**RFC to RF1**	**RFC to RF2**
Low	Low	Low	Insertion loss	Isolation (terminated)
Low	Low	High	Isolation (terminated)	Insertion loss
Low	High	Low	Insertion loss	Isolation (reflective)
Low	High	High	Isolation (reflective)	Insertion loss
High	Low	Not applicable	Isolation (terminated)	Isolation (terminated)
High	High	Not applicable	Isolation (reflective)	Isolation (reflective)

APPLICATIONS INFORMATION

Figure 26 shows the external components and connections for the ADRF5203. The VDD and VSS pins are decoupled with a 100pF, 0.01µF, and 10µF capacitors. The device pinout allows the placement of the decoupling capacitors close to the device. The VCMx pins can be decoupled to ground or biased with voltage depending on the use case.

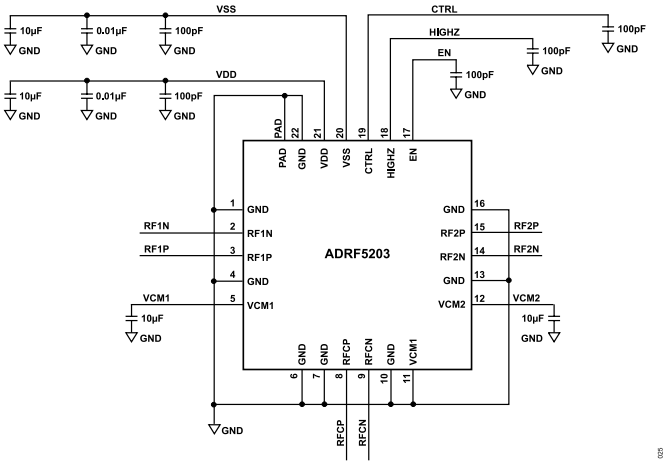

Figure 26. Recommended Schematic

RECOMMENDATIONS FOR PCB DESIGN

The ADRF5203 is designed to mate with 50Ω characteristic impedance on each of the RF pins. The RF ports are matched to differential 100Ω internally.

Figure 27 shows the reference coplanar waveguide (CPWG) RF trace design for an RF substrate with 8mil thick, Rogers RO4003 dielectric material. The RF trace with a 14mil width and a 7mil clearance is recommended for 1.5mil finished copper thickness.

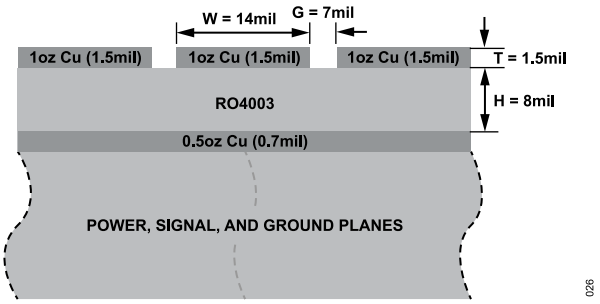

Figure 27. Recommended Stack-Up

Figure 28 shows the routing of the RF traces, supply, and control signals from the device. The ground planes are connected with densely filled through vias for optimal RF and thermal performance. The primary thermal path for the device is the bottom side.

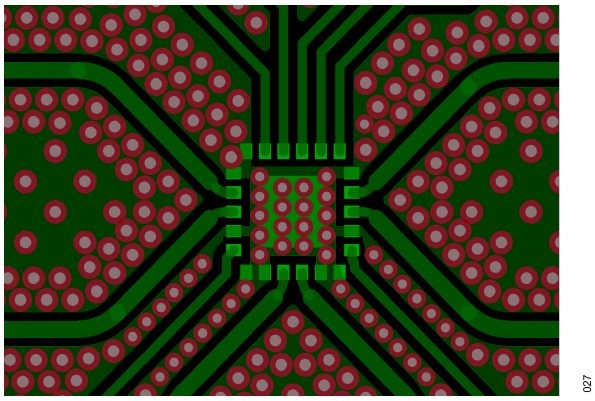

Figure 28. PCB Layout

Figure 29 shows the recommended layout from the device RF pins to the 50Ω CPWG on the referenced stack-up. PCB pads are drawn 1:1 to device pads. The ground pads are drawn solder mask defined, and the signal pads are drawn as pad defined. The RF trace from the PCB pad is extended with the same width until the package edge and tapered to the RF trace. The paste mask is designed to match the device pads without any aperture reduction. The paste mask is divided into multiple openings for the paddle.

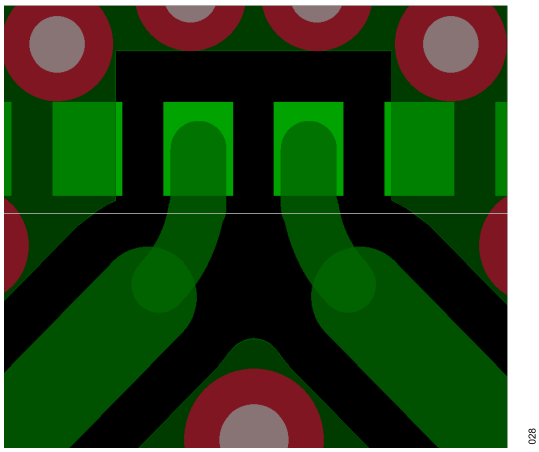

Figure 29. Recommended RF Pin Transition

For alternate PCB stack-ups with different dielectric thickness and RF trace design, contact Analog Devices, Inc., Technical Support for further recommendations.

OUTLINE DIMENSIONS

Package Drawing Option	Package Type	Package Description
CC-22-5	LGA	22-Terminal Land Grid Array

For the latest package outline information and land patterns (footprints), go to Package Index.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Packing Quantity	Package Option
ADRF5203BCCZN	−40°C to +105°C	22-Terminal Land Grid Array [LGA]	Reel, 500	CC-22-5
ADRF5203BCCZN-R7	−40°C to +105°C	22-Terminal Land Grid Array [LGA]	Reel, 500	CC-22-5

[1] Z = RoHS Compliant Part.