FEATURES

Extreme high temperature operation
−40°C to +210°C, 8-lead FLATPACK
−40°C to +175°C, 8-lead SOIC

Temperature coefficient
40 ppm/°C, 8-lead FLATPACK
10 ppm/°C, 8-lead SOIC

High output current: 10 mA
Low supply current: 50 µA maximum

Initial accuracy: ±0.4% (±10 mV maximum), 8-lead SOIC
Low dropout voltage
Wide supply range: 3.3 V to 16 V

APPLICATIONS

Down-hole drilling and instrumentation
Avionics
Heavy industrial
High temperature environments

GENERAL DESCRIPTION

The ADR225 is a precision 2.5 V band gap voltage reference specified for a high temperature operation of 175°C and 210°C. It uses a micropower core topology and laser trimming of highly stable, thin film resistors to achieve a temperature coefficient of 30 ppm/°C (maximum) up to 175°C and an initial accuracy of 0.4% (±10 mV maximum). A maximum operating current of 50 µA and a low dropout voltage allow the ADR225 to function very well in battery-powered equipment.

The ADR225 voltage reference is offered in an 8-lead SOIC package with an operating temperature range of −40°C to +175°C. It is also available in an 8-lead ceramic flat pack (FLATPACK) with an operating temperature range of −40°C to +210°C. Both devices are designed for robustness at extreme temperatures and are qualified for 1000 hours of operation at the maximum temperature rating.

The ADR225 is a member of a growing series of high temperature qualified products offered by Analog Devices, Inc. For a complete selection table of the available high temperature products, see the high temperature product list and qualification data available at www.analog.com/hightemp.
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REVISION HISTORY

11/13—Rev. A to Rev. B
  Change to Features Section .................................. 1
  Added Caption to Figure 1 .................................... 1
  Changes to Table 1 .............................................. 3
  Added Figure 6, Figure 7, Figure 8, Figure 12, Figure 13,
  Figure 14, Figure 18, and Figure 19; Renumbered
  Sequentially ..................................................... 5

9/13—Rev. 0 to Rev. A
  Changes to Data Sheet Title and Added Wide Supply Range: 3.3 V
to 16 V to Features Section ................................... 1
  Changed Supply Voltage from −0.3 V to +15 V to −0.3 V to
  +18 V; Table 2 .................................................. 4

7/13—Revision 0: Initial Version
## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS

$V_S = 3.3\,V$, $V_{OUT} = 2.5\,V$, $T_{MIN} < T_A < T_{MAX}$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>8-Lead SOIC $-40^\circ C \leq T_A \leq +175^\circ C$</th>
<th>8-Lead FLATPACK $-40^\circ C \leq T_A \leq +210^\circ C$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>SUPPLY CURRENT</td>
<td>$I_{SY}$</td>
<td>No load</td>
<td>Min  30  Typ  50  Max  40  60</td>
<td>Min  30  Typ  40  Max  60  80</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>INITIAL ACCURACY$^1$</td>
<td>$V_O$</td>
<td>$I_{OUT} = 0,mA$</td>
<td>Min  2  Typ  10  Max  5  60</td>
<td>Min  2  Typ  5  Max  60  80</td>
<td>$mV$</td>
</tr>
<tr>
<td>TEMPERATURE COEFFICIENT$^2$</td>
<td>$TC_{OUT}$</td>
<td>$I_{OUT} = 0,mA$</td>
<td>Min  10  Typ  30  Max  40  80</td>
<td>Min  10  Typ  40  Max  80  100</td>
<td>ppm/$^\circ C$</td>
</tr>
<tr>
<td>REGULATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Line Regulation</td>
<td>$\Delta V_{OUT}/\Delta V_N$</td>
<td>$3.0,V \leq V_S \leq 15,V$, $I_{OUT} = 0,mA$</td>
<td>Min  0.025  Typ  0.1  Max  0.25  1.5</td>
<td>Min  0.025  Typ  0.1  Max  0.25  1.5</td>
<td>$mV/V$</td>
</tr>
<tr>
<td>Load Regulation$^3$</td>
<td>$\Delta V_{OUT}/\Delta I_{LOAD}$</td>
<td>$V_S = 5.0,V$, $0,mA \leq I_{OUT} \leq 10,mA$</td>
<td>Min  0.025  Typ  0.1  Max  0.25  1.5</td>
<td>Min  0.025  Typ  0.1  Max  0.25  1.5</td>
<td>$mV/mA$</td>
</tr>
<tr>
<td>VOLTAGE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td>$V_S-V_{OUT}$</td>
<td>$I_{LOAD} = 10,mA$</td>
<td>Min  1.00  Max  1.00</td>
<td>Min  1.00  Max  1.00</td>
<td>$V$</td>
</tr>
<tr>
<td>Noise Voltage</td>
<td>$\epsilon_N$</td>
<td>$0.1,Hz$ to $10,Hz$</td>
<td>Min  25  Max  25</td>
<td>Min  25  Max  25</td>
<td>$\mu V$ p-p</td>
</tr>
</tbody>
</table>

$^1$ For proper operation, a 1 $\mu F$ capacitor is required between the OUTPUT pin and the GND pin of the device.

$^2$ $TC_{OUT}$ is defined as the ratio of output change with temperature variation to the specified temperature range expressed in ppm/$^\circ C$.

$^3$ $TC_{OUT} = (V_{MAX} - V_{MIN})/V_{OUT}(T_{MAX} - T_{MIN})$.

$^4$ Load regulation specification includes the effect of self-heating.
ABSOLUTE MAXIMUM RATINGS

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>−0.3 V to +18 V</td>
</tr>
<tr>
<td>OUTPUT to GND</td>
<td>−0.3 V to V_F + 0.3 V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
</tr>
<tr>
<td>8-Lead SOIC</td>
<td>−40°C to +175°C</td>
</tr>
<tr>
<td>8-Lead FLATPACK</td>
<td>−40°C to +210°C</td>
</tr>
<tr>
<td>Junction Temperature Range</td>
<td></td>
</tr>
<tr>
<td>8-Lead SOIC</td>
<td>−40°C to +200°C</td>
</tr>
<tr>
<td>8-Lead FLATPACK</td>
<td>−40°C to +245°C</td>
</tr>
<tr>
<td>Lead Temperature (Soldering 60 sec)</td>
<td>300°C</td>
</tr>
</tbody>
</table>

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PREDICTED LIFETIME vs. OPERATING TEMPERATURE

Comprehensive reliability testing is performed on the ADR225. Product lifetimes at extended operating temperature are obtained using high temperature operating life (HTOL). Lifetimes are predicted from the Arrhenius equation, taking into account potential design and manufacturing failure mechanism assumptions. HTOL is performed to JEDEC JESD22-A108. A minimum of three wafer fab and assembly lots are processed through HTOL at the maximum operating temperature. Comprehensive reliability testing is performed on all Analog Devices, Inc., high temperature (HT) products.

Table 3.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>θ_JA</th>
<th>θ_JC</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Lead SOIC</td>
<td>121</td>
<td>43</td>
<td>°C/W</td>
</tr>
<tr>
<td>8-Lead FLATPACK</td>
<td>100</td>
<td>15</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

THERMAL RESISTANCE

θ_JA is specified for worst-case conditions; that is, θ_JA is specified for the device soldered in the circuit board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
TYPICAL PERFORMANCE CHARACTERISTICS

$V_s = 3.3\, \text{V, } V_{\text{OUT}} = 2.5\, \text{V, } T_{\text{MIN}} \leq T_A \leq T_{\text{MAX}}$ for 8-lead SOIC package, unless otherwise noted.

Figure 3. Output Voltage ($V_{\text{OUT}}$) vs. Temperature

Figure 4. $TC_{\text{OUT}}$ Distribution, $-40^\circ\text{C}$ to $+175^\circ\text{C}$

Figure 5. Output Voltage Accuracy at $175^\circ\text{C}$

Figure 6. Output Voltage ($V_{\text{OUT}}$) vs. Temperature, FLATPACK Package

Figure 7. $TC_{\text{OUT}}$ Distribution, $-40^\circ\text{C}$ to $+210^\circ\text{C}$, FLATPACK Package

Figure 8. Output Voltage Accuracy at $210^\circ\text{C}$, FLATPACK Package
Figure 9. Supply Current (ISY) vs. Temperature

Figure 10. Load Regulation vs. Temperature (ILOAD = 0 mA to 10 mA)

Figure 11. Line Regulation vs. Temperature

Figure 12. Supply Current (ISY) vs. Temperature, FLATPACK Package

Figure 13. Load Regulation vs. Temperature (ILOAD = 0 mA to 10 mA), FLATPACK Package

Figure 14. Line Regulation vs. Temperature, FLATPACK Package
Figure 15. Dropout Voltage vs. Load Current ($I_{LOAD}$)

Figure 16. Thermal Hysteresis, $I_{LOAD} = 0$ mA

Figure 17. Power-On Response (see Figure 25)

Figure 18. Dropout Voltage vs. Load Current ($I_{LOAD}$), FLATPACK Package

Figure 19. Thermal Hysteresis, $I_{LOAD} = 0$ mA, FLATPACK Package

Figure 20. Line Transient Response (see Figure 25)
Figure 21. Load Transient Response

Figure 22. Power Supply Rejection Ratio (PSRR) vs. Frequency, $C_{LOAD} = 1 \, \mu F$

Figure 23. Output Impedance ($Z_{OUT}$) vs. Frequency, $C_{IN} = C_{OUT} = 1 \, \mu F$
THEORY OF OPERATION

BASIC VOLTAGE REFERENCE CONNECTIONS

The circuit shown in Figure 24 is the basic configuration for the ADR225. Note that a 10 µF and 0.1 µF bypass network on the input and at least a 1 µF bypass capacitor on the output are required for proper device operation. It is recommended that no connections be made to Pin 1, Pin 3, Pin 5, Pin 7, and Pin 8.

Figure 24. Basic Voltage Reference Connections

Figure 25. Typical High Temperature Resistance Temperature Detector (RTD) Signal Conditioning Circuit
OUTLINE DIMENSIONS

Figure 26. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

Figure 27. 8-Lead Ceramic Flat Package [FLATPACK] (F-8-2)

Dimensions shown in inches

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADR225HRZN</td>
<td>−40°C to +175°C</td>
<td>8-Lead Standard Small Outline Package [SOIC_N]</td>
<td>R-8</td>
</tr>
<tr>
<td>ADR225HFZ</td>
<td>−40°C to +210°C</td>
<td>8-Lead Ceramic Flat Package [FLATPACK]</td>
<td>F-8-2</td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.