The ADPA7005CHIP is a gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT), monolithic microwave integrated circuit (MMIC), distributed power amplifier that operates from 20 GHz to 44 GHz. The amplifier provides 17 dB of small signal gain, 31 dBm output power for 1 dB compression (P1dB), and a typical output third-order intercept (IP3) of 41 dBm. The ADPA7005CHIP requires 1200 mA from a 5 V supply on the supply voltage (VDD) and features inputs and outputs that are internally matched to 50 Ω, facilitating integration into multichip modules (MCMs). All data is taken with the chip connected via two 0.025 mm wire bonds that are at least 0.31 mm long.
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REVcISION HISTORY

2/2019—Revision 0: Initial Version
### SPECIFICATIONS

#### 20 GHz TO 34 GHz FREQUENCY RANGE

$T_a = 25^\circ C$, $V_{DD} = 5$ V, and quiescent supply current ($I_{DQ}$) = 1200 mA for nominal operation, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>FREQUENCY RANGE</td>
<td></td>
<td>20</td>
<td>34</td>
<td></td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>GAIN</td>
<td></td>
<td>15</td>
<td>17</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Flatness</td>
<td></td>
<td>±0.5</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td></td>
<td>0.012</td>
<td></td>
<td></td>
<td>dB/°C</td>
<td></td>
</tr>
<tr>
<td>NOISE FIGURE</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td></td>
<td>18</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td>20</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Power for 1 dB Compression</td>
<td>$P_{1\text{dB}}$</td>
<td>28</td>
<td>31</td>
<td></td>
<td>dBm</td>
<td>Measurement taken at output power ($P_{OUT}$) per tone = 14 dBm</td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>$P_{SAT}$</td>
<td>32</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Output Third-Order Intercept</td>
<td>$I_{P3}$</td>
<td>41</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>NOISE FIGURE</td>
<td></td>
<td>6</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td>17</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Power for 1 dB Compression</td>
<td>$P_{1\text{dB}}$</td>
<td>27</td>
<td>30</td>
<td></td>
<td>dBm</td>
<td>Measurement taken at $P_{OUT}$ per tone = 14 dBm</td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>$P_{SAT}$</td>
<td>31</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Output Third-Order Intercept</td>
<td>$I_{P3}$</td>
<td>40.5</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>$I_{DQ}$</td>
<td>1200</td>
<td></td>
<td></td>
<td>mA</td>
<td>Adjust the gate bias voltage ($V_{GG1}$) between $−1.5$ V up to $0$ V to achieve the desired $I_{DQ}$</td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{DD}$</td>
<td>4</td>
<td>5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
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</table>

#### 34 GHz TO 44 GHz FREQUENCY RANGE

$T_a = 25^\circ C$, $V_{DD} = 5$ V, and $I_{DQ} = 1200$ mA for nominal operation, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions/Comments</th>
</tr>
</thead>
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<td>FREQUENCY RANGE</td>
<td></td>
<td>34</td>
<td>44</td>
<td></td>
<td>GHz</td>
<td></td>
</tr>
<tr>
<td>GAIN</td>
<td></td>
<td>11.5</td>
<td>14.5</td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Flatness</td>
<td></td>
<td>±0.7</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Gain Variation Over Temperature</td>
<td></td>
<td>0.024</td>
<td></td>
<td></td>
<td>dB/°C</td>
<td></td>
</tr>
<tr>
<td>NOISE FIGURE</td>
<td></td>
<td>6</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>RETURN LOSS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input</td>
<td></td>
<td>15</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>Output</td>
<td></td>
<td>17</td>
<td></td>
<td></td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Power for 1 dB Compression</td>
<td>$P_{1\text{dB}}$</td>
<td>27</td>
<td>30</td>
<td></td>
<td>dBm</td>
<td>Measurement taken at $P_{OUT}$ per tone = 14 dBm</td>
</tr>
<tr>
<td>Saturated Output Power</td>
<td>$P_{SAT}$</td>
<td>31</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>Output Third-Order Intercept</td>
<td>$I_{P3}$</td>
<td>40.5</td>
<td></td>
<td></td>
<td>dBm</td>
<td></td>
</tr>
<tr>
<td>SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current</td>
<td>$I_{DQ}$</td>
<td>1200</td>
<td></td>
<td></td>
<td>mA</td>
<td>Adjust $V_{GG1}$ between $−1.5$ V up to $0$ V to achieve the desired $I_{DQ}$</td>
</tr>
<tr>
<td>Voltage</td>
<td>$V_{DD}$</td>
<td>4</td>
<td>5</td>
<td></td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### ABSOLUTE MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain Bias Voltage (V_{DDx})</td>
<td>6.0 V</td>
</tr>
<tr>
<td>(V_{GG})</td>
<td>(-1.5) to (0) V</td>
</tr>
<tr>
<td>Radio Frequency Input Power (RFIN)</td>
<td>27 dBm</td>
</tr>
<tr>
<td>Continuous Power Dissipation (P_{oss}),</td>
<td>13.4 W</td>
</tr>
<tr>
<td>(T = 85^\circ) C (Derate 149.2 mW/°C Above</td>
<td></td>
</tr>
<tr>
<td>85°C)</td>
<td></td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>(-65^\circ) C to +150°C</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>(-55^\circ) C to +85°C</td>
</tr>
<tr>
<td>Electrostatic Discharge (ESD) Sensitivity</td>
<td>Class 1B (passed 500 V)</td>
</tr>
<tr>
<td>Human Body Model (HBM)</td>
<td></td>
</tr>
</tbody>
</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to the printed circuit board (PCB) thermal design is required. \(\theta_{JC}\) is the channel to case thermal resistance, channel to bottom of die using die attach epoxy.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>(\theta_{JC})</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>C-12-3</td>
<td>6.7</td>
<td>°C/W</td>
</tr>
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</table>

### Table 5. Reliability Information

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Temperature (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Junction Temperature to Maintain 1,000,000 Hour Mean Time to Failure (MTTF)</td>
<td>175</td>
</tr>
<tr>
<td>Nominal Junction Temperature (T = 85^\circ) C, (V_{DD} = 5) V, (I_{DD} = 600) mA</td>
<td>125.2</td>
</tr>
</tbody>
</table>

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

**Figure 2. Pin Configuration**

**Table 6. Pin Function Descriptions**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RFIN</td>
<td>RF Signal Input. This pad is ac-coupled and matched to 50 Ω.</td>
</tr>
<tr>
<td>2, 12</td>
<td>VGG1, VGG2</td>
<td>Amplifier Gate Control. External bypass capacitors of 4.7 μF, 0.01 μF, and 100 pF are required. ESD protection diodes are included and turn on below –1.5 V.</td>
</tr>
<tr>
<td>3, 4, 5, 9, 10, 11</td>
<td>VDD5, VDD3, VDD1, VDD2, VDD4, VDD6</td>
<td>Drain Bias for the amplifier. External bypass capacitors of 4.7 μF, 0.01 μF, and 100 pF are required.</td>
</tr>
<tr>
<td>6</td>
<td>VREF</td>
<td>Reference Diode. Use this pin in combination with VDET. The voltage provides temperature compensation to the VDET RF output power measurements.</td>
</tr>
<tr>
<td>7</td>
<td>RFOUT</td>
<td>RF Signal Output. This pad is ac-coupled and matched to 50 Ω.</td>
</tr>
<tr>
<td>8</td>
<td>VDET</td>
<td>Detector Diode Used for Measuring the RF Output Power. Detection via this pin requires the application of a dc bias voltage through an external series resistor. Used in combination with VREF, the difference voltage, VREF – VDET, is a temperature compensated dc voltage proportional to the RF output power.</td>
</tr>
<tr>
<td>Die Bottom</td>
<td>GND</td>
<td>Ground. The pads and die bottom must be connected to RF and dc ground.</td>
</tr>
</tbody>
</table>
INTERFACE SCHEMATICS

Figure 3. GND Interface Schematic

Figure 4. VREF Interface Schematic

Figure 5. VDET Interface Schematic

Figure 6. RFIN Interface Schematic

Figure 7. VGG1, VGG2 Interface Schematic

Figure 8. RFOUT Interface Schematic

Figure 9. VDD1 to VDD6 Interface Schematic
TYPICAL PERFORMANCE CHARACTERISTIC

Figure 10. Gain and Return Loss vs. Frequency, $V_{DD} = 5\, V$, $I_{DDQ} = 1200\, mA$

Figure 11. Gain vs. Frequency for Various $V_{DD}$, $I_{DDQ} = 1200\, mA$

Figure 12. Input Return Loss vs. Frequency for Various Temperatures, $V_{DD} = 5\, V$, $I_{DDQ} = 1200\, mA$

Figure 13. Gain vs. Frequency for Various Temperatures, $V_{DD} = 5\, V$, $I_{DDQ} = 1200\, mA$

Figure 14. Gain vs. Frequency for Various $I_{DDQ}$, $V_{DD} = 5\, V$

Figure 15. Input Return Loss vs. Frequency for Various $V_{DD}$, $I_{DDQ} = 1200\, mA$
Figure 16. Input Return Loss vs. Frequency for Various $I_{DO}$, $V_{DO} = 5$ V

Figure 17. Output Return Loss vs Frequency for Various $V_{DO}$, $I_{DO} = 1200$ mA

Figure 18. Reverse Isolation vs. Frequency for Various Temperatures, $V_{DO} = 5$ V, $I_{DO} = 1200$ mA

Figure 19. Output Return Loss vs. Frequency for Various Temperature, $V_{DO} = 5$ V, $I_{DO} = 1200$ mA

Figure 20. Output Return Loss vs. Frequency for Various $I_{DO}$, $V_{DO} = 5$ V

Figure 21. Noise Figure vs. Frequency for Various Temperatures, $V_{DO} = 5$ V, $I_{DO} = 1200$ mA
Figure 22. Output P1dB vs. Frequency for Various Temperatures, \(V_{DD} = 5\) V, \(I_{Q} = 1200\) mA

Figure 23. P1dB vs. Frequency for Various \(I_{Q}\), \(V_{DD} = 5\) V

Figure 24. PSAT vs. Frequency for Various \(V_{DD}\), \(I_{Q} = 1200\) mA

Figure 25. P1dB vs. Frequency for Various \(V_{DD}\), \(I_{Q} = 1200\) mA

Figure 26. PSAT vs. Frequency for Various Temperatures, \(V_{DD} = 5\) V, \(I_{Q} = 1200\) mA

Figure 27. PSAT vs. Frequency for Various \(I_{Q}\), \(V_{DD} = 5\) V
**Figure 28.** Power Added Efficiency (PAE) at $P_{\text{SAT}}$ vs. Frequency for Various Temperatures, $V_{\text{DD}} = 5\, V$, $I_{\text{DD}} = 1200\, mA$, PAE Measured at $P_{\text{SAT}}$

**Figure 29.** PAE at $P_{\text{SAT}}$ vs. Frequency for Various $I_{\text{DD}}$, $V_{\text{DD}} = 5\, V$, $I_{\text{DD}} = 1200\, mA$, PAE Measured at $P_{\text{SAT}}$

**Figure 30.** $P_{\text{OUT}}$, Gain, PAE, and $I_{\text{DD}}$ vs. Input Power, 26 GHz, $V_{\text{DD}} = 5\, V$, $I_{\text{DD}} = 1200\, mA$

**Figure 31.** PAE at $P_{\text{SAT}}$ vs. Frequency for Various $V_{\text{DD}}$, $I_{\text{DD}} = 1200\, mA$, PAE Measured at $P_{\text{SAT}}$

**Figure 32.** $P_{\text{OUT}}$, Gain, PAE, and $I_{\text{DD}}$ vs. Input Power, 22 GHz, $V_{\text{DD}} = 5\, V$, $I_{\text{DD}} = 1200\, mA$

**Figure 33.** $P_{\text{OUT}}$, Gain, PAE, and $I_{\text{DD}}$ vs. Input Power, 30 GHz, $V_{\text{DD}} = 5\, V$, $I_{\text{DD}} = 1200\, mA$
Figure 34. $P_{\text{OUT}}$, Gain, PAE, and $I_{\text{DD}}$ vs. Input Power, 34 GHz, $V_{\text{DD}} = 5\, \text{V}$, $I_{\text{DD}} = 1200\, \text{mA}$

Figure 37. $P_{\text{OUT}}$, Gain, PAE, and $I_{\text{DD}}$ vs. Input Power, 38 GHz, $V_{\text{DD}} = 5\, \text{V}$, $I_{\text{DD}} = 1200\, \text{mA}$

Figure 35. $P_{\text{OUT}}$, Gain, PAE, and $I_{\text{DD}}$ vs. Input Power, 42 GHz, $V_{\text{DD}} = 5\, \text{V}$, $I_{\text{DD}} = 1200\, \text{mA}$

Figure 38. Power Dissipation vs. Input Power at $T = 85^\circ\text{C}$, $V_{\text{DD}} = 5\, \text{V}$, $I_{\text{DD}} = 1200\, \text{mA}$

Figure 36. Output IP3 vs. Frequency for Various Temperatures, $P_{\text{OUT}}$ per Tone = 14 dBm, $V_{\text{DD}} = 5\, \text{V}$, $I_{\text{DD}} = 1200\, \text{mA}$

Figure 39. Output IP3 vs. Frequency for Various $V_{\text{DD}}$, $P_{\text{OUT}}$ per Tone = 14 dBm, $V_{\text{DD}} = 5\, \text{V}$, $I_{\text{DD}} = 1200\, \text{mA}$
Figure 40. Output IP3 vs Frequency for Various IDQ, POUT per Tone = 14 dBm, VDD = 5 V

Figure 41. Quiescent Drain Supply Current vs. Gate Supply Voltage

Figure 42. Supply Current IDQ vs. Input Power at Various Frequencies, VDD = 5 V, IDQ = 1200 mA

Figure 43. Third-Order Intermodulation (IM3) Distortion Relative to Carrier vs. POUT per Tone, VDD = 4 V, IDQ = 1200 mA

Figure 44. IM3 Distortion Relative to Carrier vs. POUT per Tone, VDD = 5 V, IDQ = 1200 mA

Figure 45. VREF – VDET vs. Output Power for Various Temperatures at 32 GHz
CONSTANT $I_{DD}$ OPERATION

Biased with HMC980LP4E active bias controller (see Figure 55), $T_A = 25^\circ C$, $V_{DD} = 5$ V, and $I_{DD} = 1600$ mA for nominal operation, unless otherwise noted.

Figure 46. $P_{1dB}$ vs. Frequency for Various Temperatures, $V_{DD} = 5$ V, Data Measured with Constant $I_{DD}$

Figure 47. $P_{SAT}$ vs. Frequency for Various Temperatures, $V_{DD} = 5$ V, Data Measured with Constant $I_{DD}$

Figure 48. $P_{1dB}$ vs. Frequency for Various Drain Currents, $V_{DD} = 5$ V, Data Measured with Constant $I_{DD}$

Figure 49. $P_{SAT}$ vs. Frequency for Various Drain Currents, $V_{DD} = 5$ V, Data Measured with Constant $I_{DD}$
THEORY OF OPERATION

The architecture of the ADPA7005CHIP, a medium power amplifier, is shown in Figure 50. The ADPA7005CHIP uses two cascaded, three stage amplifiers operating in quadrature between six 90° hybrids.

The input signal is divided evenly into two, and then each signal is divided into two again. Each of these new paths are amplified through three independent gain stages. The amplified signals are then combined at the output. This balanced amplifier approach forms an amplifier with a combined gain of 15 dB and a $P_{\text{Sat}}$ value of 32 dBm.

A portion of the RF output signal is directionally coupled to a diode for detection of the RF output power. When the diode is dc biased, the diode rectifies the RF power and makes the RF power available for measurement as a dc voltage at VDET. To allow temperature compensation of VDET, an identical and symmetrically located circuit, minus the coupled RF power, is available via VREF. Taking the difference of VREF – VDET provides a temperature compensated signal that is proportional to the RF output (see Figure 50).

The 90° hybrids ensure that the input and output return losses are greater than 15 dB. See the application circuits shown in Figure 63 and Figure 64 for further details on biasing the various blocks.

![Figure 50. ADPA7005CHIP Architecture](image-url)
APPLICATIONS INFORMATION

The ADPA7005CHIP is a GaAs, pHEMT, MMIC power amplifier. Capacitive bypassing is required for all VGGx and VDDx pins (see Figure 51). VGG1 is the gate bias pad for the top cascaded amplifiers. VGG2 is the gate bias pad for the bottom cascaded amplifiers. VDD1, VDD3, and VDD5 are drain bias pads for the top cascaded amplifiers. VDD2, VDD4, and VDD6 are drain bias pads for the bottom cascaded amplifiers.

All measurements for this device were taken using the typical application circuit (see Figure 63) and were configured as shown in the assembly diagram (Figure 64).

The following is the recommended bias sequence during power-up:
1. Connect GND to RF and dc ground.
2. Set all gate bias voltages, VGG1 and VGG2, to −2 V.
3. Set all drain bias voltages, VDDxx, to 5 V.
4. Increase the gate bias voltage to achieve the quiescent supply current and set IDQ = 1200 mA.
5. Apply the RF signal.

The following is the recommended bias sequence during power-down:
1. Turn off the RF signal.
2. Decrease the gate bias voltages, VGG1 and VGG2, to −2 V to achieve an IDQ = 0 mA (approximately).
3. Decrease all drain bias voltages to 0 V.
4. Increase the VGG1 and VGG2 gate bias voltage to 0 V.

![Figure 51. Simplified Block Diagram](image)

Simplified bias pad connections to the dedicated gain stages and dependence and independence among pads are shown in Figure 51.

The VDD = 5 V and IDQ = 1200 mA bias conditions are recommended to optimize overall performance. Unless otherwise noted, the data shown was taken using the recommended bias conditions. Operation of the ADPA7005CHIP at different bias conditions may provide performance that differs from what is shown in Figure 63 and Figure 64. Basing the ADPA7005CHIP for higher drain current typically results in higher P1dB, output IP3, and gain at the expense of increased power consumption (see Table 7).

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

Attach the die directly to the ground plane with conductive epoxy (see the Handling Precautions section, the Mounting section, and the Wire Bonding section).

Microstrip, 50 Ω transmission lines on 0.127 mm thick alumina thin film substrates are recommended for bringing the RF to and from the chip. Raise the die 0.075 mm to ensure that the surface of the die is coplanar with the surface of the substrate.

Place the microstrip substrates as close to the die as possible to minimize ribbon bond length. Typical die to substrate spacing is 0.076 mm to 0.152 mm. To ensure wideband matching, a 15 fF capacitive stub is recommended on the PCB before the ribbon bond.

![Figure 52. High Frequency Input Wideband Matching](image)

---

Table 7. Power Selection Table

<table>
<thead>
<tr>
<th>IDQ (mA)</th>
<th>Gain (dB)</th>
<th>P1dB (dBm)</th>
<th>OIP3 (dBm)</th>
<th>PDISS (W)</th>
<th>VGG (V)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>17</td>
<td>32.0</td>
<td>42</td>
<td>6</td>
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<td>1400</td>
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<td>32.3</td>
<td>40.2</td>
<td>7</td>
<td>−0.53</td>
</tr>
<tr>
<td>1600</td>
<td>17.7</td>
<td>32.5</td>
<td>38.4</td>
<td>8</td>
<td>−0.46</td>
</tr>
</tbody>
</table>

1 Data taken at the following nominal bias conditions: VDD = 5 V, T = 25°C.
2 Adjust VGG1 and VGG2 from −2 V to 0 V to achieve the desired drain current.
Handling Precautions
To avoid permanent damage, follow these storage, cleanliness, static sensitivity, transient, and general handling precautions:

- Place all bare die in either waffle or gel-based ESD protective containers and then seal the die in an ESD protective bag for shipment. After the sealed ESD protective bag is opened, store all die in a dry nitrogen environment.
- Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.
- Follow ESD precautions to protect against ESD strikes.
- While bias is applied, suppress instrument and bias supply transients. Use shielded signal and bias cables to minimize inductive pickup.
- Handle the chip along the edges with a vacuum collet or with a sharp pair of tweezers. The surface of the chip has fragile air bridges and must not be touched with a vacuum collet, tweezers, or fingers.

Mounting
Before the epoxy die is attached, apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip after the chip is placed into position. Cure the epoxy per the schedule of the manufacturer.

Wire Bonding
RF bonds made with 3 mil × 0.5 mil gold ribbon are recommended for the RF ports. These bonds must be thermosonically bonded with a force of 40 g to 60 g. Thermosonically bonded dc bonds of 0.025 mm diameter, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds with a force of 18 g to 22 g. Create all bonds with a nominal stage temperature of 150°C. Apply the minimum amount of ultrasonic energy (depending on the process and package being used) to achieve reliable bonds. Keep all bonds as short as possible, less than 0.31 mm.

Alternatively, short RF bonds that are ≤3 mm and made with two 1 mm wires can be used.
BIASING ADPA7005CHIP WITH THE HMC980LP4E

The HMC980LP4E is an active bias controller that is designed to meet the bias requirements for enhancement mode and depletion mode amplifiers such as the ADPA7005CHIP. The controller provides constant drain current biasing over temperature and part to part variation, and properly sequences gate and drain voltages to ensure the safe operation of the amplifier. The HMC980LP4E also offers self protection in the event of a short circuit, as well as an internal charge pump that generates the negative voltage needed on the gate of the ADPA7005CHIP, and the option to use an external negative voltage source. HMC980LP4E is also available in die form as the HMC980-DIE.

APPLICATION CIRCUIT SETUP

Figure 55 displays the schematic of an application circuit using the HMC980LP4E to control the ADPA7005CHIP. When using an external negative supply for VNEG, refer to the schematic in Figure 56.

In the application circuit shown in Figure 55, the ADPA7005CHIP drain voltage and drain current are set by the following equations:

\[ V_{\text{DRAIN}} (5 \text{ V}) = V_{\text{DD}} (6.12 \text{ V}) − IDRAIN (1600 \text{ mA}) \times 0.7 \Omega \] (1)

\[ IDRAIN (1600 \text{ mA}) = \frac{150 \text{ mA}}{R10 (93.1 \Omega)} \] (2)

where \( IDRAIN \) is constant drain current.

LIMITING \( V_{\text{GATE}} \) FOR ADPA7005CHIP \( V_{\text{GGx}} \) ABSOLUTE MAXIMUM RATING REQUIREMENT

When using the HMC980LP4E to control the ADPA7005CHIP, the minimum voltages for VNEG and VGATE must be \(-1.5 \text{ V}\) to keep these voltages within the absolute maximum rating limits for the \( V_{\text{GGx}} \) pads of the ADPA7005CHIP. To set the minimum voltages, set R15 and R16 to the values shown in Figure 55 and Figure 56. Please refer to the AN-1363 for more information and calculations for R15 and R16.
Figure 55. Application Circuit using HMC980LP4E with ADPA7005CHIP

Figure 56. Application Circuit using HMC980LP4E with ADPA7005CHIP with External Negative Voltage Source
**HMC980LP4E BIAS SEQUENCE**

The dc supply sequencing in the Power-Up Sequence section and the Power-Down Sequence section is required to prevent damage to the HMC980LP4E when using it to control the ADPA7005CHIP.

**Power-Up Sequence**

The power-up sequence is as follows:

1. VDIG = 3.3 V
2. S0 = 3.3 V
3. VDD = 5.68 V
4. VNEG = −1.5 V (unnecessary if using internally generated voltage)
5. EN = 3.3 V (transition from 0 V to 3.3 V turns on VGATE and VDRAIN)

**Power-Down Sequence**

The power-down sequence is as follows:

1. EN = 0 V (transition from 3.3 V to 0 V turns off VDRAIN and VGATE)
2. VNEG = 0 V (unnecessary if using internally generated voltage)
3. VDD = 0 V
4. S0 = 0 V
5. VDIG = 0 V

After the HMC980LP4E bias control circuit is set up, toggle the bias to the ADPA7005CHIP on or off by applying 3.3 V or 0 V, respectively, to the EN pad. At EN = 3.3 V, VGATE drops to −1.5 V and VDRAIN turns on at 5 V. VGATE then rises until \( I_{DRAIN} = 800 \text{ mA} \), and the closed control loop regulates \( I_{DRAIN} \) at 1600 mA. When EN = 0 V, VGATE is set to −1.5 V, and VDRAIN is set to 0 V (see Figure 57 and Figure 58).

**CONSTANT DRAIN CURRENT BIASING vs. CONSTANT GATE VOLTAGE BIASING**

The HMC980LP4E uses a closed-loop feedback to continuously adjust VGATE to maintain a constant gate current bias over dc supply variation, temperature, and part to part variation. In addition, constant drain current bias is the optimum method for reducing time in calibration procedures and for maintaining consistent performance over time. By comparing with a constant gate voltage bias where the current is driven to increase when RF power is applied, a slightly lower output P1dB is seen with a constant drain current bias. This output P1db is displayed in Figure 62, where the RF performance is slightly lower than constant gate voltage bias operation due to a lower drain current at the high input powers as the device reaches 1 dB compression.

The output P1dB performance for constant drain current bias can be increased towards constant gate voltage bias performance by increasing the set current towards the \( I_{DQ} \) it would reach under RF drive in the constant gate voltage bias condition, as shown in Figure 62. The limit of increasing \( I_{DQ} \) under the constant current operation is set by the thermal limitations that can be found in the absolute maximum ratings table (see Table 3) from the amplifier data sheet with the maximum power dissipation specification. As the \( I_{DQ} \) increase continues, the actual output P1dB does not continue to increase indefinitely, and the power dissipation increases. Therefore, take the exchange between the power dissipation and output P1dB performance into consideration when using constant drain current biasing.
Figure 59. IDD vs. RF Input Power (PIN), VDD = 5 V, Frequency = 32 GHz for
Constant Drain Current Bias and Constant Gate Voltage Bias

Figure 60. POUT vs. PIN, VDD = 5 V, Frequency = 32 GHz, Constant Drain Current Bias and Constant Gate Voltage Bias

Figure 61. PAE vs. PIN, VDD = 5 V, Frequency = 32 GHz, Constant Drain Current Bias and Constant Gate Voltage Bias

Figure 62. Output P1dB vs. PIN, VDD = 5 V, Frequency = 32 GHz, Constant Drain Current Bias and Constant Gate Voltage Bias
TYPICAL APPLICATION CIRCUIT

Figure 63. Typical Application Circuit Using the HMC980LP4E with the ADPA7005CHIP
ASSEMBLY DIAGRAM

Figure 64. Assembly Diagram
**OUTLINE DIMENSIONS**

*This die utilizes fragile air bridges. Any pickup tools used must not contact this area.*

*Figure 65. 12-Pad Bare Die [CHIP]
(C-12-3)*

*Dimensions shown in millimeters*

<table>
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<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
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<td>12-Pad Bare Die [CHIP]</td>
<td>C-12-3</td>
</tr>
<tr>
<td>ADPA7005C-KIT</td>
<td>−55°C to +85°C</td>
<td>12-Pad Bare Die [CHIP]</td>
<td>C-12-3</td>
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