20 V, 6 A, Synchronous Step-Down DC-to-DC Regulator

ADP2386 Data Sheet

FEATURES
- Input voltage: 4.5 V to 20 V
- Integrated MOSFET: 44 mΩ/11 mΩ
- Reference voltage: 0.6 V ± 1%
- Continuous output current: 6 A
- Programmable switching frequency: 200 kHz to 1.4 MHz
- Synchronizes to external clock: 200 kHz to 1.4 MHz
- 180° out of phase clock synchronization
- Precision enable and power good
- External compensation
- Internal soft start with external adjustable option
- Startup into a precharged output
- Supported by ADIsimPower design tool

APPLICATIONS
- Communications infrastructure
- Networking and servers
- Industrial and instrumentation
- Healthcare and medical
- Intermediate power rail conversion
- DC-to-dc point-of-load applications

GENERAL DESCRIPTION
The ADP2386 is a synchronous step-down, dc-to-dc regulator with an integrated 44 mΩ, high-side power MOSFET and an 11 mΩ, synchronous rectifier MOSFET to provide a high efficiency solution in a compact 4 mm × 4 mm LFCSP package. This device uses a peak current mode, constant frequency pulse-width modulation (PWM) control scheme for excellent stability and transient response. The switching frequency of the ADP2386 can be programmed from 200 kHz to 1.4 MHz. To minimize system noise, the synchronization function allows the switching frequency to be synchronized to an external clock.

The ADP2386 requires minimal external components and operates from an input voltage of 4.5 V to 20 V. The output voltage can be adjusted from 0.6 V to 90% of the input voltage and delivers up to 6 A of continuous current. Each IC draws less than 110 μA current from the input source when it is disabled.

This regulator targets high performance applications that require high efficiency and design flexibility. External compensation and an adjustable soft start function provide design flexibility. The power-good output and precision enable input provide simple and reliable power sequencing.

Other key features include undervoltage lockout (UVLO), overvoltage protection (OVP), overcurrent protection (OCP), short-circuit protection (SCP), and thermal shutdown (TSD).

The ADP2386 operates over the −40°C to +125°C junction temperature range and is available in a 24-lead, 4 mm × 4 mm LFCSP package.

Figure 1. TYPICAL APPLICATIONS CIRCUIT

Figure 2. Efficiency vs. Output Current, VIN = 12 V, fSW = 300 kHz

Figure 10211-002
**TABLE OF CONTENTS**

Features .............................................................................................. 1
Applications ....................................................................................... 1
Typical Applications Circuit ............................................................ 1
General Description ......................................................................... 1
Revision History ............................................................................... 2
Specifications ..................................................................................... 3
Absolute Maximum Ratings ............................................................ 5
Thermal Resistance ...................................................................... 5
ESD Caution .................................................................................. 5
Pin Configuration and Function Descriptions ............................. 6
Typical Performance Characteristics ............................................. 7
Functional Block Diagram ............................................................ 11
Theory of Operation ...................................................................... 12
Control Scheme .......................................................................... 12
Precision Enable/Shutdown ...................................................... 12
Internal Regulator (VREG) ....................................................... 12
Bootstrap Circuitry .................................................................... 12
Oscillator ..................................................................................... 12
Synchronization .......................................................................... 12
Soft Start ...................................................................................... 13
Power Good ................................................................................. 13
Peak Current-Limit and Short-Circuit Protection ................... 13
Overvoltage Protection (OVP) ............................................... 14
Undervoltage Lockout (UVLO) ............................................. 14
Thermal Shutdown...................................................................... 14
Applications Information .............................................................. 15
Input Capacitor Selection.......................................................... 15
Output Voltage Setting .............................................................. 15
Voltage Conversion Limitations ............................................... 15
Inductor Selection .................................................................... 15
Output Capacitor Selection....................................................... 16
Programming the Input Voltage UVLO................................. 17
Compensation Design ............................................................... 17
ADIsimPower Design Tool ....................................................... 18
Design Example ........................................................................... 19
Output Voltage Setting (Design Example)................................. 19
Frequency Setting ........................................................................ 19
Inductor Selection (Design Example) ....................................... 19
Output Capacitor Selection (Design Example) ....................... 20
Compensation Components ..................................................... 20
Soft Start Time Program ........................................................... 20
Input Capacitor Selection (Design Example) ......................... 20
Recommended External Components .................................... 21
Circuit Board Layout Recommendations .................................. 22
Typical Applications Circuits ........................................................ 23
Outline Dimensions ....................................................................... 24
Ordering Guide .......................................................................... 24

**REVISION HISTORY**

10/15—Rev. B to Rev. C
Changes to Inductor Selection Section ........................................ 16

7/14—Rev. A to Rev. B
Changes to Table 2 and Table 3 ....................................................... 5
Changes to Inductor Selection Section ........................................ 15
Changes to Figure 33 ...................................................................... 19
Changes to Compensation Components Section .................... 20
Updated Outline Dimensions ....................................................... 24

4/13—Rev. 0 to Rev. A
Changes to Figure 4 and Figure 7 ................................................... 7
Updated Outline Dimensions ....................................................... 23
Changes to Ordering Guide ......................................................... 23

11/12—Revision 0: Initial Version
**SPECIFICATIONS**

$V_{PVIN} = 12\,\text{V}$, $T_J = -40^\circ\text{C}$ to $+125^\circ\text{C}$ for minimum/maximum specifications, and $T_A = 25^\circ\text{C}$ for typical specifications, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>PVIN</td>
<td>$V_{PVIN}$</td>
<td>No switching</td>
<td>4.5</td>
<td>20</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>$I_Q$</td>
<td></td>
<td>2.4</td>
<td>2.9</td>
<td>3.6</td>
<td>mA</td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>$I_{SHDN}$</td>
<td>$EN = \text{GND}$</td>
<td>50</td>
<td>80</td>
<td>110</td>
<td>µA</td>
</tr>
<tr>
<td>PVIN Undervoltage Lockout Threshold</td>
<td>$UVLO$</td>
<td>PVIN rising</td>
<td>4.3</td>
<td>4.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>PVIN falling</td>
<td>3.6</td>
<td>3.8</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>FB</td>
<td>$V_{FB}$</td>
<td>$-40^\circ\text{C} &lt; T_J &lt; 85^\circ\text{C}$</td>
<td>0.594</td>
<td>0.6</td>
<td>0.606</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40^\circ\text{C} &lt; T_J &lt; 125^\circ\text{C}$</td>
<td>0.591</td>
<td>0.6</td>
<td>0.609</td>
<td>V</td>
</tr>
<tr>
<td>FB Bias Current</td>
<td>$I_{FB}$</td>
<td></td>
<td>0.01</td>
<td>0.1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Internal Regulator (VREG)</td>
<td>$V_{VREG}$</td>
<td>$V_{PVIN} = 12,\text{V}$, $I_{VREG} = 50,\text{mA}$</td>
<td>7.6</td>
<td>8</td>
<td>8.4</td>
<td>V</td>
</tr>
<tr>
<td>Dropout Voltage</td>
<td></td>
<td>$V_{PVIN} = 12,\text{V}$, $I_{VREG} = 50,\text{mA}$</td>
<td>340</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>Regulator Current Limit</td>
<td></td>
<td></td>
<td>62</td>
<td>100</td>
<td>137</td>
<td>mA</td>
</tr>
<tr>
<td>SW</td>
<td>$V_{BST} - V_{SW} = 5,\text{V}$</td>
<td>44</td>
<td>70</td>
<td></td>
<td>mΩ</td>
<td></td>
</tr>
<tr>
<td>High-Side On Resistance</td>
<td></td>
<td>$V_{VREG} = 8,\text{V}$</td>
<td>11</td>
<td>18</td>
<td></td>
<td>mΩ</td>
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<tr>
<td>Low-Side On Resistance</td>
<td></td>
<td></td>
<td>7.2</td>
<td>9.6</td>
<td>11.5</td>
<td>A</td>
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<tr>
<td>High-Side Peak Current Limit</td>
<td></td>
<td>2.5</td>
<td></td>
<td></td>
<td>A</td>
<td></td>
</tr>
<tr>
<td>Low-Side Negative Current-Limit</td>
<td></td>
<td></td>
<td>125</td>
<td>165</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SW Minimum On Time</td>
<td>$t_{MIN_ON}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SW Minimum Off Time</td>
<td>$t_{MIN_OFF}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>BST</td>
<td>$V_{BOOT}$</td>
<td></td>
<td>4.6</td>
<td>5</td>
<td>5.4</td>
<td>V</td>
</tr>
<tr>
<td>Oscillator (RT PIN)</td>
<td>$f_{SW}$</td>
<td>$R_T = 100,\text{kΩ}$</td>
<td>540</td>
<td>600</td>
<td>660</td>
<td>kHz</td>
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<tr>
<td>Switching Frequency Range</td>
<td></td>
<td></td>
<td>200</td>
<td>1400</td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>SYNC</td>
<td>$D_{MAX_SYNC}$</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Synchronization Range</td>
<td></td>
<td>200</td>
<td>1400</td>
<td></td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>SYNC Minimum Pulse Width</td>
<td></td>
<td>100</td>
<td></td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>SYNC Positive Pulse Maximum Duty Cycle</td>
<td></td>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>SYNC Input High Voltage</td>
<td></td>
<td>1.3</td>
<td></td>
<td></td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>SYNC Input Low Voltage</td>
<td></td>
<td></td>
<td></td>
<td>0.4</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>SS</td>
<td>Internal Soft Start</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SS Pin Pull-Up Current</td>
<td>$I_{SS_UP}$</td>
<td></td>
<td>1600</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>2.3</td>
<td>3.2</td>
<td>3.9</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Conditions/Comments</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
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<td>---------------------------</td>
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<td>----------------------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
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</tr>
<tr>
<td>PGOOD</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-Good Range</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB Rising Threshold</td>
<td></td>
<td>PGOOD from low to high</td>
<td>95</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>FB Rising Hysteresis</td>
<td></td>
<td>PGOOD from high to low</td>
<td>5</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>FB Falling Threshold</td>
<td></td>
<td>PGOOD from low to high</td>
<td>105</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>FB Falling Hysteresis</td>
<td></td>
<td>PGOOD from high to low</td>
<td>11.7</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Power-Good Deglitch Time</td>
<td></td>
<td>PGOOD from low to high</td>
<td>1024</td>
<td></td>
<td></td>
<td>Clock cycles</td>
</tr>
<tr>
<td>Power-Good Leakage Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power-Good Output Low Voltage</td>
<td></td>
<td>$V_{PGOOD} = 5,\text{V}$</td>
<td>0.01</td>
<td>0.1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>EN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>EN Rising Threshold</td>
<td></td>
<td>$V_{EN} = 1.17,\text{V}$</td>
<td>1.17</td>
<td>1.25</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>EN Falling Threshold</td>
<td></td>
<td>$V_{EN} = 0.97,\text{V}$</td>
<td>0.97</td>
<td>1.07</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>EN Source Current</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>THERMAL SHUTDOWN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Thermal Shutdown Threshold</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ºC</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ºC</td>
</tr>
</tbody>
</table>

1 Pin-to-pin measurement.
2 Guaranteed by design.
## ABSOLUTE MAXIMUM RATINGS

### Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>PVIN, SW, EN, PGOOD</td>
<td>−0.3 V to +22 V</td>
</tr>
<tr>
<td>SW 10 ns Transient</td>
<td>−2.5 V to +22 V</td>
</tr>
<tr>
<td>SW 100 ns Transient</td>
<td>−1 V to +22 V</td>
</tr>
<tr>
<td>BST</td>
<td>VS + 6 V</td>
</tr>
<tr>
<td>FB, SS, COMP, SYNC, RT</td>
<td>−0.3 V to +6 V</td>
</tr>
<tr>
<td>VREG</td>
<td>−0.3 V to +12 V</td>
</tr>
<tr>
<td>PGND to GND</td>
<td>−0.3 V to +0.3 V</td>
</tr>
<tr>
<td>Operating Junction Temperature</td>
<td>−40°C to +125°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Soldering Conditions</td>
<td>JEDEC J-STD-020</td>
</tr>
</tbody>
</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### THERMAL RESISTANCE

θJA is specified for the worst-case conditions, that is, a device soldered in a 4-layer, JEDEC standard circuit board for surfacemount packages.

### Table 3. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>θJA</th>
<th>θJC</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>24-Lead LFCSP_WQ</td>
<td>42.6</td>
<td>6.8 (EP, SW)</td>
<td>2.3 (EP, GND)</td>
</tr>
</tbody>
</table>

### ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
### Table 4. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>COMP</td>
<td>Error Amplifier Output. Connect an RC network from COMP to GND.</td>
</tr>
<tr>
<td>2</td>
<td>FB</td>
<td>Feedback Voltage Sense Input. Connect to a resistor divider from the output voltage, V_out.</td>
</tr>
<tr>
<td>3</td>
<td>VREG</td>
<td>Output of the Internal 8 V Regulator. The control circuits are powered from this voltage. Place a 1 µF, X7R or X5R ceramic capacitor between this pin and GND.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Analog Ground. Return of internal control circuit.</td>
</tr>
<tr>
<td>5, 6, 7, 14</td>
<td>SW</td>
<td>Switch Node Output. Connect to the output inductor.</td>
</tr>
<tr>
<td>8, 9, 10, 11, 12, 13</td>
<td>PGND</td>
<td>Power Ground. Return of low-side power MOSFET.</td>
</tr>
<tr>
<td>15</td>
<td>BST</td>
<td>Supply Rail for the High-Side Gate Drive. Place a 0.1 µF, X7R or X5R capacitor between SW and BST.</td>
</tr>
<tr>
<td>16, 17, 18, 19</td>
<td>PVIN</td>
<td>Power Input. Connect to the input power source and connect a bypass capacitor between this pin and PGND.</td>
</tr>
<tr>
<td>20</td>
<td>EN</td>
<td>Precision Enable Pin. An external resistor divider can be used to set the turn-on threshold. To enable the part automatically, connect the EN pin to the PVIN pin.</td>
</tr>
<tr>
<td>21</td>
<td>PGOOD</td>
<td>Power-Good Output (Open Drain). A pull-up resistor of 10 kΩ to 100 kΩ is recommended.</td>
</tr>
<tr>
<td>22</td>
<td>RT</td>
<td>Frequency Setting. Connect a resistor between RT and GND to program the switching frequency from 200 kHz to 1.4 MHz.</td>
</tr>
<tr>
<td>23</td>
<td>SYNC</td>
<td>Synchronization Input. Connect this pin to an external clock to synchronize the switching frequency within a range from 200 kHz to 1.4 MHz. See the Oscillator section and Synchronization section for more information.</td>
</tr>
<tr>
<td>24</td>
<td>SS</td>
<td>Soft Start Control. Connect a capacitor from SS to GND to program the soft start time. If this pin is open, the regulator uses the internal soft start time.</td>
</tr>
<tr>
<td>25</td>
<td>EP, GND</td>
<td>The exposed GND pad must be soldered to a large, external, copper GND plane to reduce thermal resistance.</td>
</tr>
<tr>
<td>26</td>
<td>EP, SW</td>
<td>The exposed SW pad must be connected to the SW pins of the ADP2386 by using short, wide traces, or else soldered to a large, external, copper SW plane to reduce thermal resistance.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

\[ T_A = 25^\circ C, \ V_{IN} = 12 \ V, \ V_{OUT} = 3.3 \ V, \ L = 2.2 \ \mu H, \ C_{OUT} = 100 \ \mu F + 47 \ \mu F, \ f_{SW} = 600 \ \text{kHz}, \] unless otherwise noted.

**Figure 4. Efficiency at \( V_{IN} = 12 \ V, f_{SW} = 600 \ \text{kHz} \)**

**Figure 5. Efficiency at \( V_{IN} = 18 \ V, f_{SW} = 600 \ \text{kHz} \)**

**Figure 7. Efficiency at \( V_{IN} = 12 \ V, f_{SW} = 300 \ \text{kHz} \)**

**Figure 8. Efficiency at \( V_{IN} = 5 \ V, f_{SW} = 600 \ \text{kHz} \)**

**Figure 6. Shutdown Current vs. Input Voltage (\( V_{IN} \))**

**Figure 9. Quiescent Current vs. \( V_{IN} \)**
Figure 10. PVIN UVLO Threshold vs. Temperature

Figure 11. SS Pin Pull-Up Current vs. Temperature

Figure 12. Frequency vs. Temperature

Figure 13. EN Threshold vs. Temperature

Figure 14. Feedback Voltage vs. Temperature

Figure 15. VREG Voltage vs. Temperature
Figure 16. MOSFET $R_{DSON}$ vs. Temperature

Figure 17. Working Mode Waveform

Figure 18. Voltage Precharged Output

Figure 19. Current-Limit Threshold vs. Temperature

Figure 20. Soft Start with Full Load

Figure 21. External Synchronization
Figure 22. Load Transient Response, 1 A to 5 A

Figure 23. Output Short Entry

Figure 24. Load Current vs. Ambient Temperature at $V_{IN} = 12$ V, $f_{SW} = 600$ kHz

Figure 25. Line Transient Response, $V_{IN}$ from 8 V to 14 V, $I_{OUT} = 6$ A

Figure 26. Output Short Recovery

Figure 27. Load Current vs. Ambient Temperature at $V_{IN} = 12$ V, $f_{SW} = 300$ kHz
FUNCTIONAL BLOCK DIAGRAM

Figure 28. Functional Block Diagram
THEORY OF OPERATION

The ADP2386 is a synchronous step-down, dc-to-dc regulator that uses a current-mode architecture with an integrated high-side power switch and a low-side synchronous rectifier. The regulator targets high performance applications that require high efficiency and design flexibility.

The ADP2386 operates from an input voltage that ranges from 4.5 V to 20 V and regulates the output voltage from 0.6 V to 90% of the input voltage. Additional features that maximize design flexibility include the following: programmable switching frequency, programmable soft start, external compensation, precision enable, and a power-good output.

CONTROL SCHEME

The ADP2386 uses a fixed frequency, peak current-mode PWM control architecture. At the start of each oscillator cycle, the high-side N-MOSFET is turned on, putting a positive voltage across the inductor. When the inductor current crosses the peak inductor current threshold, the high-side N-MOSFET is turned off and the low-side N-MOSFET is turned on. This puts a negative voltage across the inductor, causing the inductor current to decrease. The low-side N-MOSFET stays on for the rest of the cycle (see Figure 17).

PRECISION ENABLE/SHUTDOWN

The EN input pin has a precision analog threshold of 1.17 V (typical) with 100 mV of hysteresis. When the enable voltage exceeds 1.17 V, the regulator turns on; when it falls to less than 1.07 V (typical), the regulator turns off. To force the regulator to automatically start when input power is applied, connect EN to PVIN.

The precision EN pin has an internal pull-down current source (5 µA) that provides a default turn-off when the EN pin is open.

When the EN pin voltage exceeds 1.17 V (typical), the ADP2386 is enabled and the internal pull-down current source at the EN pin decreases to 1 µA, which allows users to program the PVIN UVLO and hysteresis.

INTERNAL REGULATOR (VREG)

The on-board regulator provides a stable supply for the internal circuits. It is recommended that a 1 µF ceramic capacitor be placed between the VREG and GND pins. The internal regulator includes a current-limit circuit to protect the output if the maximum external load current is exceeded.

BOOTSTRAP CIRCUITRY

The ADP2386 includes a regulator to provide the gate drive voltage for the high-side N-MOSFET. It uses differential sensing to generate a 5 V bootstrap voltage between the BST and SW pins. It is recommended that a 0.1 µF, X7R or X5R ceramic capacitor be placed between the BST pin and the SW pin.

OSCILLATOR

The ADP2386 switching frequency is controlled by the RT pin. A resistor from RT to GND can program the switching frequency according to the following equation:

\[ f_{SW} (kHz) = \frac{69,120}{R_t (k\Omega)} + 15 \]

A 100 kΩ resistor sets the frequency to 600 kHz, and a 42.2 kΩ resistor sets the frequency to 1.2 MHz. Figure 29 shows the typical relationship between \( f_{SW} \) and \( R_t \).

![Figure 29. Switching Frequency vs. \( R_t \)](image)

SYNCHRONIZATION

To synchronize the ADP2386, connect an external clock to the SYNC pin. The external clock frequency can be in the range of 200 kHz to 1.4 MHz. During synchronization, the regulator operates in continuous conduction mode (CCM), and the rising edge of the switching waveform runs 180° out of phase to the rising edge of the external clock.

When the ADP2386 operates in synchronization mode, a resistor must be connected from the RT pin to GND to program the internal oscillator to run at 90% to 110% of the external synchronization clock.
SOFT START

The ADP2386 has integrated soft start circuitry to limit the output voltage rising time and reduce inrush current at startup. The internal soft start time is calculated using the following equation:

$$t_{SS\_INT} = \frac{1600}{f_{SW} \text{ (kHz)}} \text{ (ms)}$$

A slower soft start time can be programmed by using the SS pin. When a capacitor is connected between the SS pin and GND, an internal current charges the capacitor to establish the soft start ramp. The soft start time is calculated using the following equation:

$$t_{SS\_EXT} = \frac{0.6 \times C_{SS}}{I_{SS\_UP}}$$

where:

- $C_{SS}$ is the soft start capacitance.
- $I_{SS\_UP}$ is the soft start pull-up current (3.2 μA).

The internal error amplifier includes three positive inputs: the internal reference voltage, the internal digital soft start voltage, and the SS pin voltage. The error amplifier regulates the FB voltage to the lowest of the three voltages.

If the output voltage is charged prior to turn-on, the ADP2386 prevents reverse inductor current that would discharge the output capacitor. This function remains active until the soft start voltage exceeds the voltage on the FB pin.

POWER GOOD

The power-good pin (PGOOD) is an active high, open-drain output that requires an external resistor to pull it up to a voltage. A logic high on the PGOOD pin indicates that the voltage on the FB pin (and, therefore, the output voltage) is within regulation.

The power-good circuitry monitors the output voltage on the FB pin and compares it to the rising and falling thresholds that are specified in Table 1. If the rising output voltage exceeds the target value, the PGOOD pin is held low. The PGOOD pin continues to be held low until the falling output voltage returns to the target value.

If the output voltage falls below the target output voltage, the PGOOD pin is held low. The PGOOD pin continues to be held low until the rising output voltage returns to the target value.

For protection against heavy loads, the ADP2386 uses a hiccup mode for overcurrent protection. When the inductor peak current reaches the current-limit value, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle. The overcurrent counter increments during this process. If the overcurrent counter reaches 10, or the FB pin voltage falls to 0.4 V after the soft start, the regulator enters hiccup mode. The high-side and low-side MOSFETs are both turned off. The regulator remains in hiccup mode for 4096 clock cycles and then attempts to restart. If the current-limit fault has cleared, the regulator resumes normal operation. Otherwise, it reenters hiccup mode.

The ADP2386 also provides a sink current limit to prevent the low-side MOSFET from sinking a lot of current from the load. When the voltage across the low-side MOSFET exceeds the sink current-limit threshold, which is typically 2.5 A, the low-side MOSFET turns off immediately for the rest of the cycle. Both high-side and low-side MOSFETs turn off until the next clock cycle.

In some cases, the input voltage ($V_{PIN}$) ramp rate is too slow or the output capacitor is too large for the output to reach regulation during the soft start process, which causes the regulator to enter the hiccup mode. To avoid such occurrences, use a resistor divider at the EN pin to program the input voltage UVLO, or use a longer soft start time.

PEAK CURRENT-LIMIT AND SHORT-CIRCUIT PROTECTION

The ADP2386 has a peak current-limit protection circuit to prevent current runaway. During the initial soft start, the ADP2386 uses frequency foldback to prevent output current runaway. The switching frequency is reduced according to the voltage on the FB pin, which allows more time for the inductor to discharge. The correlation between the switching frequency and the FB pin voltage is shown in Table 5.

<table>
<thead>
<tr>
<th>FB Pin Voltage</th>
<th>Switching Frequency</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{FB} \geq 0.4 \text{ V}$</td>
<td>$f_{SW}$</td>
</tr>
<tr>
<td>$0.4 \text{ V} &gt; V_{FB} \geq 0.2 \text{ V}$</td>
<td>$f_{SW}/2$</td>
</tr>
<tr>
<td>$V_{FB} &lt; 0.2 \text{ V}$</td>
<td>$f_{SW}/4$</td>
</tr>
</tbody>
</table>

For protection against heavy loads, the ADP2386 uses a hiccup mode for overcurrent protection. When the inductor peak current reaches the current-limit value, the high-side MOSFET turns off and the low-side MOSFET turns on until the next cycle. The overcurrent counter increments during this process. If the overcurrent counter reaches 10, or the FB pin voltage falls to 0.4 V after the soft start, the regulator enters hiccup mode. The high-side and low-side MOSFETs are both turned off. The regulator remains in hiccup mode for 4096 clock cycles and then attempts to restart. If the current-limit fault has cleared, the regulator resumes normal operation. Otherwise, it reenters hiccup mode.

The ADP2386 also provides a sink current limit to prevent the low-side MOSFET from sinking a lot of current from the load. When the voltage across the low-side MOSFET exceeds the sink current-limit threshold, which is typically 2.5 A, the low-side MOSFET turns off immediately for the rest of the cycle. Both high-side and low-side MOSFETs turn off until the next clock cycle.

In some cases, the input voltage ($V_{PIN}$) ramp rate is too slow or the output capacitor is too large for the output to reach regulation during the soft start process, which causes the regulator to enter the hiccup mode. To avoid such occurrences, use a resistor divider at the EN pin to program the input voltage UVLO, or use a longer soft start time.
OVERVOLTAGE PROTECTION (OVP)
The ADP2386 includes an overvoltage protection feature to protect the regulator against an output short to a higher voltage supply or when a strong load disconnect transient occurs. If the feedback voltage increases to 0.7 V, the internal high-side and low-side MOSFETs are turned off until the voltage at the FB pin decreases to 0.63 V. At that time, the ADP2386 resumes normal operation.

UNDERVOLTAGE LOCKOUT (UVLO)
Undervoltage lockout circuitry is integrated in the ADP2386 to prevent the occurrence of power-on glitches. If the $V_{\text{VIN}}$ voltage falls to less than 3.8 V typical, the part shuts down, and both the power switch and synchronous rectifier turn off. When the $V_{\text{VIN}}$ voltage rises to greater than 4.3 V typical, the soft start period is initiated, and the part is enabled.

THERMAL SHUTDOWN
If the ADP2386 junction temperatures rises to greater than 150°C, the internal thermal shutdown circuit turns off the regulator for self-protection. Extreme junction temperatures can be the result of high current operation, poor circuit board thermal design, and/or high ambient temperature. A 25°C hysteresis is included in the thermal shut-down circuit so that, if an overtemperature event occurs, the ADP2386 does not return to normal operation until the on-chip temperature falls to less than 125°C. Upon recovery, a soft start is initiated before normal operation begins.
APPLICATIONS INFORMATION

INPUT CAPACITOR SELECTION

The input capacitor reduces the input voltage ripple caused by the switch current on PVIN. Place the input capacitor as close as possible to the PVIN pin. A ceramic capacitor in the 10 μF to 47 μF range is recommended. The loop that is composed of this input capacitor, the high-side N-MOSFET, and the low-side N-MOSFET must be kept as small as possible.

The voltage rating of the input capacitor must be greater than the maximum input voltage. Ensure that the rms current rating of the input capacitor is larger than the value calculated from the following equation:

\[ I_{\text{INV rms}} = I_{\text{OUT}} \times \sqrt{D \times (1 - D)} \]

OUTPUT VOLTAGE SETTING

The output voltage of the ADP2386 is set by an external resistive divider. The resistor values are calculated using

\[ V_{\text{OUT}} = 0.6 \times \left( 1 + \frac{R_{\text{TOP}}}{R_{\text{BOT}}} \right) \]

To limit the output voltage accuracy degradation due to the FB bias current (0.1 µA maximum) to less than 0.5% (maximum), ensure that \( R_{\text{BOT}} < 30 \, \text{kΩ} \).

Table 6 lists the recommended resistor divider values for the various output voltages.

Table 6. Resistor Divider Values for Various Output Voltages

<table>
<thead>
<tr>
<th>( V_{\text{OUT}} ) (V)</th>
<th>( R_{\text{TOP}} \pm 1% ) (kΩ)</th>
<th>( R_{\text{BOT}} \pm 1% ) (kΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.0</td>
<td>10</td>
<td>15</td>
</tr>
<tr>
<td>1.2</td>
<td>10</td>
<td>10</td>
</tr>
<tr>
<td>1.5</td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>1.8</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>2.5</td>
<td>47.5</td>
<td>15</td>
</tr>
<tr>
<td>3.3</td>
<td>10</td>
<td>2.21</td>
</tr>
<tr>
<td>5.0</td>
<td>22</td>
<td>3</td>
</tr>
</tbody>
</table>

VOLTAGE CONVERSION LIMITATIONS

The minimum output voltage for a given input voltage and switching frequency is constrained by the minimum on time. The minimum on time of the ADP2386 is typically 125 ns. The minimum output voltage for a given input voltage and switching frequency can be calculated using the following:

\[ V_{\text{OUT, min}} = V_{\text{IN}} \times I_{\text{MIN, on}} \times f_{\text{SW}} - (R_{\text{DSON, HS}} - R_{\text{DSON, LS}}) \times I_{\text{OUT, min}} \times I_{\text{MIN, on}} \times f_{\text{SW}} - (R_{\text{DSON, LS}} + R_{t}) \times I_{\text{OUT, min}} \] (1)

where:

\( V_{\text{OUT, min}} \) is the minimum output voltage.
\( V_{\text{IN}} \) is the input voltage.
\( I_{\text{MIN, on}} \) is the minimum on time.
\( f_{\text{SW}} \) is the switching frequency.
\( R_{\text{DSON, HS}} \) is the high-side MOSFET on resistance.
\( R_{\text{DSON, LS}} \) is the low-side MOSFET on resistance.
\( I_{\text{OUT, min}} \) is the minimum output current.
\( R_{t} \) is the series resistance of the output inductor.

The maximum output voltage, limited by the minimum off time at a given input voltage and switching frequency, can be calculated using the following equation:

\[ V_{\text{OUT, max}} = V_{\text{IN}} \times (1 - I_{\text{MIN, off}} \times f_{\text{SW}}) - (R_{\text{DSON, HS}} - R_{\text{DSON, LS}}) \times I_{\text{OUT, max}} \times (1 - I_{\text{MIN, off}} \times f_{\text{SW}}) - (R_{\text{DSON, LS}} + R_{t}) \times I_{\text{OUT, max}} \] (2)

where:

\( V_{\text{OUT, max}} \) is the maximum output voltage.
\( V_{\text{IN}} \) is the input voltage.
\( I_{\text{MIN, off}} \) is the minimum off time.
\( f_{\text{SW}} \) is the switching frequency.
\( R_{\text{DSON, HS}} \) is the high-side MOSFET on resistance.
\( R_{\text{DSON, LS}} \) is the low-side MOSFET on resistance.
\( I_{\text{OUT, max}} \) is the maximum output current.
\( R_{t} \) is the series resistance of the output inductor.

As shown in Equation 1 to Equation 3, reducing the switching frequency alleviates the minimum on time and minimum off time limitation.

INDUCTOR SELECTION

The inductor value is determined by the operating frequency, input voltage, output voltage, and inductor ripple current. Using a small inductor value leads to a faster transient response; however, it degrades efficiency, due to a larger inductor ripple current. Using a large inductor value leads to smaller ripple current and better efficiency, but it results in a slower transient response.

As a guideline, the inductor ripple current, \( \Delta I_{L} \), is typically set to one-third of the maximum load current. The inductor value is calculated using the following equation:

\[ L = \frac{(V_{\text{IN}} - V_{\text{OUT}}) \times D}{\Delta I_{L} \times f_{\text{SW}}} \]

where:

\( V_{\text{IN}} \) is the input voltage.
\( V_{\text{OUT}} \) is the output voltage.
\( D \) is the duty cycle (\( D = V_{\text{OUT}}/V_{\text{IN}} \)).
\( \Delta I_{L} \) is the inductor current ripple.
\( f_{\text{SW}} \) is the switching frequency.
The ADP2386 uses adaptive slope compensation in the current loop to prevent subharmonic oscillations when the duty cycle is larger than 50%. The internal slope compensation limits the minimum inductor value.

For a duty cycle that is larger than 50%, the minimum inductor value is determined using the following equation:

\[
L \text{ (Minimum)} = \frac{V_{\text{OUT}} \times (1 - D)}{4 \times f_{\text{SW}}} \]

The peak inductor current is calculated by

\[
I_{\text{PEAK}} = I_{\text{OUT}} + \frac{\Delta I_L}{2}
\]

The saturation current of the inductor must be larger than the peak inductor current. For ferrite core inductors with a quick saturation characteristic, the saturation current rating of the inductor must be higher than the current-limit threshold of the switch. This prevents the inductor from reaching saturation.

The rms current of the inductor is calculated as follows:

\[
I_{\text{Ems}} = \sqrt{I_{\text{OUT}}^2 + \frac{\Delta I_L^2}{12}}
\]

Shielded ferrite core materials are recommended for low core loss and low EMI. Table 7 lists some recommended inductors.

### OUTPUT CAPACITOR SELECTION

The output capacitor selection affects the output ripple voltage load step transient and the loop stability of the regulator.

For example, during a load step transient where the load is suddenly increased, the output capacitor supplies the load until the control loop can ramp up the inductor current. The delay caused by the control loop causes output undershoot. To calculate the output capacitance that is required to satisfy the voltage droop requirement use the following equation:

\[
C_{\text{OUT,UV}} = \frac{K_{UV} \times \Delta I_{\text{STEP}}^2 \times L}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{\text{OUT,UV}}}
\]

where:
- \(K_{UV}\) is a factor, with a typical setting of \(K_{UV} = 2\).
- \(\Delta I_{\text{STEP}}\) is the load step.
- \(\Delta V_{\text{OUT,UV}}\) is the allowable undershoot on the output voltage.

Another example occurs when a load is suddenly removed from the output, and the energy stored in the inductor rushes into the output capacitor, causing the output to overshoot.

To calculate the output capacitance that is required to meet the overshoot requirement use the following equation:

\[
C_{\text{OUT,OV}} = \frac{K_{OV} \times \Delta I_{\text{STEP}}^2 \times L}{(V_{OUT} + \Delta V_{\text{OUT,OV}})^2 - V_{OUT}^2}
\]

where:
- \(\Delta V_{\text{OUT,OV}}\) is the allowable overshoot on the output voltage.
- \(K_{OV}\) is a factor, with a typical setting of \(K_{OV} = 2\).

The output ripple is determined by the ESR and the value of the capacitance. Use the following equations to select a capacitor that can meet the output ripple requirements:

\[
C_{\text{OUT,ripp}} = \frac{\Delta I_L}{8 \times f_{\text{SW}} \times \Delta V_{\text{OUT,ripp}}}
\]

\[
R_{\text{ESR}} = \frac{\Delta V_{\text{OUT,ripp}}}{\Delta I_L}
\]

where:
- \(\Delta I_L\) is the inductor current ripple.
- \(\Delta V_{\text{OUT,ripp}}\) is the allowable output ripple voltage.
- \(R_{\text{ESR}}\) is the equivalent series resistance of the output capacitor in ohms (\(\Omega\)).

Select the largest output capacitance given by \(C_{\text{OUT,UV}}, C_{\text{OUT,OV}},\) and \(C_{\text{OUT,ripp}}\) to meet both load transient and output ripple performance.

### Table 7. Recommended Inductors

<table>
<thead>
<tr>
<th>Vendor</th>
<th>Part No.</th>
<th>Value (µH)</th>
<th>(I_{\text{SAT}}) (A)</th>
<th>(I_{\text{SMS}}) (A)</th>
<th>DCR (mΩ)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Toko</td>
<td>FDVE0630-R47M</td>
<td>0.47</td>
<td>15.6</td>
<td>14.1</td>
<td>3.7</td>
</tr>
<tr>
<td></td>
<td>FDVE0630-R75M</td>
<td>0.75</td>
<td>10.9</td>
<td>10.7</td>
<td>6.2</td>
</tr>
<tr>
<td></td>
<td>FDVE0630-1R0M</td>
<td>1.0</td>
<td>9.5</td>
<td>9.5</td>
<td>8.5</td>
</tr>
<tr>
<td></td>
<td>FDVE1040-1R5M</td>
<td>1.5</td>
<td>13.7</td>
<td>14.6</td>
<td>4.6</td>
</tr>
<tr>
<td></td>
<td>FDVE1040-2R2M</td>
<td>2.2</td>
<td>11.4</td>
<td>11.6</td>
<td>6.8</td>
</tr>
<tr>
<td></td>
<td>FDVE1040-3R3M</td>
<td>3.3</td>
<td>9.8</td>
<td>9.0</td>
<td>10.1</td>
</tr>
<tr>
<td></td>
<td>FDVE1040-4R7M</td>
<td>4.7</td>
<td>8.2</td>
<td>8.0</td>
<td>13.8</td>
</tr>
<tr>
<td>Vishay</td>
<td>IHLP3232DZ-R47M-11</td>
<td>0.47</td>
<td>14.5</td>
<td>25</td>
<td>2.38</td>
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<td>IHLP3232DZ-R68M-11</td>
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<td>3.22</td>
</tr>
<tr>
<td></td>
<td>IHLP3232DZ-1R0M-11</td>
<td>1.0</td>
<td>12</td>
<td>18.2</td>
<td>4.63</td>
</tr>
<tr>
<td></td>
<td>IHLP4040DZ-1R5M-01</td>
<td>1.5</td>
<td>27.5</td>
<td>15</td>
<td>5.8</td>
</tr>
<tr>
<td></td>
<td>IHLP4040DZ-2R2M-01</td>
<td>2.2</td>
<td>25.6</td>
<td>12</td>
<td>9</td>
</tr>
<tr>
<td></td>
<td>IHLP4040DZ-3R3M-01</td>
<td>3.3</td>
<td>18.6</td>
<td>10</td>
<td>14.4</td>
</tr>
<tr>
<td></td>
<td>IHLP4040DZ-4R7M-01</td>
<td>4.7</td>
<td>17</td>
<td>9.5</td>
<td>16.5</td>
</tr>
<tr>
<td>Wurth Elektronik</td>
<td>744 325 120</td>
<td>1.2</td>
<td>25</td>
<td>20</td>
<td>1.8</td>
</tr>
<tr>
<td></td>
<td>744 325 180</td>
<td>1.8</td>
<td>18</td>
<td>16</td>
<td>3.5</td>
</tr>
<tr>
<td></td>
<td>744 325 240</td>
<td>2.4</td>
<td>17</td>
<td>14</td>
<td>4.75</td>
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<tr>
<td></td>
<td>744 325 420</td>
<td>4.2</td>
<td>14</td>
<td>11</td>
<td>7.1</td>
</tr>
</tbody>
</table>
The selected output capacitor voltage rating must be greater than the output voltage. The rms current rating of the output capacitor must be larger than the value that is calculated by \[ I_{\text{OUT},\text{RMS}} = \frac{\Delta I}{\sqrt{2}} \]

**PROGRAMMING THE INPUT VOLTAGE UVLO**

The ADP2386 has a precision enable input that can be used to program the UVLO threshold of the input voltage (see Figure 31).

**COMPENSATION DESIGN**

For peak current-mode control, the power stage can be simplified as a voltage controlled current source supplying current to the output capacitor and load resistor. It is composed of one domain pole and a zero that is contributed by the output capacitor ESR. The control-to-output transfer function is based on the following:

\[
G_{\text{VD}}(s) = \frac{V_{\text{OUT}}(s)}{V_{\text{COMP}}(s)} = A_{\text{VT}} \times R \times \left( \frac{1 + \frac{s}{2 \times \pi \times f_z}}{1 + \frac{s}{2 \times \pi \times f_b}} \right)
\]

\[
f_z = \frac{1}{2 \times \pi \times R \times ESR \times C_{\text{OUT}}}
\]

\[
f_b = \frac{1}{2 \times \pi \times (R + R_{\text{ESR}}) \times C_{\text{OUT}}}
\]

where:

- \( A_{\text{VT}} = 8.7 \text{ A/V} \)
- \( R \) is the load resistance.
- \( C_{\text{OUT}} \) is the output capacitance.
- \( R_{\text{ESR}} \) is the equivalent series resistance of the output capacitor.

The ADP2386 uses a transconductance amplifier for the error amplifier and to compensate the system. Figure 32 shows the simplified, peak current-mode control, small signal circuit.

The compensation components, \( R_C \) and \( C_C \), contribute a zero, and \( R_C \) and the optional \( C_C \) contribute an optional pole.

The closed-loop transfer equation is as follows:

\[
T_V(s) = \frac{R_{\text{BOT}}}{R_{\text{BOT}} + R_{\text{TOP}}} \times \frac{-g_m}{C_C + C_{\text{CP}}} \times \frac{1 + R_C \times C_C \times s}{s \times (1 + \frac{R_C \times C_C \times s}{C_C + C_{\text{CP}}})} \times G_{\text{ID}}(s)
\]

The following design guideline shows how to select the \( R_C, C_C, \) and \( C_{\text{CP}} \) compensation components for ceramic output capacitor applications:

1. Determine the cross frequency, \( f_c \). Generally, \( f_c \) is between \( f_{SW}/12 \) and \( f_{SW}/6 \).
2. Calculate \( R_C \) using the following equation:

\[
R_C = \frac{2 \times \pi \times V_{\text{OUT}} \times C_{\text{OUT}} \times f_C}{0.6 \times g_m \times A_{\text{VT}}}
\]

3. Place the compensation zero at the domain pole, \( f_v \); then determine \( C_C \) by using the following equation:

\[
C_C = \frac{(R + R_{\text{ESR}}) \times C_{\text{OUT}}}{R_C}
\]

4. \( C_{\text{CP}} \) is optional. It can be used to cancel the zero caused by the ESR of the output capacitor.

\[
C_{\text{CP}} = \frac{R_{\text{ESR}} \times C_{\text{OUT}}}{R_C}
\]
ADIsimPOWER DESIGN TOOL

The ADP2386 is supported by the ADIsimPower™ design tool set. ADIsimPower is a collection of tools that produce complete power designs that are optimized for a specific design goal. The tools enable the user to generate a full schematic and bill of materials and calculate performance in minutes. ADIsimPower can optimize designs for cost, area, efficiency, and part count, while taking into consideration the operating conditions and limitations of the IC and all real external components. For more information about the ADIsimPower design tools, refer to www.analog.com/ADIsimPower. The tool set is available from this website, and users can request an unpopulated board.
This section describes the procedures for selecting the external components, based on the example specifications that are listed in Table 8. See Figure 33 for the schematic of this design example.

Table 8. Step-Down DC-to-DC Regulator Requirements

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Specification</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage</td>
<td>$V_{IN} = 12.0\ V \pm 10%$</td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{OUT} = 3.3\ V$</td>
</tr>
<tr>
<td>Output Current</td>
<td>$I_{OUT} = 6\ A$</td>
</tr>
<tr>
<td>Output Voltage Ripple</td>
<td>$\Delta V_{OUT_RIPPLE} = 33\ mV$</td>
</tr>
<tr>
<td>Load Transient</td>
<td>$\pm5%, 1\ A$ to $5\ A$, $2\ A/\mu s$</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$f_{SW} = 600\ kHz$</td>
</tr>
</tbody>
</table>

**OUTPUT VOLTAGE SETTING (DESIGN EXAMPLE)**

Choose a 10 kΩ resistor as the top feedback resistor ($R_{TOP}$), and calculate the bottom feedback resistor ($R_{BOT}$) by using the following equation:

$$R_{BOT} = R_{TOP} \times \left( \frac{0.6}{V_{OUT} - 0.6} \right)$$

To set the output voltage to 3.3 V, the resistors values are as follows: $R_{TOP} = 10\ k\Omega$, and $R_{BOT} = 2.21\ k\Omega$.

**FREQUENCY SETTING**

To set the switching frequency to 600 kHz, connect a 100 kΩ resistor from the RT pin to GND.

**INDUCTOR SELECTION (DESIGN EXAMPLE)**

The peak-to-peak inductor ripple current, $\Delta I_L$, is set to 30% of the maximum output current. Use the following equation to estimate the inductor value:

$$L = \frac{(V_{IN} - V_{OUT}) \times D}{\Delta I_L \times f_{SW}}$$

where:

- $V_{IN} = 12\ V$.
- $V_{OUT} = 3.3\ V$.
- $D = 0.275$.
- $\Delta I_L = 1.8\ A$.
- $f_{SW} = 600\ kHz$.

This calculation results in $L = 2.215\ \mu H$. Choose the standard inductor value of 2.2 µH.

The peak-to-peak inductor ripple current can be calculated by using the following equation:

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times D}{L \times f_{SW}}$$

This calculation results in $\Delta I_L = 1.81\ A$.

Use the following equation to calculate the peak inductor current:

$$I_{PEAK} = I_{OUT} + \frac{\Delta I_L}{2}$$

This calculation results in $I_{PEAK} = 6.905\ A$.

Use the following equation to calculate the rms current flowing through the inductor:

$$I_{RMS} = \sqrt{\frac{I_{OUT}^2 + \frac{\Delta I_L^2}{12}}{2}}$$

This calculation results in $I_{RMS} = 6.023\ A$.

Based on the calculated current value, select an inductor with a minimum rms current rating of 6.03 A and a minimum saturation current rating of 6.91 A.

However, to protect the inductor from reaching its saturation point under the current-limit condition, the inductor should be rated for at least 9.6 A saturation current for reliable operation.

Based on the requirements described previously, select a 2.2 µH inductor, such as the FDVE1040-2R2M from Toko, which has a 6.8 mΩ DCR and a 11.4 A saturation current.
OUTPUT CAPACITOR SELECTION (DESIGN EXAMPLE)

The output capacitor is required to meet both the output voltage ripple and load transient response requirements.

To meet the output voltage ripple requirement, use the following equation to calculate the ESR and capacitance value of the output capacitor:

\[ C_{\text{OUT, RIPPLE}} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{\text{OUT, RIPPLE}}} \]

\[ R_{\text{ESR}} = \frac{\Delta V_{\text{OUT, RIPPLE}}}{\Delta I_L} \]

This calculation results in \( C_{\text{OUT, RIPPLE}} = 11.4 \, \mu\text{F} \) and \( R_{\text{ESR}} = 18 \, \text{mΩ} \).

To meet the ±5% overshoot and undershoot transient requirements, use the following equations to calculate the capacitance:

\[ C_{\text{OUT, OV}} = \frac{K_{\text{OV}} \times \Delta I_{\text{STEP}}^2 \times L}{(V_{\text{OUT}} + \Delta V_{\text{OUT, OV}})^2 - V_{\text{OUT}}^2} \]

\[ C_{\text{OUT, UV}} = \frac{K_{\text{UV}} \times \Delta I_{\text{STEP}}^2 \times L}{2 \times (V_{\text{IN}} - V_{\text{OUT}}) \times \Delta V_{\text{OUT, UV}}} \]

where:

\( K_{\text{OV}} = K_{\text{UV}} = 2 \) are the coefficients for estimation purposes.

\( \Delta I_{\text{STEP}} = 4 \, \text{A} \) is the load transient step.

\( \Delta V_{\text{OUT, OV}} \) is the overshoot voltage.

\( \Delta V_{\text{OUT, UV}} \) is the undershoot voltage.

This calculation results in \( C_{\text{OUT, OV}} = 63.1 \, \mu\text{F} \) and \( C_{\text{OUT, UV}} = 24.5 \, \mu\text{F} \).

According to the calculation, the output capacitance must be greater than 63 \( \mu\text{F} \), and the ESR of the output capacitor must be smaller than 18 mΩ. It is recommended that one 100 \( \mu\text{F} \)/X5R/6.3 V ceramic capacitor and one 47 \( \mu\text{F} \)/X5R/6.3 V ceramic capacitor be used, such as the GRM32ER60J107ME20 and GRM32ER60J476ME20 from Murata, with an ESR of 2 mΩ.

COMPENSATION COMPONENTS

For better load transient and stability performance, set the cross frequency, \( f_c \), to \( f_{SW}/10 \). In this case, \( f_{SW} \) is running at 600 kHz; therefore, the \( f_c \) is set to 60 kHz.

The 100 \( \mu\text{F} \) and 47 \( \mu\text{F} \) ceramic output capacitors have a derated value of 62 \( \mu\text{F} \) and 32 \( \mu\text{F} \).

\[ R_C = \frac{2 \times \pi \times 3.3 \, \text{V} \times 94 \, \mu\text{F} \times 60 \, \text{kHz}}{0.6 \, \text{V} \times 480 \, \mu\text{S} \times 8.7 \, \text{A/V}} = 46.7 \, \text{kΩ} \]

\[ C_C = \frac{(0.55 \, \Omega + 0.002 \, \Omega) \times 94 \, \mu\text{F}}{46.7 \, \text{kΩ}} = 1111 \, \text{pF} \]

\[ C_{CP} = \frac{0.002 \, \Omega \times 94 \, \mu\text{F}}{46.7 \, \text{kΩ}} = 4.0 \, \text{pF} \]

Choose standard components, as follows: \( R_C = 44.2 \, \text{kΩ} \), \( C_C = 1200 \, \text{pF} \), and \( C_{CP} = 4.7 \, \text{pF} \).

Figure 34 shows the bode plot at 6 A. The cross frequency is 58 kHz, and the phase margin is 61°.

SOFT START TIME PROGRAM

The soft start feature allows the output voltage to ramp up in a controlled manner, eliminating output voltage overshoot during soft start and limiting the inrush current. Set the soft start time to 4 ms.

\[ C_{SS} = \frac{I_{SS \_EXT} \times I_{SS \_LP}}{0.6} = \frac{4 \, \text{ms} \times 3.2 \, \mu\text{A}}{0.6 \, \text{V}} = 21.3 \, \text{nF} \]

Choose a standard component value, as follows: \( C_{SS} = 22 \, \text{nF} \).

INPUT CAPACITOR SELECTION (DESIGN EXAMPLE)

Place a minimum 10 \( \mu\text{F} \) ceramic capacitor near the PVIN pin.

In this application, it is recommended that one 10 \( \mu\text{F} \), X5R, 25 V ceramic capacitor be used.
## RECOMMENDED EXTERNAL COMPONENTS

Table 9. Recommended External Components for Typical Applications with 6 A Output Current

<table>
<thead>
<tr>
<th>$f_{SW}$ (kHz)</th>
<th>$V_{IN}$ (V)</th>
<th>$V_{OUT}$ (V)</th>
<th>L (µH)</th>
<th>$C_{OUT}$ (µF)$^1$</th>
<th>$R_{TOP}$ (kΩ)</th>
<th>$R_{BOT}$ (kΩ)</th>
<th>$R_C$ (kΩ)</th>
<th>$C_L$ (pF)</th>
<th>$C_P$ (pF)</th>
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CIRCUIT BOARD LAYOUT RECOMMENDATIONS

Good printed circuit board (PCB) layout is essential for obtaining the best performance from the ADP2386. Poor PCB layout can degrade the output regulation, as well as the electromagnetic interference (EMI) and electromagnetic compatibility (EMC) performance. Figure 36 shows an example of a good PCB layout for the ADP2386. For optimum layout, refer to the following guidelines:

- Use separate analog ground planes and power ground planes. Connect the ground reference of sensitive analog circuitry, such as output voltage divider components, to analog ground. In addition, connect the ground reference of power components, such as input and output capacitors, to power ground. Connect both ground planes to the exposed GND pad of the ADP2386.
- Place the input capacitor, inductor, and output capacitor as close as possible to the IC, and use short traces.
- Ensure that the high current loop traces are as short and as wide as possible. Make the high current path from the input capacitor through the inductor, the output capacitor, and the power ground plane back to the input capacitor as short as possible. To accomplish this, ensure that the input and output capacitors share a common power ground plane.

In addition, ensure that the high current path from the power ground plane through the inductor and output capacitor back to the power ground plane is as short as possible by tying the PGND pins of the ADP2386 to the PGND plane as close as possible to the input and output capacitors.

- Connect the exposed GND pad of the ADP2386 to a large, external copper ground plane to maximize its power dissipation capability and minimize junction temperature. In addition, connect the exposed SW pad to the SW pins of the ADP2386, using short, wide traces; or connect the exposed SW pad to a large copper plane of the switching node for high current flow.
- Place the feedback resistor divider network as close as possible to the FB pin to prevent noise pickup. Minimize the length of the trace that connects the top of the feedback resistor divider to the output while keeping the trace away from the high current traces and the switching node to avoid noise pickup. To further reduce noise pickup, place an analog ground plane on either side of the FB trace and ensure that the trace is as short as possible to reduce the parasitic capacitance pickup.

![Figure 36. Recommended PCB Layout](image-url)
TYPICAL APPLICATIONS CIRCUITS

Figure 37. Typical Applications Circuit, \( V_{IN} = 12 \text{ V}, V_{OUT} = 1.2 \text{ V}, I_{OUT} = 6 \text{ A}, f_{SW} = 500 \text{ kHz} \)

Figure 38. Typical Applications Circuit Using Internal Soft Start, \( V_{IN} = 12 \text{ V}, V_{OUT} = 1.8 \text{ V}, I_{OUT} = 6 \text{ A}, f_{SW} = 600 \text{ kHz} \)

Figure 39. Programming Input Voltage UVLO Rising Threshold at 11 V, Falling Threshold at 10 V, \( V_{IN} = 12 \text{ V}, V_{OUT} = 5 \text{ V}, I_{OUT} = 6 \text{ A}, f_{SW} = 600 \text{ kHz} \)
OUTLINE DIMENSIONS

COMPLIANT TO JEDEC STANDARDS MO-220-WGGD.

Figure 40. 24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Thin Quad
(CP-24-12)
Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
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<td>−40°C to +125°C</td>
<td>24-Lead Lead Frame Chip Scale Package [LFCSP_WQ], Tape and Reel Evaluation Board</td>
<td>CP-24-12</td>
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1 Z = RoHS Compliant Part.