FEATURES

- Ultralow on resistance (RDS\text{on})
  - 50 mΩ @ 3.6 V
  - 55 mΩ @ 2.5 V
  - 65 mΩ @ 1.8 V
  - 100 mΩ @ 1.2 V
- Input voltage range: 1.1 V to 3.6 V
- 1.1 A maximum continuous operating current
- Low enable control logic threshold can be operated from 1.2 V to 3.3 V
- Low 1 μA (typical) ground current @ 1.8 V
- Low 4 μA (maximum) reverse current @ 3.6 V
- Ultralow shutdown current: 0.7 μA (typical) @ 1.8 V
- Reverse current blocking
- Tiny 4-ball wafer level chip scale package (WLCSP)
  - 1.0 mm × 1.0 mm, 0.5 mm pitch
- Tiny 6-lead lead frame chip scale package (LFCSP)
  - 2.0 mm × 2.0 mm × 0.55 mm, 0.65 mm pitch

APPLICATIONS

- Mobile phones
- Digital cameras and audio devices
- GPS devices
- Personal media players
- Portable and battery-powered equipment

GENERAL DESCRIPTION

The ADP195 is a high-side load switch designed for operation between 1.1 V to 3.6 V and protected against reverse current flow from output to input. This load switch provides power domain isolation helping extended power domain isolation. The device contains a low on-resistance, P-channel MOSFET that supports over 1.1 A of continuous current and minimizes power loss. The low 1 μA of quiescent current and ultralow shutdown current make the ADP195 ideal for battery-operated portable equipment. The built-in level shifter for enable logic makes the ADP195 compatible with many processors and GPIO controllers.

In addition to operating performance, the ADP195 occupies minimal printed circuit board (PCB) space with an area of less than 1.0 mm² and a height of 0.60 mm.

It is available in an ultrasmall 1 mm × 1 mm, 4-ball, 0.5 mm pitch WLCSP. A 6-lead 2 mm × 2 mm × 0.55 mm, 0.65 mm pitch LFCSP is also available.
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REVISION HISTORY

1/12—Rev. B to Rev. C
Changes to General Description Section .......................................... 1
Changes to Table 2 ............................................................................. 4
Updated Outline Dimensions ............................................................. 12

2/11—Rev. A to Rev. B
Added 6-Lead LFCSP ........................................................................ Universal Changes to Features, Applications, and General Description
Sections ............................................................................................. 1
Added \( V_{IN} \) to \( V_{OUT} \) Resistance, LFCSP Parameter, Table 1 ........ 3
Changes to Table 2 and Table 3 .......................................................... 4
Added Figure 4; Renumbered Sequentially ..................................... 5
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Changes to Theory of Operation Section ....................................... 9
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7/10—Rev. 0 to Rev. A
Changes to Features and Applications Sections .............................. 1
Changed 10 \( \mu A \) Ground Current to 1 \( \mu A \) Ground Current in
General Description Section ............................................................... 1
Changes to Table 2 and Thermal Resistance Section ...................... 4
Added Thermal Data Section ............................................................ 4

3/10—Revision 0: Initial Version
SPECIFICATIONS

$V_{IN} = 1.8\, \text{V}, V_{EN} = V_{IN}, I_{OUT} = 200\, \text{mA}, T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>$V_{IN}$</td>
<td>$T_J = -40^\circ\text{C} \text{ to } +85^\circ\text{C}$</td>
<td>1.1</td>
<td>3.6</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>EN INPUT</td>
<td>$V_{IH}$</td>
<td>$1.1, \text{V} \leq V_{IN} &lt; 1.8, \text{V}, T_J = -40^\circ\text{C} \text{ to } +85^\circ\text{C}$</td>
<td>0.29</td>
<td>1.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>$V_{IL}$</td>
<td>$1.8, \text{V} \leq V_{IN} \leq 3.6, \text{V}, T_J = -40^\circ\text{C} \text{ to } +85^\circ\text{C}$</td>
<td>0.45</td>
<td>1.2</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>EN Input Pull-Down Current</td>
<td>$I_{EN}$</td>
<td>$V_{IN} = 1.8, \text{V}$</td>
<td>500</td>
<td>1</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{EN} = 0, \text{V}, V_{IN} = 0, \text{V}, V_{OUT} = 3.6, \text{V}$</td>
<td>$I_{EN}$</td>
<td>$V_{EN} = 0, \text{V}, V_{IN} = 0, \text{V}, V_{OUT} = 3.6, \text{V}$</td>
<td>500</td>
<td>1</td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>REVERSE BLOCKING</td>
<td>$V_{OUT}$ Current</td>
<td>$V_{EN} = 0, \text{V}, V_{IN} = 0, \text{V}, V_{OUT} = 3.6, \text{V}$</td>
<td>4</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Hysteresis</td>
<td>$</td>
<td>V_{IN} - V_{OUT}</td>
<td>$</td>
<td>$V_{EN} = 0, \text{V}, V_{IN} = 0, \text{V}, V_{OUT} = 3.6, \text{V}$</td>
<td>75</td>
<td></td>
</tr>
<tr>
<td>CURRENT</td>
<td>$I_{GND}$</td>
<td>$V_{OUT} = 0, \text{V}$, includes $V_{EN}$ pull-down and reverse blocking bias current, $V_{IN} = 3.6, \text{V}, T_J = -40^\circ\text{C} \text{ to } +85^\circ\text{C}$</td>
<td>10</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>$I_{OFF}$</td>
<td>$V_{OUT} = 0, \text{V}$, includes $V_{EN}$ pull-down and reverse blocking bias current, $V_{IN} = 1.8, \text{V}$</td>
<td>1</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{EN} = \text{GND}$ (includes reverse blocking bias current), $V_{OUT} = 0, \text{V}$</td>
<td>$I_{OFF}$</td>
<td>$V_{EN} = \text{GND}$ (includes reverse blocking bias current), $V_{OUT} = 0, \text{V}$</td>
<td>0.7</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{EN} = \text{GND}$, $T_J = -40^\circ\text{C} \text{ to } +85^\circ\text{C}, V_{OUT} = 0, \text{V}$</td>
<td>$I_{OFF}$</td>
<td>$V_{EN} = \text{GND}$ (includes reverse blocking bias current), $V_{OUT} = 0, \text{V}$</td>
<td>5</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>$V_{IN} \text{ to } V_{OUT}$ RESISTANCE</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 3.6, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 3.6, \text{V}$</td>
<td>0.050</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>WLCSP</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 2.5, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 2.5, \text{V}$</td>
<td>0.055</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{IN} = 1.8, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.8, \text{V}$</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 1.8, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.8, \text{V}, T_J = -40^\circ\text{C} \text{ to } +85^\circ\text{C}$</td>
<td>0.065</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{IN} = 1.5, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.5, \text{V}$</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 1.5, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.5, \text{V}$</td>
<td>0.075</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{IN} = 1.2, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.2, \text{V}$</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 1.2, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.2, \text{V}$</td>
<td>0.100</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{IN} = 1.8, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.8, \text{V}$</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 1.8, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.8, \text{V}$</td>
<td>0.070</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{IN} = 1.5, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.5, \text{V}$</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 1.5, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.5, \text{V}$</td>
<td>0.078</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{IN} = 1.8, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.8, \text{V}$</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 1.8, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.8, \text{V}$</td>
<td>0.090</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{IN} = 1.5, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.5, \text{V}$</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 1.5, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.5, \text{V}$</td>
<td>0.130</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{IN} = 1.2, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.2, \text{V}$</td>
<td>$R_{DS_{ON}}$</td>
<td>$V_{IN} = 1.2, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.2, \text{V}$</td>
<td>0.125</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>$V_{OUT}$ TURN-ON DELAY TIME</td>
<td>$t_{ON_DLY}$</td>
<td>$V_{IN} = 1.8, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 1.8, \text{V}, C_{LOAD} = 1, \text{µF}$</td>
<td>5</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Turn-On Delay Time</td>
<td>$t_{ON_DLY}$</td>
<td>$V_{IN} = 3.6, \text{V}, I_{LOAD} = 200, \text{mA}, V_{EN} = 3.6, \text{V}, C_{LOAD} = 1, \text{µF}$</td>
<td>1.5</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
</tbody>
</table>

TIMING DIAGRAM

![Timing Diagram](image-url)
ABSOLUTE MAXIMUM RATINGS

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN, VIN1, VIN2 to GND</td>
<td>−0.3 V to +4.0 V</td>
</tr>
<tr>
<td>VOUT, VOUT1, VOUT2 to GND</td>
<td>−0.3 V to +4.0 V</td>
</tr>
<tr>
<td>EN to GND</td>
<td>−0.3 V to +4.0 V</td>
</tr>
<tr>
<td>Continuous Drain Current</td>
<td>±2 A</td>
</tr>
<tr>
<td>Continuous Diode Current</td>
<td>±1.1 A</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>−40°C to +125°C</td>
</tr>
<tr>
<td>Operating Ambient Temperature Range</td>
<td>−40°C to +85°C</td>
</tr>
<tr>
<td>Soldering Conditions</td>
<td>JEDEC J-STD-020</td>
</tr>
</tbody>
</table>

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL DATA

Absolute maximum ratings apply individually only, not in combination. The ADP195 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that TJ is within the specified temperature limits. In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated.

In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature (TJ) of the device is dependent on the ambient temperature (TA), the power dissipation of the device (PD), and the junction-to-ambient thermal resistance of the package (θJA).

Maximum junction temperature (TJ) is calculated from the ambient temperature (TA) and power dissipation (PD) using the formula

\[ TJ = TA + (PD \times \theta_{JA}) \]

Junction-to-ambient thermal resistance (θJA) of the package is typically based on modeling and calculation using a 4-layer board. The junction-to-ambient thermal resistance is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of θJA may vary, depending on PCB material, layout, and environmental conditions. The specified values of θJA are based on a 4-layer, 4 inch × 3 inch PCB.

See JESD51-7 and JESD51-9 for detailed information regarding board construction. For additional information, see the AN-617 application note, MicroCSP™ Wafer Level Chip Scale Package.

ΨJB is the junction-to-board thermal characterization parameter with units of °C/W. ΨJB of the package is based on modeling and calculation using a 4-layer board. The JESD51-12 document, Guidelines for Reporting and Using Electronic Package Thermal Information, states that thermal characterization parameters are not the same as thermal resistances. ΨJB measures the component power flowing through multiple thermal paths rather than through a single path, as in thermal resistance (θJA). Therefore, ΨJB thermal paths include convection from the top of the package as well as radiation from the package, factors that make ΨJB more useful in real-world applications. Maximum junction temperature (TJ) is calculated from the board temperature (TB) and the power dissipation (PD) using the formula

\[ TJ = TB + (PD \times \Psi_{JB}) \]

See JESD51-8, JESD51-9, and JESD51-12 for more detailed information about ΨJB.

THERMAL RESISTANCE

θJA and ΨJB are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>θJA</th>
<th>ΨJB</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>4-Ball, 0.5 mm Pitch WLCSP</td>
<td>260</td>
<td>58.4</td>
<td>°C/W</td>
</tr>
<tr>
<td>6-Lead, 2 mm × 2 mm LFCSP</td>
<td>72.1</td>
<td>24.0</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 4. WLCSP Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A1</td>
<td>VIN</td>
<td>Input Voltage.</td>
</tr>
<tr>
<td>A2</td>
<td>VOUT</td>
<td>Output Voltage.</td>
</tr>
<tr>
<td>B1</td>
<td>EN</td>
<td>Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.</td>
</tr>
<tr>
<td>B2</td>
<td>GND</td>
<td>Ground.</td>
</tr>
</tbody>
</table>

Table 5. LFCSP Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VOUT1</td>
<td>Output Voltage. Connect VOUT1 and VOUT2 together.</td>
</tr>
<tr>
<td>2</td>
<td>VOUT2</td>
<td>Output Voltage. Connect VOUT1 and VOUT2 together.</td>
</tr>
<tr>
<td>3</td>
<td>GND</td>
<td>Ground.</td>
</tr>
<tr>
<td>4</td>
<td>EN</td>
<td>Enable Input. Drive EN high to turn on the switch and drive EN low to turn off the switch.</td>
</tr>
<tr>
<td>5</td>
<td>VIN2</td>
<td>Input Voltage. Connect VIN1 and VIN2 together.</td>
</tr>
<tr>
<td>6</td>
<td>VIN1</td>
<td>Input Voltage. Connect VIN1 and VIN2 together.</td>
</tr>
<tr>
<td>EP</td>
<td>EP</td>
<td>The exposed pad must be connected to ground.</td>
</tr>
</tbody>
</table>

NOTES
1. THE EXPOSED PAD MUST BE CONNECTED TO GND.
TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN} = 1.8 \, V, \, V_{EN} = V_{IN}, \, C_{IN} = C_{OUT} = 1 \, \mu F, \, T_A = 25^\circ C$, unless otherwise noted.

---

**Figure 5.** $R_{DS(ON)}$ vs. Temperature, WLCSP

---

**Figure 6.** $R_{DS(ON)}$ vs. Temperature, LFCSP

---

**Figure 7.** $R_{DS(ON)}$ vs. Input Voltage ($V_{IN}$), WLCSP

---

**Figure 8.** $R_{DS(ON)}$ vs. Input Voltage ($V_{IN}$), LFCSP

---

**Figure 9.** Voltage Drop vs. Load Current, WLCSP

---

**Figure 10.** Voltage Drop vs. Load Current, LFCSP
Figure 11. Typical Rise Time and Inrush Current, $V_{IN} = 3.6\, \text{V}, \text{No Load}$

Figure 12. Typical Rise Time and Inrush Current, $V_{IN} = 3.6\, \text{V}, \text{Load} = 200\, \text{mA}$

Figure 13. Typical Rise Time and Inrush Current, $V_{IN} = 1.2\, \text{V}, \text{No Load}$

Figure 14. Typical Rise Time and Inrush Current, $V_{IN} = 1.2\, \text{V}, \text{Load} = 200\, \text{mA}$

Figure 15. Ground Current vs. Temperature

Figure 16. Ground Current vs. Input Voltage ($V_{IN}$)
TEMPERATURE (°C)

SHUTDOWN CURRENT (µA)

VIN = 1.2V
VIN = 1.4V
VIN = 2.0V
VIN = 2.4V
VIN = 2.8V
VIN = 3.2V
VIN = 3.4V
VIN = 3.6V

Figure 17. Shutdown Current vs. Temperature

Figure 18. Reverse Input Shutdown Current vs. Temperature

Figure 19. Reverse Output Shutdown Current vs. Temperature

Figure 20. Reverse Shutdown Current vs. Temperature
The ADP195 is a high-side PMOS load switch. It is designed for supply operation between 1.1 V to 3.6 V. The PMOS load switch is designed for low on resistance, 65 mΩ at $V_{IN} = 1.8$ V and supports greater than 1 A of continuous current. It is a low quiescent current device with a nominal 4 MΩ pull-down resistor on its enable pin (EN).

The reverse current protection circuitry prevents current flow backward through the ADP195 when the output voltage is greater than the input voltage. A comparator senses the difference between the input and output voltages. When the difference between the input voltage and output voltage exceeds 75 mV, the body of the pFET is switched to $V_{OUT}$ and is turned off or opened; that is, the gate is connected to $V_{OUT}$.

The packaging is a space-saving 1.0 mm × 1.0 mm, 4-ball WLCSP. The ADP195 is also available in a 2 mm × 2 mm × 0.55 mm, 0.65 mm pitch LFCSP.
APPLICATIONS INFORMATION

GROUND CURRENT

The major source for ground current in the ADP195 is an internal 4 MΩ pull-down on the enable pin. Figure 22 shows the typical ground current when $V_{EN} = V_{IN}$ and varies from 1.2 V to 3.6 V.

![Figure 22. Ground Current vs. Load Current](image)

As shown in Figure 23, an increase in quiescent current can occur when $V_{EN} \neq V_{IN}$. This is caused by the CMOS logic nature of the level shift circuitry as it translates an $V_{EN}$ signal ≥ 1.2 V to a logic high. This increase is a function of the $V_{IN} - V_{EN}$ delta.

![Figure 23. Typical Ground Current when $V_{EN} \neq V_{IN}$](image)

ENABLE FEATURE

The ADP195 uses the EN pin to enable and disable the VOUT pin under normal operating conditions. As shown in Figure 24, when a rising voltage on $V_{EN}$ crosses the active threshold, $V_{OUT}$ turns on. When a falling voltage on $V_{EN}$ crosses the inactive threshold, $V_{OUT}$ turns off.

![Figure 24. Typical EN Operation](image)

As shown in Figure 24, the EN pin has hysteresis built in. This prevents on/off oscillations that can occur due to noise on the EN pin as it passes through the threshold points.

The EN pin active/inactive thresholds derive from the $V_{IN}$ voltage; therefore, these thresholds vary with the changing input voltage. Figure 25 shows the typical EN active/inactive thresholds when the input voltage varies from 1.2 V to 3.6 V.

![Figure 25. Typical EN Thresholds vs. Input Voltage ($V_{IN}$)](image)
TIMING

Turn-on delay is defined as the delta between the time that $V_{EN}$ reaches >1.2 V until $V_{OUT}$ rises to ~10% of its final value. The ADP195 includes circuitry to have typical 5 $\mu$s turn-on delay at 3.6 V $V_{IN}$ to limit the $V_{IN}$ inrush current. As shown in Figure 26, the turn-on delay is dependent on the input voltage.

The rise time is defined as the delta between the time from 10% to 90% of $V_{OUT}$ reaching its final value. It is dependent on the RC time constant where $C = \text{load capacitance (CLOAD)}$ and $R = \text{RDS}_{\text{ON}} || \text{RLOAD}$. Because $\text{RDS}_{\text{ON}}$ is usually smaller than $\text{RLOAD}$, an adequate approximation for RC is $\text{RDS}_{\text{ON}} \times \text{CLOAD}$. An input or load capacitor is not needed for the ADP195; however, capacitors can be used to suppress noise on the board. If significant load capacitance is connected, inrush current is a concern.

The turn-off time is defined as the delta between the time from 90% to 10% of $V_{OUT}$ reaching its final value. It is also dependent on the RC time constant.
OUTLINE DIMENSIONS

Figure 30. 4-Ball Wafer Level Chip Scale Package [WLCSP] (CB-4-4)
Dimensions shown in millimeters

Figure 31. 6-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 x 2.00 mm Body, Ultra Thin, Dual Lead (CP-6-3)
Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
<th>Branding</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADP195ACBZ-R7</td>
<td>−40°C to +85°C</td>
<td>4-Ball Wafer Level Chip Scale Package [WLCSP]</td>
<td>CB-4-4</td>
<td>5Y</td>
</tr>
<tr>
<td>ADP195ACPZ-R7</td>
<td>−40°C to +85°C</td>
<td>6-Lead Lead Frame Chip Scale Package [LFCSP_UD]</td>
<td>CP-6-3</td>
<td>LJ6</td>
</tr>
<tr>
<td>ADP195-EVALZ</td>
<td></td>
<td>Evaluation Board</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADP195-CP-EVALZ</td>
<td></td>
<td>Evaluation Board</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.