Synchronous Current-Mode with Constant On-Time, PWM Buck Controller

FEATURES
- Power input voltage as low as 2.75 V to 20 V
- Bias supply voltage range: 2.75 V to 5.5 V
- Minimum output voltage: 0.6 V
- 0.6 V reference voltage with ±1.0% accuracy
- Supports all N-channel MOSFET power stages
- Available in 300 kHz, 600 kHz, and 1.0 MHz options
- No current-sense resistor required
- Power saving mode (PSM) for light loads (ADP1873 only)
- Resistor-programmable current-sense gain
- Thermal overload protection
- Short-circuit protection
- Precision enable input
- Integrated bootstrap diode for high-side drive
- 140 µA shutdown supply current
- Starts into a precharged load
- Small, 10-lead MSOP package

APPLICATIONS
- Telecom and networking systems
- Mid to high end servers
- Set-top boxes
- DSP core power supplies

GENERAL DESCRIPTION
The ADP1872/ADP1873 are versatile current-mode, synchronous step-down controllers that provide superior transient response, optimal stability, and current limit protection by using a constant on-time, pseudo-fixed frequency with a programmable current-sense gain, current-control scheme. In addition, these devices offer optimum performance at low duty cycles by using valley current-mode control architecture. This allows the ADP1872/ADP1873 to drive all N-channel power stages to regulate output voltages as low as 0.6 V.

The ADP1873 is the power saving mode (PSM) version of the device and is capable of pulse skipping to maintain output regulation while achieving improved system efficiency at light loads (see the Power Saving Mode (PSM) Version (ADP1873) section for more information).

Available in three frequency options (300 kHz, 600 kHz, and 1.0 MHz, plus the PSM option), the ADP1872/ADP1873 are well suited for a wide range of applications. These ICs not only operate from a 2.75 V to 5.5 V bias supply, but can also accept a power input as high as 20 V.

In addition, an internally fixed, soft start period is included to limit input in-rush current from the input supply during startup and to provide reverse current protection during soft start for a precharged output. The low-side current-sense, current-gain scheme and integration of a boost diode, along with the PSM/forced pulse-width modulation (PWM) option, reduce the external part count and improve efficiency.

The ADP1872/ADP1873 operate over the −40°C to +125°C junction temperature range and are available in a 10-lead MSOP.
SPECIFICATIONS

All limits at temperature extremes are guaranteed via correlation using standard statistical quality control (SQC). VDD = 5 V, BST – SW = 5 V, VIN = 13 V. The specifications are valid for TJ = −40°C to +125°C, unless otherwise specified.

<table>
<thead>
<tr>
<th>Table 1. Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>POWER SUPPLY CHARACTERISTICS</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Input Voltage Range</td>
<td>VIN</td>
<td>ADP1872ARMZ-0.3/ADP1873ARMZ-0.3 (300 kHz)</td>
<td>2.75</td>
<td>12</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADP1872ARMZ-0.6/ADP1873ARMZ-0.6 (600 kHz)</td>
<td>2.75</td>
<td>12</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADP1872ARMZ-1.0/ADP1873ARMZ-1.0 (1.0 MHz)</td>
<td>3.0</td>
<td>12</td>
<td>20</td>
<td>V</td>
</tr>
<tr>
<td>Low Input Voltage Range</td>
<td>VDD</td>
<td>CIN = 1 µF to PGND, CIN = 0.22 µF to GND</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADP1872ARMZ-0.3/ADP1873ARMZ-0.3 (300 kHz)</td>
<td>2.75</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADP1872ARMZ-0.6/ADP1873ARMZ-0.6 (600 kHz)</td>
<td>2.75</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>ADP1872ARMZ-1.0/ADP1873ARMZ-1.0 (1.0 MHz)</td>
<td>3.0</td>
<td>5</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>Quiescent Current</td>
<td>IQ_DD + IQ_BST</td>
<td>FB = 1.5 V, no switching</td>
<td>1.1</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Shutdown Current</td>
<td>IDD, SD + IBST, SD COMP/EN &lt; 285 mV</td>
<td>140</td>
<td>215</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Undervoltage Lockout</td>
<td>UVLO</td>
<td>Rising VDD (See Figure 34 for temperature variation)</td>
<td>2.65</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling VDD from operational state</td>
<td>190</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SOFT START</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Soft Start Period</td>
<td></td>
<td></td>
<td>3.0</td>
<td>ms</td>
<td></td>
<td></td>
</tr>
<tr>
<td>ERROR AMPLIFIER</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>FB Regulation Voltage</td>
<td>VFB</td>
<td>TJ = 25°C</td>
<td>600</td>
<td>mV</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>TJ = −40°C to +85°C</td>
<td>595.5</td>
<td>600</td>
<td>605.4</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>TJ = −40°C to +125°C</td>
<td>594.2</td>
<td>600</td>
<td>606.5</td>
<td>mV</td>
</tr>
<tr>
<td>Transconductance</td>
<td>GM</td>
<td>300</td>
<td>515</td>
<td>730</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>FB Input Leakage Current</td>
<td>IFB, LEAK</td>
<td>FB = 0.6 V, COMP/EN = released</td>
<td>1</td>
<td>50</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>CURRENT-SENSE AMPLIFIER GAIN</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Programming Resistor (RES) Value from DRVL to PGND</td>
<td></td>
<td>RES = 47 kΩ ± 1%</td>
<td>2.7</td>
<td>3</td>
<td>3.3</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES = 22 kΩ ± 1%</td>
<td>5.5</td>
<td>6</td>
<td>6.5</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES = none</td>
<td>11</td>
<td>12</td>
<td>13</td>
<td>V/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>RES = 100 kΩ ± 1%</td>
<td>22</td>
<td>24</td>
<td>26</td>
<td>V/V</td>
</tr>
<tr>
<td>SWITCHING FREQUENCY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ADP1872ARMZ-0.3/ADP1873ARMZ-0.3 (300 kHz)</td>
<td>On-Time</td>
<td>VIN = 5 V, VOUT = 2 V, TJ = 25°C</td>
<td>1120</td>
<td>1200</td>
<td>1280</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VIN = 20 V</td>
<td>145</td>
<td>190</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>84% duty cycle (maximum)</td>
<td>320</td>
<td>385</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>ADP1872ARMZ-0.6/ADP1873ARMZ-0.6 (600 kHz)</td>
<td>On-Time</td>
<td>VIN = 5 V, VOUT = 2 V, TJ = 25°C</td>
<td>500</td>
<td>520</td>
<td>580</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VIN = 20 V, VOUT = 0.8 V</td>
<td>82</td>
<td>110</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>65% duty cycle (maximum)</td>
<td>320</td>
<td>385</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>ADP1872ARMZ-1.0/ADP1873ARMZ-1.0 (1.0 MHz)</td>
<td>On-Time</td>
<td>VIN = 5 V, VOUT = 2 V, TJ = 25°C</td>
<td>285</td>
<td>312</td>
<td>340</td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>VIN = 20 V</td>
<td>60</td>
<td>85</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>45% duty cycle (maximum)</td>
<td>320</td>
<td>385</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>
### OUTPUT DRIVER CHARACTERISTICS

**High-Side Driver**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Source Resistance</td>
<td></td>
<td>$I_{\text{SOURCE}} = 1.5 \text{ A, 100 ns, positive pulse (0 V to 5 V)}$</td>
<td>2</td>
<td>3.5</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Output Sink Resistance</td>
<td></td>
<td>$I_{\text{Sink}} = 1.5 \text{ A, 100 ns, negative pulse (5 V to 0 V)}$</td>
<td>0.8</td>
<td></td>
<td>2</td>
<td>Ω</td>
</tr>
<tr>
<td>Rise Time $^2$</td>
<td>$t_{\text{DRVH}}$</td>
<td>$\text{BST} \rightarrow \text{SW} = 4.4 \text{ V, } C_{\text{IN}} = 4.3 \text{ nF (see Figure 59)}$</td>
<td>25</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time $^2$</td>
<td>$t_{\text{DRVH}}$</td>
<td>$\text{BST} \rightarrow \text{SW} = 4.4 \text{ V, } C_{\text{IN}} = 4.3 \text{ nF (see Figure 60)}$</td>
<td>11</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Low-Side Driver**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Output Source Resistance</td>
<td></td>
<td>$I_{\text{SOURCE}} = 1.5 \text{ A, 100 ns, positive pulse (0 V to 5 V)}$</td>
<td>1.7</td>
<td>3</td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Output Sink Resistance</td>
<td></td>
<td>$I_{\text{Sink}} = 1.5 \text{ A, 100 ns, negative pulse (5 V to 0 V)}$</td>
<td>0.75</td>
<td></td>
<td>2</td>
<td>Ω</td>
</tr>
<tr>
<td>Rise Time $^2$</td>
<td>$t_{\text{DRVL}}$</td>
<td>$\text{VDD} = 5.0 \text{ V, } C_{\text{IN}} = 4.3 \text{ nF (see Figure 60)}$</td>
<td>18</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Fall Time $^2$</td>
<td>$t_{\text{DRVL}}$</td>
<td>$\text{VDD} = 5.0 \text{ V, } C_{\text{IN}} = 4.3 \text{ nF (see Figure 59)}$</td>
<td>16</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

**Propagation Delays**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRVL Fall to DRVH Rise $^2$</td>
<td>$t_{\text{PDH, DRVH}}$</td>
<td>$\text{BST} \rightarrow \text{SW} = 4.4 \text{ V (see Figure 59)}$</td>
<td>22</td>
<td>ns</td>
</tr>
<tr>
<td>DRVH Fall to DRVL Rise $^2$</td>
<td>$t_{\text{PDH, DRVL}}$</td>
<td>$\text{BST} \rightarrow \text{SW} = 4.4 \text{ V (see Figure 60)}$</td>
<td>24</td>
<td>ns</td>
</tr>
</tbody>
</table>

**SW Leakage Current**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low-Side Driver</td>
<td>$I_{\text{Sink, SW, LEAK}}$</td>
<td>$\text{BST} = 25 \text{ V, SW} = 20 \text{ V, VDD} = 5.5 \text{ V}$</td>
<td>110</td>
<td>μA</td>
</tr>
</tbody>
</table>

**Integrated Rectifier**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Channel Impedance</td>
<td>$I_{\text{IN, LEAK}}$</td>
<td>$\text{BST} = 10 \text{ mA}$</td>
<td>22</td>
<td>Ω</td>
</tr>
</tbody>
</table>

### PRECISION ENABLE THRESHOLD

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Logic High Level</td>
<td></td>
<td>$\text{VIN} = 2.9 \text{ V to 20 V, VDD} = 2.75 \text{ V to 5.5 V}$</td>
<td>235</td>
<td>285</td>
<td>330</td>
<td>mV</td>
</tr>
<tr>
<td>Enable Hysteresis</td>
<td></td>
<td>$\text{VIN} = 2.9 \text{ V to 20 V, VDD} = 2.75 \text{ V to 5.5 V}$</td>
<td>35</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
</tbody>
</table>

### COMP VOLTAGE

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMP Clamp Low Voltage</td>
<td>$V_{\text{COMP (LOW)}}$</td>
<td>From disable state, release COMP/EN pin to enable device ($2.75 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$)</td>
<td>0.47</td>
<td>V</td>
</tr>
<tr>
<td>COMP Clamp High Voltage</td>
<td>$V_{\text{COMP (HIGH)}}$</td>
<td>($2.75 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$)</td>
<td>2.55</td>
<td>V</td>
</tr>
<tr>
<td>COMP Zero Current Threshold</td>
<td>$V_{\text{COMP, ZCT}}$</td>
<td>($2.75 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$)</td>
<td>1.15</td>
<td>V</td>
</tr>
</tbody>
</table>

### THERMAL SHUTDOWN

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Thermal Shutdown Threshold</td>
<td>$T_{\text{MSD}}$</td>
<td>Rising temperature</td>
<td>155</td>
<td>°C</td>
</tr>
<tr>
<td>Thermal Shutdown Hysteresis</td>
<td></td>
<td>$\text{VDD} \leq 5 \text{ V}$</td>
<td>15</td>
<td>°C</td>
</tr>
<tr>
<td>Hiccup Current Limit Timing</td>
<td></td>
<td>$\text{VDD} \leq 5 \text{ V}$</td>
<td>6</td>
<td>ms</td>
</tr>
</tbody>
</table>

---

$^1$ The maximum specified values are with the closed loop measured at 10% to 90% time points (see Figure 59 and Figure 60), $C_{\text{GATE}} = 4.3 \text{ nF}$ and upper- and lower-side MOSFETs being Infineon BSC042N03MS G.

$^2$ Not automatic test equipment (ATE) tested.
ABSOLUTE MAXIMUM RATINGS

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VDD to GND</td>
<td>−0.3 V to +6 V</td>
</tr>
<tr>
<td>VIN to PGND</td>
<td>−0.3 V to +28 V</td>
</tr>
<tr>
<td>FB, COMP/EN to GND</td>
<td>−0.3 V to (VDD + 0.3 V)</td>
</tr>
<tr>
<td>DRVL to PGND</td>
<td>−0.3 V to (VDD + 0.3 V)</td>
</tr>
<tr>
<td>SW to PGND</td>
<td>−0.3 V to +28 V</td>
</tr>
<tr>
<td>SW to PGND</td>
<td>−2 V pulse (20 ns)</td>
</tr>
<tr>
<td>BST to SW</td>
<td>−0.6 V to (VDD + 0.3 V)</td>
</tr>
<tr>
<td>BST to PGND</td>
<td>−0.3 V to +28 V</td>
</tr>
<tr>
<td>DRVH to SW</td>
<td>−0.3 V to VDD</td>
</tr>
<tr>
<td>PGND to GND</td>
<td>±0.3 V</td>
</tr>
<tr>
<td>Operating Junction Temperature Range</td>
<td>−40°C to +125°C</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Soldering Conditions</td>
<td>JEDEC J-STD-020</td>
</tr>
<tr>
<td>Maximum Soldering Lead Temperature (10 sec)</td>
<td>300°C</td>
</tr>
</tbody>
</table>

Absolute maximum ratings apply individually only, not in combination. Unless otherwise specified, all other voltages are referenced to PGND.

THERMAL RESISTANCE

θJA is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>θJA</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>θJA (10-Lead MSOP)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2-Layer Board</td>
<td>213.1</td>
<td>°C/W</td>
</tr>
<tr>
<td>4-Layer Board</td>
<td>171.7</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

BOUNDARY CONDITION

In determining the values given in Table 2 and Table 3, natural convection was used to transfer heat to a 4-layer evaluation board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

Table 4. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VIN</td>
<td>High Input Voltage. Connect VIN to the drain of the upper-side MOSFET.</td>
</tr>
<tr>
<td>2</td>
<td>COMP/EN</td>
<td>Output of the Internal Error Amplifier/IC Enable. When this pin functions as EN, applying 0 V to this pin disables the IC.</td>
</tr>
<tr>
<td>3</td>
<td>FB</td>
<td>Noninverting Input of the Internal Error Amplifier. This is the node where the feedback resistor is connected.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Analog Ground Reference Pin of the IC. All sensitive analog components should be connected to this ground plane (see the Layout Considerations Section).</td>
</tr>
<tr>
<td>5</td>
<td>VDD</td>
<td>Bias Voltage Supply for the ADP1872/ADP1873 Controller (Includes the Output Gate Drivers). A bypass capacitor of 1 μF directly from this pin to PGND and a 0.1 μF across VDD and GND are recommended.</td>
</tr>
<tr>
<td>6</td>
<td>DRVL</td>
<td>Drive Output for the External Lower Side, N-Channel MOSFET. This pin also serves as the current-sense gain setting pin (see Figure 68).</td>
</tr>
<tr>
<td>7</td>
<td>PGND</td>
<td>Power GND. Ground for the lower side gate driver and lower side, N-channel MOSFET.</td>
</tr>
<tr>
<td>8</td>
<td>DRVH</td>
<td>Drive Output for the External Upper Side, N-Channel MOSFET.</td>
</tr>
<tr>
<td>9</td>
<td>SW</td>
<td>Switch Node Connection.</td>
</tr>
<tr>
<td>10</td>
<td>BST</td>
<td>Bootstrap for the Upper Side MOSFET Gate Drive Circuitry. An internal boot rectifier (diode) is connected between VDD and BST. A capacitor from BST to SW is required. An external Schottky diode can also be connected between VDD and BST for increased gate drive capability.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. Efficiency—300 kHz, V_{OUT} = 0.8 V

Figure 5. Efficiency—300 kHz, V_{OUT} = 1.8 V

Figure 6. Efficiency—300 kHz, V_{OUT} = 7 V

Figure 7. Efficiency—600 kHz, V_{OUT} = 0.8 V

Figure 8. Efficiency—600 kHz, V_{OUT} = 1.8 V

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Figure 11. Efficiency—1.0 MHz, \(V_{\text{OUT}} = 1.8\ V\)

Figure 12. Efficiency—1.0 MHz, \(V_{\text{OUT}} = 4\ V\)

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Figure 14. Output Voltage Accuracy—300 kHz, \(V_{\text{OUT}} = 1.8\ V\)

Figure 15. Output Voltage Accuracy—300 kHz, \(V_{\text{OUT}} = 7\ V\)
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Figure 26. Frequency vs. Load Current, 300 kHz, V_{OUT} = 1.8 V

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Figure 30. Frequency vs. Load Current, 600 kHz, $V_{OUT} = 5$ V

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20 A, $V_{OUT} = 1.8$ V (See Figure 91 Application Circuit)

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20 A (See Figure 91 Application Circuit)

Figure 49. Load Transient Step—Forced PWM at Light Load, 20 A
(See Figure 91 Application Circuit)

Figure 50. Positive Step During Heavy Load Transient Behavior—Forced PWM at Light Load, 20 A, $V_{OUT} = 1.8$ V (See Figure 91 Application Circuit)

Figure 51. Negative Step During Heavy Load Transient Behavior—Forced PWM at Light Load, 20 A (See Figure 91 Application Circuit)
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THEORY OF OPERATION

The ADP1872/ADP1873 are versatile current-mode, synchronous step-down controllers that provide superior transient response, optimal stability, and current limit protection by using a constant on-time, pseudo-fixed frequency with a programmable current-sense gain, current-control scheme. In addition, these devices offer optimum performance at low duty cycles by using valley current-mode control architecture. This allows the ADP1872/ADP1873 to drive all N-channel power stages to regulate output voltages as low as 0.6 V.

STARTUP

The ADP1872/ADP1873 have an input low voltage pin (VDD) for biasing and supplying power for the integrated MOSFET drivers. A bypass capacitor should be located directly across the VDD (Pin 5) and PGND (Pin 7) pins. Included in the power-up sequence is the biasing of the current-sense amplifier, the current-sense gain circuit (see the Programming Resistor (RES) Detect Circuit section), the soft start circuit, and the error amplifier.

The current-sense blocks provide valley current information (see the Programming Resistor (RES) Detect Circuit section) and are a variable of the compensation equation for loop stability (see the Compensation Network section). The valley current information is extracted by forcing 0.4 V across the DRVL output and the PGND pin, which generates a current depending on the resistor across DRVL and PGND in a process performed by the RES detect circuit. The current through the resistor is used to set the current-sense amplifier gain. This process takes approximately 800 µs, after which the drive signal pulses appear at the DRVL and DRVH pins synchronously and the output voltage begins to rise in a controlled manner through the soft start sequence. The rise time of the output voltage is determined by the soft start and error amplifier blocks (see the Soft Start section). At the beginning of a soft start, the error amplifier charges the external compensation capacitor, causing the COMP/EN pin to rise above the enable threshold of 285 mV, thus enabling the ADP1872/ADP1873.

SOFT START

The ADP1872/ADP1873 have digital soft start circuitry, which involves a counter that initiates an incremental increase in current, by 1 µA, via a current source on every cycle through a fixed internal capacitor. The output tracks the ramping voltage by producing PWM output pulses to the upper side MOSFET. The purpose is to limit the in-rush current from the high voltage input supply (VIN) to the output (VOUT).

PRECISION ENABLE CIRCUITRY

The ADP1872/ADP1873 employ precision enable circuitry. The enable threshold is 285 mV typical with 35 mV of hysteresis. The devices are enabled when the COMP/EN pin is released, allowing the error amplifier output to rise above the enable threshold (see Figure 65). Grounding this pin disables the ADP1872/ADP1873, reducing the supply current of the devices to approximately 140 µA. For more information, see Figure 66.

UNDervoltage LOCKout

The undervoltage lockout (UVLO) feature prevents the part from operating both the upper side and lower side MOSFETs at extremely low or undefined input voltage (VDD) ranges. Operation at an undefined bias voltage may result in the incorrect propagation of signals to the high-side power switches. This, in turn, results in invalid output behavior that can cause damage to the output devices, ultimately destroying the device tied at the output. The UVLO level has been set at 2.65 V (nominal).

THERMAL SHUTDOWN

The thermal shutdown is a self-protection feature to prevent the IC from damage due to a very high operating junction temperature. If the junction temperature of the device exceeds 155°C, the part enters the thermal shutdown state. In this state, the device shuts off both the upper side and lower side MOSFETs and disables the entire controller immediately, thus reducing the power consumption of the IC. The part resumes operation after the junction temperature of the part cools to less than 140°C.
PROGRAMMING RESISTOR (RES) DETECT CIRCUIT

Upon startup, one of the first blocks to become active is the RES detect circuit. This block powers up before soft start begins. It forces a 0.4 V reference value at the DRVL output (see Figure 67) and is programmed to identify four possible resistor values: 47 kΩ, 22 kΩ, open, and 100 kΩ.

The RES detect circuit digitizes the value of the resistor at the DRVL pin (Pin 6). An internal ADC outputs a 2-bit digital code that is used to program four separate gain configurations in the current-sense amplifier (see Figure 68). Each configuration corresponds to a current-sense gain ($A_{CS}$) of 3 V/V, 6 V/V, 12 V/V, 24 V/V, respectively (see Table 5 and Table 6). This variable is used for the valley current-limit setting, which sets up the appropriate current-sense gain for a given application and sets the compensation necessary to achieve loop stability (see the Valley Current-Limit Setting and Compensation Network sections).

VALLEY CURRENT-LIMIT SETTING

The architecture of the ADP1872/ADP1873 is based on valley current-mode control. The current limit is determined by three components: the $R_{ON}$ of the lower side MOSFET, the error amplifier output voltage swing (COMP), and the current-sense gain. The COMP range is internally fixed at 1.4 V. The current-sense gain is programmable via an external resistor at the DRVL pin (see the Programming Resistor (RES) Detect Circuit section). The $R_{ON}$ of the lower side MOSFET can vary over temperature and usually has a positive $T_C$ (meaning that it increases with temperature); therefore, it is recommended to program the current-sense gain resistor based on the rated $R_{ON}$ of the MOSFET at 125°C.

Because the ADP1872/ADP1873 are based on valley current control, the relationship between $I_{CLIM}$ and $I_{LOAD}$ is

$$I_{CLIM} = I_{LOAD} \times \left(1 - \frac{K_I}{2}\right)$$

where:

- $I_{CLIM}$ is the desired valley current limit.
- $I_{LOAD}$ is the current load.
- $K_I$ is the ratio between the inductor ripple current and the desired average load current (see Figure 10). Establishing $K_I$ helps to determine the inductor value (see the Inductor Selection section), but in most cases, $K_I = 0.33$.

When the desired valley current limit ($I_{CLIM}$) has been determined, the current-sense gain can be calculated by

$$I_{CLIM} = \frac{1.4 \text{ V}}{A_{CS} \times R_{ON}}$$

where:

- $A_{CS}$ is the current-sense gain multiplier (see Table 5 and Table 6).
- $R_{ON}$ is the channel impedance of the lower side MOSFET.

Although the ADP1872/ADP1873 have only four discrete current-sense gain settings for a given $R_{ON}$ variable, Table 6 and Figure 70 outline several available options for the valley current setpoint based on various $R_{ON}$ values.
Table 6. Valley Current Limit Program

<table>
<thead>
<tr>
<th>$R_{ON}$ (mΩ)</th>
<th>Valley Current Level</th>
<th>ACS = 3 V/V</th>
<th>ACS = 6 V/V</th>
<th>ACS = 12 V/V</th>
<th>ACS = 24 V/V</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td></td>
<td>38.9</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>29.2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2.5</td>
<td></td>
<td>23.3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>39.0</td>
<td>19.5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3.5</td>
<td>33.4</td>
<td>16.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>26.0</td>
<td>13</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>23.4</td>
<td>11.7</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5.5</td>
<td>21.25</td>
<td>10.6</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>23.3</td>
<td>11.7</td>
<td>5.83</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15</td>
<td>31.0</td>
<td>15.5</td>
<td>7.75</td>
<td>3.87</td>
<td></td>
</tr>
<tr>
<td>18</td>
<td>26.0</td>
<td>13.0</td>
<td>6.5</td>
<td>3.25</td>
<td></td>
</tr>
</tbody>
</table>

1 Refer to Figure 70 for more information and a graphical representation.

The valley current limit is programmed as outlined in Table 6 and Figure 70. The inductor chosen must be rated to handle the peak current, which is equal to the valley current from Table 6 plus the peak-to-peak inductor ripple current (see the Inductor Selection section). In addition, the peak current value must be used to compute the worst-case power dissipation in the MOSFETs (see Figure 71).

**HICCUP MODE DURING SHORT CIRCUIT**

A current-limit violation occurs when the current across the source and drain of the lower side MOSFET exceeds the current-limit setpoint. When 32 current-limit violations are detected, the controller enters idle mode and turns off the MOSFETs for 6 ms, allowing the converter to cool down. Then, the controller re-establishes soft start and begins to cause the output to ramp up again (see Figure 72). While the output ramps up, COMP is monitored to determine if the violation is still present. If it is still present, the idle event occurs again, followed by the full-chip power-down sequence. This cycle continues until the violation no longer exists. If the violation disappears, the converter is allowed to switch normally, maintaining regulation.
SYNCHRONOUS RECTIFIER

The ADP1872/ADP1873 employ an internal lower side MOSFET driver to drive the external upper side and lower side MOSFETs. The synchronous rectifier not only improves overall conduction efficiency but also ensures proper charging to the bootstrap capacitor located at the upper side driver input. This is beneficial during startup to provide sufficient drive signal to the external upper side MOSFET and attain fast turn-on response, which is essential for minimizing switching losses. The integrated upper and lower side MOSFET drivers operate in complementary fashion with built-in anticross conduction circuitry to prevent unwanted shoot-through current that may potentially damage the MOSFETs or reduce efficiency as a result of excessive power loss.

POWER SAVING MODE (PSM) VERSION (ADP1873)

The power saving mode version of the ADP1872 is the ADP1873. The ADP1873 operates in the discontinuous conduction mode (DCM) and pulse skips at light load to midload currents. It outputs pulses as necessary to maintain output regulation. Unlike the continuous conduction mode (CCM), DCM operation prevents negative current, thus allowing improved system efficiency at light loads. Current in the reverse direction through this pathway, however, results in power dissipation and therefore a decrease in efficiency.

As soon as the forward current through the lower side MOSFET decreases to a level where
\[ 10 \text{ mV} = I_{Q2} \times R_{ON(Q2)} \]
the zero-cross comparator (or \( I_{REV} \) comparator) emits a signal to turn off the lower side MOSFET. From this point, the slope of the inductor current ramping down becomes steeper (see Figure 75) as the body diode of the lower side MOSFET begins to conduct current and continues conducting current until the remaining energy stored in the inductor has been depleted.

Figure 75. 10 mV Offset to Ensure Prevention of Negative Inductor Current

The system remains in idle mode until the output voltage drops below regulation. A PWM pulse is then produced, turning on the upper side MOSFET to maintain system regulation. The ADP1873 does not have an internal clock; therefore, it switches purely as a hysteretic controller, as described in this section.

TIMER OPERATION

The ADP1872/ADP1873 employ a constant on-time architecture, which provides a variety of benefits, including improved load and line transient response when compared with a constant (fixed) frequency current-mode control loop of comparable loop design. The constant on-time timer, or \( t_{ON} \) timer, senses the high input voltage (\( V_{IN} \)) and the output voltage (\( V_{OUT} \)) using SW waveform information to produce an adjustable one-shot PWM pulse that varies the on-time of the upper side MOSFET in response to dynamic changes in input voltage, output voltage, and load current conditions to maintain regulation. It then generates an on-time (\( t_{ON} \)) pulse that is inversely proportional to \( V_{IN} \).

\[ t_{ON} = K \times \frac{V_{OUT}}{V_{IN}} \]

where \( K \) is a constant that is trimmed using an RC timer product for the 300 kHz, 600 kHz, and 1.0 MHz frequency options.
The constant on-time \( t_{\text{ON}} \) is not strictly constant because it varies with \( \text{VIN} \) and \( \text{VOUT} \). However, this variation occurs in such a way as to keep the switching frequency virtually independent of \( \text{VIN} \) and \( \text{VOUT} \).

The \( t_{\text{ON}} \) timer uses a feedforward technique, applied to the constant on-time control loop, making it pseudo-fixed frequency to a first order. Second-order effects, such as dc losses in the external power MOSFETs (see the Efficiency Consideration section), cause some variation in frequency vs. \( \text{VIN} \) and \( \text{VOUT} \). These effects are shown in Figure 22 to Figure 33. The variations in frequency are much reduced compared with the variations generated when the feedforward technique is not used.

The feedforward technique establishes the following relationship:

\[
f_{\text{SW}} = \frac{1}{K}
\]

where \( f_{\text{SW}} \) is the controller switching frequency (300 kHz, 600 kHz, and 1.0 MHz).

The \( t_{\text{ON}} \) timer senses \( \text{VIN} \) and \( \text{VOUT} \) to minimize frequency variation with \( \text{VIN} \) and \( \text{VOUT} \) as previously explained. This provides a pseudo-fixed frequency, see the Pseudo-Fixed Frequency section for additional information. To allow headroom for \( \text{VIN}/\text{VOUT} \) sensing, the following two equations must be adhered to. For typical applications where \( \text{VDD} \) is 5 V, these equations are not relevant; however, for lower \( \text{VDD} \), care may be required.

\[
\text{VDD} \geq \frac{\text{VIN}}{8} + 1.5
\]

\[
\text{VDD} \geq \frac{\text{VOUT}}{4}
\]

**PSEUDO-FIXED FREQUENCY**

The ADP1872/ADP1873 employ a constant on-time control scheme. During steady state operation, the switching frequency stays relatively constant, or pseudo-fixed. This is due to the one-shot \( t_{\text{ON}} \) timer that produces a high-side PWM pulse with a fixed duration, given that external conditions such as input voltage, output voltage, and load current are also at steady state. During load transients, the frequency momentarily changes for the duration of the transient event so that the output comes back within regulation quicker than if the frequency were fixed or if it were to remain unchanged. After the transient event is complete, the frequency returns to a pseudo-fixed value to a first-order.

To illustrate this feature more clearly, this section describes one such load transient event—a positive load step—in detail. During load transient events, the high-side driver output pulse width stays relatively consistent from cycle to cycle; however, the off-time (DRVL on-time) dynamically adjusts according to the instantaneous changes in the external conditions mentioned.

When a positive load step occurs, the error amplifier (out of phase of the output, \( \text{VOUT} \)) produces new voltage information at its output (COMP). In addition, the current-sense amplifier senses new inductor current information during this positive load transient event. The error amplifier's output voltage reaction is compared to the new inductor current information that sets the start of the next switching cycle. Because current information is produced from valley current sensing, it is sensed at the down ramp of the inductor current, whereas the voltage loop information is sensed through the counter action upswing of the error amplifier's output (COMP).

The result is a convergence of these two signals (see Figure 77), which allows an instantaneous increase in switching frequency during the positive load transient event. In summary, a positive load step causes \( \text{VOUT} \) to transient down, which causes COMP to transient up and therefore shortens the off time. This resulting increase in frequency during a positive load transient helps to quickly bring \( \text{VOUT} \) back up in value and within the regulation window.

Similarly, a negative load step causes the off time to lengthen in response to \( \text{VOUT} \) rising. This effectively increases the inductor demagnetizing phase, helping to bring \( \text{VOUT} \) to within regulation. In this case, the switching frequency decreases, or experiences a foldback, to help facilitate output voltage recovery.

Because the ADP1872/ADP1873 has the ability to respond rapidly to sudden changes in load demand, the recovery period in which the output voltage settles back to its original steady state operating point is much quicker than it would be for a fixed-frequency equivalent. Therefore, using a pseudo-fixed frequency, results in significantly better load transient performance than using a fixed frequency.
APPLICATIONS INFORMATION

FEEDBACK RESISTOR DIVIDER

The required resistor divider network can be determined for a given \( V_{\text{OUT}} \) value because the internal band gap reference (\( V_{\text{REF}} \)) is fixed at 0.6 V. Selecting values for \( R_T \) and \( R_S \) determines the minimum output load current of the converter. Therefore, for a given value of \( R_S \), the \( R_T \) value can be determined by

\[
R_T = R_S \times \frac{(V_{\text{OUT}} - 0.6 \text{ V})}{0.6 \text{ V}}
\]

INDUCTOR SELECTION

The inductor value is inversely proportional to the inductor ripple current. The peak-to-peak ripple current is given by

\[
\Delta I_L = K_I \times I_{\text{LOAD}} \approx \frac{I_{\text{LOAD}}}{3}
\]

where \( K_I \) is typically 0.33.

The equation for the inductor value is given by

\[
L = \frac{(V_{\text{IN}} - V_{\text{OUT}})}{\Delta I_L \times f_{\text{SW}}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}}}
\]

where:
- \( V_{\text{IN}} \) is the high voltage input.
- \( V_{\text{OUT}} \) is the desired output voltage.
- \( f_{\text{SW}} \) is the controller switching frequency (300 kHz, 600 kHz, and 1.0 MHz).

When selecting the inductor, choose an inductor saturation rating that is above the peak current level and then calculate the inductor current ripple (see the Valley Current-Limit Setting section and Figure 78).

![Figure 78. Peak Current vs. Valley Current Threshold for 33%, 40%, and 50% of Inductor Ripple Current](image)

Table 7. Recommended Inductors

<table>
<thead>
<tr>
<th>L (( \mu \text{H} ))</th>
<th>DCR (mΩ)</th>
<th>( I_{\text{SAT}} ) (A)</th>
<th>Dimensions (mm)</th>
<th>Manufacturer</th>
<th>Model No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.12</td>
<td>0.33</td>
<td>55</td>
<td>10.2 × 7</td>
<td>Würth Elektronik</td>
<td>744303012</td>
</tr>
<tr>
<td>0.22</td>
<td>0.33</td>
<td>30</td>
<td>10.2 × 7</td>
<td>Würth Elektronik</td>
<td>744303022</td>
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<tr>
<td>0.47</td>
<td>0.8</td>
<td>50</td>
<td>14.2 × 12.8</td>
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<td>744355147</td>
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<tr>
<td>0.72</td>
<td>1.65</td>
<td>35</td>
<td>10.5 × 10.2</td>
<td>Würth Elektronik</td>
<td>744325072</td>
</tr>
<tr>
<td>0.9</td>
<td>1.6</td>
<td>28</td>
<td>13 × 12.8</td>
<td>Würth Elektronik</td>
<td>744355090</td>
</tr>
<tr>
<td>1.2</td>
<td>1.8</td>
<td>25</td>
<td>10.5 × 10.2</td>
<td>Würth Elektronik</td>
<td>744325120</td>
</tr>
<tr>
<td>1.0</td>
<td>3.3</td>
<td>20</td>
<td>10.5 × 10.2</td>
<td>Würth Elektronik</td>
<td>7443552100</td>
</tr>
<tr>
<td>1.4</td>
<td>3.2</td>
<td>24</td>
<td>14 × 12.8</td>
<td>Würth Elektronik</td>
<td>744318180</td>
</tr>
<tr>
<td>2.0</td>
<td>2.6</td>
<td>22</td>
<td>13.2 × 12.8</td>
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<td>7443551200</td>
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<tr>
<td>0.8</td>
<td>27.5</td>
<td></td>
<td></td>
<td>Sumida</td>
<td>CEP125U-0R8</td>
</tr>
</tbody>
</table>

OUTPUT RIPPLE VOLTAGE (\( \Delta V_{\text{RR}} \))

The output ripple voltage is the ac component of the dc output voltage during steady state. For a ripple error of 1.0%, the output capacitor value needed to achieve this tolerance can be determined using the following equation. (Note that an accuracy of 1.0% is only possible during steady state conditions, not during load transients.)

\[
\Delta V_{\text{RR}} = (0.01) \times V_{\text{OUT}}
\]

OUTPUT CAPACITOR SELECTION

The primary objective of the output capacitor is to facilitate the reduction of the output ripple voltage; however, the output capacitor also assists in the output voltage recovery during load transient events. For a given load current step, the output voltage ripple generated during this step event is inversely proportional to the value chosen for the output capacitor. The speed at which the output voltage settles during this recovery period depends on where the crossover frequency (loop bandwidth) is set. This crossover frequency is determined by the output capacitor, the equivalent series resistance (ESR) of the capacitor, and the compensation network.

To calculate the small signal voltage ripple (output ripple voltage) at the steady state operating point, use the following equation:

\[
C_{\text{OUT}} = \frac{\Delta I_L}{8 \times f_{\text{SW}} \times \left[ \Delta V_{\text{RIEPPLE}} - (\Delta I_L \times \text{ESR}) \right]}
\]

where ESR is the equivalent series resistance of the output capacitors.

To calculate the output load step, use the following equation:

\[
C_{\text{OUT}} = 2 \times f_{\text{SW}} \times \frac{\Delta I_{\text{LOAD}}}{(\Delta V_{\text{DROOP}} - (\Delta I_{\text{LOAD}} \times \text{ESR}))}
\]

where \( \Delta V_{\text{DROOP}} \) is the amount that \( V_{\text{OUT}} \) is allowed to deviate for a given positive load current step (\( \Delta I_{\text{LOAD}} \)).
Ceramic capacitors are known to have low ESR. However, the trade-off of using X5R technology is that up to 80% of its capacitance may be lost due to derating because the voltage applied across the capacitor is increased (see Figure 79). Although X7R series capacitors can also be used, the available selection is limited to only up to 22 µF.

![Figure 79. Capacitance vs. DC Voltage Characteristics for Ceramic Capacitors](image)

Electrolytic capacitors satisfy the bulk capacitance requirements for most high current applications. Because the ESR of electrolytic capacitors is much higher than that of ceramic capacitors, when using electrolytic capacitors, several MLCCs should be mounted in parallel to reduce the overall series resistance.

### COMPENSATION NETWORK

Due to its current-mode architecture, the ADP1872/ADP1873 require Type II compensation. To determine the component values needed for compensation (resistance and capacitance values), it is necessary to examine the converter’s overall loop gain (H) at the unity gain frequency (fSW/10) when H = 1 V/V.

\[
H = 1 \frac{V}{V} = G_M \times \frac{V_{OUT}}{V_{REF}} \times Z_{COMP} \times Z_{FILT}
\]

Examining each variable at high frequency enables the unity gain transfer function to be simplified to provide expressions for the RCOMP and CCOMP component values.

### Output Filter Impedance (Z\text{FILT})

Examining the filter’s transfer function at high frequencies simplifies to

\[
Z_{\text{FILTER}} = \frac{1}{sC_{\text{OUT}}}
\]

at the crossover frequency (s = 2πf\text{CROSS}).

### Error Amplifier Output Impedance (Z\text{COMP})

Assuming C\text{C2} is significantly smaller than C\text{COMP}, C\text{C2} can be omitted from the output impedance equation of the error amplifier. The transfer function simplifies to

\[
Z_{\text{COMP}} = \frac{R_{\text{COMP}}(f_{\text{CROSS}} + f_{\text{ZERO}})}{f_{\text{CROSS}}}
\]

and

\[
f_{\text{CROSS}} = \frac{1}{12} f_{\text{SW}}
\]

where f\text{ZERO}, the zero frequency, is set to be 1/4th of the crossover frequency for the ADP1872.

### Error Amplifier Gain (G\text{M})

The error amplifier gain (transconductance) is

\[
G_M = 500 \mu A/V
\]

### Current-Sense Loop Gain (G\text{CS})

The current-sense loop gain is

\[
G_{\text{CS}} = \frac{1}{A_{\text{CS}} \times R_{\text{ON}}} (\text{A/V})
\]

where:

- A\text{CS} (V/V) is programmable for 3 V/V, 6 V/V, 12 V/V, and 24 V/V (see the Programming Resistor (RES) Detect Circuit and Valley Current-Limit Setting sections).
- R\text{ON} is the channel impedance of the lower side MOSFET.

### Crossover Frequency

The crossover frequency is the frequency at which the overall loop (system) gain is 0 dB (H = 1 V/V). It is recommended for current-mode converters, such as the ADP1872, that the user set the crossover frequency between 1/10th and 1/15th of the switching frequency.

\[
f_{\text{CROSS}} = \frac{1}{12} f_{\text{SW}}
\]

The relationship between C\text{COMP} and f\text{ZERO} (zero frequency) is

\[
f_{\text{ZERO}} = \frac{1}{2\pi \times R_{\text{COMP}} \times C_{\text{COMP}}}
\]

The zero frequency is set to 1/4th of the crossover frequency. Combining all of the above parameters results in

\[
R_{\text{COMP}} = \frac{f_{\text{CROSS}} + f_{\text{ZERO}}}{2\pi} \times \frac{2\pi f_{\text{CROSS}} C_{\text{OUT}}}{G_M G_{\text{CS}}} \times \frac{V_{\text{OUT}}}{V_{\text{REF}}}
\]

\[
C_{\text{COMP}} = \frac{1}{2 \pi \times R_{\text{COMP}} \times f_{\text{ZERO}}}
\]
EFFICIENCY CONSIDERATION

One of the important criteria to consider in constructing a dc-to-dc converter is efficiency. By definition, efficiency is the ratio of the output power to the input power. For high power applications at load currents up to 20 A, the following are important MOSFET parameters that aid in the selection process:

- $V_{GS(TH)}$: the MOSFET support voltage applied between the gate and the source.
- $R_{DS(ON)}$: the MOSFET on resistance during channel conduction.
- $Q_g$: the total gate charge
- $C_{NI}$: the input capacitance of the upper side switch
- $C_{N2}$: the input capacitance of the lower side switch

The following are the losses experienced through the external component during normal switching operation:

- Channel conduction loss (both the MOSFETs)
- MOSFET driver loss
- MOSFET switching loss
- Body diode conduction loss (lower side MOSFET)
- Inductor loss (copper and core loss)

**Channel Conduction Loss**

During normal operation, the bulk of the loss in efficiency is due to the power dissipated through MOSFET channel conduction. Power loss through the upper side MOSFET is directly proportional to the duty cycle ($D$) for each switching period, and the power loss through the lower side MOSFET is directly proportional to $1 - D$ for each switching period. The selection of MOSFETs is governed by the amount of maximum dc load current that the converter is expected to deliver. In particular, the selection of the lower side MOSFET is dictated by the maximum load current because a typical high current application employs duty cycles of less than 50%. Therefore, the lower side MOSFET is in the on state for most of the switching period.

$$P_{NL,N2(CL)} = [D \times R_{N2(ON)} + (1 - D) \times R_{N2(ON)}] \times I_{LOAD}^2$$

**MOSFET Driver Loss**

Other dissipative elements are the MOSFET drivers. The contributing factors are the dc current flowing through the driver during operation and the $Q_{GATE}$ parameter of the external MOSFETs.

$$P_{DR(LOSS)} = \left[ V_{DR} \times \left( f_{SW} C_{upperFET} V_{DR} + I_{BLAS} \right) \right] + \left[ V_{DD} \times \left( f_{SW} C_{lowerFET} V_{DD} + I_{BLAS} \right) \right]$$

where:

- $C_{upperFET}$ is the input gate capacitance of the upper-side MOSFET.
- $C_{lowerFET}$ is the input gate capacitance of the lower-side MOSFET.
- $V_{DR}$ is the driver bias voltage (that is, the low input voltage ($V_{DD}$) minus the rectifier drop (see Figure 80)).
- $I_{BLAS}$ is the dc current flowing into the upper- and lower-side drivers.
- $V_{DD}$ is the bias voltage.

**MOSFET Switching Loss**

The SW node transitions due to the switching activities of the upper and lower side MOSFETs. This causes removal and replenishing of charge to and from the gate oxide layer of the MOSFET, as well as to and from the parasitic capacitance associated with the gate oxide edge overlap and the drain and source terminals. The current that enters and exits these charge paths presents additional loss during these transition times. This can be approximately quantified by using the following equation, which represents the time in which charge enters and exits these capacitive regions.

$$I_{SW-TRANS} = R_{GATE} \times C_{TOTAL}$$

where:

- $R_{GATE}$ is the gate input resistance of the MOSFET.
- $C_{TOTAL}$ is the $C_{GS} + C_{GD}$ of the external MOSFET used.

The ratio of this time constant to the period of one switching cycle is the multiplying factor to be used in the following expression:

$$P_{SW(LOSS)} = \frac{I_{SW-TRANS} \times I_{LOAD} \times V_{IN} \times 2}{t_{SW}}$$

or

$$P_{SW(LOSS)} = f_{SW} \times R_{GATE} \times C_{TOTAL} \times I_{LOAD} \times V_{IN} \times 2$$

---

**Figure 80. Internal Rectifier Voltage Drop vs. Switching Frequency**
**Body Diode Conduction Loss**

The ADP1872/ADP1873 employ anticross conduction circuitry that prevents the upper side and lower side MOSFETs from conducting current simultaneously. This overlap control is beneficial, avoiding large current flow that may lead to irreparable damage to the external components of the power stage. However, this blanking period comes with the trade-off of a diode conduction loss occurring immediately after the MOSFETs change states and continuing well into idle mode.

The amount of loss through the body diode of the lower side MOSFET during the antioverlap state is given by

\[ P_{BODY(LOSS)} = \frac{t_{BODY(LOSS)}}{t_{SW}} \times I_{LOAD} \times V_F \times 2 \]

where:
- \( t_{BODY(LOSS)} \) is the body conduction time (refer to Figure 81 for dead time periods).
- \( t_{SW} \) is the period per switching cycle.
- \( V_F \) is the forward drop of the body diode during conduction.

(Refer to the selected external MOSFET data sheet for more information about the \( V_F \) parameter.)

**Inductor Loss**

During normal conduction mode, further power loss is caused by the conduction of current through the inductor windings, which have dc resistance (DCR). Typically, larger sized inductors have smaller DCR values.

The inductor core loss is a result of the eddy currents generated within the core material. These eddy currents are induced by the changing flux, which is produced by the current flowing through the windings. The amount of inductor core loss depends on the core material, the flux swing, the frequency, and the core volume. Ferrite inductors have the lowest core losses, whereas powdered iron inductors have higher core losses. It is recommended to use shielded ferrite core material type inductors with the ADP1872/ADP1873 for a high current, dc-to-dc switching application to achieve minimal loss and negligible electromagnetic interference (EMI).

\[ P_{DCR(LOSS)} = DCR \times I_{LOAD}^2 + Core \ Loss \]

**INPUT CAPACITOR SELECTION**

The goal in selecting an input capacitor is to reduce or to minimize input voltage ripple and to reduce the high frequency source impedance, which is essential for achieving predictable loop stability and transient performance.

The problem with using bulk capacitors, other than their physical geometries, is their large equivalent series resistance (ESR) and large equivalent series inductance (ESL). Aluminum electrolytic capacitors have such high ESR that they cause undesired input voltage ripple magnitudes and are generally not effective at high switching frequencies.

If bulk capacitors are to be used, it is recommended to use multi-layered ceramic capacitors (MLCC) in parallel due to their low ESR values. This dramatically reduces the input voltage ripple amplitude as long as the MLCCs are mounted directly across the drain of the upper side MOSFET and the source terminal of the lower side MOSFET (see the Layout Considerations section). Improper placement and mounting of these MLCCs may cancel their effectiveness due to stray inductance and an increase in trace impedance.

\[ I_{CIN,RMS} = I_{LOAD,MAX} \times \frac{\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}}{V_{OUT}} \]

The maximum input voltage ripple and maximum input capacitor rms current occur at the end of the duration of \( 1 - D \) while the upper side MOSFET is in the off state. The input capacitor rms current reaches its maximum at time \( D \). When calculating the maximum input voltage ripple, account for the ESR of the input capacitor as follows:

\[ V_{MAX, RIPPLE} = V_{RIPP} + (I_{LOAD, MAX} \times ESR) \]

where:
- \( V_{RIPP} \) is usually 1% of the minimum voltage input.
- \( I_{LOAD, MAX} \) is the maximum load current.

ESR is the equivalent series resistance rating of the input capacitor used.

Inserting \( V_{MAX, RIPPLE} \) into the charge balance equation to calculate the minimum input capacitor requirement gives

\[ C_{IN, min} = \frac{I_{LOAD,MAX}}{V_{MAX, RIPPLE}} \times \frac{D(1-D)}{f_{SW}} \]

or

\[ C_{IN, min} = \frac{I_{LOAD,MAX}}{4f_{SW}V_{MAX, RIPPLE}} \]

where \( D = 50\% \).
THERMAL CONSIDERATIONS

The ADP1872/ADP1873 are used for dc-to-dc, step down, high current applications that have an on-board controller and on-board MOSFET drivers. Because applications may require up to 20 A of load current delivery and be subjected to high ambient temperature surroundings, the selection of external upper side and lower side MOSFETs must be associated with careful thermal consideration to not exceed the maximum allowable junction temperature of 125°C. To avoid permanent or irreparable damage if the junction temperature reaches or exceeds 155°C, the part enters thermal shutdown, turning off both external MOSFETs, and does not re-enable until the junction temperature cools to 140°C (see the Thermal Shutdown section).

The maximum junction temperature allowed for the ADP1872/ADP1873 ICs is 125°C. This means that the sum of the ambient temperature ($T_A$) and the rise in package temperature ($T_R$), which is caused by the thermal impedance of the package and the internal power dissipation, should not exceed 125°C, as dictated by

$$T_J = T_R + T_A$$

where:
- $T_J$ is the maximum junction temperature.
- $T_R$ is the rise in package temperature due to the power dissipated from within.
- $T_A$ is the ambient temperature.

The rise in package temperature is directly proportional to its thermal impedance characteristics. The following equation represents this proportionality relationship:

$$T_R = \theta_{JA} \times P_{D\text{R (LOSS)}}$$

where:
- $\theta_{JA}$ is the thermal resistance of the package from the junction to the outside surface of the die, where it meets the surrounding air.
- $P_{D\text{R (LOSS)}}$ is the overall power dissipated by the IC.

The bulk of the power dissipated is due to the gate capacitance of the external MOSFETs. The power loss equation of the MOSFET drivers (see the MOSFET Driver Loss section in the Efficiency Consideration section) is

$$P_{D\text{R (LOSS)}} = [V_{DR} \times (f_{SW}C_{\text{upperFET}}V_{DR} + I_{BIAS})] + [V_{DD} \times (f_{SW}C_{\text{lowerFET}}V_{DD} + I_{BIAS})]$$

where:
- $C_{\text{upperFET}}$ is the input gate capacitance of the upper side MOSFET.
- $C_{\text{lowerFET}}$ is the input gate capacitance of the lower side MOSFET.
- $I_{BIAS}$ is the dc current (2 mA) flowing into the upper side and lower side drivers.
- $V_{DR}$ is the driver bias voltage (that is, the low input voltage ($V_{DD}$) minus the rectifier drop (see Figure 80)).
- $V_{DD}$ is the bias voltage.

For example, if the external MOSFET characteristics are $\theta_{JA}$ (10-lead MSOP) = 171.2°C/W, $f_{SW}$ = 300 kHz, $I_{BIAS} = 2$ mA, $C_{\text{upperFET}} = 3.3$ nF, $C_{\text{lowerFET}} = 3.3$ nF, $V_{DR} = 5.12$ V, and $V_{DD} = 5.5$ V, then the power loss is

$$P_{D\text{R (LOSS)}} = [5.12 \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 5.12 + 0.002)] + [5.5 \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 5.5 + 0.002)]$$

$$= 77.13 \text{ mW}$$

The rise in package temperature is

$$T_R = \theta_{JA} \times P_{D\text{R (LOSS)}}$$

$$= 171.2^\circ \text{C} \times 77.13 \text{ mW}$$

$$= 13.2^\circ \text{C}$$

Assuming a maximum ambient temperature environment of 85°C, the junction temperature is

$$T_J = T_R + T_A$$

$$= 13.2^\circ \text{C} + 85^\circ \text{C} = 98.2^\circ \text{C}$$

which is below the maximum junction temperature of 125°C.

DESIGN EXAMPLE

The ADP1872/ADP1873 are easy to use, requiring only a few design criteria. For example, the example outlined in this section uses only four design criteria: $V_{OUT} = 1.8$ V, $I_{LOAD} = 15$ A (pulsing), $V_{IN} = 12$ V (typical), and $f_{SW} = 300$ kHz.

**Input Capacitor**

The maximum input voltage ripple is usually 1% of the minimum input voltage (11.8 V × 0.01 = 120 mV).

$$V_{RIPPLE} = 120 \text{ mV}$$

$$V_{MAX, RIPPLE} = V_{RIPPLE} - (I_{LOAD, MAX} \times ESR)$$

$$= 120 \text{ mV} - (15 \text{ A} \times 0.001) = 45 \text{ mV}$$

$$C_{IN, min} = \frac{I_{LOAD, MAX}}{4f_{SW}V_{MAX, RIPPLE}} = \frac{15 \text{ A}}{4 \times 300 \times 10^3 \times 105 \text{ mV}}$$

$$= 120 \mu \text{F}$$

Choose five 22 µF ceramic capacitors. The overall ESR of five 22 µF ceramic capacitors is less than 1 mΩ.

$$I_{ESR} = I_{LOAD}/2 = 7.5 \text{ A}$$

$$P_{CDN} = (I_{ESR})^2 \times ESR = (7.5 \text{ A})^2 \times 1 \text{ mΩ} = 56.25 \text{ mW}$$

**Inductor**

Determining inductor ripple current amplitude:

$$\Delta I_L = \frac{I_{LOAD}}{3} = 5 \text{ A}$$

so calculating for the inductor value

$$L = \frac{(V_{IN, MAX} - V_{OUT})}{\Delta I_L \times f_{SW}} \times \frac{V_{OUT}}{V_{IN, MAX}}$$

$$= \frac{(13.2 \text{ V} - 1.8 \text{ V})}{5 \times 300 \times 10^3} \times \frac{1.8 \text{ V}}{13.2 \text{ V}}$$

$$= 1.03 \mu \text{H}$$
The inductor peak current is approximately

\[
15 \text{ A} + (5 \text{ A} \times 0.5) = 17.5 \text{ A}
\]

Therefore, an appropriate inductor selection is 1.0 µH with DCR = 3.3 mΩ (7443552100) from Table 7 with peak current handling of 20 A.

\[
P_{\text{DCR(LOSS)}} = \text{DCR} \times I^2_{\text{LOAD}}
\]

\[
= 0.003 \times (15 \text{ A})^2 = 675 \text{ mW}
\]

**Current Limit Programming**

The valley current is approximately

\[
15 \text{ A} - (5 \text{ A} \times 0.5) = 12.5 \text{ A}
\]

Assuming a lower side MOSFET R\text{ON} of 4.5 mΩ, choosing 13 A as the valley current limit from Table 6 and Figure 70 indicates that a programming resistor (RES) of 100 kΩ corresponds to an A\text{CS} of 24 V/V.

Choose a programmable resistor of R\text{RES} = 100 kΩ for a current-sense gain of 24 V/V.

**Output Capacitor**

Assume a load step of 15 A occurs at the output and no more than 5% is allowed for the output to deviate from the steady state operating point. The ADP1872's advantage is, because the frequency is pseudo-fixed, the converter is able to respond quickly because of the immediate, though temporary, increase in switching frequency.

\[
\Delta V_{\text{DROOP}} = 0.05 \times 1.8 \text{ V} = 90 \text{ mV}
\]

Assuming the overall ESR of the output capacitor ranges from 5 mΩ to 10 mΩ,

\[
C_{\text{OUT}} = 2 \times \frac{\Delta I_{\text{LOAD}}}{f_{\text{SW}} \times (\Delta V_{\text{DROOP}})}
\]

\[
= 2 \times \frac{15 \text{ A}}{300 \times 10^3 \times (90 \text{ mV})} = 1.11 \text{ mF}
\]

Therefore, an appropriate inductor selection is five 270 µF polymer capacitors with a combined ESR of 3.5 mΩ.

Assuming an overshoot of 45 mV, determine if the output capacitor that was calculated previously is adequate:

\[
C_{\text{OUT}} = \frac{(L \times I^2_{\text{LOAD}})}{(V_{\text{OUT}} - \Delta V_{\text{OVSHT}})^2 - V_{\text{OUT}})}
\]

\[
= \frac{1 \times 10^{-6} \times (15 \text{ A})^2}{(1.8 - 45 \text{ mV})^2 - (1.8)^2}
\]

\[
= 1.4 \text{ mF}
\]

Choose five 270 µF polymer capacitors.

The rms current through the output capacitor is

\[
I_{\text{RMS}} = \frac{1}{\sqrt{2} \times \sqrt{L \times f_{\text{SW}} \times V_{\text{OUT}} \times V_{\text{IN,MAX}}}}
\]

\[
= \frac{1}{\sqrt{2} \times \sqrt{1 \text{ µF} \times 300 \times 10^3 \times 1.8 \text{ V} \times 13.2 \text{ V}}} = 1.49 \text{ A}
\]

The power loss dissipated through the ESR of the output capacitor is

\[
P_{\text{OUT}} = (I_{\text{RMS}})^2 \times \text{ESR} = (1.5 \text{ A})^2 \times 1.4 \text{ mΩ} = 3.15 \text{ mW}
\]

**Feedback Resistor Network Setup**

It is recommended to use R\text{B} = 15 kΩ. Calculate R\text{T} as

\[
R_T = 15 \text{ kΩ} \times \frac{(1.8 \text{ V} - 0.6 \text{ V})}{0.6 \text{ V}} = 30 \text{ kΩ}
\]

**Compensation Network**

To calculate R\text{COMP}, C\text{COMP}, and C\text{PAR}, the transconductance parameter and the current-sense gain variable are required. The transconductance parameter (G\text{M}) is 500 µA/V, and the current-sense loop gain is

\[
G_{\text{CS}} = \frac{1}{\lambda_{\text{CS}}R_{\text{ON}}} = \frac{1}{24 \times 0.005} = 8.33 \text{ A/V}
\]

where A\text{CS} and R\text{ON} are taken from setting up the current limit (see the Programming Resistor (RES) Detect Circuit and Valley Current-Limit Setting sections).

The crossover frequency is 1/12 of the switching frequency:

\[
300 \text{ kHz}/12 = 25 \text{ kHz}
\]

The zero frequency is 1/4 of the crossover frequency:

\[
25 \text{ kHz}/4 = 6.25 \text{ kHz}
\]

\[
R_{\text{COMP}} = \frac{f_{\text{CROSS}}}{f_{\text{CROSS}} + f_{\text{ZERO}}} \times \frac{2\pi f_{\text{CROSS}}C_{\text{OUT}}}{G_{\text{M}}G_{\text{CS}}} \times \frac{V_{\text{OUT}}}{V_{\text{REF}}}
\]

\[
= \frac{25 \times 10^3}{25 \times 10^3 + 6.25 \times 10^3} \times \frac{2 \times 3.141 \times 25 \times 10^3 \times 1.11 \times 10^{-3} \times 1.8}{500 \times 10^{-6} \times 8.3} = 100 \text{ kΩ}
\]

\[
C_{\text{COMP}} = \frac{1}{2\pi R_{\text{COMP}} f_{\text{ZERO}}}
\]

\[
= \frac{1}{2 \times 3.14 \times 100 \times 10^3 \times 6.25 \times 10^3} = 250 \text{ pF}
\]
**Loss Calculations**

- Duty cycle = 1.8/12 V = 0.15
- $R_{ON(N2)} = 5.4 \text{ m}\Omega$
- $t_{BODY(LOSS)} = 20 \text{ ns}$ (body conduction time)
- $V_F = 0.84 \text{ V}$ (MOSFET forward voltage)
- $C_{IN} = 3.3 \text{ nF}$ (MOSFET gate input capacitance)
- $Q_{N1,N2} = 17 \text{ nC}$ (total MOSFET gate charge)
- $R_{GATE} = 1.5 \Omega$ (MOSFET gate input resistance)

\[
P_{NL,N2(CL)} = \left[ D \times R_{N1(ON)} + (1 - D) \times R_{N2(ON)} \right] \times I_{LOAD}^2
\]
\[
= (0.15 \times 0.0054 + 0.85 \times 0.0054) \times (15 \text{ A})^2
\]
\[
= 1.215 \text{ W}
\]

\[
P_{BODY(LOSS)} = \frac{t_{BODY(LOSS)}}{t_{SW}} \times I_{LOAD} \times V_F \times 2
\]
\[
= 20 \text{ ns} \times 300 \times 10^3 \times 15 \text{ A} \times 0.84 \times 2
\]
\[
= 151.2 \text{ mW}
\]

\[
P_{SW(LOSS)} = f_{SW} \times R_{GATE} \times C_{TOTAL} \times I_{LOAD} \times V_{IN} \times 2
\]
\[
= 300 \times 10^3 \times 1.5 \Omega \times 3.3 \times 10^{-9} \times 15 \text{ A} \times 12 \times 2
\]
\[
= 534.6 \text{ mW}
\]

\[
P_{DR(LOSS)} = \left[ V_{DD} \times f_{SW} C_{upperFET} (V_{DD} + I_{BIAS}) \right] + \left[ V_{DD} \times f_{SW} C_{lowerFET} (V_{DD} + I_{BIAS}) \right]
\]
\[
= (5.12 \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 5.12 + 0.002)) + (5.5 \times (300 \times 10^3 \times 3.3 \times 10^{-9} \times 5.5 + 0.002))
\]
\[
= 77.13 \text{ mW}
\]

\[
P_{OUT} = (I_{RMS})^2 \times ESL = (1.5 \text{ A})^2 \times 1.4 \text{ m}\Omega = 3.15 \text{ mW}
\]

\[
P_{DCR(LOSS)} = DCR \times I_{LOAD}^2 = 0.003 \times (15 \text{ A})^2 = 675 \text{ mW}
\]

\[
P_{CIN} = (I_{RMS})^2 \times ESL = (7.5 \text{ A})^2 \times 1 \text{ m}\Omega = 56.25 \text{ mW}
\]

\[
P_{LOSS} = P_{N1,N2} + P_{BODY(LOSS)} + P_{SW} + P_{DCR} + P_{DR} + P_{OUT} + P_{CIN}
\]
\[
= 1.215 \text{ W} + 151.2 \text{ mW} + 534.6 \text{ mW} + 77.13 \text{ mW} + 3.15 \text{ mW} + 675 \text{ mW} + 56.25 \text{ mW}
\]
\[
= 2.62 \text{ W}
\]
EXTERNAL COMPONENT RECOMMENDATIONS

The configurations listed in Table 8 are with $f_{\text{CROSS}} = 1/12 \times f_{\text{SW}}$, $f_{\text{ZERO}} = 1/4 \times f_{\text{CROSS}}$, $R_{\text{RES}} = 100 \ \text{k}\Omega$, $R_{\text{BOT}} = 15 \ \text{k}\Omega$, $R_{\text{ON}} = 5.4 \ \text{m}\Omega$ (BSC042N03MS G), $V_{\text{DD}} = 5 \ \text{V}$, and a maximum load current of 14 \text{A}.

The ADP1873 models listed in Table 8 are the PSM versions of the device.

Table 8. External Component Values

<table>
<thead>
<tr>
<th>SAP Model</th>
<th>Marking Code</th>
<th>$V_{\text{OUT}}$ (V)</th>
<th>$V_{\text{IN}}$ (V)</th>
<th>$C_{\text{IN}}$ ($\mu\text{F}$)</th>
<th>$C_{\text{OUT}}$ ($\mu\text{F}$)</th>
<th>$L$ ($\mu\text{H}$)</th>
<th>$R_{\text{C}}$ (k$\Omega$)</th>
<th>$C_{\text{COMP}}$ (pF)</th>
<th>$C_{\text{PAR}}$ (pF)</th>
<th>$R_{\text{TOP}}$ (k$\Omega$)</th>
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<tbody>
<tr>
<td>ADP1872ARMZ-0.3-R7/</td>
<td>LDT</td>
<td>0.8</td>
<td>13</td>
<td>$5 \times 22^2$</td>
<td>$5 \times 560^3$</td>
<td>0.72</td>
<td>47</td>
<td>740</td>
<td>74</td>
<td>5.0</td>
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<td>$5 \times 22^2$</td>
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<td>47</td>
<td>339</td>
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<td>3.0</td>
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<td></td>
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<td></td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

Note: The component values are listed for specific Marking Codes, which vary with the model. The table includes a range of component values to accommodate different power requirements and application needs.
### Table 9. Recommended Inductors

<table>
<thead>
<tr>
<th>L (µH)</th>
<th>DCR (mΩ)</th>
<th>ISAT (A)</th>
<th>Dimension (mm)</th>
<th>Manufacturer</th>
<th>Model Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.12</td>
<td>0.33</td>
<td>55</td>
<td>10.2 × 7</td>
<td>Würth Elektronik</td>
<td>744303012</td>
</tr>
<tr>
<td>0.22</td>
<td>0.33</td>
<td>30</td>
<td>10.2 × 7</td>
<td>Würth Elektronik</td>
<td>744303022</td>
</tr>
<tr>
<td>0.47</td>
<td>0.8</td>
<td>50</td>
<td>14.2 × 12.8</td>
<td>Würth Elektronik</td>
<td>744355147</td>
</tr>
<tr>
<td>0.72</td>
<td>1.65</td>
<td>35</td>
<td>10.5 × 10.2</td>
<td>Würth Elektronik</td>
<td>744355090</td>
</tr>
<tr>
<td>0.9</td>
<td>1.6</td>
<td>50</td>
<td>13 × 12.8</td>
<td>Würth Elektronik</td>
<td>744355090</td>
</tr>
<tr>
<td>1.2</td>
<td>1.8</td>
<td>25</td>
<td>10.5 × 10.2</td>
<td>Würth Elektronik</td>
<td>744355120</td>
</tr>
<tr>
<td>1.0</td>
<td>3.3</td>
<td>20</td>
<td>10.5 × 10.2</td>
<td>Würth Elektronik</td>
<td>744355120</td>
</tr>
<tr>
<td>1.4</td>
<td>3.2</td>
<td>24</td>
<td>14 × 12.8</td>
<td>Würth Elektronik</td>
<td>744318180</td>
</tr>
<tr>
<td>2.0</td>
<td>2.6</td>
<td>22</td>
<td>13.2 × 12.8</td>
<td>Sumida</td>
<td>CEP125U-0R8</td>
</tr>
<tr>
<td>0.8</td>
<td>27.5</td>
<td></td>
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### Table 10. Recommended MOSFETs

<table>
<thead>
<tr>
<th>VGS = 4.5 V</th>
<th>RON (mΩ)</th>
<th>ID (A)</th>
<th>VDS (V)</th>
<th>CIN (nF)</th>
<th>QTOTAL (nC)</th>
<th>Package</th>
<th>Manufacturer</th>
<th>Model Number</th>
</tr>
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<tbody>
<tr>
<td>Upper-Side MOSFET (Q1/Q2)</td>
<td>5.4</td>
<td>47</td>
<td>30</td>
<td>3.2</td>
<td>20</td>
<td>PG-TDSON8</td>
<td>Infineon</td>
<td>BSC042N03MS G</td>
</tr>
<tr>
<td></td>
<td>10.2</td>
<td>53</td>
<td>30</td>
<td>1.6</td>
<td>10</td>
<td>SO-8</td>
<td>Infineon</td>
<td>BSC080N03MS G</td>
</tr>
<tr>
<td></td>
<td>6.0</td>
<td>19</td>
<td>30</td>
<td>2.4</td>
<td>25</td>
<td>SO-8</td>
<td>Infineon</td>
<td>Si4842DY</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>14</td>
<td>30</td>
<td>2.4</td>
<td>25</td>
<td>SO-8</td>
<td>International Rectifier</td>
<td>IRF7811</td>
</tr>
<tr>
<td>Lower-Side MOSFET (Q3/Q4)</td>
<td>5.4</td>
<td>47</td>
<td>30</td>
<td>3.2</td>
<td>20</td>
<td>PG-TDSON8</td>
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<td>BSC042N03MS G</td>
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<tr>
<td></td>
<td>10.2</td>
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<td>30</td>
<td>2.4</td>
<td>25</td>
<td>SO-8</td>
<td>Infineon</td>
<td>Si4842DY</td>
</tr>
</tbody>
</table>
LAYOUT CONSIDERATIONS

The performance of a dc-to-dc converter depends highly on how the voltage and current paths are configured on the printed circuit board (PCB). Optimizing the placement of sensitive analog and power components are essential to minimize output ripple, maintain tight regulation specifications, and reduce PWM jitter and electromagnetic interference.

Figure 82 shows the schematic of a typical ADP1872/ADP1873 used for a high power application. Blue traces denote high current pathways. VIN, PGND, and VOUT traces should be wide and possibly replicated, descending down into the multiple layers. Vias should populate, mainly around the positive and negative terminals of the input and output capacitors, alongside the source of Q1/Q2, the drain of Q3/Q4, and the inductor.
OUTPUT CAPACITORS ARE MOUNTED ON THE RIGHTMOST AREA OF THE EVB, WRAPPING BACK AROUND TO THE MAIN POWER GROUND PLANE, WHERE IT MEETS WITH THE NEGATIVE TERMINALS OF THE INPUT CAPACITORS.

INPUT CAPACITORS ARE MOUNTED CLOSE TO DRAIN OF Q1/Q2 AND SOURCE OF Q3/Q4.

BYPASS POWER CAPACITOR (C1) FOR VREG BIAS DECOUPLING AND HIGH FREQUENCY CAPACITOR (C2) AS CLOSE AS POSSIBLE TO THE IC.

SENSITIVE ANALOG COMPONENTS LOCATED FAR FROM THE NOISY POWER SECTION.

SEPARATE ANALOG GROUND PLANE FOR THE ANALOG COMPONENTS (THAT IS, COMPENSATION AND FEEDBACK RESISTORS).

 INPUT CAPACITORS ARE MOUNTED CLOSE TO DRAIN OF Q1/Q2 AND SOURCE OF Q3/Q4.

BYPASS POWER CAPACITOR (C1) FOR VREG BIAS DECOUPLING AND HIGH FREQUENCY CAPACITOR (C2) AS CLOSE AS POSSIBLE TO THE IC.

Figure 83. Overall Layout of the ADP1872 High Current Evaluation Board
VOUT SENSE TAP LINE EXTENDING BACK TO THE TOP RESISTOR IN THE FEEDBACK DIVIDER NETWORK (SEE FIGURE 82). THIS OVERLAPS WITH PGND SENSE TAP LINE EXTENDING BACK TO THE ANALOG PLANE (SEE FIGURE 86, LAYER 4 FOR PGND TAP).

Figure 85. Layer 3 of Evaluation Board
BOTTOM RESISTOR TAP TO THE ANALOG GROUND PLANE

PGND SENSE TAP FROM NEGATIVE TERMINALS OF OUTPUT BULK CAPACITORS. THIS TRACK PLACEMENT SHOULD BE DIRECTLY BELOW THE VOUT SENSE LINE FROM FIGURE 84.

Figure 86. Layer 4 (Bottom Layer) of Evaluation Board
IC SECTION (LEFT SIDE OF EVALUATION BOARD)

A dedicated plane for the analog ground plane (GND) should be separate from the main power ground plane (PGND). With the shortest path possible, connect the analog ground plane to the GND pin (Pin 4). This plane should only be on the top layer of the evaluation board. To avoid crosstalk interference, there should not be any other voltage or current pathway directly below this plane on Layer 2, Layer 3, or Layer 4. Connect the negative terminals of all sensitive analog components to the analog ground plane. Examples of such sensitive analog components include the resistor divider’s bottom resistor, the high frequency bypass capacitor for biasing (0.1 µF), and the compensation network.

Mount a 1 µF bypass capacitor directly across the VDD pin (Pin 5) and the PGND pin (Pin 7). In addition, a 0.1 µF should be tied across the VDD pin (Pin 5) and the GND pin (Pin 4).

POWER SECTION

As shown in Figure 83, an appropriate configuration to localize large current transfer from the high voltage input (VIN) to the output (VOUT) and then back to the power ground is to put the VIN plane on the left, the output plane on the right, and the main power ground plane in between the two. Current transfers from the input capacitors to the output capacitors, through Q1/Q2, during the on state (see Figure 87). The direction of this current (yellow arrow) is maintained as Q1/Q2 turns off and Q3/Q4 turns on. When Q3/Q4 turns on, the current direction continues to be maintained (red arrow) as it circles from the bulk capacitor’s power ground terminal to the output capacitors, through the Q3/Q4. Arranging the power planes in this manner minimizes the area in which changes in flux occur if the current through Q1/Q2 stops abruptly. Sudden changes in flux, usually at source terminals of Q1/Q2 and drain terminals of Q3/Q4, cause large dV/dts at the SW node.

The SW node is near the top of the evaluation board. The SW node should use the least amount of area possible and be away from any sensitive analog circuitry and components because this is where most sudden changes in flux density occur. When possible, replicate this pad onto Layer 2 and Layer 3 for thermal relief and eliminate any other voltage and current pathways directly beneath the SW node plane. Populate the SW node plane with vias, mainly around the exposed pad of the inductor terminal and around the perimeter of the source of Q1/Q2 and the drain of Q3/Q4. The output voltage power plane (VOUT) is at the rightmost end of the evaluation board. This plane should be replicated, descending down to multiple layers with vias surrounding the inductor terminal and the positive terminals of the output bulk capacitors. Ensure that the negative terminals of the output capacitors are placed close to the main power ground (PGND), as previously mentioned. All of these points form a tight circle (component geometry permitting) that minimizes the area of flux change as the event switches between D and 1 − D.

DIFFERENTIAL SENSING

Because the ADP1872/ADP1873 operate in valley current-mode control, a differential voltage reading is taken across the drain and source of the lower-side MOSFET. The drain of the lower-side MOSFET should be connected as close as possible to the SW pin (Pin 9) of the IC. Likewise, the source should be connected as close as possible to the PGND pin (Pin 7) of the IC. When possible, both of these track lines should be narrow and away from any other active device or voltage/current paths.

Differential sensing should also be applied between the outermost output capacitor to the feedback resistor divider (see Figure 85 and Figure 86). Connect the positive terminal of the output capacitor to the top resistor (R7). Connect the negative terminal of the output capacitor to the negative terminal of the bottom resistor, which connects to the analog ground plane as well. Both of these track lines, as previously mentioned, should be narrow and away from any other active device or voltage/current paths.
TYPICAL APPLICATION CIRCUITS

DUAL-INPUT, 300 kHz HIGH CURRENT APPLICATION CIRCUIT

![Diagram of Dual-Input, 300 kHz High Current Application Circuit](image)

Figure 89. Application Circuit for 12 V Input, 1.8 V Output, 15 A, 300 kHz (Q2/Q4 No Connect).

SINGLE-INPUT, 600 kHz APPLICATION CIRCUIT

![Diagram of Single-Input, 600 kHz Application Circuit](image)

Figure 90. Application Circuit for 5.5 V Input, 2.5 V Output, 15 A, 600 kHz (Q2/Q4 No Connect)
DUAL-INPUT, 300 kHz HIGH CURRENT APPLICATION CIRCUIT

Figure 91. Application Circuit for 13 V Input, 1.8 V Output, 20 A, 300 kHz (Q2/Q4 No Connect)
### OUTLINE DIMENSIONS

![Outline Dimensions Diagram]

**Figure 92. 10-Lead Mini Small Outline Package (MSOP) (RM-10)**

*Dimensions shown in millimeters*

### ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
<th>Branding</th>
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<td>RM-10</td>
<td>LDT</td>
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<tr>
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<td>10-Lead Mini Small Outline Package [MSOP]</td>
<td>RM-10</td>
<td>LDU</td>
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<td>LDV</td>
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<td>Forced PWM, 600 kHz Evaluation Board</td>
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<td>Forced PWM, 1 MHz Evaluation Board</td>
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<td>LDL</td>
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<td>Power Saving Mode, 600 kHz Evaluation Board</td>
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1. Z = RoHS Compliant Part.

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