APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP1754/ADP1755 are designed for operation with small, space-saving ceramic capacitors, but they can function with most commonly used capacitors as long as care is taken with the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 3.3 µF capacitance with an ESR of 500 mΩ or less is recommended to ensure the stability of the ADP1754/ADP1755. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP1754/ADP1755 to large changes in load current. Figure 33 and Figure 34 show the transient responses for output capacitance values of 4.7 µF and 22 µF, respectively.

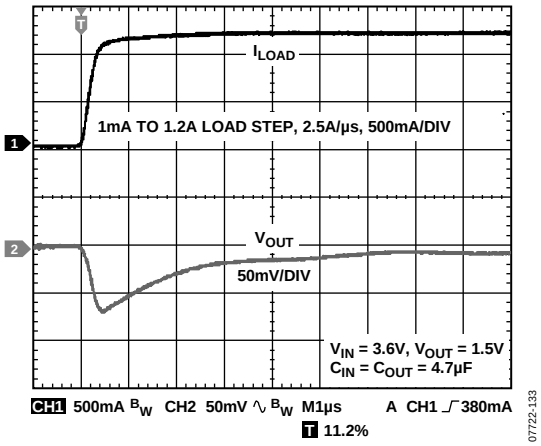

Figure 33. Output Transient Response, C_{OUT} = 4.7 µF

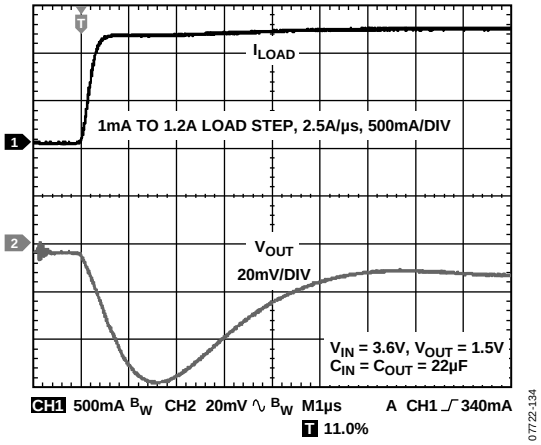

Figure 34. Output Transient Response, C_{OUT} = 22 µF

Input Bypass Capacitor

Connecting a 4.7 µF capacitor from the VIN pin to GND reduces the circuit sensitivity to printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If output capacitance greater than 4.7 µF is required, it is recommended that the input capacitor be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP1754, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended. Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 35 shows the capacitance vs. voltage bias characteristics of an 0805 case, 4.7 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is about ±15% over the −40°C to +85°C temperature range and is not a function of package size or voltage rating.

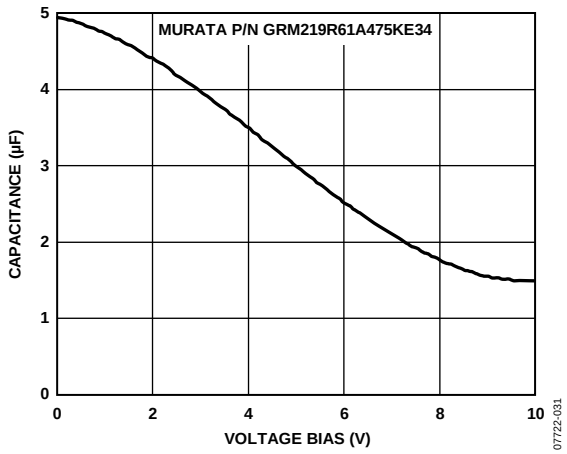

Figure 35. Capacitance vs. Voltage Bias Characteristics

Equation 3 can be used to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{OUT} \times (1 - TEMPCO) \times (1 - TOL) \quad (3)$$

where:

C_{EFF} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{OUT} = 4.46 µF at 1.8 V, as shown in Figure 35.

Substituting these values in Equation 3 yields

$$C_{EFF} = 4.46\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 3.41\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP1754/ADP1755, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

UNDERVOLTAGE LOCKOUT

The ADP1754/ADP1755 have an internal undervoltage lockout circuit that disables all inputs and the output when the input voltage is less than approximately 1.58 V. This ensures that the ADP1754/ADP1755 inputs and the output behave in a predictable manner during power-up.

CURRENT-LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP1754/ADP1755 are protected against damage due to excessive power dissipation by current-limit and thermal overload protection circuits. The ADP1754/ADP1755 are designed to reach current limit when the output load reaches 2 A (typical). When the output load exceeds 2 A, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 150°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature begins to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C (typical), the output is turned on again and the output current is restored to its nominal value.

Consider the case where a hard short from VOUT to ground occurs. At first, the ADP1754/ADP1755 reach current limit so that only 2 A is conducted into the short. If self-heating of the junction becomes great enough to cause its temperature to rise above 150°C, thermal shutdown activates, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 2 A into the short, again causing the junction temperature to rise above 150°C. This thermal oscillation between 135°C and 150°C causes a current oscillation between 2A and 0 A that continues as long as the short remains at the output.

Current-limit and thermal overload protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation should be externally limited so that junction temperatures do not exceed 125°C.

THERMAL CONSIDERATIONS

To guarantee reliable operation, the junction temperature of the ADP1754/ADP1755 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user needs to be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistance between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds used and the amount of copper to which the GND pin and the exposed pad (EPAD) of the package are soldered on the PCB. Table 6 shows typical θ_{JA} values for the 16-lead LFCSP for various PCB copper sizes. Table 7 shows typical Ψ_{JB} values for the 16-lead LFCSP.

Table 6. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W), LFCSP
0[1]	130
100	80
500	69
1000	54
6400	42

[1] Device soldered to minimum size pin traces.

Table 7. Typical Ψ_{JB} Values

Copper Size (mm²)	Ψ_{JB} (°C/W) at 1 W
100	32.7
500	31.5
1000	25.5

The junction temperature of the ADP1754/ADP1755 can be calculated from the following equation:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (4)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND}) \quad (5)$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation can be simplified as follows:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\} \quad (6)$$

As shown in Equation 6, for a given ambient temperature, input-to-output voltage differential, and continuous load current, a minimum copper size requirement exists for the PCB to ensure that the junction temperature does not rise above 125°C.

Figure 36 through Figure 41 show junction temperature calculations for different ambient temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

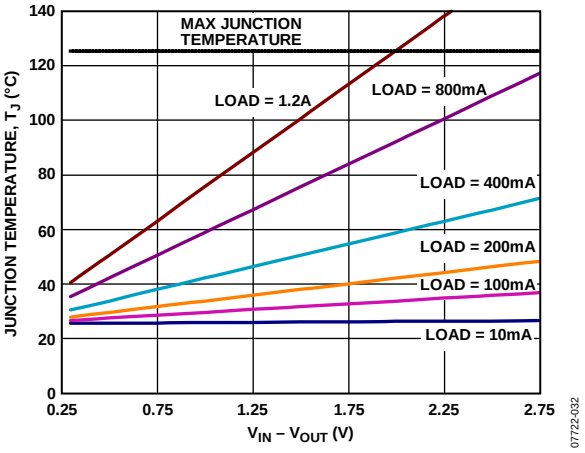

Figure 36. 6400 mm² of PCB Copper, T_A = 25°C, LFCSP

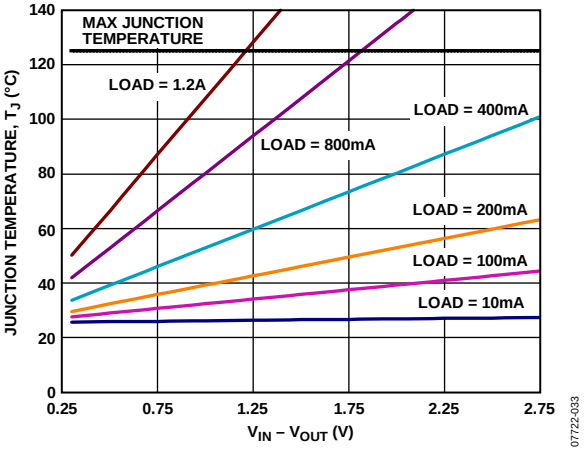

Figure 37. 500 mm² of PCB Copper, T_A = 25°C, LFCSP

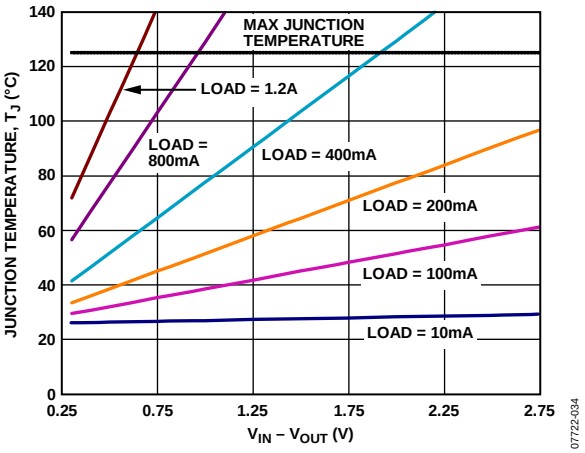

Figure 38. 0 mm² of PCB Copper, T_A = 25°C, LFCSP

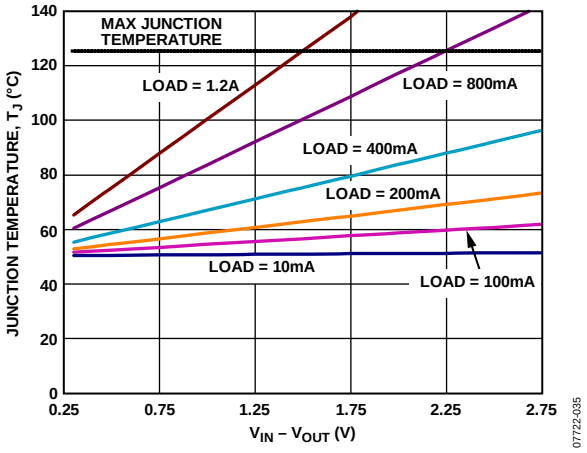

Figure 39. 6400 mm² of PCB Copper, T_A = 50°C, LFCSP

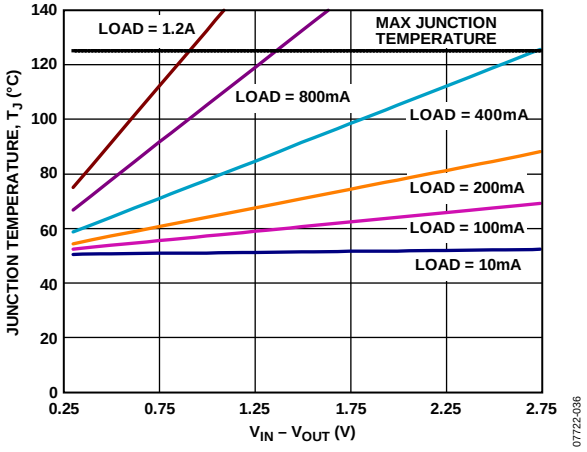

Figure 40. 500 mm² of PCB Copper, T_A = 50°C, LFCSP

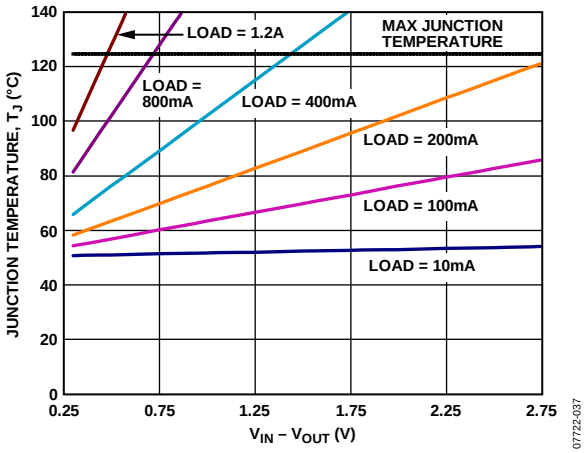

Figure 41. 0 mm² of PCB Copper, T_A = 50°C, LFCSP

In cases where the board temperature is known, the thermal characterization parameter, Ψ_{JB}, can be used to estimate the junction temperature rise. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (7)$$

Figure 42 through Figure 45 show junction temperature calculations for different board temperatures, load currents, V_{IN} to V_{OUT} differentials, and areas of PCB copper.

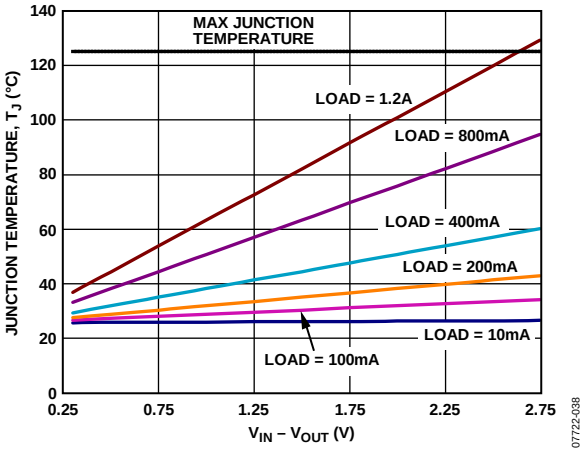

Figure 42. 500 mm² of PCB Copper, T_B = 25°C, LFCSP

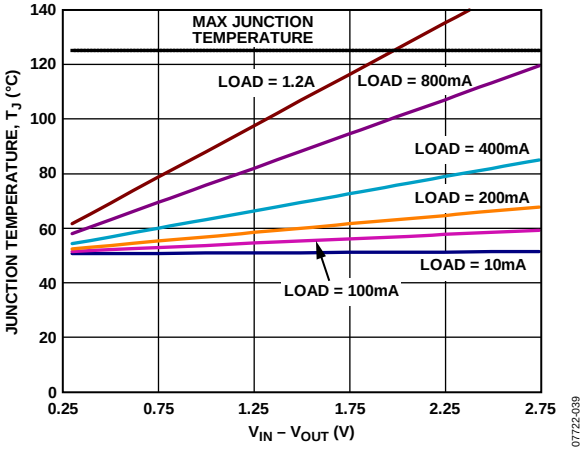

Figure 43. 500 mm² of PCB Copper, T_B = 50°C, LFCSP

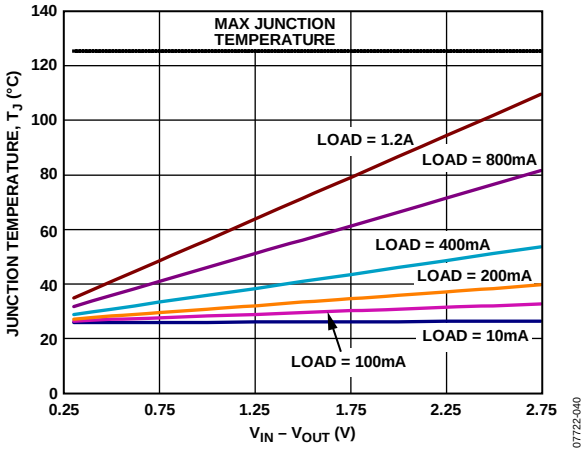

Figure 44. 1000 mm² of PCB Copper, T_B = 25°C, LFCSP

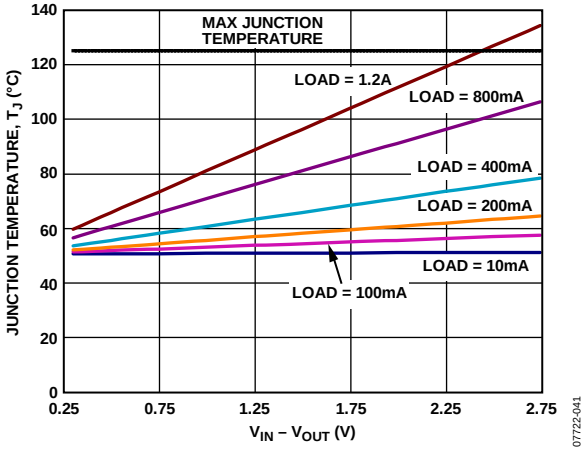

Figure 45. 1000 mm² of PCB Copper, T_B = 50°C, LFCSP

PCB LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP1754/ADP1755. However, as shown in Table 6, a point of diminishing returns is eventually reached, beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Here are a few general tips when designing PCBs:

- Place the input capacitor as close as possible to the VIN and GND pins.
- Place the output capacitor as close as possible to the VOUT and GND pins.
- Place the soft start capacitor as close as possible to the SS pin.
- Connect the load as close as possible to the VOUT and SENSE pins (ADP1754) or to the VOUT and ADJ pins (ADP1755).

Use of 0603 or 0805 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

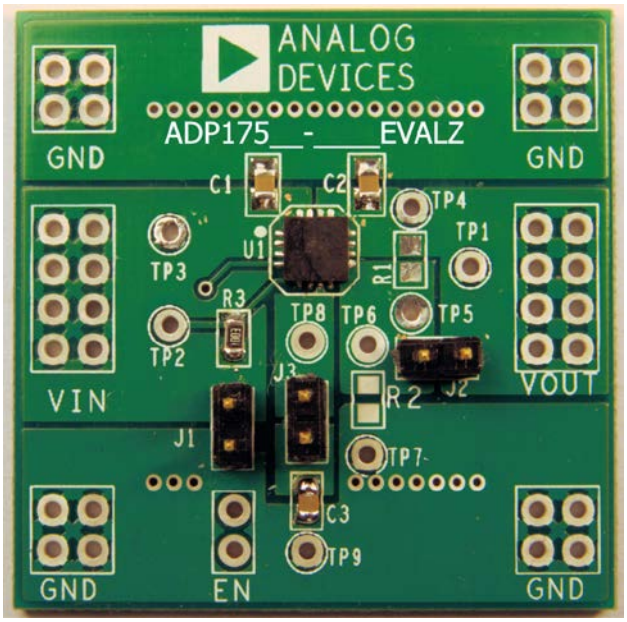

Figure 46. Evaluation Board

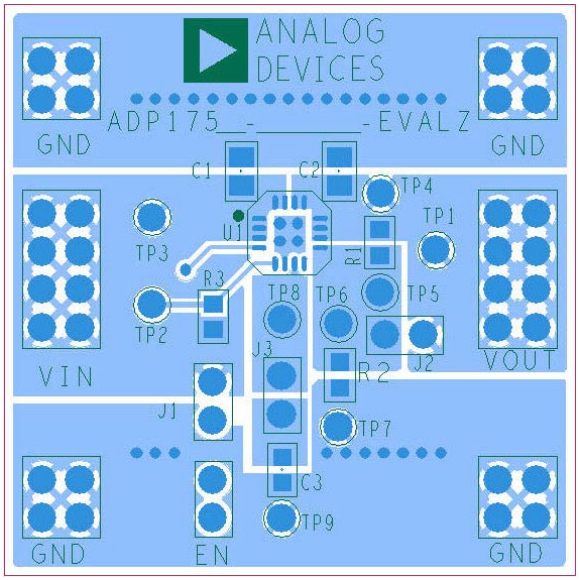

Figure 47. Typical Board Layout—Top Side

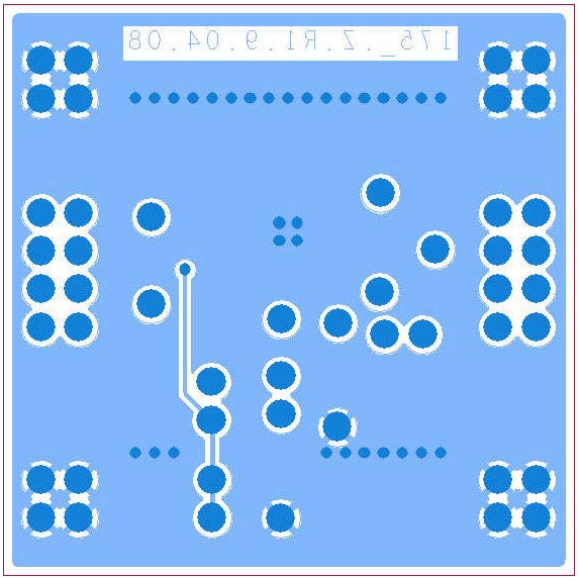

Figure 48. Typical Board Layout—Bottom Side

OUTLINE DIMENSIONS

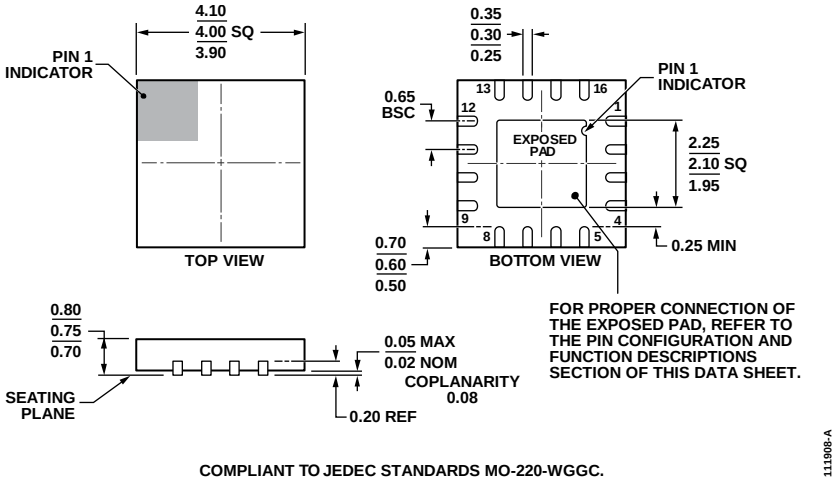

Figure 49. 16-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-16-23)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)	Package Description	Package Option
ADP1754ACPZ-0.75R7	−40°C to +125°C	0.75	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.0-R7	−40°C to +125°C	1.0	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.1-R7	−40°C to +125°C	1.1	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.2-R7	−40°C to +125°C	1.2	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.3-R7	−40°C to +125°C	1.3	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.5-R7	−40°C to +125°C	1.5	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-1.8-R7	−40°C to +125°C	1.8	16-Lead LFCSP_WQ	CP-16-23
ADP1754ACPZ-2.5-R7	−40°C to +125°C	2.5	16-Lead LFCSP_WQ	CP-16-23
ADP1755ACPZ-R7	−40°C to +125°C	Adjustable from 0.75 to 3.3	16-Lead LFCSP_WQ	CP-16-23
ADP1754-1.5-EVALZ		1.5	Evaluation Board	
ADP1755-EVALZ		Adjustable	Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D07722-0-4/14(G)