Transition Loss (P_{TRAN})

Transition losses occur because the high-side MOSFET cannot turn on or off instantaneously. During a switch node transition, the MOSFET provides all the inductor current. The source-to-drain voltage of the MOSFET is half the input voltage, resulting in power loss. Transition losses increase with both load and input voltage and occur twice for each switching cycle. Use the following equation to estimate the transition loss:

$$P_{TRAN} = 0.5 \times V_{IN} \times I_{OUT} \times (t_R + t_F) \times f_{SW}$$

where:
t_R is the rise time of the switch node.
t_F is the fall time of the switch node.

For the ADN8833, t_R and t_F are both approximately 1 ns.

Linear Regulator Power Dissipation

The power dissipation of the linear regulator is given by the following equation:

$$P_{LINEAR} = [(V_{IN} - V_{OUT}) \times I_{OUT}] + (V_{IN} \times I_{GND})$$

where:
V_{IN} and V_{OUT} are the input and output voltages of the linear regulator.
I_{OUT} is the load current of the linear regulator.
I_{GND} is the ground current of the linear regulator.

Power dissipation due to the ground current is generally small and can be ignored for the purposes of this calculation.

PCB LAYOUT GUIDELINES

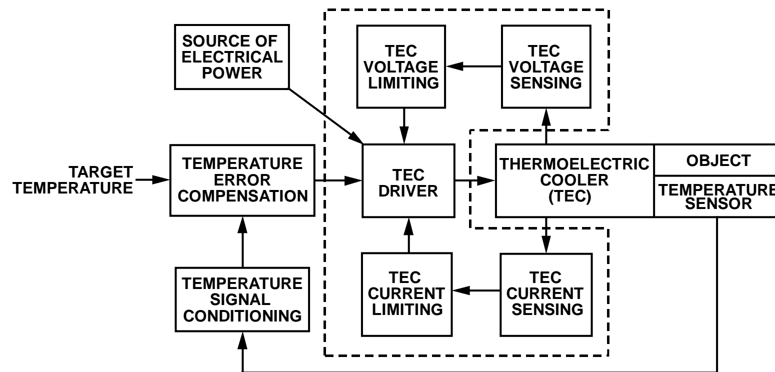

Figure 34. System Block Diagram

BLOCK DIAGRAMS AND SIGNAL FLOW

The ADN8833 integrates analog signal conditioning blocks, a load protection block, and a TEC driver power stage all in a single IC. To achieve the best possible circuit performance, attention must be paid to keep noise of the power stage from contaminating the sensitive analog conditioning and protection circuits. In addition, the layout of the power stage must be performed such that the IR losses are minimized to obtain the best possible electrical efficiency. The system block diagram of the ADN8833 is shown in Figure 34.

GUIDELINES FOR REDUCING NOISE AND MINIMIZING POWER LOSS

Each printed circuit board (PCB) layout is unique because of the physical constraints defined by the mechanical aspects of a given design. In addition, several other circuits work in conjunction with the TEC driver; these circuits have their own layout requirements, so there are always compromises that must be made for a given system. However, to minimize noise and keep power losses to a minimum during the PCB layout process, observe the following guidelines.

General PCB Layout Guidelines

Switching noise can interfere with other signals in the system; therefore, the switching signal traces must be placed away from the power stage to minimize the effect. If possible, place the ground plate between the small signal layer and power stage layer as a shield.

Supply voltage drop on traces is also an important consideration because it determines the voltage headroom of the TEC driver at high currents. For example, if the supply voltage from the front-end system is 3.3 V, and the voltage drop on the traces is 0.5 V, PVIN sees only 2.8 V, which limits the maximum voltage of the linear regulator as well as the maximum voltage across the TEC. To mitigate the voltage waste on traces and impedance interconnection, place the ADN8833 and the input decoupling components close to the supply voltage terminal. This placement not only improves the system efficiency, but also provides better regulation performance at the output.

To prevent noise signal from circulating through ground plates, reference all of the sensitive analog signals to AGND and connect AGND to PGNDS using only a single point connection. This ensures that the switching currents of the power stage do not flow into the sensitive AGND node.

PWM Power Stage Layout Guidelines

The PWM power stage consists of a MOSFET pair that forms a switch mode output that switches current from PVIN to the load via an LC filter. The ripple voltage on the PVIN pin is caused by the discontinuous current switched by the PWM side MOSFETs. This rapid switching causes voltage ripple to form at the PVIN input, which must be filtered using a bypass capacitor. Place a 10 µF capacitor as close as possible to the PVIN pin to connect PVIN to PGNDS. Because the 10 µF capacitor is sometimes bulky and has higher ESR and ESL, a 100 nF decoupling capacitor is usually used in parallel with it, placed between PVIN and PGNDS.

Because the decoupling is part of the pulsating current loop, which carries high di/dt signals, the traces must be short and wide to minimize the parasitic inductance. As a result, this capacitor is usually placed on the same side of the board as the ADN8833 to ensure short connections. If the layout requires that 10 µF capacitor be on the opposite side of the PCB, use multiple vias to reduce via impedance.

The layout around the SW node is also critical because it switches between PVIN and ground rapidly, which makes this node a strong EMI source. Keep the copper area that connects the SW node to the inductor small to minimize parasitic capacitance between the SW node and other signal traces. This helps minimize noise on the SW node due to excessive charge injection. However, in high current applications, the copper area may be increased reasonably to provide heat sink and to sustain high current flow.

Connect the ground side of the capacitor in the LC filter as close as possible to PGNDS to minimize the ESL in the return path.

Linear Power Stage Layout Guidelines

The linear power stage consists of a MOSFET pair that forms a linear amplifier, which operates in linear mode for very low output currents, and changes to fully enhanced mode for greater output currents.

Because the linear power stage does not switch currents rapidly like the PWM power stage, it does not generate noise currents. However, the linear power stage still requires a minimum amount of bypass capacitance to decouple its input.

Place a 100 nF capacitor that connects from PVIN to PGNDL as close as possible to the PVIN pin.

EXAMPLE PCB LAYOUT USING TWO LAYERS

Figure 35, Figure 36, and Figure 37 show an example ADN8833 WLCSP PCB layout that uses two layers. This layout example achieves a small solution size of approximately 18 mm^2 with all of the conditioning circuitry and PID included. Using more layers and blind vias allows the solution size to be reduced even further because more of the discrete components can relocate to the bottom side of the PCB.

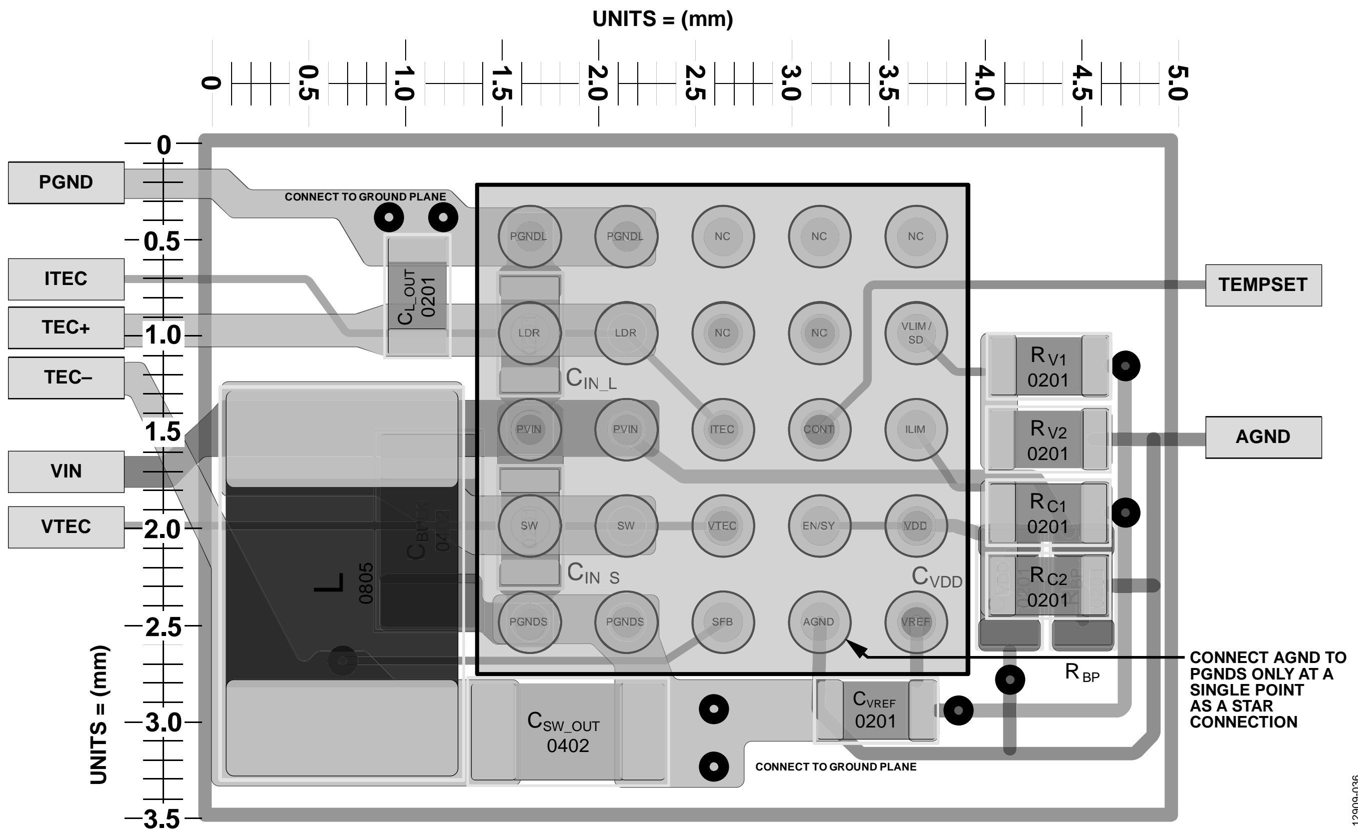

Figure 35. Example PCB Layout Using Two Layers (Top and Bottom Layers)

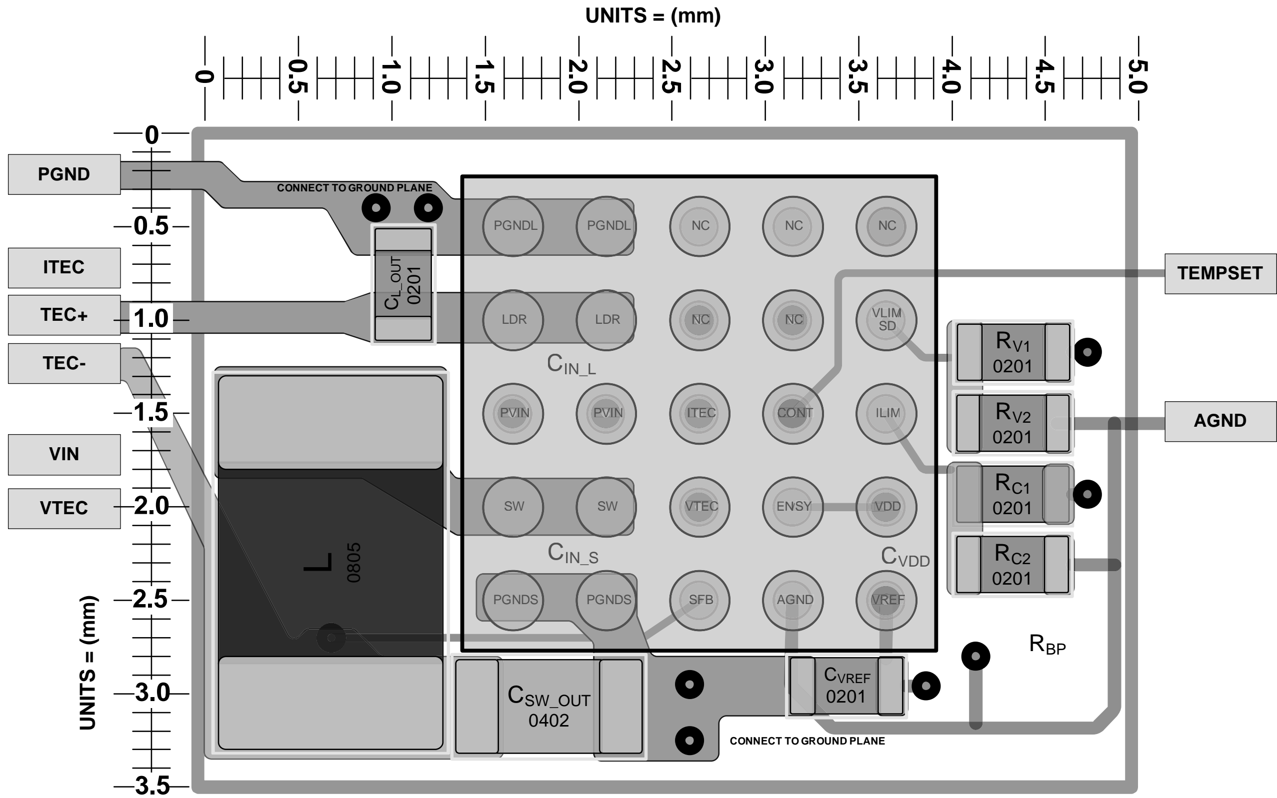

Figure 36. Example PCB Layout Using Two Layers (Top Layer Only)

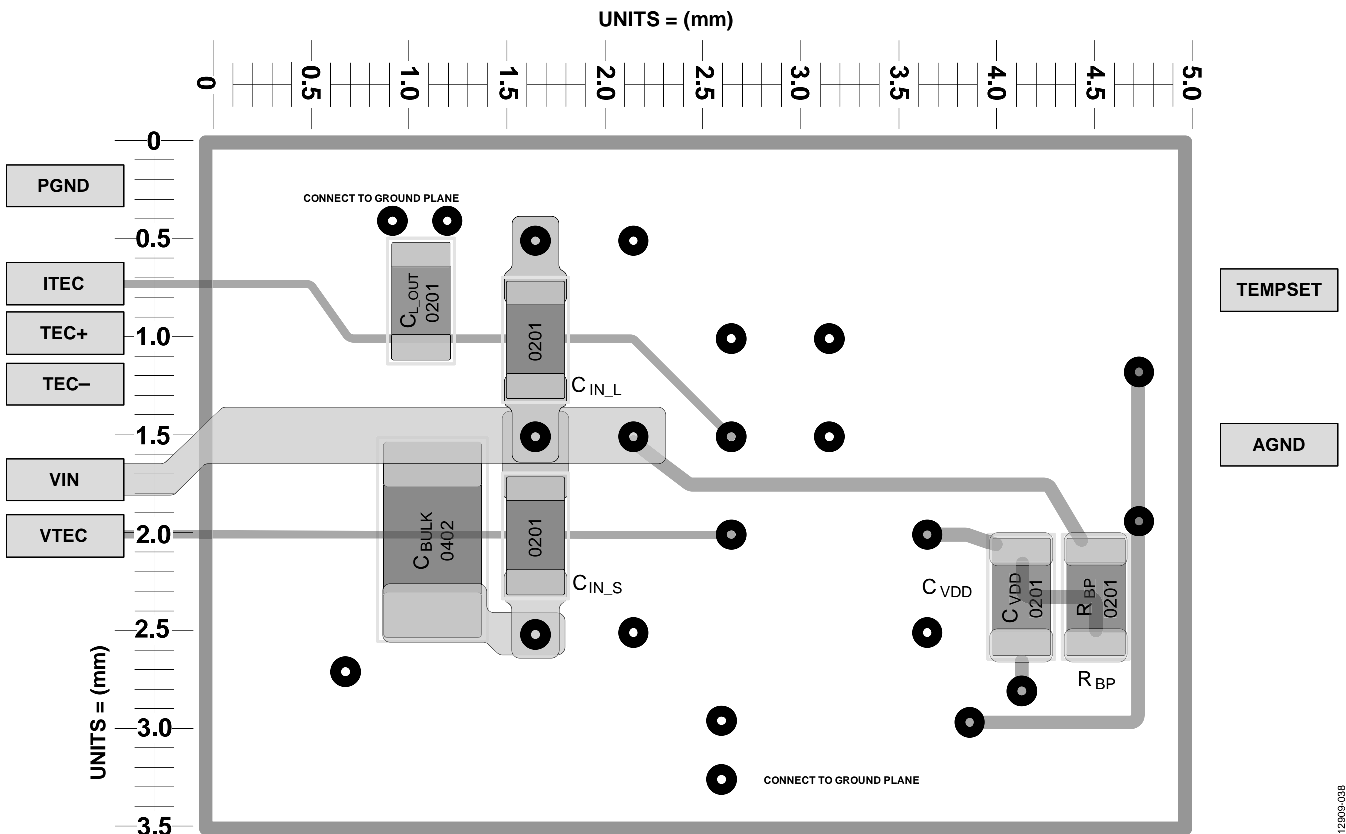

Figure 37. Example PCB Layout Using Two Layers (Bottom Layer Only)

OUTLINE DIMENSIONS

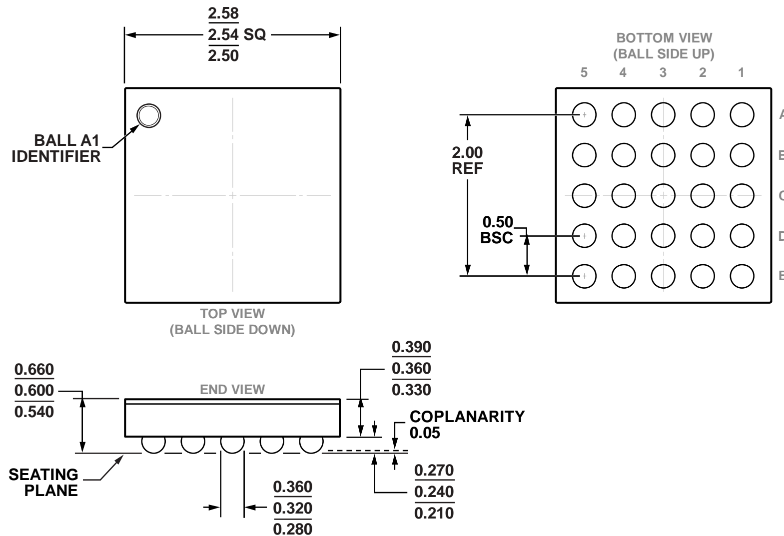

Figure 38. 25-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-25-7)
Dimensions shown in millimeters

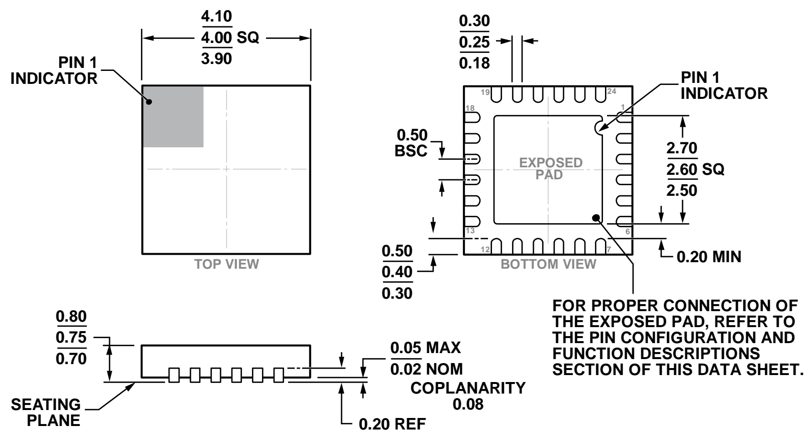

Figure 39. 24-Lead Lead-frame Chip Scale Package [LFCSP_WQ]
4 mm × 4 mm Body, Very Very Thin Quad
(CP-24-15)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range[2]	Package Description	Package Option
ADN8833ACBZ-R7	−40°C to +125°C	25-Ball Wafer Level Chip Scale Package [WLCSP]	CB-25-7
ADN8833CB-EVALZ		25-Ball WLCSP Evaluation Board: ±1 A TEC Current Limit, 3 V TEC Voltage Limit	
ADN8833ACPZ-R2	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-15
ADN8833ACPZ-R7	−40°C to +125°C	24-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-24-15
ADN8833CP-EVALZ		24-Lead LFCSP Evaluation Board: ±1 A TEC Current Limit, 3 V TEC Voltage Limit	

[1] Z = RoHS Compliant Part.
[2] Operating junction temperature range. The ambient operating temperature range is −40°C to +85°C.

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D12909-0-8/18(B)