FEATURES

- ±15 kV ESD protection on input pins
- 400 Mbps (200 MHz) switching rates
- Flow-through pinout simplifies PCB layout
- 2.5 ns maximum propagation delay
- 3.3 V power supply
- High impedance outputs on power-down
- Low power design: typically 18 mW (quiescent)
- Interoperable with existing 5 V LVDS drivers
- Accepts small swing (310 mV typical) differential signal levels
- Supports open, short, and terminated input fail-safe
- 0 V to −100 mV threshold region
- Conforms to TIA/EIA-644 LVDS standard
- Industrial operating temperature range: −40°C to +85°C
- Available in surface-mount (SOIC) package

APPLICATIONS

- Point-to-point data transmission
- Multidrop buses
- Clock distribution networks
- Backplane receivers

GENERAL DESCRIPTION

The ADN4662 is a single, CMOS, low voltage differential signaling (LVDS) line receiver offering data rates of over 400 Mbps (200 MHz), and ultralow power consumption. It features a flow-through pinout for easy PCB layout and separation of input and output signals.

The device accepts low voltage (310 mV typical) differential input signals and converts them to a single-ended 3 V TTL/CMOS logic level.

The ADN4662 and its companion driver, the ADN4661, offer a new solution to high speed, point-to-point data transmission, and a low power alternative to emitter-coupled logic (ECL) or positive emitter-coupled logic (PECL).
TABLE OF CONTENTS

Features .............................................................................................. 1
Applications........................................................................................ 1
Functional Block Diagram .............................................................. 1
General Description ......................................................................... 1
Revision History ............................................................................... 2
Specifications..................................................................................... 3
  AC Characteristics........................................................................... 4
Absolute Maximum Ratings............................................................... 6

REVISION HISTORY

10/13—Rev. 0 to Rev. A
Change to Features Section .............................................................. 1

1/09—Revision 0: Initial Version
### SPECIFICATIONS

$V_{DD} = 3.0 \text{ V to } 3.6 \text{ V}; C_L = 15 \text{ pF to GND};$ all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

#### Table 1.

<table>
<thead>
<tr>
<th>Parameter1</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ2</th>
<th>Max</th>
<th>Unit</th>
<th>Conditions/Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LVDS INPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High Threshold at $R_{IN+}$, $R_{IN-}$3</td>
<td>$V_{TH}$</td>
<td>$-100$</td>
<td>+100</td>
<td>mV</td>
<td>$V_{CM} = 1.2 \text{ V, } 0.05 \text{ V, } 2.95 \text{ V}$</td>
<td></td>
</tr>
<tr>
<td>Low Threshold at $R_{IN+}$, $R_{IN-}$3</td>
<td>$V_{TL}$</td>
<td>$-10$</td>
<td>±1</td>
<td>+10</td>
<td>μA</td>
<td>$V_{IN} = 2.8 \text{ V}, V_{CC} = 3.6 \text{ V or } 0 \text{ V}$</td>
</tr>
<tr>
<td>Input Current at $R_{IN+}$, $R_{IN-}$</td>
<td>$I_{IN}$</td>
<td>$-10$</td>
<td>±1</td>
<td>+10</td>
<td>μA</td>
<td>$V_{IN} = 0 \text{ V}, V_{CC} = 3.6 \text{ V or } 0 \text{ V}$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-20$</td>
<td>±1</td>
<td>+20</td>
<td>μA</td>
<td>$V_{IN} = 3.6 \text{ V}, V_{CC} = 0 \text{ V}$</td>
</tr>
<tr>
<td>OUTPUT</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output High Voltage</td>
<td>$V_{OH}$</td>
<td>2.7</td>
<td>3.1</td>
<td>V</td>
<td>$I_{OH} = -0.4 \text{ mA}, V_{ID} = +200 \text{ mV}$</td>
<td></td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>$V_{OL}$</td>
<td>2.7</td>
<td>3.1</td>
<td>V</td>
<td>$I_{OH} = -0.4 \text{ mA, input terminated}$</td>
<td></td>
</tr>
<tr>
<td>Output Short-Circuit Current4</td>
<td>$I_{OS}$</td>
<td>$-15$</td>
<td>$-47$</td>
<td>$-100$</td>
<td>mA</td>
<td>Enabled; $V_{OUT} = 0 \text{ V}$</td>
</tr>
<tr>
<td>Input Clamp Voltage</td>
<td>$V_{CL}$</td>
<td>$-1.5$</td>
<td>$-0.8$</td>
<td>V</td>
<td>$I_{CL} = -18 \text{ mA}$</td>
<td></td>
</tr>
<tr>
<td>POWER SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>No Load Supply Current</td>
<td>$I_{CC}$</td>
<td>5.4</td>
<td>9</td>
<td>mA</td>
<td>Inputs open</td>
<td></td>
</tr>
<tr>
<td>ESD PROTECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{IN+}$, $R_{IN-}$ Pins</td>
<td></td>
<td>±15</td>
<td></td>
<td>kV</td>
<td>Human body model</td>
<td></td>
</tr>
<tr>
<td>All Pins Except $R_{IN+}$, $R_{IN-}$</td>
<td></td>
<td>±4</td>
<td></td>
<td>kV</td>
<td>Human body model</td>
<td></td>
</tr>
</tbody>
</table>

1 Current into device pins is defined as positive. Current out of device pins is defined as negative. All voltages are referenced to ground, unless otherwise specified.

2 All typicals are given for: $V_{CC} = +3.3 \text{ V, } T_A = 25^\circ \text{C}$. 

3 $V_{CC}$ is always higher than $R_{IN+}$ and $R_{IN-}$ voltage. $R_{IN+}$ and $R_{IN-}$ are allowed to have a voltage range of $-0.2 \text{ V to } V_{CC} - V_{OH}/2$. However, to be compliant with ac specifications, the common voltage range is $0.1 \text{ V to } 2.3 \text{ V}$.

4 Output short-circuit current ($I_{OS}$) is specified as magnitude only; the minus sign indicates direction only. Only one output should be shorted at a time. Do not exceed maximum junction temperature specification.
AC CHARACTERISTICS

$V_{DD} = 3.0 \text{ V to 3.6 V}$; $C_L^1 = 15 \text{ pF to GND}$; all specifications $T_{MIN}$ to $T_{MAX}$, unless otherwise noted.

### Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ $^2$</th>
<th>Max</th>
<th>Unit</th>
<th>Conditions/Comments $^3$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Differential Propagation Delay High to Low</td>
<td>$t_{PHLD}$</td>
<td>1.0</td>
<td>2.15</td>
<td>2.5</td>
<td>ns</td>
<td>$C_L = 15 \text{ pF}, V_{DD} = 200 \text{ mV}$ (see Figure 2 and Figure 3)</td>
</tr>
<tr>
<td>Differential Propagation Delay Low to High</td>
<td>$t_{PLHD}$</td>
<td>1.0</td>
<td>2.03</td>
<td>2.5</td>
<td>ns</td>
<td>$C_L = 15 \text{ pF}, V_{DD} = 200 \text{ mV}$ (see Figure 2 and Figure 3)</td>
</tr>
<tr>
<td>Differential Pulse Skew $</td>
<td>t_{PHLD}−t_{PLHD}</td>
<td>$</td>
<td>$t_{SKD1}$</td>
<td>0</td>
<td>80</td>
<td>400</td>
</tr>
<tr>
<td>Differential Part-to-Part Skew $^5$</td>
<td>$t_{SKD3}$</td>
<td></td>
<td>1.0</td>
<td></td>
<td>ns</td>
<td>$C_L = 15 \text{ pF}, V_{DD} = 200 \text{ mV}$ (see Figure 2 and Figure 3)</td>
</tr>
<tr>
<td>Differential Part-to-Part Skew $^6$</td>
<td>$t_{SKD4}$</td>
<td></td>
<td>1.5</td>
<td></td>
<td>ns</td>
<td>$C_L = 15 \text{ pF}, V_{DD} = 200 \text{ mV}$ (see Figure 2 and Figure 3)</td>
</tr>
<tr>
<td>Rise Time</td>
<td>$t_{RLH}$</td>
<td>510</td>
<td>800</td>
<td></td>
<td>ps</td>
<td>$C_L = 15 \text{ pF}, V_{DD} = 200 \text{ mV}$ (see Figure 2 and Figure 3)</td>
</tr>
<tr>
<td>Fall Time</td>
<td>$t_{THL}$</td>
<td>445</td>
<td>800</td>
<td></td>
<td>ps</td>
<td>$C_L = 15 \text{ pF}, V_{DD} = 200 \text{ mV}$ (see Figure 2 and Figure 3)</td>
</tr>
<tr>
<td>Maximum Operating Frequency $^7$</td>
<td>$f_{MAX}$</td>
<td>200</td>
<td>250</td>
<td></td>
<td>MHz</td>
<td>All channels switching</td>
</tr>
</tbody>
</table>

$^1$ $C_L$ includes probe and jig capacitance.

$^2$ All typicals are given for $V_{CC} = 3.3 \text{ V}, T_a = 25^\circ\text{C}$.

$^3$ Generator waveform for all tests unless otherwise specified: $f = 1 \text{ MHz}, Z_0 = 50 \Omega$, $t_{TLH}$ and $t_{THL}$ (0% to 100%) $< 3 \text{ ns}$ for $R_{IN+}/R_{IN-}$.

$^4$ $t_{SKD1}$ is the magnitude difference in differential propagation delay time between the positive going edge and the negative going edge of the same channel.

$^5$ $t_{SKD3}$, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices at the same $V_{CC}$ and within 5°C of each other within the operating temperature range.

$^6$ $t_{SKD4}$, part-to-part skew, is the differential channel-to-channel skew of any event between devices. This specification applies to devices over recommended operating temperature and voltage ranges, and across process distribution. $t_{SKD4}$ is defined as $|maximum − minimum|$ differential propagation delay.

$^7$ $f_{MAX}$ generator input conditions: $f = 200 \text{ MHz}, t_{TLH} = t_{THL} < 1 \text{ ns}$ (0% to 100%), 50% duty cycle, differential (1.05 V to 1.35 V peak-to-peak). Output criteria: 60%/40% duty cycle, $V_{OL}$ (maximum 0.4 V), $V_{OH}$ (minimum 2.7 V), load = 15 pF (stray plus probes).
Test Circuits and Timing Diagrams

Figure 2. Test Circuit for Receiver Propagation Delay and Transition Time

Figure 3. Receiver Propagation Delay and Transition Time Waveforms
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ C$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$ to GND</td>
<td>$-0.3 \text{ V to } +4 \text{ V}$</td>
</tr>
<tr>
<td>Input Voltage ($R_{\text{IN}+}$, $R_{\text{IN}-}$) to GND</td>
<td>$-0.3 \text{ V to } V_{CC} + 3.9 \text{ V}$</td>
</tr>
<tr>
<td>Output Voltage ($R_{\text{OUT}}$) to GND</td>
<td>$-0.3 \text{ V to } V_{CC} + 0.3 \text{ V}$</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td></td>
</tr>
<tr>
<td>Industrial Temperature Range</td>
<td>$-40^\circ \text{ C to } +85^\circ \text{ C}$</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$-65^\circ \text{ C to } +150^\circ \text{ C}$</td>
</tr>
<tr>
<td>Junction Temperature ($T_J \text{ max}$)</td>
<td>$150^\circ \text{ C}$</td>
</tr>
<tr>
<td>Power Dissipation</td>
<td>$(T_J \max - T_A)/\theta_{JA}$</td>
</tr>
<tr>
<td>SOIC Package</td>
<td>149.5°C/W</td>
</tr>
<tr>
<td>$\theta_{JA}$ Thermal Impedance</td>
<td></td>
</tr>
<tr>
<td>Reflow Soldering Peak Temperature Pb-Free</td>
<td>260°C ± 5°C</td>
</tr>
</tbody>
</table>

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

![ADN4662 TOP VIEW](https://lorempixel.com/400/300)

### Table 4. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RIN−</td>
<td>Receiver Channel 1 Inverting Input. When this input is more negative than RIN+, ROUT is high. When this input is more positive than RIN+, ROUT is low.</td>
</tr>
<tr>
<td>2</td>
<td>RIN+</td>
<td>Receiver Channel 1 Noninverting Input. When this input is more positive than RIN−, ROUT is high. When this input is more negative than RIN−, ROUT is low.</td>
</tr>
<tr>
<td>3</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>4</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>Ground reference point for all circuitry on the part.</td>
</tr>
<tr>
<td>6</td>
<td>NC</td>
<td>No Connect.</td>
</tr>
<tr>
<td>7</td>
<td>ROUT</td>
<td>Receiver Output (3 V TTL/CMOS). If the differential input voltage between RIN+ and RIN− is positive, this output is high. If the differential input voltage is negative, this output is low.</td>
</tr>
<tr>
<td>8</td>
<td>VCC</td>
<td>Power Supply Input. This part can be operated from 3.0 V to 3.6 V.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 5. Output High Voltage vs. Power Supply Voltage

Figure 8. Threshold Voltage vs. Power Supply Voltage

Figure 6. Output Low Voltage vs. Power Supply Voltage

Figure 9. Power Supply Current vs. Frequency

Figure 7. Output Short-Circuit Current vs. Power Supply Voltage

Figure 10. Power Supply Current vs. Ambient Temperature
2.5 2.4 2.3 2.2 2.1 2.0 1.9 1.8

-40 -15 10 35 85 60

AMBIENT TEMPERATURE, $T_A$ (°C)

Differential Propagation Delay, $t_{PHLD}, t_{PLHD}$ (ns)

VCC = 3.3V
VID = 200mV
FREQUENCY = 200MHz
CL = 15pF

Figure 11. Differential Propagation Delay vs. Ambient Temperature

4.0 3.5 3.0 2.5 2.0 1.5 1.0

0 0.5 1.0 1.5 2.0 2.5 3.0

COMMON-MODE VOLTAGE, $V_{CM}$ (V)

Differential Propagation Delay, $t_{PHLD}, t_{PLHD}$ (ns)

TA = 25°C
VID = 200mV
FREQUENCY = 200MHz
CL = 15pF

Figure 12. Differential Propagation Delay vs. Common-Mode Voltage

250 200 150 100 50 0

-50

-100

3.0 3.1 3.2 3.3 3.4 3.5 3.6

DIFFERENTIAL SKEW, $t_{SKEW}$ (ps)

POWER SUPPLY VOLTAGE, $V_{CC}$ (V)

TA = 25°C
VID = 200mV
FREQUENCY = 200MHz
CL = 15pF

Figure 15. Differential Skew vs. Power Supply Voltage

160 140 120 100 80 60 40 20 0

-40 -15 10 35 60 85

DIFFERENTIAL SKEW, $t_{SKEW}$ (ps)

AMBIENT TEMPERATURE, $T_A$ (°C)

VCC = 3.3V
VID = 200mV
FREQUENCY = 200MHz
CL = 15pF

Figure 16. Differential Skew vs. Ambient Temperature

3.0 3.1 3.2 3.3 3.4 3.5 3.6

DIFFERENTIAL INPUT VOLTAGE, $V_{ID}$ (V)

Power Supply Voltage, $V_{CC}$ (V)

TA = 25°C
VID = 200mV
FREQUENCY = 200MHz
CL = 15pF

Figure 14. Differential Propagation Delay vs. Differential Input Voltage

2.30 2.25 2.20 2.15 2.10 2.05 2.00 1.95 1.90 1.85

0 0.5 1.0 1.5 2.0 2.5 3.0

Differential Propagation Delay, $t_{PHLD}, t_{PLHD}$ (ps)

VCC = 3.3V
CL = 15pF
FREQUENCY = 200MHz

Figure 13. Differential Propagation Delay vs. Power Supply Voltage
Figure 17. Transition Time vs. Power Supply Voltage

Figure 18. Transition Time vs. Ambient Temperature

Figure 19. Differential Propagation Delay vs. Load at 1 MHz

Figure 20. Transition Time vs. Load

Figure 21. Differential Propagation Delay vs. Load at 200 MHz

Figure 22. Transition Time vs. Load at 200 MHz
THEORY OF OPERATION

The ADN4662 is a single line receiver for low voltage differential signaling. It takes a differential input signal of 310 mV typically and converts it into a single-ended 3 V TTL/CMOS logic signal.

A differential current input signal, received via a transmission medium, such as a twisted pair cable, develops a voltage across a terminating resistor, RT. This resistor is chosen to match the characteristic impedance of the medium, typically around 100 Ω. The differential voltage is detected by the receiver and converted back into a single-ended logic signal.

When the noninverting receiver input, RIN+, is positive with respect to the inverting input RIN− (current flows through RT from RIN+ to RIN−), then ROUT is high. When the noninverting receiver input RIN+ is negative with respect to the inverting input RIN− (current flows through RT from RIN− to RIN+), then ROUT is low.

The ADN4662 differential line receiver is capable of receiving signals of 100 mV over a ±1 V common-mode range centered around 1.2 V. This relates to the typical driver offset voltage value of 1.2 V. The signal originating from the driver is centered around 1.2 V and may shift ±1 V around this center point. This ±1 V shifting may be caused by a difference in the ground potential of the driver and receiver, the common-mode effect of coupled noise, or both.

Using the ADN4663 as a driver, the received differential current is between 2.5 mA and 4.5 mA (typically 3.1 mA), developing between 250 mV and 450 mV across a 100 Ω termination resistor. The received voltage is centered around the receiver offset of 1.2 V. In other words, the noninverting receiver input is typically

\[(1.2 \text{ V} + [310 \text{ mV}/2]) = 1.355 \text{ V}, \text{ and the inverting receiver input} \]
\[(1.2 \text{ V} - [310 \text{ mV}/2]) = 1.045 \text{ V} \text{ for Logic 1}. \text{ For Logic 0, the inverting and noninverting input voltages are reversed.} \text{ Note that because the differential voltage reverses polarity, the peak-to-peak voltage swing across } R_T \text{ is twice the differential voltage.} \]

Current mode signalling offers considerable advantages over voltage mode signalling, such as RS-422. The operating current remains fairly constant with increased switching frequency, whereas with voltage mode drivers the current increases exponentially in most cases. This is caused by the overlap as internal gates switch between high and low, which causes currents to flow from VCC to ground. A current mode device simply reverses a constant current between its two outputs, with no significant overlap currents.

This is similar to emitter-coupled logic (ECL) and positive emitter-coupled logic (PECL), but without the high quiescent current of ECL and PECL.

APPLICATIONS INFORMATION

Figure 23 shows a typical application for point-to-point data transmission using the ADN4663 as the driver.
OUTLINE DIMENSIONS

Figure 24. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)

Dimensions shown in millimeters and (inches)

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model1</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADN4662BRZ</td>
<td>−40°C to +85°C</td>
<td>8-Lead Standard Small Outline Package [SOIC_N]</td>
<td>R-8</td>
</tr>
<tr>
<td>ADN4662BRZ-REEL7</td>
<td>−40°C to +85°C</td>
<td>8-Lead Standard Small Outline Package [SOIC_N]</td>
<td>R-8</td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.