

FEATURES

- TIA/EIA RS-485 compliant over full supply range
- 3.0 V to 5.5 V operating voltage range on V_{CC}
- 1.62 V to 5.5 V V_{IO} logic supply
- ESD protection on the bus pins
 - IEC 61000-4-2 ± 12 kV contact discharge
 - IEC 61000-4-2 $\geq \pm 12$ kV air discharge
 - HBM $\geq \pm 30$ kV
- Full hot swap support (glitch free power-up/power-down)
- High speed 50 Mbps data rate (ADM3065E/ADM3066E/ADM3067E)
- Low speed 500 kbps data rate for long cables (ADM3061E/ADM3062E)
- Full receiver short-circuit, open circuit, and bus idle fail-safe
- Extended temperature range up to 125°C
- PROFIBUS compliant at $V_{CC} \geq 4.5$ V
- Half duplex and full duplex models available
- Allows connection of up to 128 transceivers onto the bus
- Space-saving package options
 - 10-lead, 3 mm \times 3 mm LFCSP
 - 8-lead and 10-lead MSOP
 - 8-lead, narrow-body SOIC package
 - 14-lead, narrow-body SOIC package

APPLICATIONS

- Industrial fieldbuses
- Process control
- Building automation
- PROFIBUS networks
- Motor control servo drives and encoders

FUNCTIONAL BLOCK DIAGRAMS

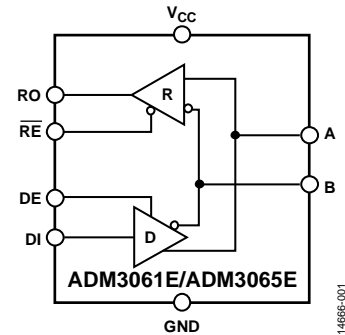


Figure 1. ADM3061E/ADM3065E Functional Block Diagram

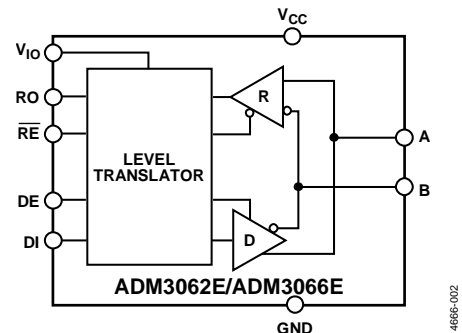


Figure 2. ADM3062E/ADM3066E Functional Block Diagram

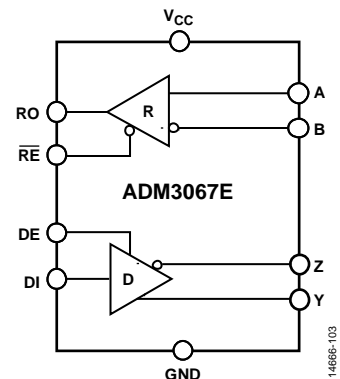


Figure 3. ADM3067E Functional Block Diagram

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REVISION HISTORY

3/2019—Rev. C to Rev. D

| | |
|---|----|
| Added ADM3067E and 14-Lead SOIC_N, R-14..... Universal Changes to Feature Section | 1 |
| Added Figure 3; Renumbered Sequentially | 1 |
| Moved Table 1 to | 4 |
| Changes to Table 2 | 5 |
| Changes to ADM3065E/ADM3066E/ADM3067E Section..... | 7 |
| Change to Pin 3, Description Column, Table 7 | 11 |
| Changes to Figure 10, Figure 11, and Table 8..... | 12 |
| Added Figure 12 and Table 9; Renumbered Sequentially | 13 |
| Changes to Figure 14..... | 14 |
| Moved Test Circuits to | 18 |
| Changes to Table 10 and Table 11 | 20 |
| Updated Outline Dimensions | 26 |
| Changes to Ordering Guide..... | 27 |

1/2018—Rev. B to Rev. C

| | |
|---|-----------|
| Added ADM3062E | Universal |
| Changes to Figure 2 and Table 1 | 1 |
| Changes to ADM3061E/ADM3062E Timing Specifications Section and Figure 3 | 6 |
| Changes to Figure 5 and Figure 6 | 7 |
| Changes to Figure 9 and Figure 10 | 11 |
| Changes to Figure 16 and Figure 17 | 12 |
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12/2017—Rev. A to Rev. B

| | |
|--|----|
| Added ADM3061E..... Universal Changes to Product Title, Features Section, Figure 1, and Table 1... 1 | 1 |
| Changes to General Description Section | 3 |
| Changes to Table 2..... | 4 |
| Added ADM3061E Timing Specification Section and Table 3; Renumbered Sequentially | 6 |
| Moved Figure 3 | 6 |
| Moved Figure 4, Figure 5, and Figure 6..... | 7 |
| Changes to ADM3065E/ADM3066E Timing Specification Section Title..... | 8 |
| Added 10-Lead MSOP Parameter and 10-Lead LFCSP Parameter, Table 5..... | 9 |
| Changes to Operating Temperature Range Parameter, Table 5 and Table 6..... | 9 |
| Changes to Figure 7, Figure 8, and Table 7 | 10 |
| Changes to Table 8..... | 11 |
| Changes to Figure 11..... | 12 |
| Added Figure 23; Renumbered Sequentially | 13 |
| Added Figure 24, Figure 25, Figure 26, Figure 27, and Figure 28... 14 | 14 |
| Changed High Speed IEC ESD Protected RS-485 Section to IEC ESD Protected RS-485 Section | 17 |
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| Added Endnote 4, Table 9 | 18 |
| Changes to Table 10..... | 18 |
| Changes to Figure 44 | 21 |
| Changes to Figure 45 | 22 |
| Changes to Ordering Guide | 25 |

5/2017—Rev. 0 to Rev. A

| | |
|--|-----------|
| Added ADM3066E..... | Universal |
| Changes to Features Section, Figure 1, and Table 1..... | 1 |
| Added Figure 2; Renumbered Sequentially | 1 |
| Moved General Description Section | 3 |
| Changes to General Description Section | 3 |
| Changes to Specifications Section and Table 2..... | 4 |
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| Added V_{IO} to GND Parameter, Table 4..... | 7 |
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| Added Figure 8 | 8 |
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| Added Figure 42 and Figure 43 | 20 |
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3/2017—Revision 0: Initial Version

GENERAL DESCRIPTION

The ADM3061E/ADM3062E/ADM3065E/ADM3067E are 3.0 V to 5.5 V, IEC electrostatic discharge (ESD) protected RS-485 transceivers, allowing the devices to withstand ± 12 kV contact discharges on the transceiver bus pins without latch-up or damage. The ADM3062E/ADM3066E feature a V_{IO} logic supply pin allowing a flexible digital interface capable of operating as low as 1.62 V.

The ADM3065E/ADM3066E/ADM3067E are suitable for high speed, 50 Mbps, bidirectional data communication on multipoint bus transmission lines. The ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E feature a one fourth unit load input impedance, which allows up to 128 transceivers on a bus. The ADM3061E/ADM3062E models offer all of the same features as the ADM3065E/ADM3066E/ADM3067E models, but at a low 500 kbps data rate suitable for operation over long cable runs.

The ADM3061E/ADM3062E/ADM3065E/ADM3066E are half-duplex RS-485 transceivers, fully compliant to the PROFIBUS® standard with increased 2.1 V bus differential voltage at $V_{CC} \geq 4.5$ V. The ADM3067E is a full duplex RS-485 transceiver option.

The RS-485 transceivers are available in a number of space-saving packages, such as the 10-lead, 3 mm \times 3 mm LFCSP; the 8-lead or 10-lead, 3 mm \times 3 mm MSOP; and the 8-lead or 14-lead, narrow body SOIC packages. Models with operating temperature ranges of -40°C to $+125^{\circ}\text{C}$ and -40°C to $+85^{\circ}\text{C}$ are available.

Excessive power dissipation caused by bus contention or by output shorting is prevented by a thermal shutdown circuit. If, during fault conditions, a significant temperature increase is detected in the internal driver circuitry, this feature forces the driver output into a high impedance state.

The ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E guarantee a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled.

Table 1 presents an overview of the ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E data rate capability across temperature, power supply, and package options. Refer to the Ordering Guide for model numbering.

Table 1. Summary of the ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E Operating Conditions—Data Rate Capability Across Temperature, Power Supply, and Package

| Maximum Data Rate ¹ | Maximum V_{CC} (V) | Maximum Temperature | Package Description |
|--------------------------------|----------------------|---|---|
| 50 Mbps | 5.5 | -40°C to $+125^{\circ}\text{C}$ | 10-lead LFCSP |
| 50 Mbps | 5.5 | -40°C to $+105^{\circ}\text{C}$ | 8-lead SOIC_N, 8-lead MSOP, and 10-lead MSOP |
| 50 Mbps | 3.6 | -40°C to $+125^{\circ}\text{C}$ | 8-lead SOIC_N, 8-lead MSOP, and 10-lead MSOP |
| 500 kbps | 5.5 | -40°C to $+125^{\circ}\text{C}$ | 8-lead SOIC_N, 8-lead MSOP, 10-lead MSOP, 10-lead LFCSP |

¹ The ADM3065E/ADM3066E/ADM3067E data input (DI) is transmitting 50 Mbps (or 500 kbps for the ADM3061E/ADM3062E) clock data, and the ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E driver enable (DE) is enabled for 50% of the DI transmit time

SPECIFICATIONS

$V_{CC} = 3.0\text{ V}$ to 5.5 V , $V_{IO} = 1.62\text{ V}$ to V_{CC} , $T_A = T_{MIN}$ (-40°C) to T_{MAX} ($+125^\circ\text{C}$), unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{IO} = V_{CC} = 3.3\text{ V}$, unless otherwise noted.

Table 2.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--|------------------|----------------------|------|----------------------|---------------|---|
| POWER SUPPLY | | | | | | |
| Supply Current | I_{CC} | | 2 | 7.5 | mA | No load, $DE = V_{CC}$, $\overline{RE} = 0\text{ V}$ |
| | | | | 7.5 | mA | No load, $DE = V_{CC}$, $\overline{RE} = V_{CC}$ |
| | | | | 4.5 | mA | No load, $DE = 0\text{ V}$, $\overline{RE} = 0\text{ V}$ |
| | | | | 172 | mA | 50 Mbps, load resistance (R_L) = $54\ \Omega$, $DE = V_{CC}$, $\overline{RE} = 0\text{ V}$ |
| | | | 67 | 75 | mA | 50 Mbps, $R_L = 54\ \Omega$, $DE = V_{CC}$, $\overline{RE} = 0\text{ V}$ ($V_{CC} = 3.0\text{ V}$) |
| | | | | 165 | mA | 500 kbps, $R_L = 54\ \Omega$, $DE = V_{CC}$, $\overline{RE} = 0\text{ V}$ |
| Supply Current in Shutdown Mode | I_{SHDN} | | | 450 | μA | $DE = 0\text{ V}$, $\overline{RE} = V_{CC}$ |
| V_{IO} Shutdown Current | $I_{IO SHDN}$ | | | 50 | μA | $DE = 0\text{ V}$, $\overline{RE} = V_{IO}$ |
| DRIVER | | | | | | |
| Differential Outputs | | | | | | |
| Output Voltage, Loaded | $ V_{OD2} $ | 2.0 | | V_{CC} | V | $V_{CC} \geq 3.0\text{ V}$, $R_L = 50\ \Omega$, see Figure 36 |
| | | 1.5 | | V_{CC} | V | $V_{CC} \geq 3.0\text{ V}$, $R_L = 27\ \Omega$ (RS-485), see Figure 36 |
| | | 2.1 | | V_{CC} | V | $V_{CC} \geq 4.5\text{ V}$, $R_L = 50\ \Omega$, see Figure 36 |
| | | 2.1 | | V_{CC} | V | $V_{CC} \geq 4.5\text{ V}$, $R_L = 27\ \Omega$ (RS-485), see Figure 36 |
| | | 1.5 | | V_{CC} | V | $V_{CC} \geq 3.0\text{ V}$, $-7\text{ V} \leq V_{CM} \leq +12\text{ V}$, see Figure 37 |
| | | 2.1 | | V_{CC} | V | $V_{CC} \geq 4.5\text{ V}$, $-7\text{ V} \leq V_{CM} \leq +12\text{ V}$, see Figure 37 |
| Change in Differential Input Voltage for Complementary Output States | $\Delta V_{OD} $ | | | 0.2 | V | $R_L = 27\ \Omega$ or $50\ \Omega$, see Figure 36 |
| Common-Mode Output Voltage | V_{OC} | | | 3.0 | V | $R_L = 27\ \Omega$ or $50\ \Omega$, see Figure 36 |
| Change in Common Mode Voltage for Complementary Output States | $\Delta V_{OC} $ | | | 0.2 | V | $R_L = 27\ \Omega$ or $50\ \Omega$, see Figure 36 |
| Output Short-Circuit Current | I_{OS} | -250 | | +250 | mA | $-7\text{ V} < \text{output voltage } (V_{OUT}) < +12\text{ V}$ |
| Output Leakage (Y, Z) Full Duplex | I_O | | | +100 | μA | $DE = 0\text{ V}$, $\overline{RE} = 0\text{ V}$, $V_{CC} = 0\text{ V}$ or 3.6 V , input voltage (V_{IN}) = 12 V |
| | | | -100 | | μA | $DE = 0\text{ V}$, $\overline{RE} = 0\text{ V}$, $V_{CC} = 0\text{ V}$ or 3.6 V , $V_{IN} = -7\text{ V}$ |
| Logic Inputs (DE, \overline{RE}, DI) | | | | | | |
| Input Voltage | | | | | | |
| Low | V_{IL} | | | $0.33 \times V_{IO}$ | V | $DE, \overline{RE}, DI, 1.62\text{ V} \leq V_{IO} \leq 5.5\text{ V}$ |
| High | V_{IH} | $0.67 \times V_{IO}$ | | | V | $DE, \overline{RE}, DI, 1.62\text{ V} \leq V_{IO} \leq 5.5\text{ V}$ |
| Input Current | I_I | -2 | | +2 | μA | $DE, \overline{RE}, DI, 1.62\text{ V} \leq V_{IO} \leq 5.5\text{ V}$, $0\text{ V} \leq V_{IN} \leq V_{IO}$ |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|--------------------------------------|-----------|----------------|------|---------|---------------|--|
| RECEIVER | | | | | | |
| Differential Inputs | | | | | | |
| Differential Input Threshold Voltage | V_{TH} | -200 | -125 | -30 | mV | $-7\text{ V} < \text{common-mode voltage } (V_{CM}) < +12\text{ V}$ |
| Input Voltage Hysteresis | V_{HYS} | | 30 | | mV | $-7\text{ V} < V_{CM} < +12\text{ V}$ |
| Input Current (A, B) | I_i | | | 0.25 | mA | $DE = 0\text{ V}, V_{CC} = \text{powered/unpowered}, V_{IN} = 12\text{ V}$ |
| | | -0.20 | | | mA | $DE = 0\text{ V}, V_{CC} = \text{powered/unpowered}, V_{IN} = -7\text{ V}$ |
| Line Input Resistance | R_{IN} | 48 | | | k Ω | $-7\text{ V} \leq V_{CM} \leq +12\text{ V}$ |
| Logic Outputs | | | | | | |
| Output Voltage | | | | | | |
| Low | V_{OL} | | | 0.4 | V | $V_{IO} = 3.6\text{ V}, \text{output current } (I_{OUT}) = 2\text{ mA}, V_{ID}^1 \leq -0.2\text{ V}$ |
| | | | | 0.4 | V | $V_{IO} = 2.7\text{ V}, I_{OUT} = 1\text{ mA}, V_{ID} \leq -0.2\text{ V}$ |
| | | | | 0.2 | V | $V_{IO} = 1.95\text{ V}, I_{OUT} = +500\text{ }\mu\text{A}, V_{ID} \leq -0.2\text{ V}$ |
| High | V_{OH} | 2.4 | | | V | $V_{IO} = 3.0\text{ V}, I_{OUT} = -2\text{ mA}, V_{ID} \geq +0.2\text{ V}$ |
| | | 2.0 | | | V | $V_{IO} = 2.3\text{ V}, I_{OUT} = -1\text{ mA}, V_{ID} \geq +0.2\text{ V}$ |
| | | $V_{IO} - 0.2$ | | | V | $V_{IO} = 1.65\text{ V}, I_{OUT} = -500\text{ }\mu\text{A}, V_{ID} \geq +0.2\text{ V}$ |
| Short-Circuit Current | | | | 85 | mA | $V_{OUT} = \text{GND or } V_{CC}$ |
| Three-State Output Leakage | I_{OZR} | | | ± 2 | μA | $RO = 0\text{ V or } V_{CC}$ |

¹ V_{ID} is the receiver input differential voltage.

TIMING SPECIFICATIONS**ADM3061E/ADM3062E**

$V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{IO} = 1.62\text{ V to }V_{CC}$, $T_A = T_{MIN} (-40^\circ\text{C})$ to $T_{MAX} (+125^\circ\text{C})$, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{IO} = V_{CC} = 3.3\text{ V}$, unless otherwise noted.

Table 3.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|-----------------------------------|----------------------|-----|-----|------|------|---|
| DRIVER | | | | | | |
| Maximum Data Rate ¹ | | 500 | | | kbps | |
| Propagation Delay | t_{DPLH}, t_{DPHL} | | 220 | 800 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 38 |
| Skew | t_{DSKEW} | | 5 | 100 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 38 |
| Rise/Fall Times | t_{DR}, t_{DF} | 120 | | 800 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 38 |
| Enable to Output High | t_{DZH} | | | 1000 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Enable to Output Low | t_{DZL} | | | 1000 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Disable Time from Low | t_{DLZ} | | | 2000 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Disable Time from High | t_{DHZ} | | | 2000 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Enable Time from Shutdown to High | $t_{DZH(SHDN)}^2$ | | | 2000 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Enable Time from Shutdown to Low | $t_{DZL(SHDN)}^2$ | | | 2000 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| RECEIVER | | | | | | |
| Maximum Data Rate | | 500 | | | kbps | |
| Propagation Delay | t_{RPLH}, t_{RPHL} | | | 200 | ns | $C_L = 15\text{ pF}$, $ V_{ID} \geq 1.5\text{ V}$, see Figure 40 |
| Skew/Pulse Width Distortion | t_{RSKEW} | | | 50 | ns | $C_L = 15\text{ pF}$, $ V_{ID} \geq 1.5\text{ V}$, $V_{CM} = 1.5\text{ V}$, see Figure 40 |
| Enable to Output High | t_{RZH} | | 10 | 50 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, $ V_{ID} \geq 1.5\text{ V}$, DE high, see Figure 42 |
| Enable to Output Low | t_{RZL} | | 10 | 50 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, $ V_{ID} \geq 1.5\text{ V}$, DE high, see Figure 42 |
| Disable Time from Low | t_{RLZ} | | 10 | 50 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, $ V_{ID} \geq 1.5\text{ V}$, see Figure 42 |
| Disable Time from High | t_{RHZ} | | 10 | 50 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, $ V_{ID} \geq 1.5\text{ V}$, see Figure 42 |
| Enable from Shutdown to High | $t_{RZH(SHDN)}^3$ | | | 2000 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, $ V_{ID} \geq 1.5\text{ V}$, see Figure 41 |
| Enable from Shutdown to Low | $t_{RZL(SHDN)}^3$ | | | 2000 | ns | $R_L = 1\text{ k}\Omega$, $C_L = 15\text{ pF}$, $ V_{ID} \geq 1.5\text{ V}$, see Figure 41 |
| TIME TO SHUTDOWN | t_{SHDN}^4 | 40 | | | ns | |

¹ Maximum data rate assumes a ratio of $t_{DR}:t_{BIT}:t_{DF}$ equal to 1:0.5:1.

² $t_{DZH(SHDN)}$ and $t_{DZL(SHDN)}$ refer to the time for the device to enable when \overline{RE} changes from 0 V to V_{CC} . $\overline{RE} = V_{CC}$ for this condition.

³ $t_{RZH(SHDN)}$ and $t_{RZL(SHDN)}$ refer to the time for the device to enable when \overline{RE} changes from V_{CC} to 0 V. $DE = 0\text{ V}$ for this condition.

⁴ Minimum time required to put the device into shutdown: DE and \overline{RE} must be disabled for more than 40 ns for the device to go into shutdown.

ADM3065E/ADM3066E/ADM3067E

$V_{CC} = 3.0\text{ V to }5.5\text{ V}$, $V_{IO} = 1.62\text{ V to }V_{CC}$, $T_A = T_{MIN} (-40^\circ\text{C})$ to $T_{MAX} (+125^\circ\text{C})$, unless otherwise noted. All typical specifications are at $T_A = 25^\circ\text{C}$, $V_{IO} = V_{CC} = 3.3\text{ V}$, unless otherwise noted.

Table 4.

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|-----------------------------------|----------------------|-----|-----|------|------|--|
| DRIVER | | | | | | |
| Maximum Data Rate ¹ | | 50 | | | Mbps | |
| Propagation Delay | t_{DPLH}, t_{DPHL} | | 9 | 15 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 38 |
| Skew | t_{DSKEW} | | 1 | 2 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 38 |
| Rise/Fall Times | t_{DR}, t_{DF} | | 4 | 6.7 | ns | $R_{LDIFF} = 54\ \Omega$, $C_{L1} = C_{L2} = 100\text{ pF}$, see Figure 38 |
| Enable to Output High | t_{DZH} | | 10 | 30 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Enable to Output Low | t_{DZL} | | 10 | 30 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Disable Time from Low | t_{DLZ} | | 10 | 30 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Disable Time from High | t_{DHZ} | | 10 | 30 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Enable Time from Shutdown to High | $t_{DZH(SHDN)}^2$ | | | 2000 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |
| Enable Time from Shutdown to Low | $t_{DZL(SHDN)}^2$ | | | 2000 | ns | $R_L = 110\ \Omega$, $C_L = 50\text{ pF}$, see Figure 39 |

| Parameter | Symbol | Min | Typ | Max | Unit | Test Conditions/Comments |
|------------------------------|----------------------|-----|-----|------|------|--|
| RECEIVER | | | | | | |
| Maximum Data Rate | | 50 | | | Mbps | |
| Propagation Delay | t_{RPLH}, t_{RPHL} | | | 35 | ns | $C_L = 15 \text{ pF}, V_{ID} \geq 1.5 \text{ V}$, see Figure 40 |
| Skew/Pulse Width Distortion | t_{RSKEW} | | | 3 | ns | $C_L = 15 \text{ pF}, V_{ID} \geq 1.5 \text{ V}, V_{CM} = 1.5 \text{ V}$, see Figure 40 |
| Enable to Output High | t_{RZH} | | 10 | 35 | ns | $R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}, V_{ID} \geq 1.5 \text{ V}$, DE high, see Figure 42 |
| Enable to Output Low | t_{RZL} | | 10 | 35 | ns | $R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}, V_{ID} \geq 1.5 \text{ V}$, DE high, see Figure 42 |
| Disable Time from Low | t_{RLZ} | | 10 | 35 | ns | $R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}, V_{ID} \geq 1.5 \text{ V}$, see Figure 42 |
| Disable Time from High | t_{RHZ} | | 10 | 35 | ns | $R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}, V_{ID} \geq 1.5 \text{ V}$, see Figure 42 |
| Enable from Shutdown to High | $t_{RZH(SHDN)}^3$ | | | 2000 | ns | $R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}, V_{ID} \geq 1.5 \text{ V}$, see Figure 41 |
| Enable from Shutdown to Low | $t_{RZL(SHDN)}^3$ | | | 2000 | ns | $R_L = 1 \text{ k}\Omega, C_L = 15 \text{ pF}, V_{ID} \geq 1.5 \text{ V}$, see Figure 41 |
| TIME TO SHUTDOWN | t_{SHDN}^4 | 40 | | | ns | |

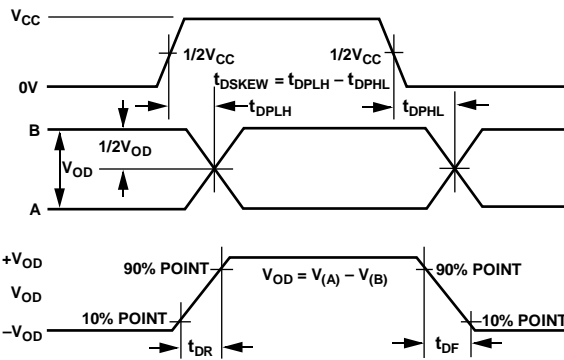
¹ Maximum data rate assumes a ratio of $t_{DR}:t_{BIT}:t_{DF}$ equal to 1:1:1.

² $t_{DZH(SHDN)}$ and $t_{DZL(SHDN)}$ refer to the time for the device to enable when \overline{DE} changes from 0 V to V_{CC} . $\overline{RE} = V_{CC}$ for this condition.

³ $t_{RZH(SHDN)}$ and $t_{RZL(SHDN)}$ refer to the time for the device to enable when \overline{RE} changes from V_{CC} to 0 V. $DE = 0 \text{ V}$ for this condition.

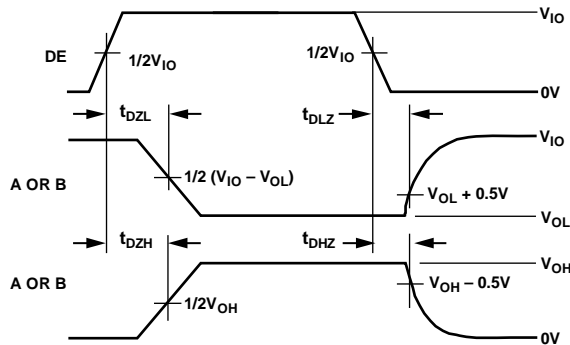
⁴ Minimum time required to put the device into shutdown: \overline{DE} and \overline{RE} must be disabled for more than 40 ns for the device to go into shutdown.

Timing Diagrams



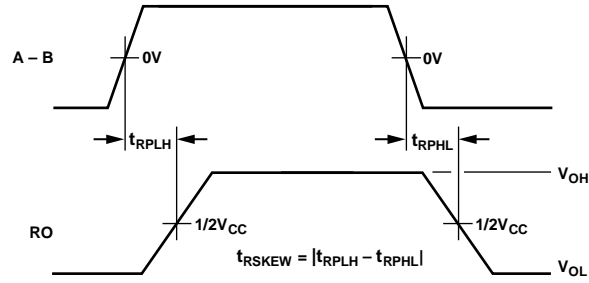
- NOTES**
- V_{OD} IS THE DIFFERENCE BETWEEN A AND B, WITH $+V_{OD}$ BEING THE MAXIMUM POINT OF V_{OD} , AND $-V_{OD}$ BEING THE MINIMUM POINT OF V_{OD} .
 - $V_{CC} = V_{IO}$ FOR ADM3062E/ADM3066E.

Figure 4. Driver Propagation Delay Rise and Fall Timing Diagram



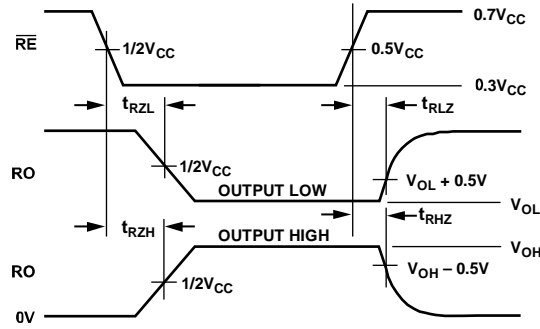
- NOTES**
- $V_{CC} = V_{IO}$ FOR ADM3062E/ADM3066E.

Figure 5. Driver Enable and Disable Timing Diagram



NOTES
1. $V_{CC} = V_{IO}$ FOR ADM3062E/ADM3066E.

Figure 6. Receiver Propagation Delay Timing Diagram



NOTES
1. $V_{CC} = V_{IO}$ FOR ADM3062E/ADM3066E.

Figure 7. Receiver Enable and Disable Timing Diagram

ABSOLUTE MAXIMUM RATINGS

Table 5.

| Parameter | Rating |
|--|-----------------------------------|
| V _{CC} to GND | 6V |
| V _{IO} to GND | −0.3 V to +6 V |
| Digital Input and Output Voltage (DE, $\overline{\text{RE}}$, DI, and RO) | −0.3 V to V _{CC} + 0.3 V |
| Driver Output and Receiver Input Voltage | −9 V to +14 V |
| Operating Temperature Ranges | −40°C to +85°C −40°C to +125°C |
| Storage Temperature Range | −65°C to +150°C |
| Continuous Total Power Dissipation | |
| 8-Lead SOIC_N | 0.225 W |
| 8-Lead MSOP | 0.151 W |
| 10-Lead MSOP | 0.151 W |
| 10-Lead LFCSP | 0.450 W |
| 14-Lead SOIC_N | 0.239 W |
| Maximum Junction Temperature | 150°C |
| Lead Temperature | |
| Soldering (10 sec) | 300°C |
| Vapor Phase (60 sec) | 215°C |
| Infrared (15 sec) | 220°C |
| ESD on the Bus Pins (A, B, Y, Z) | |
| IEC 61000-4-2 Contact Discharge | ±12 kV |
| IEC 61000-4-2 Air Discharge | |
| 10 Positive and 10 Negative Discharges | ±12 kV |
| Three Positive or Three Negative Discharges | ±15 kV |
| ESD Human Body Model (HBM) | |
| On the Bus Pins (A, B, Y, Z) | ≥ ±30 kV |
| All Other Pins | ±8 kV |

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required. θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 6. Thermal Resistance

| Package Type | θ_{JA} ¹ | θ_{JC} ¹ | Unit |
|--------------|----------------------------|----------------------------|------|
| R-8 | 110.88 | 58.63 | °C/W |
| RM-8 | 165.69 | 49.61 | °C/W |
| RM-10 | 165.69 | 49.61 | °C/W |
| R-14 | 104.5 | 42.90 | °C/W |
| CP-10-9 | 55.65 | 33.22 | °C/W |

¹ Thermal impedance simulated values are based on JEDEC 2S2P thermal test board with no bias. See JEDEC JESD-51.

ESD CAUTION



ESD (electrostatic discharge) sensitive device.

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

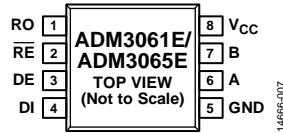


Figure 8. ADM3061E/ADM3065E 8-Lead Narrow Body SOIC_N Pin Configuration

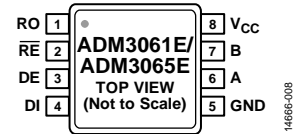


Figure 9. ADM3061E/ADM3065E 8-Lead MSOP Pin Configuration

Table 7. ADM3061E/ADM3065E Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-----------------|---|
| 1 | RO | Receiver Output Data. This output is high when $(A - B) \geq -30$ mV and low when $(A - B) \leq -200$ mV. This output is tristated when the receiver is disabled; that is, when \overline{RE} is driven high. |
| 2 | \overline{RE} | Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver. |
| 3 | DE | Driver Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state. |
| 4 | DI | Transmit Data Input. Data transmitted by the driver is applied to this input. |
| 5 | GND | Ground. |
| 6 | A | Noninverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus. |
| 7 | B | Inverting Driver Output and Receiver Input. When the driver is disabled, or when V_{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus. |
| 8 | V_{CC} | 3.0V to 5.5V Power Supply. Adding a 0.1 μ F decoupling capacitor between the V_{CC} pin and the GND pin is recommended. |

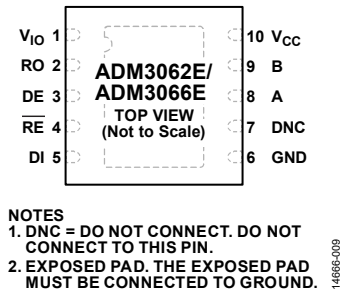


Figure 10. ADM3062E/ADM3066E 10-Lead LFCSP Pin Configuration

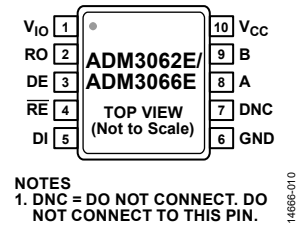


Figure 11. ADM3062E/ADM3066E 10-Lead MSOP Pin Configuration

Table 8. ADM3066E/ADM3062E Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|-------------------------|---|
| 1 | V _{IO} | 1.62 V to 5.5 V Logic Supply. Adding a 0.1 μF decoupling capacitor between the V _{IO} pin and the GND pin is recommended. |
| 2 | RO | Receiver Output Data. This output is high when (A – B) ≥ –30 mV and low when (A – B) ≤ –200 mV. This output is tristated when the receiver is disabled; that is, when RE is driven high. |
| 3 | DE | Driver Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state. |
| 4 | RE | Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver. |
| 5 | DI | Transmit Data Input. Data transmitted by the driver is applied to this input. |
| 6 | GND | Ground. |
| 7 | DNC | Do Not Connect. Do not connect to this pin. |
| 8 | A | Noninverting Driver Output and Receiver Input. When the driver is disabled, or when V _{CC} is powered down, Pin A is put into a high impedance state to avoid overloading the bus. |
| 9 | B | Inverting Driver Output and Receiver Input. When the driver is disabled, or when V _{CC} is powered down, Pin B is put into a high impedance state to avoid overloading the bus. |
| 10 | V _{CC} EPAD | 3.0V to 5.5V Power Supply. Adding a 0.1 μF decoupling capacitor between the V _{CC} pin and the GND pin is recommended. Exposed Pad. The exposed pad must be connected to ground for the LFCSP package. |

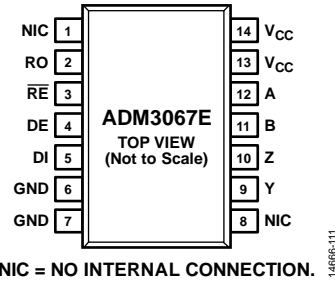


Figure 12. ADM3067E 14-Lead SOIC Pin Configuration

Table 9. ADM3067E Pin Function Descriptions

| Pin No. | Mnemonic | Description |
|---------|------------------------|--|
| 1 | NIC | No Internal Connection. This pin is not internally connected. |
| 2 | RO | Receiver Output Data. This output is high when $(A - B) \geq -30$ mV and low when $(A - B) \leq -200$ mV. This output is tristated when the receiver is disabled; that is, when RE is driven high. |
| 3 | $\overline{\text{RE}}$ | Receiver Enable Input. This is an active low input. Driving this input low enables the receiver, and driving it high disables the receiver. |
| 4 | DE | Driver Enable. A high level on this pin enables the driver differential outputs, A and B. A low level places the driver output into a high impedance state. |
| 5 | DI | Transmit Data Input. Data transmitted by the driver is applied to this input. |
| 6, 7 | GND | Ground. |
| 8 | NIC | No Internal Connection. This pin is not internally connected. |
| 9 | Y | Driver Noninverting Output. When the driver is disabled, or when V _{CC} is powered down, Pin Y is put into a high impedance state to avoid overloading the bus. |
| 10 | Z | Driver Inverting Output. When the driver is disabled, or when V _{CC} is powered down, Pin Z is put into a high impedance state to avoid overloading the bus. |
| 11 | B | Inverting Receiver Input. |
| 12 | A | Noninverting Receiver Input. |
| 13, 14 | V _{CC} | 3.0V to 5.5V Power Supply. Adding a 0.1 μF decoupling capacitor between the V _{CC} pin and the GND pin is recommended. |

TYPICAL PERFORMANCE CHARACTERISTICS

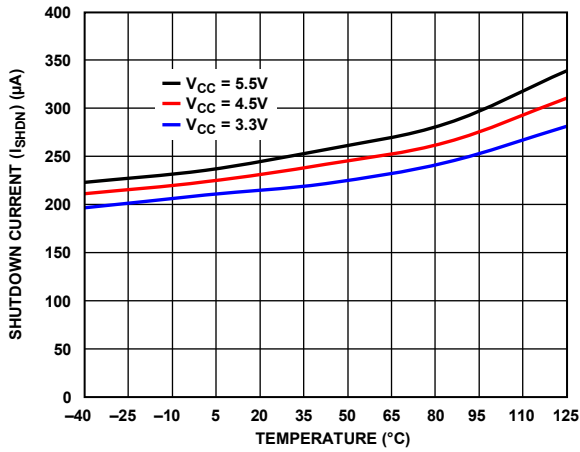


Figure 13. Shutdown Current (I_{SHDN}) vs. Temperature

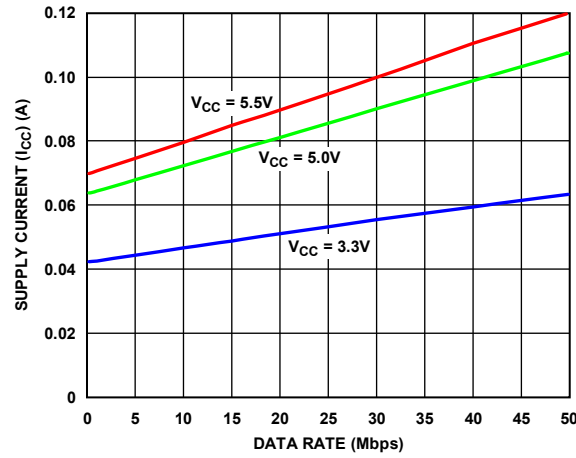


Figure 16. Supply Current (I_{CC}) vs. Data Rate with 54 Ω Load Resistance

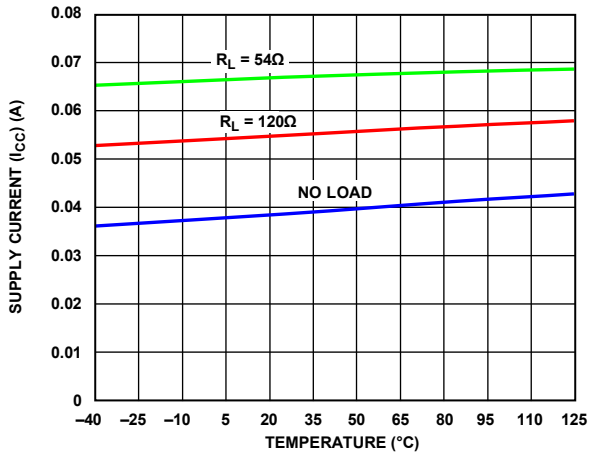


Figure 14. Supply Current (I_{CC}) vs. Temperature, Data Rate = 50 Mbps, $V_{CC} = 3.3 V$

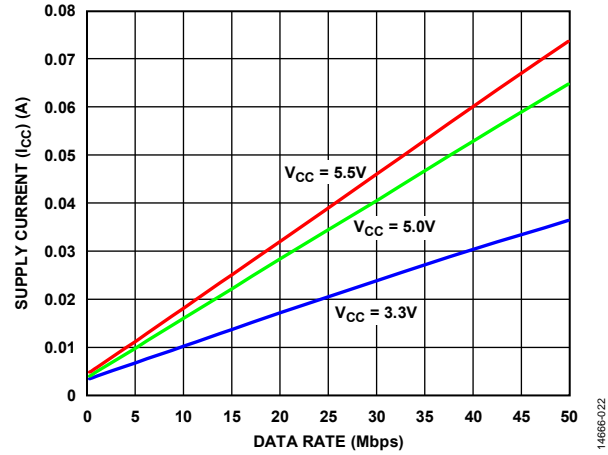


Figure 17. Supply Current (I_{CC}) vs. Data Rate with No Load Resistance

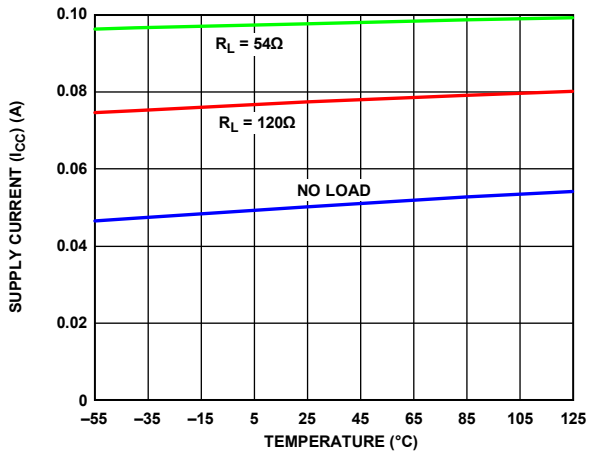


Figure 15. Supply Current (I_{CC}) vs. Temperature, Data Rate = 50 Mbps, $V_{CC} = 5.0 V$

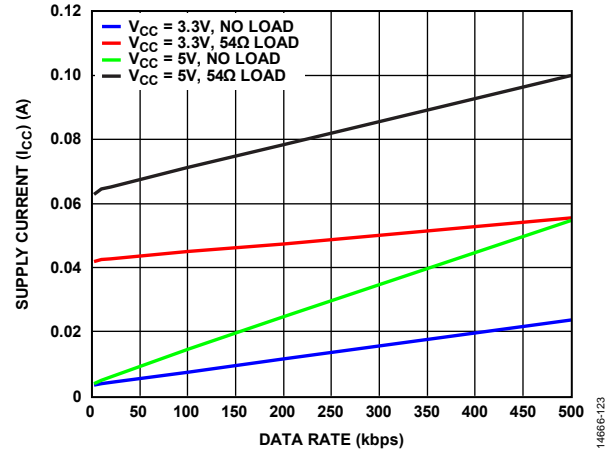


Figure 18. Supply Current (I_{CC}) vs. Data Rate with 54 Ω Load Resistance and No Load Resistance

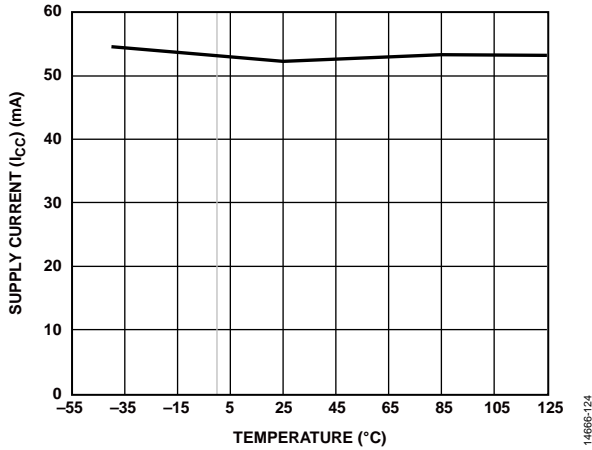


Figure 19. Supply Current (I_{CC}) vs. Temperature, Data Rate = 500 kbps, $V_{CC} = 3.0V$

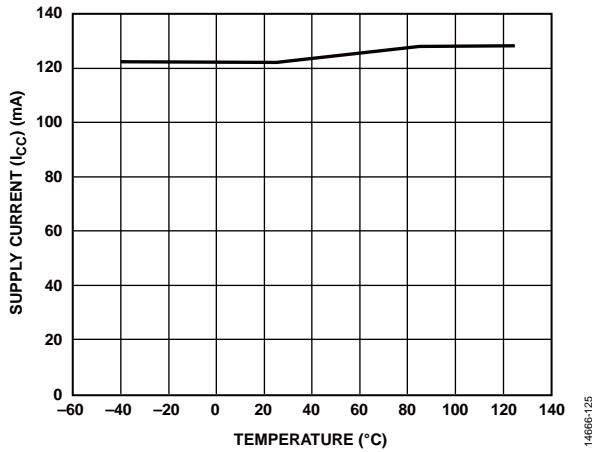


Figure 20. Supply Current (I_{CC}) vs. Temperature, Data Rate = 500 kbps, $V_{CC} = 5.5V$

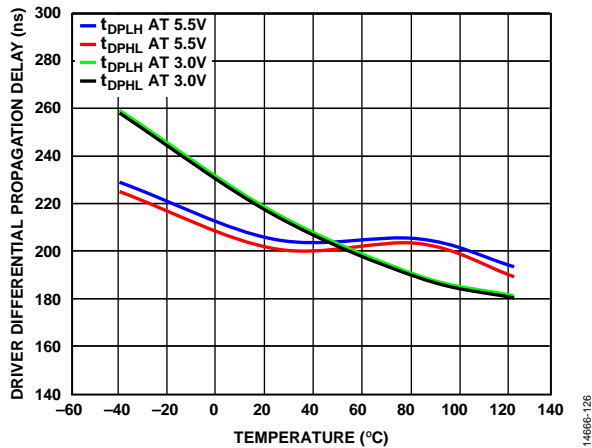


Figure 21. Driver Differential Propagation Delay vs. Temperature, 500 kbps Models

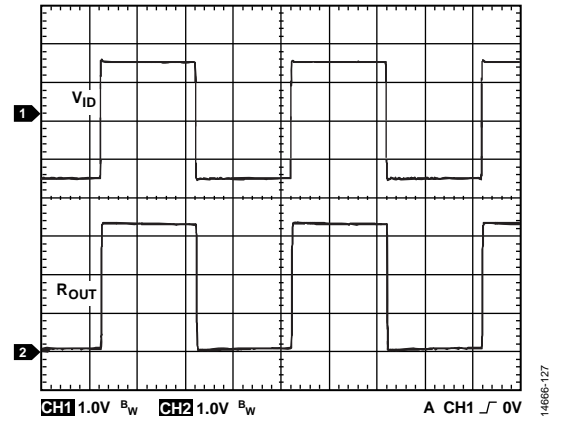


Figure 22. Receiver Propagation Delay (Oscilloscope Plot), Data Rate = 500 kbps, $V_{ID} \geq 1.5V$

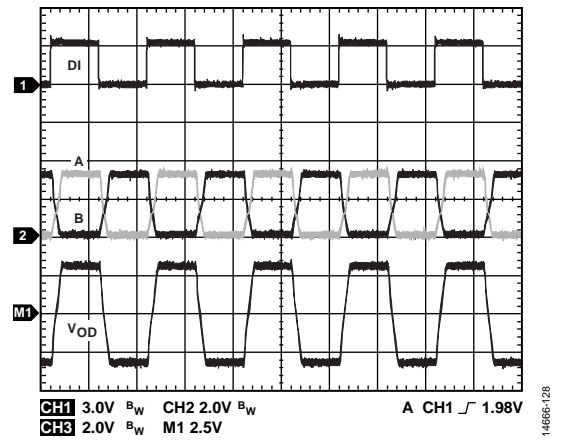


Figure 23. Driver Propagation Delay (Oscilloscope Plot), Data Rate = 500 kbps

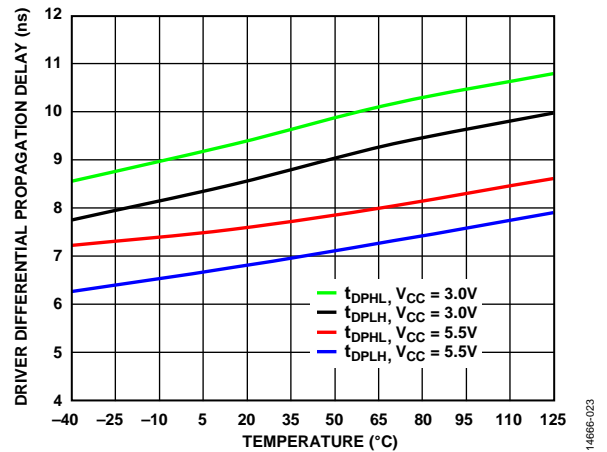


Figure 24. Driver Differential Propagation Delay vs. Temperature, 50 Mbps

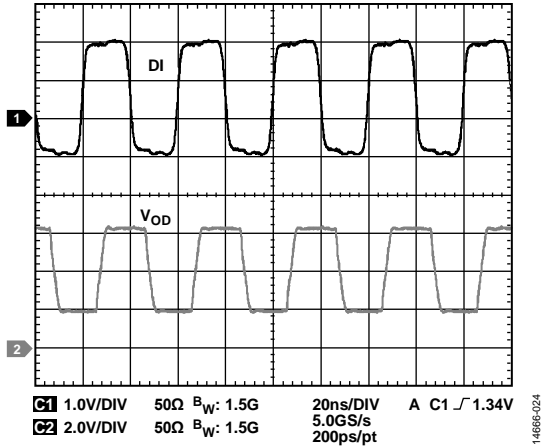


Figure 25. Driver Propagation Delay at 50 Mbps

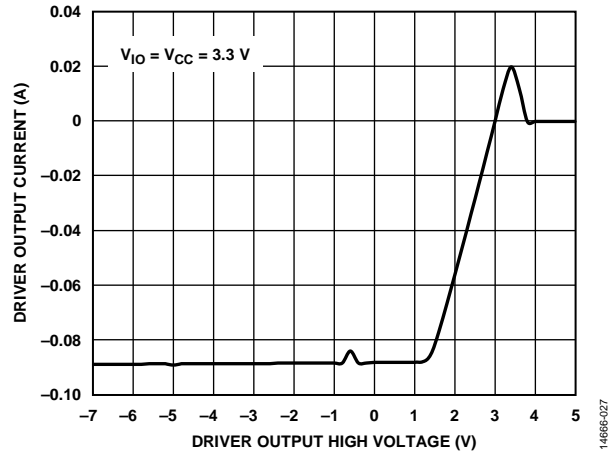


Figure 28. Driver Output Current vs. Driver Output High Voltage

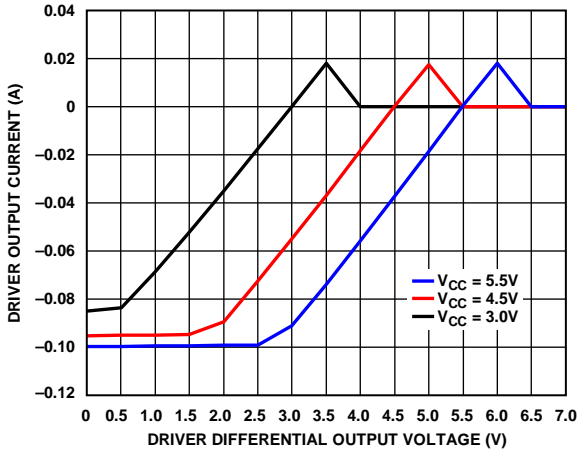


Figure 26. Driver Output Current vs. Driver Differential Output Voltage

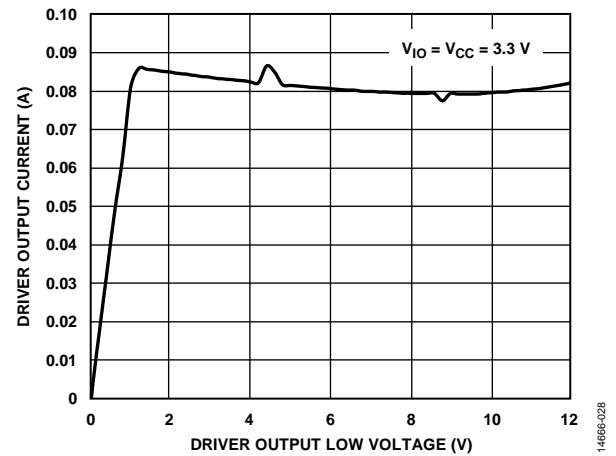


Figure 29. Driver Output Current vs. Driver Output Low Voltage

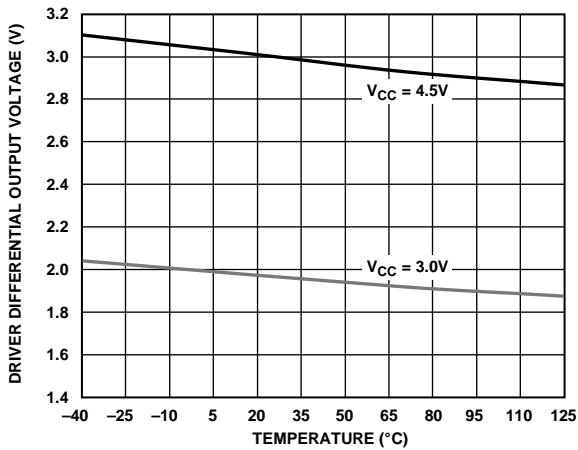


Figure 27. Driver Differential Output Voltage vs. Temperature

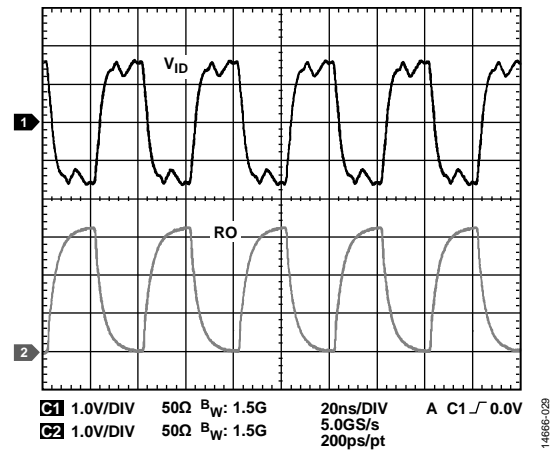


Figure 30. Receiver Propagation Delay at 50 Mbps, $|V_{ID}| \geq 1.5$ V

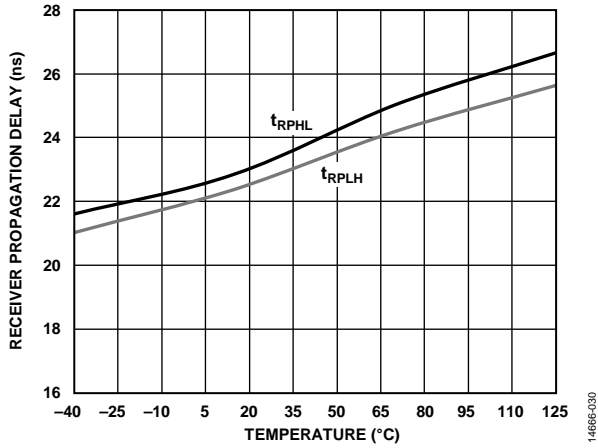


Figure 31. Receiver Propagation Delay vs. Temperature, 50 Mbps

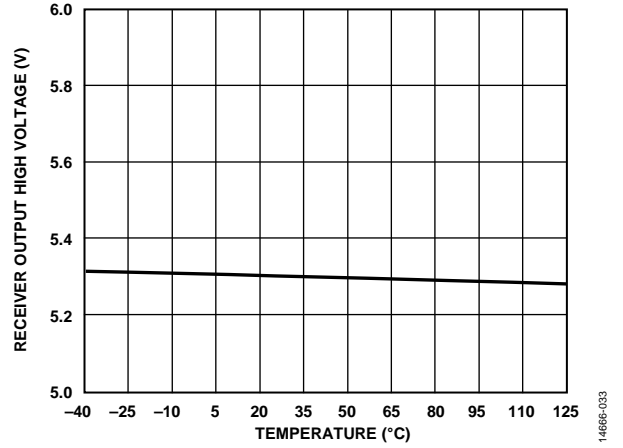


Figure 34. Receiver Output High Voltage vs. Temperature

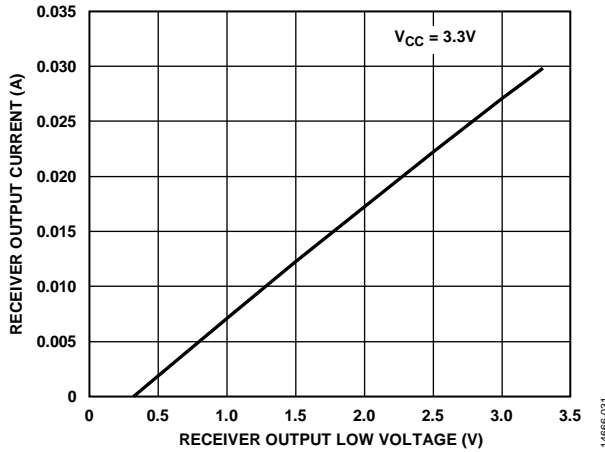


Figure 32. Receiver Output Current vs. Receiver Output Low Voltage ($V_{CC} = 3.3V$)

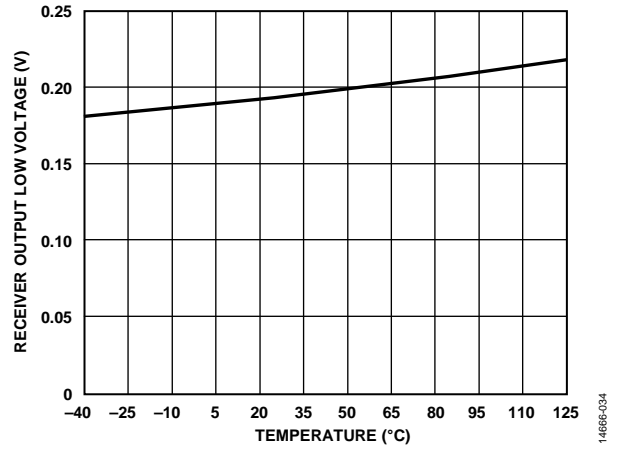


Figure 35. Receiver Output Low Voltage vs. Temperature

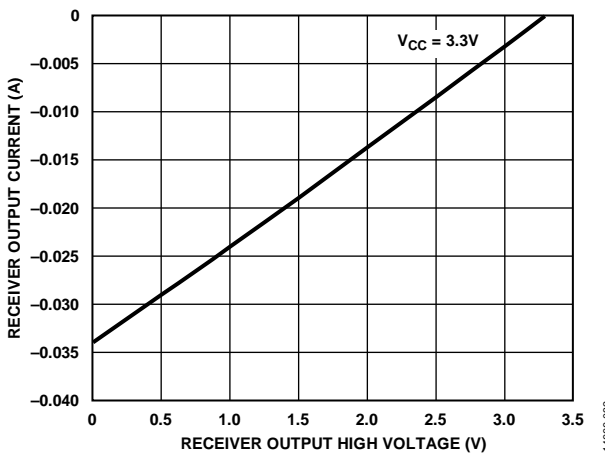


Figure 33. Receiver Output Current vs. Receiver Output High Voltage ($V_{CC} = 3.3V$)

TEST CIRCUITS

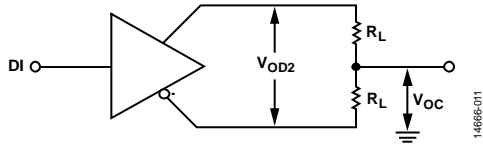


Figure 36. Driver Voltage Measurements

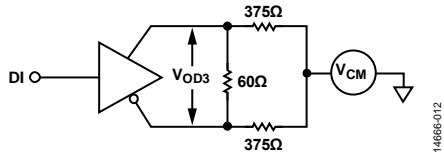


Figure 37. Driver Voltage Measurements over Common-Mode Range

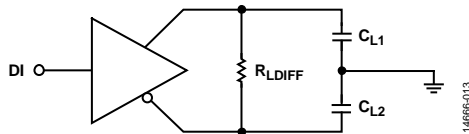
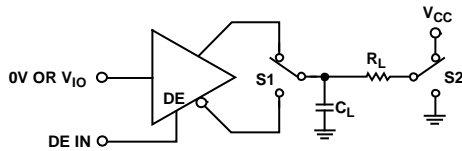


Figure 38. Driver Propagation Delay



NOTES
1. $V_{IO} = V_{CC}$ FOR ADM3061E/ADM3065E/ADM3067E.

Figure 39. Driver Enable/Disable

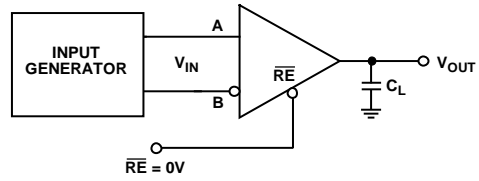
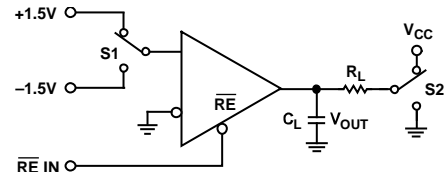
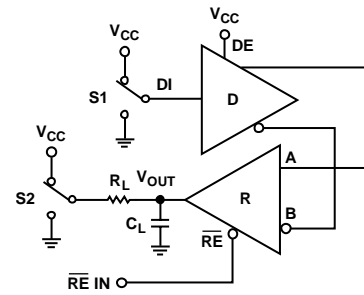


Figure 40. Receiver Propagation Delay/Skew



NOTES
1. $V_{CC} = V_{IO}$ FOR ADM3062E/ADM3066E.

Figure 41. Receiver Enable/Disable from Shutdown



NOTES
1. $V_{CC} = V_{IO}$ FOR ADM3062E/ADM3066E.

Figure 42. Receiver Enable/Disable

THEORY OF OPERATION

IEC ESD PROTECTED RS-485

The ADM3065E/ADM3066E/ADM3067E are 3.0 V to 5.5 V, 50 Mbps RS-485 transceivers with IEC 61000-4-2 Level 4 ESD protection on the bus pins. The ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E can withstand up to ± 12 kV contact discharge on transceiver bus pins (A and B) without latch-up or damage. The ADM3061E/ADM3062E has the same robust IEC 61000-4-2 ESD protection as the ADM3065E/ADM3066E/ADM3067E models and operate at a lower 500 kbps data rate.

HIGH DRIVER DIFFERENTIAL OUTPUT VOLTAGE

The ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E have characteristics optimized for use in PROFIBUS applications. When powered at $V_{CC} \geq 4.5$ V, the ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E driver output differential voltage meets or exceeds the PROFIBUS requirements of 2.1 V with a 54 Ω load.

IEC 61000-4-2 ESD PROTECTION

ESD is the sudden transfer of electrostatic charge between bodies at different potentials caused by near contact or induced by an electric field. It has the characteristics of high current in a short time period. The primary purpose of the IEC 61000-4-2 test is to determine the immunity of systems to external ESD events outside the system during operation. IEC 61000-4-2 describes testing using two coupling methods: contact discharge and air discharge. Contact discharge implies a direct contact between the discharge gun and the equipment under test (EUT). During air discharge testing, the charged electrode of the discharge gun is moved toward the EUT until a discharge occurs as an arc across the air gap. The discharge gun does not make direct contact with the EUT. A number of factors affect the results and repeatability of the air discharge test, including humidity, temperature, barometric pressure, distance, and rate of approach to the EUT. This method is a more accurate representation of an actual ESD event but is not as repeatable. Therefore, contact discharge is the preferred test method.

During testing, the data port is subjected to at least 10 positive and 10 negative single discharges. Selection of the test voltage is dependent on the system end environment.

Figure 43 shows the 8 kV contact discharge current waveform as described in the IEC 61000-4-2 specification. Some of the key waveform parameters are rise times of less than 1 ns and pulse widths of approximately 60 ns.

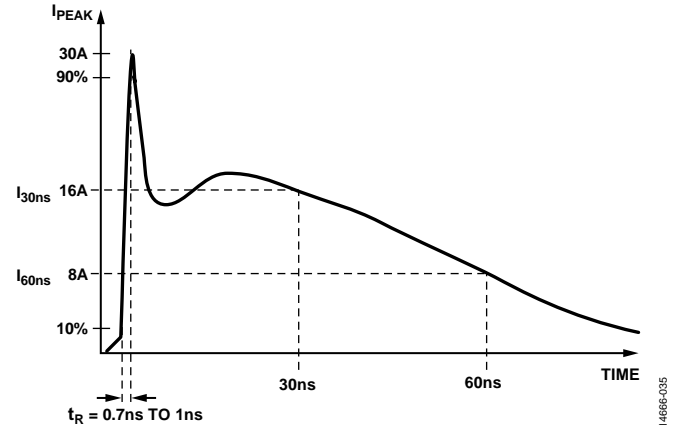


Figure 43. IEC 61000-4-2 ESD Waveform (8 kV)

Figure 44 shows the 8 kV contact discharge current waveform from the IEC 61000-4-2 standard compared to the HBM ESD 8 kV waveform. Figure 44 shows that the two standards specify a different waveform shape and peak current. The peak current associated with an IEC 61000-4-2 8 kV pulse is 30 A, whereas the corresponding peak current for HBM ESD is more than five times less, at 5.33 A. The other difference is the rise time of the initial voltage spike, with the IEC 61000-4-2 ESD waveform having a much faster rise time of 1 ns, compared to the 10 ns associated with the HBM ESD waveform. The amount of power associated with an IEC ESD waveform is much greater than that of an HBM ESD waveform. The HBM ESD standard requires the EUT to be subjected to three positive and three negative discharges, whereas the IEC ESD standard requires 10 positive and 10 negative discharge tests.

The ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E with IEC 61000-4-2 ESD ratings is better suited for operation in harsh environments compared to other RS-485 transceivers that state varying levels of HBM ESD protection.

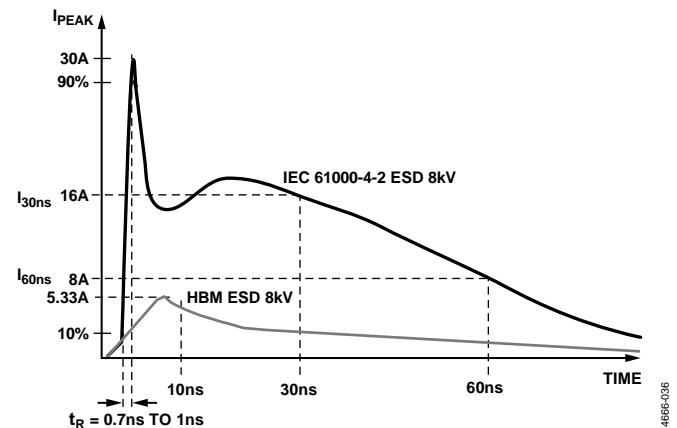


Figure 44. IEC 61000-4-2 ESD Waveform 8 kV Compared to HBM ESD Waveform 8 kV

TRUTH TABLES

Table 10. Transmitting Truth Table

| Supply Status | | Inputs | | | Outputs | |
|------------------------------|-----------------|----------------|----------------|----------------|---------------------|---------------------|
| V _{IO} ¹ | V _{CC} | RE | DE | DI | A/Y | B/Z |
| On | On | X ² | 1 | 1 | 1 | 0 |
| On | On | X ² | 1 | 0 | 0 | 1 |
| On | On | 0 | 0 | X ² | High-Z ³ | High-Z ³ |
| On | On | 1 | 0 | X ² | High-Z ³ | High-Z ³ |
| On | Off | X ² | 1 | 1 | I ⁴ | I ⁴ |
| On | Off | X ² | 1 | 0 | I ⁴ | I ⁴ |
| On | Off | X ² | 0 | X ² | I ⁴ | I ⁴ |
| Off | On | X ² | X ² | X ² | High-Z ³ | High-Z ³ |
| Off | Off | X ² | X ² | X ² | High-Z ³ | High-Z ³ |

¹ For the ADM3061E, ADM3065E, and ADM3067E, the V_{IO} pin is not applicable.

² X means don't care.

³ High-Z means high impedance.

⁴ I means indeterminate.

Table 11. Receiving Truth Table

| Supply Status | | Inputs | | | Outputs |
|------------------------------|-----------------|--------------------------|----------------|----------------|---------------------|
| V _{IO} ¹ | V _{CC} | A – B | RE | DE | RO |
| On | On | >–0.03 V | 0 | X ² | 1 |
| On | On | <–0.2 V | 0 | X ² | 0 |
| Off | On | >–0.03 V | 0 | X ² | I ⁴ |
| Off | On | <–0.2 V | 0 | X ² | I ⁴ |
| On | On | –0.2 V ≤ A – B ≤ –0.03 V | 0 | X ² | I ⁴ |
| Off | On | –0.2 V ≤ A – B ≤ –0.03 V | 0 | X ² | I ⁴ |
| On | On | Inputs open/shorted | 0 | X ² | 1 |
| Off | On | Inputs open/shorted | 0 | X ² | High-Z ³ |
| On | On | X ² | 1 | X ² | High-Z ³ |
| On | On | X ² | 1 | 0 | Shutdown |
| Off | On | X ² | 1 | X ² | I ⁴ |
| Off | Off | X ² | X ² | X ² | High-Z ³ |

¹ For the ADM3061E, ADM3065E, and ADM3067E, the V_{IO} pin is not applicable.

² X means don't care.

³ High-Z means high impedance.

⁴ I means indeterminate.

RECEIVER FAIL-SAFE

The ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E guarantee a logic high receiver output when the receiver inputs are shorted, open, or connected to a terminated transmission line with all drivers disabled; set the receiver input threshold between –30 mV and –200 mV. If the differential receiver input voltage (A – B) is greater than or equal to –30 mV, the RO pin is logic high.

If the A – B input is less than or equal to –200 mV, RO is logic low. In the case of a terminated bus with all transmitters disabled, the receiver differential input voltage is pulled to 0 V by the termination, resulting in a logic high with a 30 mV minimum noise margin.

HOT SWAP CAPABILITY

When a circuit board is inserted into a powered (or hot) backplane, differential disturbances to the data bus can lead to data errors. During this period, processor logic output drivers are high impedance and are unable to drive the DE and RE inputs of the RS-485 transceivers to a defined logic level. Leakage currents up to ±10 μA from the high impedance state of the processor logic drivers can cause standard complementary metal-oxide semiconductor (CMOS) enable inputs of a transceiver to drift to an incorrect logic level. Additionally, parasitic circuit board capacitance can cause coupling of V_{CC} or GND to the enable inputs. Without the hot swap capability, these factors can improperly enable the driver or receiver of the transceiver. When V_{CC} or V_{IO} rises, an internal pull-down circuit holds DE low and RE high. After the initial power-up sequence, the pull-down circuit becomes transparent resetting the hot swap tolerable input.

128 TRANSCEIVERS ON THE BUS

The standard RS-485 receiver input impedance is 12 kΩ (one unit load), and the standard driver can drive up to 32 unit loads. The ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E transceivers have a one fourth unit load receiver input impedance (48 kΩ), allowing up to 128 transceivers to be connected in parallel on one communication line. Any combination of these devices and other RS-485 transceivers with a total of 32 unit loads or fewer can be connected to the line.

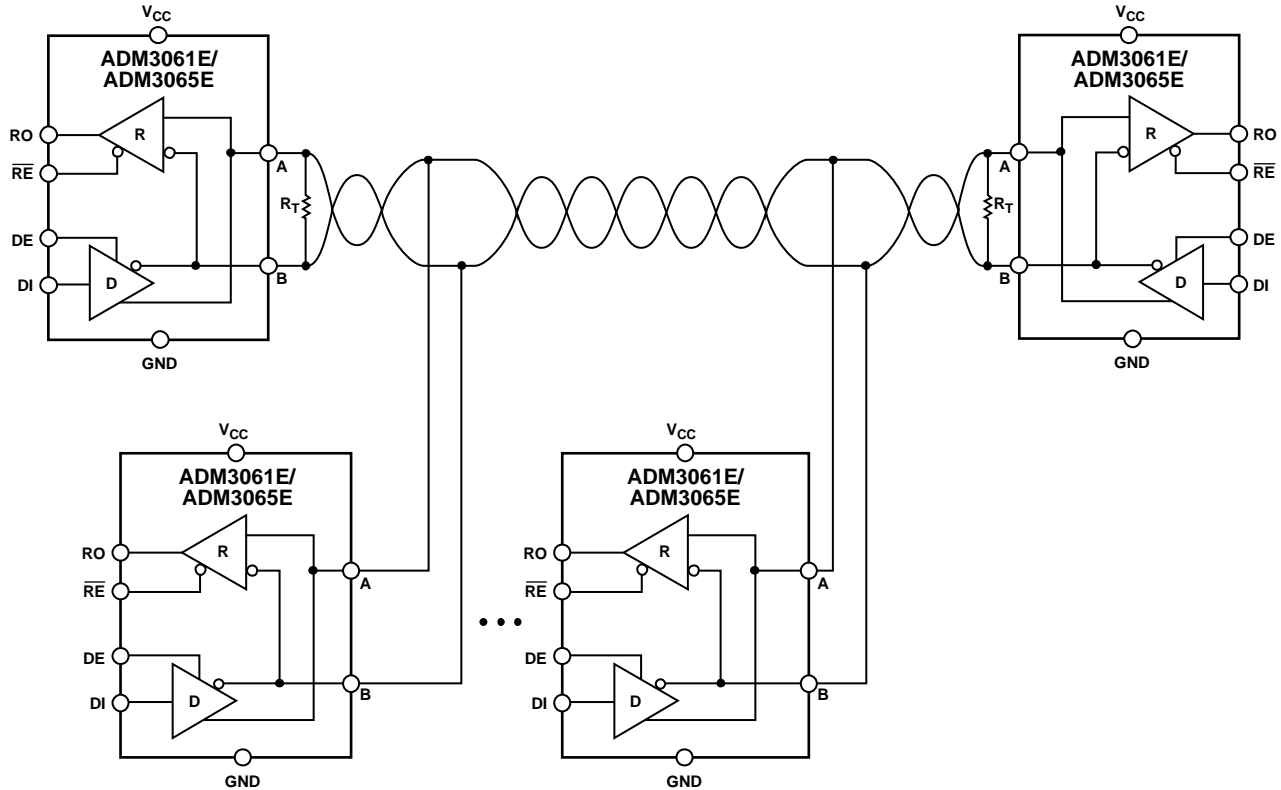
DRIVER OUTPUT PROTECTION

The ADM3061E/ADM3062E/ADM3065E/ADM3066E/ADM3067E feature two methods to prevent excessive output current and power dissipation caused by faults or by bus contention. Current-limit protection on the output stage provides immediate protection against short circuits over the whole common-mode voltage range. In addition, a thermal shutdown circuit forces the driver outputs into a high impedance state if the die temperature rises excessively. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are reenabled at a temperature of 140°C.

APPLICATIONS INFORMATION

The ADM3061E/ADM3065E transceiver is designed for bidirectional data communications on multipoint bus transmission lines. Figure 45 shows a typical network applications circuit.

To minimize reflections, terminate the line at both ends with a termination resistor (the value of the termination resistor must be equal to the characteristic impedance of the cable used) and keep stub lengths off the main line as short as possible.



- NOTES**
1. THE MAXIMUM NUMBER OF NODES IS 128.
 2. R_T IS EQUAL TO THE CHARACTERISTIC IMPEDANCE OF THE CABLE USED.

Figure 45. ADM3061E/ADM3065E Typical Half-Duplex RS-485 Communications Network

14686-037

ISOLATED HIGH SPEED RS-485 NODE

Galvanic isolation, with reinforced insulation and 5 kV rms transient withstand voltage, can be added to the ADM3065E using Analog Devices, Inc., *iCoupler*® and *isoPower*® technology. The **ADuM6401** provides the required quad channels of 5 kV rms signal isolation, operating at rates up to 25 Mbps, together with an integrated dc-to-dc converter. The **ADuM6401** combines with the ADM3065E (shown in Figure 46) with the V_{ISO} pin configured for 3.3 V by connecting the V_{SEL} pin to GND_{ISO} and a 5 V supply connected to V_{DD1} . Operation at 3.3 V ensures the ADM3065E remains within the load capability of **ADuM6401** even at 25 Mbps.

Operation at 50 Mbps data rates with isolation of the ADM3065E can be implemented using the **ADuM241D** quad-channel digital isolator and the **ADuM6000** isolated dc-to-dc converter, as shown in Figure 47. The **ADuM241D** can operate at a data rate of up to 150 Mbps, offering the precise timing

required to fully support the ADM3065E at 50 Mbps. Operation of ADM3065E at 3.3 V allows operation at the 50 Mbps data rate.

If 5 V operation is desired, V_{SEL} on **ADuM6000** can be tied to V_{ISO} , and the maximum supported data rate becomes lower (for example, <10 Mbps). Refer to the Typical Performance Characteristics section, the **ADuM241D** data sheet, and the **ADuM6000** data sheet.

The dc-to-dc converters in the **ADuM6401** and **ADuM6000** *isoPower* devices provide regulated, isolated power to the ADM3065E (and the **ADuM241D**). These *isoPower* devices use high frequency switching elements to transfer power through their transformers. Take care during PCB layout to meet emissions standards. See the **AN-0971 Application Note** for PCB layout recommendations.

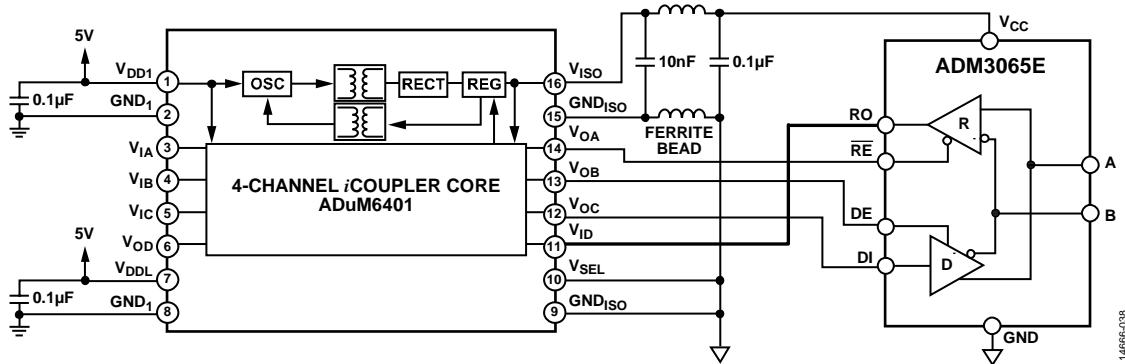


Figure 46. Signal and Power Isolated 25 Mbps RS-485 Solution (Simplified Diagram—All Connections Not Shown)

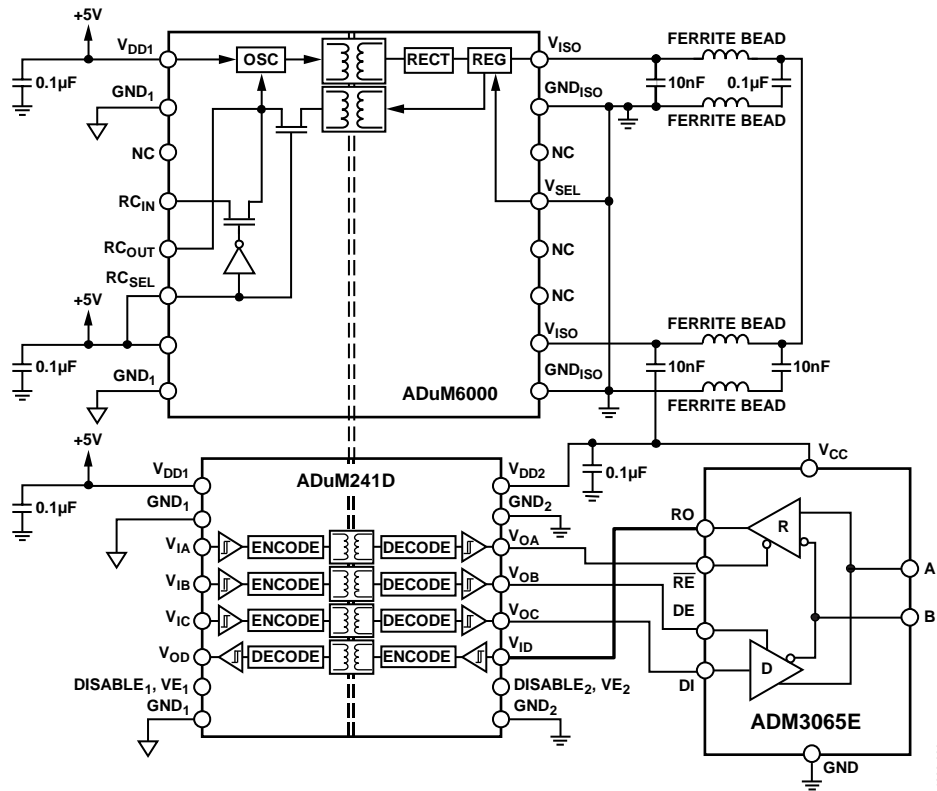
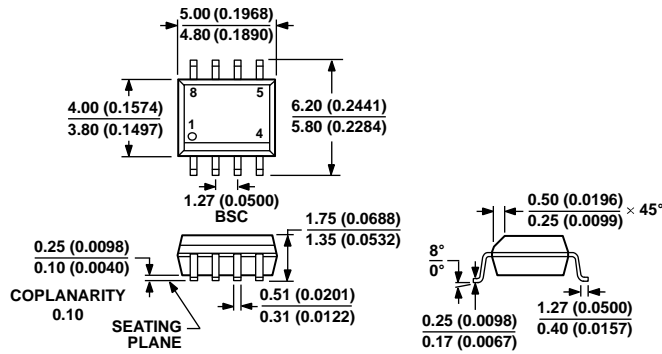


Figure 47. Signal and Power Isolated 50 Mbps RS-485 Solution (Simplified Diagram—All Connections Not Shown) Outline Dimensions

OUTLINE DIMENSIONS

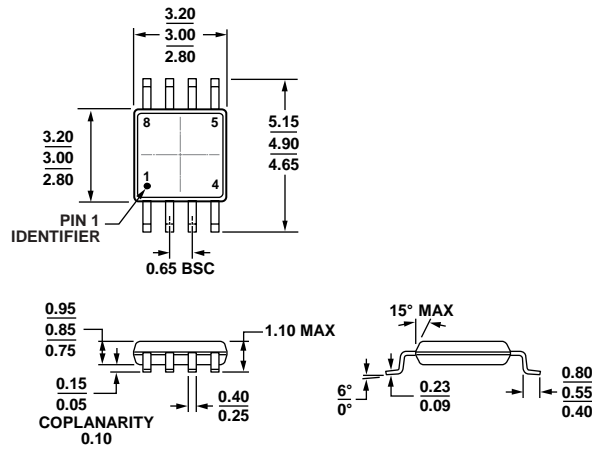


COMPLIANT TO JEDEC STANDARDS MS-012-AA
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 48. 8-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-8)

Dimensions shown in millimeters and (inches)

012407-A

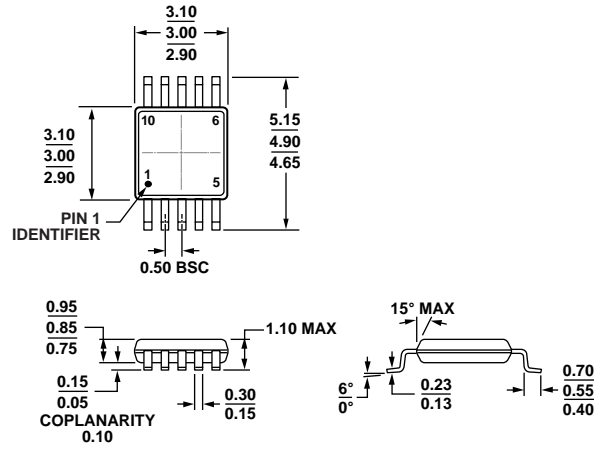


COMPLIANT TO JEDEC STANDARDS MO-187-AA

Figure 49. 8-Lead Mini Small Outline Package [MSOP]
 (RM-8)

Dimensions shown in millimeters

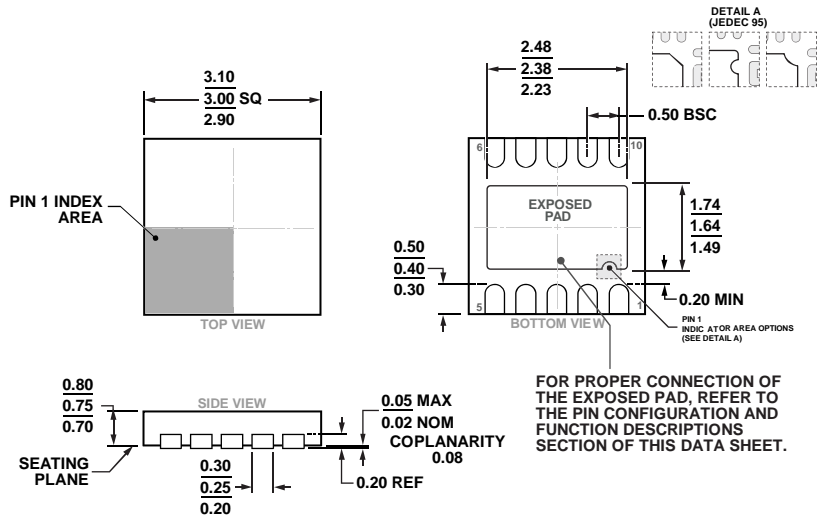
10-07-2008-B



COMPLIANT TO JEDEC STANDARDS MO-187-BA

Figure 50. 10-Lead Mini Small Outline Package [MSOP] (RM-10)

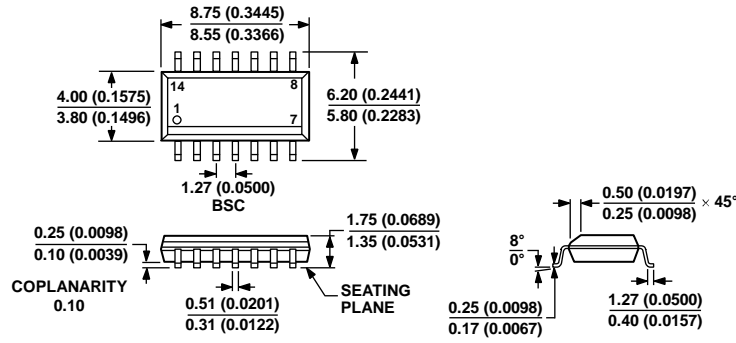
Dimensions shown in millimeters



FOR PROPER CONNECTION OF THE EXPOSED PAD, REFER TO THE PIN CONFIGURATION AND FUNCTION DESCRIPTIONS SECTION OF THIS DATA SHEET.

Figure 51. 10-Lead Lead Frame Chip Scale Package [LFCSP] 3 mm x 3 mm Body and 0.75 mm Package Height (CP-10-9)

Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-012-AB
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 52. 14-Lead Standard Small Outline Package [SOIC_N]
 Narrow Body
 (R-14)
 Dimensions shown in millimeters

060606-A

ORDERING GUIDE

| Model ¹ | Temperature Range | Package Description | Package Option | Marking Code |
|--------------------|-------------------|---|----------------|--------------|
| ADM3061EARZ | -40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADM3061EARZ-R7 | -40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADM3061EBRZ | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADM3061EBRZ-R7 | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADM3061EARMZ | -40°C to +85°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | MBY |
| ADM3061EARMZ-R7 | -40°C to +85°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | MBY |
| ADM3061EBRMZ | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | MC0 |
| ADM3061EBRMZ-R7 | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | MC0 |
| ADM3062EACPZ | -40°C to +85°C | 10-Lead Lead Frame Chip Scale Package [LFCSP] | CP-10-9 | MCC |
| ADM3062EACPZ-R7 | -40°C to +85°C | 10-Lead Lead Frame Chip Scale Package [LFCSP] | CP-10-9 | MCC |
| ADM3062EBCPZ | -40°C to +125°C | 10-Lead Lead Frame Chip Scale Package [LFCSP] | CP-10-9 | MCD |
| ADM3062EBCPZ-R7 | -40°C to +125°C | 10-Lead Lead Frame Chip Scale Package [LFCSP] | CP-10-9 | MCD |
| ADM3062EARMZ | -40°C to +85°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | MC7 |
| ADM3062EARMZ-R7 | -40°C to +85°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | MC7 |
| ADM3062EBRMZ | -40°C to +125°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | MC8 |
| ADM3062EBRMZ-R7 | -40°C to +125°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | MC8 |
| ADM3065EARZ | -40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADM3065EARZ-R7 | -40°C to +85°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADM3065EBRZ | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADM3065EBRZ-R7 | -40°C to +125°C | 8-Lead Standard Small Outline Package [SOIC_N] | R-8 | |
| ADM3065EARMZ | -40°C to +85°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | MC1 |
| ADM3065EARMZ-R7 | -40°C to +85°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | MC1 |
| ADM3065EBRMZ | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | MC2 |
| ADM3065EBRMZ-R7 | -40°C to +125°C | 8-Lead Mini Small Outline Package [MSOP] | RM-8 | MC2 |
| ADM3066EACPZ | -40°C to +85°C | 10-Lead Lead Frame Chip Scale Package [LFCSP] | CP-10-9 | MC9 |
| ADM3066EACPZ-R7 | -40°C to +85°C | 10-Lead Lead Frame Chip Scale Package [LFCSP] | CP-10-9 | MC9 |
| ADM3066EBCPZ | -40°C to +125°C | 10-Lead Lead Frame Chip Scale Package [LFCSP] | CP-10-9 | MCA |
| ADM3066EBCPZ-R7 | -40°C to +125°C | 10-Lead Lead Frame Chip Scale Package [LFCSP] | CP-10-9 | MCA |
| ADM3066EARMZ | -40°C to +85°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | MC4 |
| ADM3066EARMZ-R7 | -40°C to +85°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | MC4 |
| ADM3066EBRMZ | -40°C to +125°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | MC5 |
| ADM3066EBRMZ-R7 | -40°C to +125°C | 10-Lead Mini Small Outline Package [MSOP] | RM-10 | MC5 |
| ADM3067EARZ | -40°C to +85°C | 14-Lead Standard Small Outline Package [SOIC_N] | R-14 | |
| ADM3067EARZ-R7 | -40°C to +85°C | 14-Lead Standard Small Outline Package [SOIC_N] | R-14 | |
| ADM3067EBRZ | -40°C to +125°C | 14-Lead Standard Small Outline Package [SOIC_N] | R-14 | |
| ADM3067EBRZ-R7 | -40°C to +125°C | 14-Lead Standard Small Outline Package [SOIC_N] | R-14 | |
| EVAL-ADM3061EEBZ | | 8-Lead SOIC Evaluation Board | | |
| EVAL-ADM3061EEB1Z | | 8-Lead MSOP Evaluation Board | | |
| EVAL-ADM3062EEBZ | | 10-Lead MSOP Evaluation Board | | |
| EVAL-ADM3062EEB1Z | | 10-Lead LFCSP Evaluation Board | | |
| EVAL-ADM3065EEBZ | | 8-Lead SOIC Evaluation Board | | |
| EVAL-ADM3065EEB1Z | | 8-Lead MSOP Evaluation Board | | |
| EVAL-ADM3066EEBZ | | 10-Lead MSOP Evaluation Board | | |
| EVAL-ADM3066EEB1Z | | 10-Lead LFCSP Evaluation Board | | |
| EVAL-ADM3067EEBZ | | 14-Lead SOIC Evaluation Board | | |

¹ Z = RoHS Compliant Part.