**FEATURES**

Quad UV/OV positive/negative supervisor  
Supervises up to 2 negative rails  
Adjustable UV and OV input thresholds  
High threshold accuracy over temperature: ±1.5%  
1 V buffered reference output  
Open-drain UV and OV reset outputs  
Adjustable reset timeout with disable option  
Outputs guaranteed down to VCC of 1 V  
Glitch immunity  
62 μA supply current  
16-lead QSOP package

**APPLICATIONS**

Server supply monitoring  
FPGA/DSP core and I/O voltage monitoring  
Telecommunications equipment  
Medical equipment

**GENERAL DESCRIPTION**

The ADM2914 is a quad voltage supervisory IC ideally suited for monitoring multiple rails in a wide range of applications. Each monitored rail has two dedicated input pins, VHx and VLx, which allow each rail to be monitored for both overvoltage (OV) and undervoltage (UV) conditions. A common active low undervoltage (UV) and overvoltage (OV) pin is shared by each of the monitored voltage rails.

The ADM2914 includes a 1 V buffered reference output, REF, that acts as an offset when monitoring a negative voltage. The three-state SEL pin determines the polarity of the third and fourth inputs, that is, it configures the device to monitor positive or negative supplies.

The device incorporates an internal shunt regulator that enables the device to be used in higher voltage systems. This feature requires a resistor to be placed between the main supply rail and the VCC pin to limit the current flow into the VCC pin to no greater than 10 mA. The ADM2914 uses the internal shunt regulator to regulate VCC if the supply line exceeds the absolute maximum ratings.

The ADM2914 is available in two models. The ADM2914-1 offers a latching overvoltage output that can be cleared by toggling the LATCH input pin. The ADM2914-2 has a disable pin that can override and disable both the OV and UV output signals.

The ADM2914 is available in a 16-lead QSOP package. The device operates over the extended temperature range of −40°C to +125°C.
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REVISION HISTORY

3/2017—Rev. E to Rev. F
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5/2015—Rev. D to Rev. E
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12/2014—Rev. C to Rev. D
Changes to Figure 24.................................................................................... 14
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7/2013—Rev. B to Rev. C
Changes to Figure 17 and Figure 18.......................................................... 9
Deleted UV and OV Rise and Fall Times Section ...................................... 12
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Changes to Figure 17 and Figure 18.......................................................... 9

12/2009—Rev. 0 to Rev. A
Changes to Shunt Regulator Section ....................................................... 12

5/2009—Revision 0: Initial Version
## SPECIFICATIONS

$T_A = -40^\circ C$ to $+85^\circ C$. Typical values at $T_A = 25^\circ C$, unless otherwise noted. $V_{CC} = 3.3$ V, $VLx = 0.45$ V, $VHx = 0.55$ V, $LATCH = V_{CC}$, $SEL = V_{CC}$, $DIS = \text{open}$, unless otherwise noted.

### SHUNT REGULATOR
- **$V_{CC}$ Shunt Regulator Voltage, $V_{SHUNT}$**
  - Min: 6.2 V
  - Typ: 6.6 V
  - Max: 6.9 V
  - Unit: V
  - $I_{CC} = 5$ mA

- **$V_{CC}$ Shunt Regulator Load Regulation, $\Delta V_{SHUNT}$**
  - Values:
    - $I_{CC} = 2$ mA to 10 mA

### SUPPLY
- **Supply Voltage, $V_{CC}$**
  - Min: 2.3 V
  - Typ: $V_{SHUNT}$ V

- **Minimum $V_{CC}$ Output Valid, $V_{CRR(MIN)}$**
  - Min: 1 V
  - $DIS = 0$ V

- **Supply Undervoltage Lockout, $V_{CC(UVLO)}$**
  - Min: 1.9 V
  - Typ: 2 V
  - Max: 2.1 V
  - $DIS = 0$ V, $V_{CC}$ rising

- **Supply Undervoltage Lockout Hysteresis, $\Delta V_{CC(HYST)}$**
  - Min: 5 mV
  - Typ: 25 mV
  - Max: 50 mV
  - $DIS = 0$ V

- **Supply Current, $I_{CC}$**
  - Min: 62 μA
  - Typ: 100 μA
  - $V_{CC} = 2.3$ V to 6 V

### REFERENCE OUTPUT
- **Reference Output Voltage, $V_{REF}$**
  - Min: 0.985 V
  - Typ: 1 V
  - Max: 1.015 V
  - $I_{VREF} = \pm 1$ mA

- **$V_{REF}$ **
  - Min: 0.985 V
  - Typ: 1 V
  - Max: 1.020 V
  - $TA = -40^\circ C$ to $+125^\circ C$

### UNDERVOLTAGE/OVERVOLTAGE CHARACTERISTICS
- **Undervoltage/Overvoltage Threshold, $V_{UOT}$**
  - Min: 492.5 mV
  - Typ: 500 mV
  - Max: 507.5 mV
  - Unit: mV

- **Undervoltage/Overvoltage Threshold to Output Delay, $t_{UOD}$**
  - Min: 50 μs
  - Typ: 125 μs
  - Max: 500 μs
  - $VHx \text{ or } VLx = V_{UOT} \pm 5$ mV

- **$UV/OV$ Timeout Period, $t_{UOTO}$**
  - Min: 6 ms
  - Typ: 8.5 ms
  - Max: 12.5 ms
  - $C_{TIMER} = 1$ nF

- **$OV$ Latch Clear Input High, $V_{LATCH(IH)}$**
  - Min: 1.2 V

- **$OV$ Latch Clear Input Low, $V_{LATCH(IL)}$**
  - Min: 0.8 V

- **LATCH Input Current, $I_{LATCH}$**
  - Min: ±1 μA
  - $V_{LATCH} > 0.5$ V

### DISABLE INPUT (ADM2914-2)
- **DIS Input High, $V_{DIS(H)}$**
  - Min: 1.2 V

- **DIS Input Low, $V_{DIS(L)}$**
  - Min: 0.8 V

- **DIS Input Current, $I_{DIS}$**
  - Min: 1 μA
  - Typ: 2 μA
  - Max: 3 μA
  - $V_{DIS} > 0.5$ V

### TIMER CHARACTERISTICS
- **TIMER Pull-Up Current, $I_{TIMER(UP)}$**
  - Min: $-1.3$ μA
  - Typ: $-2.1$ μA
  - Max: $-2.8$ μA

- **TIMER Pull-Down Current, $I_{TIMER(DOWN)}$**
  - Min: 1 μA
  - Typ: 2.1 μA
  - Max: 2.8 μA

- **TIMER Disable Voltage, $V_{TIMER(DIS)}$**
  - Min: $-180$ mV
  - Typ: $-270$ mV

### OUTPUT VOLTAGE
- **Output Voltage High, $UV/OV$, $V_{OH}$**
  - Min: 1 V

- **Output Voltage Low, $UV/OV$, $V_{OL}$**
  - Min: 0.1 V
  - Typ: 0.3 V
  - Max: 0.15 V

### THREE-STATE INPUT SEL
- **Low Level Input Voltage, $V_{IL}$**
  - Min: 0.4 V

- **High Level Input Voltage, $V_{IH}$**
  - Min: 1.4 V

- **Pin Voltage When Left in High-Z State, $V_{Z}$**
  - Min: 0.7 V
  - Typ: 0.9 V
  - Max: 1.1 V

- **$SEL$ High, Low Input Current, $I_{SEL}$**
  - Min: ±25 μA

- **Maximum $SEL$ Input Current, $I_{SEL(MAX)}$**
  - Min: ±30 μA

---

1 The maximum voltage on the $VCC$ pin is limited by the input current. The $VCC$ pin has an internal 6.5 V shunt regulator and, therefore, a low impedance supply greater than 6 V may exceed the maximum allowed input current. When operating from a higher supply than 6 V, always use a dropper resistor.
ABSOLUTE MAXIMUM RATINGS

Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{CC}$</td>
<td>$-0.3 \text{ V to } +6 \text{ V}$</td>
</tr>
<tr>
<td>$U\text{V}, O\text{V}$</td>
<td>$-0.3 \text{ V to } +16 \text{ V}$</td>
</tr>
<tr>
<td>TIMER</td>
<td>$-0.3 \text{ V to } (V_{CC} + 0.3 \text{ V})$</td>
</tr>
<tr>
<td>$V_{Lx}, V_{Hx}, \text{LATCH, DIS, SEL}$</td>
<td>$-0.3 \text{ V to } +7.5 \text{ V}$</td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>10 mA</td>
</tr>
<tr>
<td>Reference Load Current ($I_{REF}$)</td>
<td>$\pm 1 \text{ mA}$</td>
</tr>
<tr>
<td>$I_{UV}, I_{OV}$</td>
<td>10 mA</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$-65^\circ \text{C to } +150^\circ \text{C}$</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$-40^\circ \text{C to } +125^\circ \text{C}$</td>
</tr>
<tr>
<td>Lead Temperature (Soldering, 10 sec)</td>
<td>300°C</td>
</tr>
</tbody>
</table>

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Table 3. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta_{JA}$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-Lead QSOP</td>
<td>104</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Figure 2. ADM2914-1 Pin Configuration

Figure 3. ADM2914-2 Pin Configuration

Table 4. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Pin No.</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>VH1</td>
<td>VH1</td>
<td>Voltage High Input 1 and Voltage High Input 2. If the voltage monitored by VH1 or VH2 drops below 0.5 V, an undervoltage condition is detected. Connect to VCC when not in use.</td>
</tr>
<tr>
<td>2</td>
<td>VH2</td>
<td>VH2</td>
<td>Voltage Low Input 1 and Voltage Low Input 2. If the voltage monitored by VL1 or VL2 rises above 0.5 V, an overvoltage condition is detected. Tie to GND when not in use.</td>
</tr>
<tr>
<td>3</td>
<td>VL1</td>
<td>VL1</td>
<td>Voltage High Input 3 and Voltage High Input 4. The polarity of these inputs is determined by the state of the SEL pin (see Table 5). When the monitored input is configured as a positive voltage and the voltage monitored by VH3 or VH4 drops below 0.5 V, an undervoltage condition is detected. Conversely, when the input is configured as a negative voltage and the input drops below 0.5 V, an overvoltage condition is detected. Connect to VCC when not in use.</td>
</tr>
<tr>
<td>4</td>
<td>VL2</td>
<td>VL2</td>
<td>Voltage Low Input 3 and Voltage Low Input 4. The polarity of these inputs is determined by the state of the SEL pin (see Table 5). When the monitored input is configured as a positive voltage and the voltage monitored by VL3 or VL4 rises above 0.5 V, an overvoltage condition is detected. Conversely, when the input is configured as a negative voltage and the input rises above 0.5 V, an undervoltage condition is detected. Tie to GND when not in use.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>GND</td>
<td>Device Ground.</td>
</tr>
<tr>
<td>6</td>
<td>REF</td>
<td>REF</td>
<td>Buffered Reference Output. This pin is a 1 V reference that is used as an offset when monitoring negative voltages. This pin can source or sink 1 mA, and drive loads up to 1 nF. Larger capacitive loads may lead to instability. Leave unconnected when not in use.</td>
</tr>
<tr>
<td>7</td>
<td>OV</td>
<td>OV</td>
<td>Overvoltage Reset Output. OV is asserted low if a negative polarity input voltage drops below its associated threshold or if a positive polarity input voltage exceeds its threshold. The ADM2914-1 allows OV to be latched low. The ADM2914-2 holds OV low for an adjustable timeout period determined by the TIMER capacitor. This pin has a weak pull-up to VCC and can be pulled up to 16 V externally. Leave this pin unconnected when not in use.</td>
</tr>
<tr>
<td>8</td>
<td>UV</td>
<td>UV</td>
<td>Undervoltage Reset Output. UV is asserted low if a negative polarity input voltage exceeds its associated threshold or if a positive polarity input voltage drops below its threshold. UV is held low for an adjustable timeout period set by the external capacitor tied to the TIMER pin. The UV pin has a weak pull-up to VCC and can be pulled up to 16 V externally via an external pull-up resistor. Leave this pin unconnected when not in use.</td>
</tr>
<tr>
<td>9</td>
<td>LATCH</td>
<td>DIS</td>
<td>OV Latch Bypass Input/Clear Pin. When pulled high, the OV latch is cleared. When held high, the OV output has the same delay and output characteristics as the UV output. When pulled low, the OV output is latched when asserted. (Applies only to the ADM2914-1.)</td>
</tr>
<tr>
<td>10</td>
<td>SEL</td>
<td>SEL</td>
<td>Input Polarity Select. This three-state input pin allows the polarity of VH3, VL3, VH4, and VL4 to be configured. Connect to VCC or GND, or leave open to select one of three possible input polarity configurations (see Table 5).</td>
</tr>
<tr>
<td>11</td>
<td>TIMER</td>
<td>TIMER</td>
<td>Adjustable Reset Delay Timer. Connect an external capacitor to the TIMER pin to program the reset timeout delay. Refer to Figure 15 in the Typical Performance Characteristics section. Connect this pin to VCC to bypass the timer.</td>
</tr>
<tr>
<td>12</td>
<td>VCC</td>
<td>VCC</td>
<td>Supply Voltage. VCC operates as a direct supply for voltages up to 6 V. For voltages greater than 6 V, it operates as a shunt regulator. A dropper resistor must be used in this configuration to limit the current to less than 10 mA. When used without the resistor, the voltage at this pin must not exceed 6 V. A 0.1 μF bypass capacitor or greater should be used.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Figure 4. Input Threshold Voltage vs. Temperature

Figure 7. Vcc Shunt Voltage vs. Icc

Figure 5. Supply Current vs. Temperature

Figure 8. Buffered Reference Voltage vs. Temperature

Figure 6. Vcc Shunt Voltage vs. Temperature

Figure 9. Transient Duration vs. Comparator Overdrive
Figure 10. UV/OV Timeout Period vs. Temperature

Figure 11. UV Output Voltage vs. VCC

Figure 12. UV Output Voltage vs. VCC

Figure 13. ISINK, IUV vs. VCC

Figure 14. UV/OV Voltage Output Low vs. Output Sink Current

Figure 15. UV/OV Timeout Period vs. Capacitance
THEORY OF OPERATION

VOLTAGE SUPERVISION

The ADM2914 supervises up to four voltage rails for overvoltage and undervoltage conditions. Two pins, VHx and VLx, are assigned to monitor each rail, one for overvoltage detection and the other for undervoltage detection. Each pin is connected to the input of an internal voltage comparator, and its voltage level is internally compared with a 0.5 V voltage reference with accuracy of ±1.5%.

The output of each of the internal undervoltage comparators is tied to a common UV output pin. Likewise, the outputs of the internal overvoltage comparators are tied to a common OV output pin.

![Figure 16. Typical Applications Diagram](image)

POLARITY CONFIGURATION

The ADM2914 is capable of monitoring supply voltages of both positive and negative polarities. The SEL pin is a three-state pin that determines the polarity of Input 3 and Input 4. As summarized in Table 5, the SEL pin is either connected to GND, Vcc, or left unconnected.

When an input is configured to monitor a positive voltage, using the three-resistor scheme shown in Figure 17, VHx is connected to the high-side tap of the resistor divider and VLx is connected to the low-side tap of the resistor divider.

Conversely, when an input is configured to monitor a negative voltage, UVx and OVx are swapped internally. The negative voltage for monitoring is then connected as shown in Figure 18. VHx is still connected to the high-side tap and VLx is still connected to the low-side tap. Within this configuration, an undervoltage condition occurs when the monitored voltage is less negative than the programmed threshold, and an overvoltage condition occurs when the monitored voltage is more negative than the configured threshold.

Table 5. Polarity Configuration

<table>
<thead>
<tr>
<th>SEL Pin</th>
<th>Input 3</th>
<th></th>
<th>Input 4</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Polarity</td>
<td>UV Condition</td>
<td>OV Condition</td>
<td>Polarity</td>
</tr>
<tr>
<td>Connected to Vcc</td>
<td>Positive</td>
<td>VH3 &lt; 0.5 V</td>
<td>VL3 &gt; 0.5 V</td>
<td>Positive</td>
</tr>
<tr>
<td>Left Unconnected</td>
<td>Positive</td>
<td>VH3 &lt; 0.5 V</td>
<td>VL3 &gt; 0.5 V</td>
<td>Negative</td>
</tr>
<tr>
<td>Connected to GND</td>
<td>Negative</td>
<td>VL3 &gt; 0.5 V</td>
<td>VH3 &lt; 0.5 V</td>
<td>Negative</td>
</tr>
</tbody>
</table>
MONITORING PIN CONNECTIONS

Positive Voltage Monitoring Scheme

When monitoring a positive supply, the desired nominal operating voltage for monitoring is denoted by \( V_M \), \( I_m \) is the nominal current through the resistor divider, \( V_{OV} \) is the overvoltage trip point, and \( V_{UV} \) is the undervoltage trip point.

\[
0.5V = \frac{V_{OV} \cdot R_Z}{R_X + R_Y + R_Z} = 0.5V
\]

The high-side voltage, \( V_{PH} \), is connected to the corresponding \( VH_x \) pin, and the low-side voltage is connected to the corresponding \( VL_x \) pin.

To trigger an overvoltage condition, the low-side voltage (in this case, \( V_{PL} \)) must exceed the 0.5 V threshold on the \( VL_x \) pin. The low-side voltage, \( V_{PL} \), is given by the following equation:

\[
V_{PL} = V_{OV} \left( \frac{R_Z}{R_X + R_Y + R_Z} \right) = 0.5V
\]

Also,

\[
R_X + R_Y + R_Z = \frac{V_M}{I_m}
\]

Therefore, \( R_Z \), which sets the desired trip point for the overvoltage monitor, is calculated using the following equation:

\[
R_Z = \frac{(0.5)(V_m)}{(V_{OV} \cdot I_m)}
\]  

(1)

Negative Voltage Monitoring Scheme

Figure 18 shows the circuit configuration for negative supply voltage monitoring. To monitor the negative voltage, a 1 V reference voltage is required to connect to the end node of the voltage divider circuit. This reference voltage is generated internally and is output through the \( REF \) pin.

\[
0.5V = \frac{V_{UV} \cdot R_Y}{R_X + R_Y + R_Z} = 0.5V
\]

Because \( R_Z \) is already known, \( R_Y \) can be expressed as follows:

\[
R_Y = \frac{(0.5)(V_m)}{(V_{UV} \cdot I_m)} - R_Z
\]  

(2)

When \( R_Y \) and \( R_Z \) are known, \( R_X \) is calculated using the following equation:

\[
R_X = \frac{V_m}{I_m} - R_Z - R_Y
\]  

(3)

If \( V_M, I_m, V_{OV}, \) or \( V_{UV} \) changes, each step must be recalculated.

If \( V_M, I_m, V_{OV}, \) or \( V_{UV} \) changes, each step must be recalculated.

The equations described in the Positive Voltage Monitoring Scheme section need some minor modifications for use with negative voltage monitoring. The 1 V reference voltage is added to the overall voltage drop; it must therefore be subtracted from \( V_{SM}, V_{UV}, \) and \( V_{OV} \) before using each in the previous equations.

To monitor a negative voltage level, the resistor divider circuit divides the voltage differential level between the 1 V reference voltage and the negative supply voltage into high-side voltage, \( V_{NH} \), and low-side voltage, \( V_{NL} \). Similar to the positive voltage monitoring scheme, the high-side voltage, \( V_{NH} \), is connected to the corresponding \( VH_x \) pin, and the low-side voltage, \( V_{NL} \), is connected to the corresponding \( VL_x \) pin. Refer to the Voltage Monitoring Example section for more information.
THRESHOLD ACCURACY

The reset threshold accuracy is fundamental, especially at lower voltage levels. Consider an FPGA application that requires a 1 V core voltage input with tolerance of ±5%, where the supply has a specified regulation, for example, ±1.5%. As shown in Figure 19, to ensure that the supply is within the FPGA input voltage requirement range, its voltage level must be monitored for UV and OV conditions. The voltage swing on the supply itself causes the voltage band available for setting the monitoring threshold to be quite narrow. In this example, the threshold voltages, including the tolerances, must fit within a monitor region of only 0.035 V. The ADM2914 device with 0.1% resistors can achieve this level of accuracy.

VOLTAGE MONITORING EXAMPLE

To illustrate how the ADM2914 device works in a real application, consider the 1 V input example shown in Figure 19, with the addition of a −12 V rail.

The first step is to choose the nominal current flow through both voltage divider circuits, for example, 5 μA.

For the 1 V ±5% input, due to the specified ±1.5% regulation of the supply, the UV and OV thresholds should be set in the middle of the voltage monitoring band. In this case, on the ±3.25% points of the supply, the UV threshold is 0.9675 V and the OV threshold is 1.0325 V.

Input these values into Equation 1.

\[
R_Z = \frac{(0.5)(1)}{(1.0325)(5 \times 10^{-6})} \approx 96.5 \text{ kΩ}
\]

Insert the value of \(R_Z\) into Equation 2.

\[
R_V = \frac{(0.5)(1)}{(0.9675)(5 \times 10^{-6})} = 96.5 \text{ kΩ} - 6.42 \text{ kΩ}
\]

Then substitute the calculated values for \(R_Z\) and \(R_V\) into Equation 3.

\[
R_X = \frac{1}{5 \times 10^{-6}} - 96.5 \text{ kΩ} - 6.42 \text{ kΩ} \approx 96.5 \text{ kΩ}
\]

This design approach meets the application specifications. As described previously, the 1 V rail is specified with an input requirement of ±5% and a supply tolerance of ±1.5%. This effectively means that the OV threshold of the monitoring device, including all the tolerance factors, must fit within the 1.015 V to 1.05 V range. Similarly, the UV threshold range must be between 0.95 V and 0.985 V.

The four worst-case scenarios of minimum and maximum undervoltage and overvoltage thresholds are calculated as follows:

Minimum overvoltage threshold

\[
V_{\text{OV Min}} = (0.5 \text{ V} - 1.5\% \left(1 + \frac{(R_X - 0.1\%) + (R_V - 0.1\%)}{R_Z + 0.1\%}\right)
\]

\[
= 0.4925 \left(1 + \frac{(96.5,000 + 6420)(0.999)}{(96,500)(1.001)}\right)
\]

\[
= 1.016 \text{ V} > 1.015 \text{ V}
\]

Maximum overvoltage threshold

\[
V_{\text{OV Max}} = (0.5 \text{ V} + 1.5\%) \left(1 + \frac{(R_X + 0.1\%) + (R_V + 0.1\%)}{R_Z - 0.1\%}\right)
\]

\[
= 1.049 \text{ V} < 1.05 \text{ V}
\]

The maximum and minimum overvoltage threshold values lie within the 1.015 V to 1.05 V range specified. The minimum and maximum undervoltage thresholds are calculated as follows:

Minimum undervoltage threshold

\[
V_{\text{UV Min}} = (0.5 \text{ V} - 1.5\%) \left(1 + \frac{(R_X - 0.1\%)}{(R_V + 0.1\%)}\right)
\]

\[
= 0.953 \text{ V} > 0.95 \text{ V}
\]

Maximum undervoltage threshold

\[
V_{\text{UV Max}} = (0.5 \text{ V} + 1.5\%) \left(1 + \frac{(R_X + 0.1\%)}{(R_V - 0.1\%)}\right)
\]

\[
= 0.984 \text{ V} < 0.985 \text{ V}
\]

Again, these values fit within the specified undervoltage monitoring range. All four worst-case scenarios satisfy the tolerance requirement; therefore, the design approach is valid.
Next, consider a −12 V input, which is specified with a ±20% input. The threshold accuracy required by the supply is chosen to be within ±5% of the −12 V rail. Therefore, the overvoltage threshold is set to −13.5 V, and the undervoltage threshold is −10.5 V. The negative voltage scheme configuration requires that the 1 V reference voltage be accounted for in Equation 1 to Equation 3. The 1 V reference voltage is subtracted from Vₘₙ, Vᵥᵥ, and Vₒₒ, and the absolute value of the result is taken.

Equation 1 becomes
\[ R_z = \frac{0.5|12 - 1|}{5|13.5 - 1|} \approx 89.8 \text{kΩ} \]

Insert the value of Rz into Equation 2.
\[ R_y = \frac{0.5|12 - 1|}{5|10.5 - 1|} \approx 23.4 \text{kΩ} \]

To calculate Rₓ, insert the value of Rz and Rᵧ into Equation 3.
\[ R_x = \frac{5|12 - 1| - (89.8 \text{kΩ}) - (23.4 \text{kΩ})}{2.49 \text{MΩ}} \]

**POWER-UP AND POWER-DOWN**

On power-up, when Vcc reaches 1 V, the active low UV output is asserted, and the OV output pulls up to Vcc. When the voltage on the Vcc pin reaches 1 V, the ADM2914 is guaranteed to assert UV low and OV high. When Vcc exceeds 1.9 V (minimum), the VHₓ and VLₓ inputs take control. When Vcc and each of the VHₓ inputs are valid, an internal timer begins. Subsequent to an adjustable time delay, UV weakly pulls high.

**UV/OV TIMING CHARACTERISTICS**

UV is an active low output. It is asserted when any of the four monitored voltages is below its associated threshold. When the voltage on the Vcc pin is above 2 V, an internal timer holds UV low for an adjustable period, tUOTO, after the voltage on all the monitoring rails rises above their thresholds. This allows time for all monitored power supplies to stabilize after power-up. Similarly, any monitored voltage that falls below its threshold initiates a timer reset, and the timer starts again when all the monitoring rails rise above their thresholds.

The UV and OV outputs are held asserted after all faults have cleared for an adjustable timeout period, determined by the value of the external capacitor attached to the TIMER pin.

**TIMER CAPACITOR SELECTION**

The UV and OV timeout period on the ADM2914 is programmable via the external timer capacitor, C_TIMER, placed between the TIMER pin and ground. The timeout period, tUOTO, is calculated using the following equation:
\[ C_{\text{TIMER}} = t_{\text{UOTO}}(115)(10^{-9}) \text{ F/sec} \]
UV/OV OUTPUT CHARACTERISTICS

Both the OV and UV outputs have a strong pull-down to ground and a weak internal pull-up to VCC. This permits the pins to behave as open-drain outputs. When the rise time on the pin is not critical, the weak pull-up removes the requirement for an external pull-up resistor. The open-drain configuration allows for wire-OR’ing of outputs, which is particularly useful when more than one signal needs to pull down on the output.

At VCC = 1 V, a maximum Vol = 0.15 V at UV is guaranteed. At VCC = 1 V, the weak pull-up current on OV is almost turned on. Consequently, if the state and pull-up strength of the OV pin are important at very low VCC, an external pull-up resistor of no more than 100 kΩ is advised. By adding an external pull-up resistor, the pull-up strength on the OV pin is greater. Therefore, if it is connected in a wire-ORed configuration, the pull-down strength of any single device must account for this additional pull-up strength.

GLITCH IMMUNITY

The ADM2914 is immune to short transients that may occur on the monitored voltage rails. The device contains internal filtering circuitry that provides immunity to fast transient glitches. Figure 9 illustrates glitch immunity performance by showing the maximum transient duration without causing a reset pulse. Glitch immunity makes the ADM2914 suitable for use in noisy environments.

UNDERVOLTAGE LOCKOUT (UVLO)

The ADM2914 has an undervoltage lockout circuit that monitors the voltage on the VCC pin. When the voltage on VCC drops below 1.9 V (minimum), the circuit is activated. The UV output is asserted and the OV output is cleared and not allowed to assert. When VCC recovers, UV exhibits the same timing characteristics as if an undervoltage condition had occurred on the inputs.

SHUNT REGULATOR

The ADM2914 is powered via the VCC pin. The VCC pin can be directly connected to a voltage rail of up to 6 V. In this mode, the supply current of the device does not exceed 100 μA. An internal shunt regulator allows the ADM2914 to operate at voltage levels greater than 6 V by simply placing a dropper resistor in series between the supply rail and the VCC pin to limit the input current to less than 10 mA.

Once the supply voltage, Vin, has been established, an appropriate value for the dropper resistor can be calculated. Begin by determining the maximum supply current required, ICCtotal, by adding the current drawn from the reference and/or the pull resistors between the outputs and the VCC pin to the maximum specified supply current. The minimum and maximum shunt regulator voltage specified in Table 1, VSHUNT min and VSHUNT max, are also required in the following calculations.

Calculate the maximum and minimum dropper resistor values

\[
R_{\text{MAX}} = \frac{V_{\text{IN min}} - V_{\text{SHUNT max}}}{I_{\text{CC total}}}
\]

\[
R_{\text{MIN}} = \frac{V_{\text{IN max}} - V_{\text{SHUNT min}}}{100 \mu A}
\]

Based on these values, choose a real-world resistor value within this range. Then, given the specified accuracy of this resistor, calculate the minimum and maximum real resistor value variation, RREALmin and RREALmax, respectively.

The maximum device power is calculated as follows:

\[
P_{\text{Device Max}} = V_{\text{SHUNT max}} \left( \frac{V_{\text{IN max}} - V_{\text{SHUNT max}}}{R_{\text{REAL min}}} - I_{\text{CC total}} \right) + V_{\text{SHUNT max}} I_{\text{CC total}}
\]

To check that the calculated value of the resistor will be acceptable, calculate the maximum device temperature rise.

\[
\text{Temp}_{\text{Rise max}} = \theta_{JA} P_{\text{Device Max}}
\]

Add this value to the ambient operating temperature. If the resistor value is acceptable, the result will lie within the specified operating temperature range of the device, −40°C to +85°C.
**OV LATCH (ADM2914-1)**

If an overvoltage condition occurs when the LATCH pin is pulled low, the OV pin latches low. Pulling the LATCH pin high clears the latch. If an overvoltage condition clears while the LATCH pin is high, the latch is bypassed and the OV pin behaves in the same way as the UV pin, with an identical timeout period. If the LATCH pin is pulled low while the timeout period is active, the OV pin latches low, as in normal operation.

If the LATCH pin is kept low during the device power up, a false positive overvoltage condition is reported by the IC. This is due to uncertainties between the rising internal reference voltage and the voltages being monitored and is more evident if the device is configured for negative voltage monitoring. It is recommended to add a delay circuit shown in Figure 23 to temporarily pull the LATCH pin high during the device power up period until the supply and reference voltage stabilize.

![Figure 23. LATCH Pin Delay Circuit](image)

Calculate the component values using the following equation:

\[
C_{LATCH} = \frac{-t_{DELAY}}{0.8 \ln \left( \frac{V_{CC}}{V_{CC}} \right) \times R_{LATCH}}
\]

where:
- \( V_{CC} \) is the final supply voltage on the VCC pin
- \( t_{DELAY} \) is the estimated delay between VCC pin power up to LATCH pin voltage dropping below threshold low voltage.

The exact delay time required, depending on the VCC power up profile and ramping rate, is always longer than VCC rise time plus a few milliseconds for margin. Some component value combinations are shown in Table 6.

**Table 6. Standard Component Values of the Latch Delay Circuit**

<table>
<thead>
<tr>
<th>( V_{CC} ) (V)</th>
<th>( t_{DELAY} ) (ms)</th>
<th>( R_{LATCH} ) (k( \Omega ))</th>
<th>( C_{LATCH} ) (( \mu )F)</th>
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</thead>
<tbody>
<tr>
<td>3.3</td>
<td>10</td>
<td>105</td>
<td>0.68</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>105</td>
<td>0.68</td>
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</tr>
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<td></td>
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</tr>
<tr>
<td>6.6</td>
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<td>10</td>
<td>0.47</td>
</tr>
<tr>
<td></td>
<td>100</td>
<td>10</td>
<td>0.47</td>
</tr>
</tbody>
</table>

**DISABLE (ADM2914-2)**

Pulling the DIS pin high disables both the UV and OV outputs, and forces both outputs to remain weakly pulled high, regardless of any faults that are detected at the inputs. If a UVLO condition is detected, the UV output is asserted and pulls low; however, the timeout function is bypassed. As soon as the UVLO condition clears, the UV output pulls high. To guarantee normal operation when the pin is left unconnected, DIS has a weak 2 \( \mu \)A internal pull-down current.
TYPICAL APPLICATIONS

Figure 24. Typical Application Diagram for Monitoring 5 V, 3.3 V, 2.5 V, and 1.8 V

Figure 25. Typical Application Diagram for Monitoring +12 V and −5 V

NOTES
1 1.5% SUPPLY TOLERANCE AND 5% INPUT TOLERANCE REQUIREMENT.
2 3% SUPPLY TOLERANCE AND 15% INPUT TOLERANCE REQUIREMENT.
NOTES

1. 1.5% SUPPLY TOLERANCE AND 10% INPUT TOLERANCE REQUIREMENT.
2. 2% SUPPLY TOLERANCE AND 15% INPUT TOLERANCE REQUIREMENT.
3. 4% SUPPLY TOLERANCE AND 15% INPUT TOLERANCE REQUIREMENT.

Figure 26. Typical Application Diagram for Monitoring +48 V, +16 V, −3.3 V, and −48 V
OUTLINE DIMENSIONS

Compliant to JEDEC Standards MO-137-AB
Controlling dimensions are in inches; millimeter dimensions (in parentheses) are rounded-off inch equivalents for reference only and are not appropriate for use in design.

Figure 27. 16-Lead Shrink Small Outline Package [QSOP] (RQ-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADM2914-1ARQZ</td>
<td>−40°C to +125°C</td>
<td>16-Lead Shrink Small Outline Package [QSOP]</td>
<td>RQ-16</td>
</tr>
<tr>
<td>ADM2914-1ARQZ-RL7</td>
<td>−40°C to +125°C</td>
<td>16-Lead Shrink Small Outline Package [QSOP]</td>
<td>RQ-16</td>
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<tr>
<td>ADM2914-2ARQZ</td>
<td>−40°C to +125°C</td>
<td>16-Lead Shrink Small Outline Package [QSOP]</td>
<td>RQ-16</td>
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<tr>
<td>ADM2914-2ARQZ-RL7</td>
<td>−40°C to +125°C</td>
<td>16-Lead Shrink Small Outline Package [QSOP]</td>
<td>RQ-16</td>
</tr>
<tr>
<td>EVAL-ADM2914EBZ</td>
<td>−40°C to +125°C</td>
<td>Evaluation Board</td>
<td></td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.