Robust, Industrial, Low Power 10/100 Ethernet PHY

Preliminary Technical Data

ADIN1200

FEATURES

- 10BASE-T/100BASE-TX IEEE® 802.3™ compliant
- MII, RMII and RGMII MAC interfaces
- 100BASE-TX RGMII latency TX <124 ns, RX < 250 ns
- 100BASE-TX MII latency TX<52 ns, RX < 248 ns
- EMC Test Standards:
  - IEC 61000-4-5 surge (±3 kV)
  - IEC 61000-4-4 electrical fast transient (EFT) (±4 kV)
  - IEC 61000-4-2 ESD (±6 kV contact discharge)
  - IEC 61000-4-6 conducted immunity (10 V)
  - EN55022 radiated emissions (CLASS A)
  - EN55022 conducted emissions (CLASS B)
- Unmanaged configuration using multi-level pin strapping
- Energy Efficient Ethernet (EEE) in accordance with
  - IEEE 802.3az
- IEEE 1588 Start-of-frame detect
- Configurable LED
- Crystal Oscillator/25MHz clock input
- 25 MHz/125MHz Synchronous clock output
- Small Package and Wide Temperature Range
  - 32-lead (5 mm x 5 mm) LFCSP
  - Specified for -40°C to +105°C ambient operation
- Low Power Consumption
  - 139mW -100BASE-TX
  - 3.3 V/2.5 V/1.8 V MAC interface VDDIO supply
  - Single supply operation with 3.3 V VDDIO
  - Integrated power supply monitoring and POR

APPLICATIONS

- Industrial automation
- Process control
- Factory automation
- Robotics/Motion Control
- Building automation
- Test and Measurement
- Industrial IoT

GENERAL DESCRIPTION

The ADIN1200 is a low power single port 10/100 Mb Ethernet transceiver with low latency specifications primarily designed for industrial Ethernet applications.

This design integrates an Energy Efficient Ethernet PHY core plus all the associated common analog circuitry, input and output clock buffering, the management interface and sub-system registers as well as the MAC interface and control logic to manage the reset and clock control and pin configuration.

The ADIN1200 is available in a 5 mm x 5 mm 32-ld package and can operate with a single 3.3 V supply, assuming the use of a 3.3 V MAC interface supply. However, for maximum flexibility in system level design, the separate VDDIO supply enables the MDIO and MAC interface supply voltages to be configured independently of the other circuitry on the ADIN1200 allowing operation at 1.8 V, 2.5 V or 3.3 V. At power-up, the ADIN1200 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value and the power is considered good. Brown-out protection is provided by monitoring the supplies to detect if one or more of them drops below a minimum falling threshold and holding the part in hardware reset until the power is good again.

The MII management interface (also referred to as MDIO interface) provides a two-wire serial interface between a host processor or MAC and the ADIN1200 allowing access to control and status information in the PHY core management registers. The interface is compatible with both IEEE 802.3 Std clause 22 and clause 45 management frame structures.

Table 1. Related Products

Part No.	Description
ADIN1300	Robust, Industrial, Low Latency 10/100/1000 Gigabit Ethernet PHY in 40-ld (6 mm x 6 mm) LFCSP
ADIN1301	Robust, Industrial, Low Latency Gigabit Ethernet PHY with GMII Interface in 64-ld (9 mm x 9 mm) LGA

Rev. PrH

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FUNCTIONAL BLOCK DIAGRAM

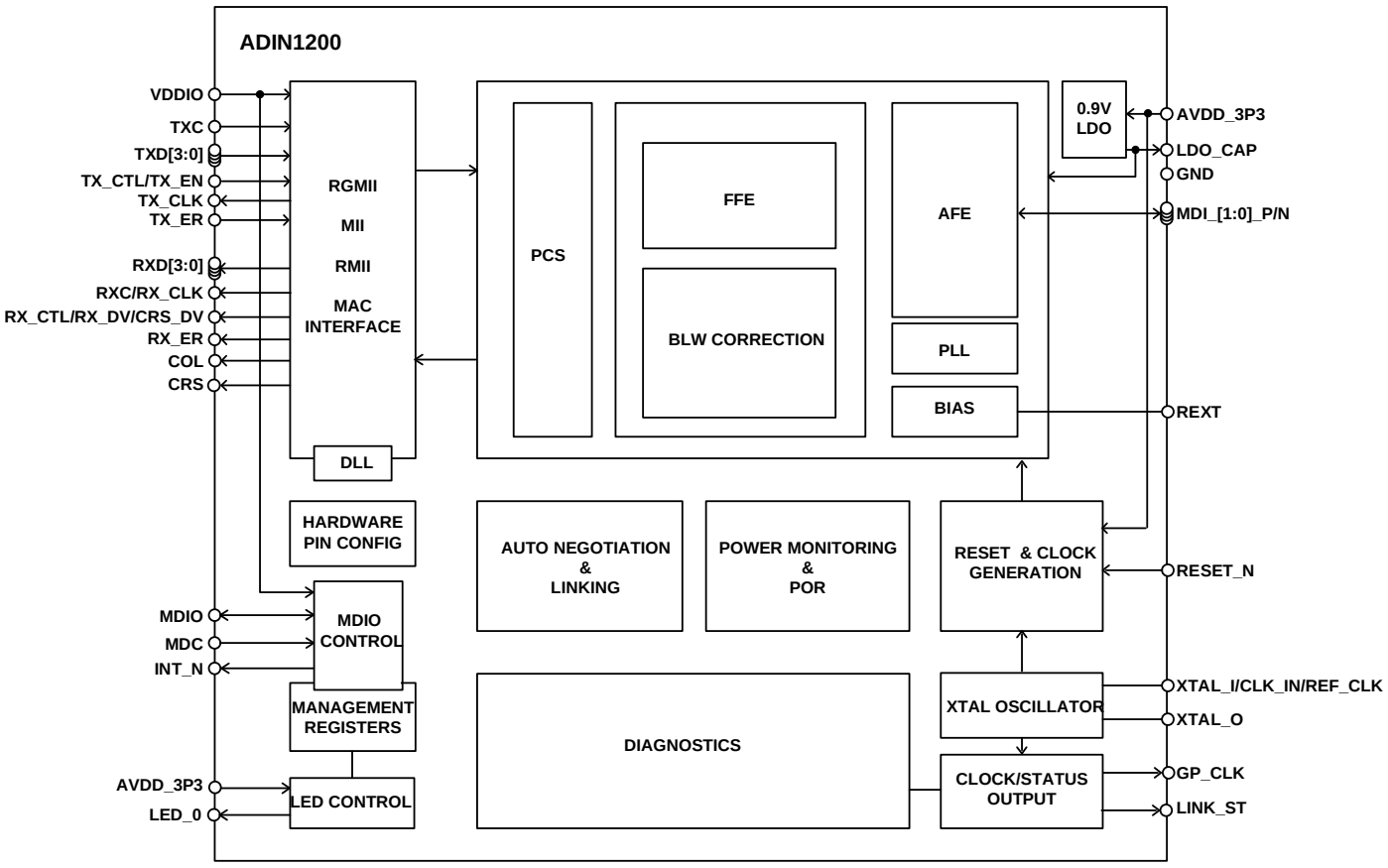


Figure 1.

SPECIFICATIONS

AVDD_3P3 = 3.3 V, VDDIO = 1.8 V, TA = -40°C to +105°C, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
POWER REQUIREMENTS					
Supply Voltages					
AVDD_3P3	3.14	3.3	3.46	V	
VDDIO	3.14	3.3	3.46	V	3.3 V mode
	2.25	2.5	2.75	V	2.5 V mode
	1.71	1.8	1.89	V	1.8 V mode
Supply Current RGMII 100BASE-TX					
AIDD_3P3		31		mA	
IDDIO		22		mA	3.3 V mode
		21		mA	2.5 V mode
		20		mA	1.8 V mode
Power Consumption RGMII					100% data throughput, full activity
100BASE-TX		175		mW	VDDIO = 3.3V
		155		mW	VDDIO = 2.5V
		139		mW	VDDIO = 1.8V
TIMING/LATENCY					
100BASE-TX MII Latency					
TX Latency			52	ns	
RX Latency			248	ns	
Total Latency			300	ns	
100BASE-TX RGMII Latency[1]					
TX Latency	84	88	92	ns	
RX Latency			250	ns	
Total Latency	334	338	342	ns	
100BASE-TX RGMII Latency[2]					
TX Latency	84	104	124	ns	
RX Latency			250	ns	
Total Latency	334	354	374	ns	
100BASE-TX RMII Latency[3]					
TX Latency	72		92	ns	
RX Latency	328	348	368	ns	
Total Latency	400	430	460	ns	
DIGITAL INPUT/OUTPUT					Applies to MDC, MDIO, MDI, INT_N , GP_CLK, LINK_ST pins
Input Low Voltage, V_{IL}			0.8	V	VDDIO = 3.3 V
			0.7	V	VDDIO = 2.5 V
			0.63	V	VDDIO = 1.8 V
Input High Voltage, V_{IH}	1.72			V	VDDIO = 3.3 V
	1.7			V	VDDIO = 2.5 V
	1.17			V	VDDIO = 1.8 V
Input Current, I_{IH}, I_{IL}			TBD	µA	
Output Low Voltage, V_{OL}			0.4	V	VDDIO = 3.3 V
			0.4	V	VDDIO = 2.5 V
			0.4	V	VDDIO = 1.8 V
Output High Voltage, V_{OH}	2.4			V	VDDIO = 3.3 V

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
	2.0			V	VDDIO = 2.5 V
	1.35			V	VDDIO = 1.8 V
Output Current, I_{IH}, I_{IL}			TBD	µA	
DIGITAL INPUT/OUTPUT					Applies to RESET_N & LED0 pins, which operate from AVDD_3P3.
Input Low Voltage, V_{IL}			0.8	V	
Input High Voltage, V_{IH}	1.72			V	
Output Low Voltage, V_{OL}			0.4	V	
Output High Voltage, V_{OH}	2.4			V	
Input Current, I_{IH}, I_{IL}			TBD	µA	

[1] This 100BASE-TX RGMII TX latency is where the TX FIFO is programmed for synchronous operation (MAC TX clock must be synchronous with the ADIN1200 reference clock).

[2] This 100BASE-TX RGMII TX latency is where the MAC TX clock does NOT have to be synchronous with the ADIN1200 reference clock and the TX FIFO takes care of any phase difference.

[3] The RMII TX latency depends on the phase relationship between the 50 MHz reference clock and the internal 25 MHz clock. The TX latency is fixed for a given link.

TIMING CHARACTERISTICS

Power-Up Timing

Table 3. Power Up Timing

Parameter	Description	Min	Typ	Max	Unit
t_{RAMP}	Power Supply Ramp Time			40	ms
t1	Minimum Time interval to Internal Power Good[1]		6.8		ms
t2	XTAL_I Crystal settling time XTAL_I External Clock settling time		1.5	2 20	ms µs
t3	Hardware configuration latch time			64	µs
t4	Management interface active			5	ms

[1] The minimum time interval is referenced to the last supply to reach its rising threshold. There is no specific power supply sequencing required.

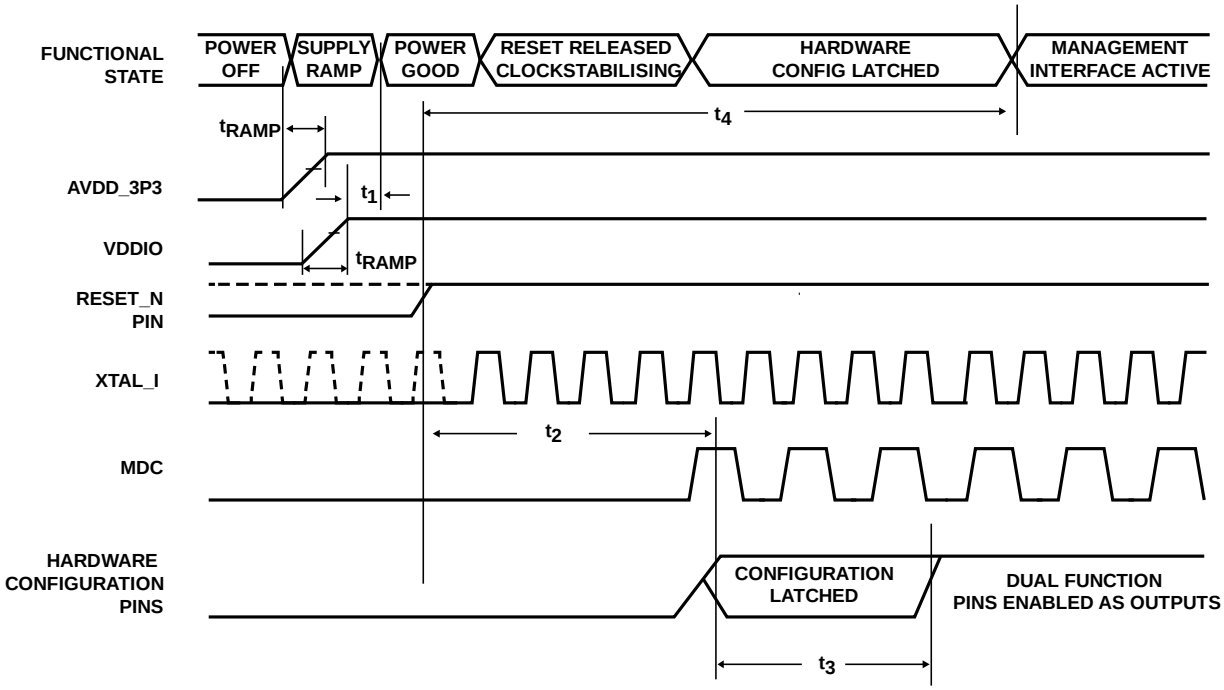


Figure 2. Power-Up Timing

Hardware RESET Timing

Table 4. Hardware Reset Timing

Parameter	Description	Min	Typ	Max	Unit
t1	RESET_N low time	10			µs
t2	XTAL_I Crystal settling time XTAL_I External Clock settling time		1.5 0		ms
t3	Hardware configuration latch time			64	µs
t4	Management interface active			5	ms

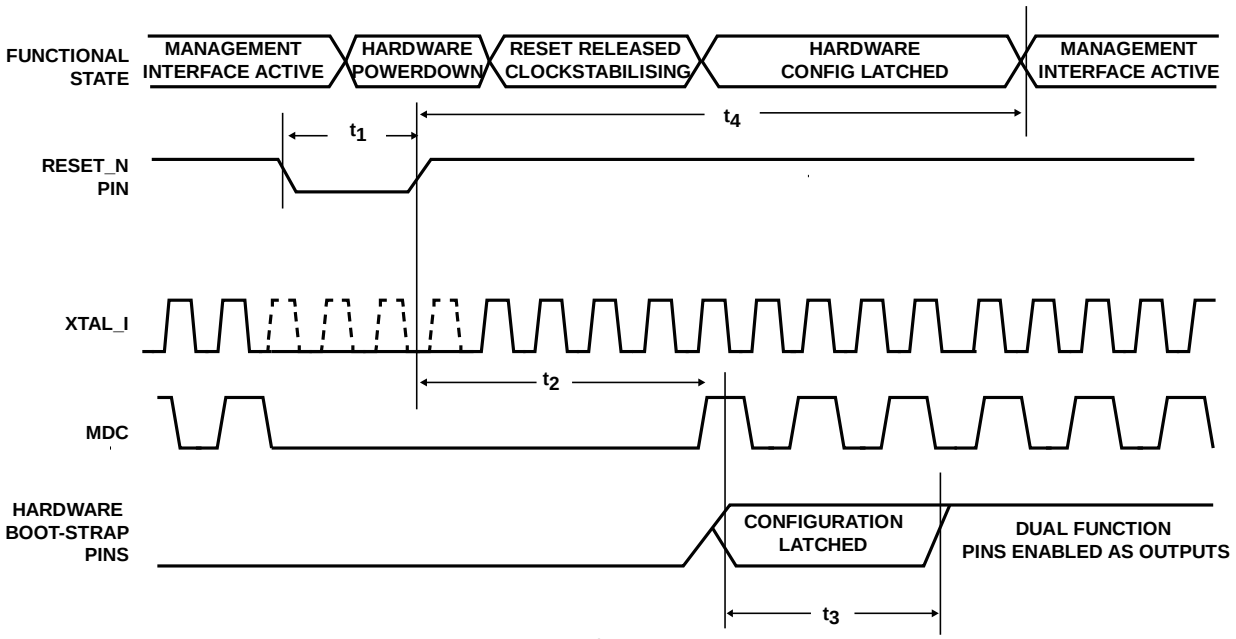


Figure 3. Hardware Reset Timing

Management Interface Timing

Table 5. Management Interface Timing

Parameter	Description	Min	Typ	Max	Unit
t1	MDC Period	180			ns
t2	MDC high time	70			ns
t3	MDC low time	70			ns
t4	MDC Rise/fall time			5	ns
t5	MDIO signal setup time to MDC	10			ns
t6	MDIO signal hold time to MDC	10			ns
t7	MDIO delay time to MDC	0		60	ns

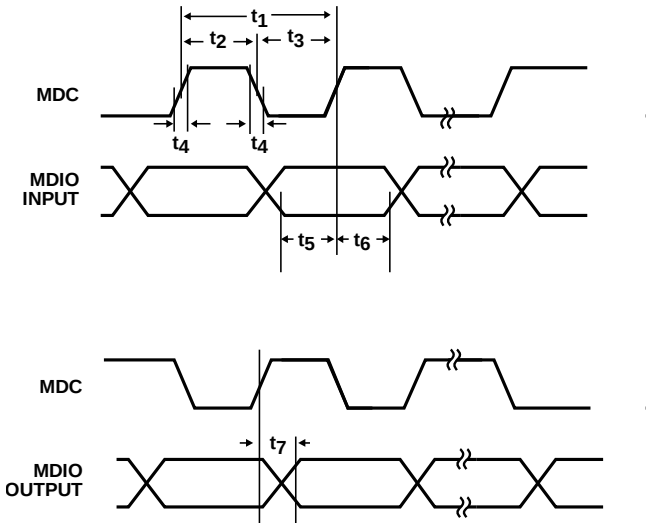


Figure 4. Management Interface Timing

MII Transmit and Receive Timing

Table 6. MII 100BASE-TX Transmit Timing

Parameter	Description	Min	Typ	Max	Unit
t1	TX_CLK Period		40		ns
t2	TX_CLK high time	14	20	26	ns
t3	TX_CLK low time	14	20	26	ns
t4	TX_CLK Rise/Fall time		5		ns
t5	MII input signal setup time to TX_CLK	10			ns
t6	MII input signal hold time to TX_CLK	0			ns

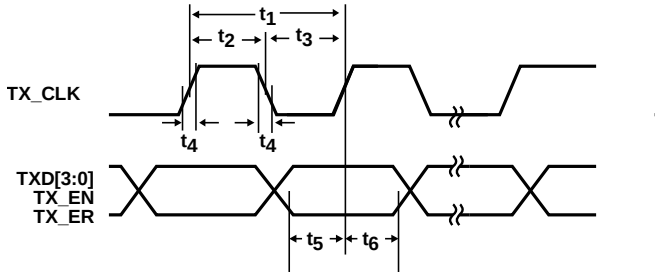


Figure 5. MII Transmit Timing

Table 7. MII 100BASE-TX Receive Timing

Parameter	Description	Min	Typ	Max	Unit
t1	RX_CLK Period		40		ns
t2	RX_CLK high time	16	20	24	ns
t3	RX_CLK low time	16	20	24	ns
t4	RX_CLK Rise/Fall time			1	ns
t5	MII output signal setup time to RX_CLK	10			ns
t6	MII output signal hold time to RX_CLK	10			ns

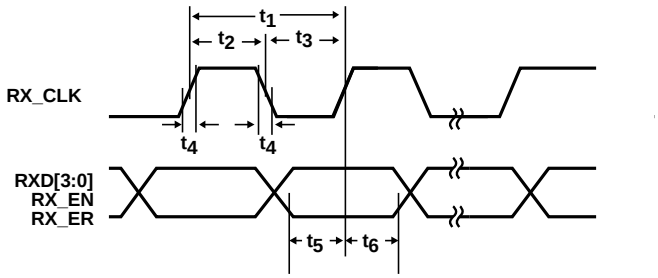


Figure 6. MII Receive Timing

Table 8. MII 10BASE-T Transmit Timing (see Figure 5)

Parameter	Description	Min	Typ	Max	Unit
t1	TX_CLK Period		400		ns
t2	TX_CLK high time	140	200	260	ns
t3	TX_CLK low time	140	200	260	ns
t4	TX_CLK Rise/Fall time		1		ns
t5	MII input signal setup time to TX_CLK	10			ns
t6	MII input signal hold time to TX_CLK	0			ns

Table 9. MII 10BASE-T Receive Timing (see Figure 6)

Parameter	Description	Min	Typ	Max	Unit
t1	RX_CLK Period		400		ns
t2	RX_CLK high time	140	200	260	ns
t3	RX_CLK low time	140	200	260	ns
t4	RX_CLK Rise/Fall time		1	1	ns
t5	MII output signal setup time to RX_CLK	10			ns
t6	MII output signal hold time to RX_CLK	10			ns

RGMII Tx/Rx

Table 10. RGMII Timing

Parameter	Description	Min	Typ	Max	Unit
t1	Data to Clock output Skew (at Transmitter)[1]	-500	0	500	ps
t2	Data to Clock Input Skew (at Receiver)[1]	1	1.8	2.6	ns
t3	Data to clock output setup time (at Transmitter – internal delay)[2]	1.2	2.0		ns
t4	Clock to Data output hold time (at Transmitter – internal delay)[2]	1.2	2.0		ns
t5	Data to Clock input setup Time (at Receiver – internal delay)[2]	1.0	2.0		ns
t6	Clock to Data input hold time (at Receiver – internal delay)[2]	1.0	2.0		ns
Tcyc	Clock Cycle Duration[3]	7.2	8	8.8	ns
Duty_T	Duty Cycle for 10/100T	40	50	60	%
tR/tF	Rise/Fall time (20% to 80%)			0.75	ns

[1] When operating without RGMII internal delay, the PCB design requires clocks to be routed such that an additional trace delay of greater than 1.5ns and less than 2.0ns is added to the associated clock signal. For 10/100T the max value is unspecified.
[2] Hardware and software programmable internal delay may be enabled or disabled.
[3] For 10Mbps and 100Mbps, Tcyc will scale to 400 ns ±40 ns and 40 ns ±4 ns respectively

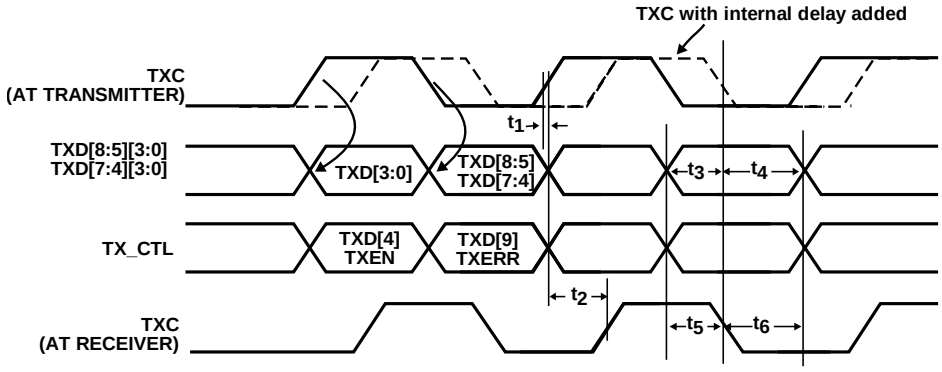


Figure 7. RGMII Transmit Timing

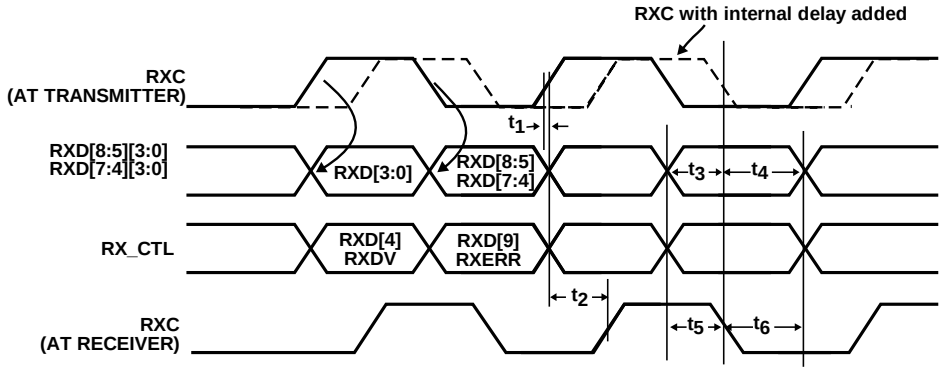


Figure 8. RGMII Receive Timing

RMII Tx/Rx

Table 11. RMII Timing

Parameter	Description	Min	Typ	Max	Unit
	REF_CLK Frequency		50		MHz
	REF_CLK Duty Cycle	35		65	%
t1	TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER Data Setup to REF_CLK rising edge	4			ns
t2	TXD[1:0], TX_EN,RXD[1:0], CRS_DV, RX_ER Data hold from REF_CLK rising edge	2			ns
t3	Output rise/fall times	1		5	ns

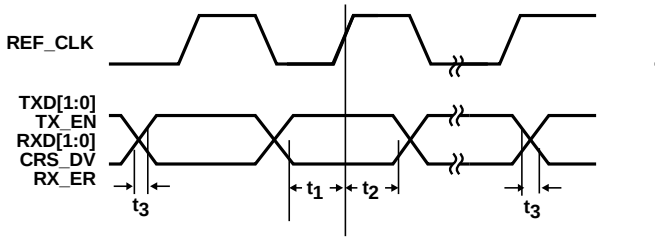


Figure 9. RMII Timing

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 12.

Parameter	Rating
VDDIO to GND	−0.3 V to +3.63 V
LDO_CAP to GND	−0.3 V to +1.1 V
AVDD_3P3 to GND	−0.3 V to +3.63V
MAC Interface	−0.3 V to VDDIO + 0.3 V
MDIO, MDC, INT_N to GND	−0.3 V to VDDIO + 1.9 V
MDI_[1:0]_P/N to GND	−0.3 V to VDDIO + 0.3 V
LINK_ST, GP_CLK	−0.3 V to VDDIO + 0.3 V
LED_0, RESET_N, XTAL_I/CLK_IN/REF_CLK, XTAL_O	−0.3 V to AVDD_3P3 + 1.9 V
Operating Temperature Range (T_A)	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
Power Dissipation	(T_J max − T_A)/θ_{JA}
Lead Temperature	JEDEC industry standard
Soldering	J-STD-020
ESD	
IEC61000-4-2 on MDI pins	4 kV
HBM	2 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Table 13. Thermal Resistance

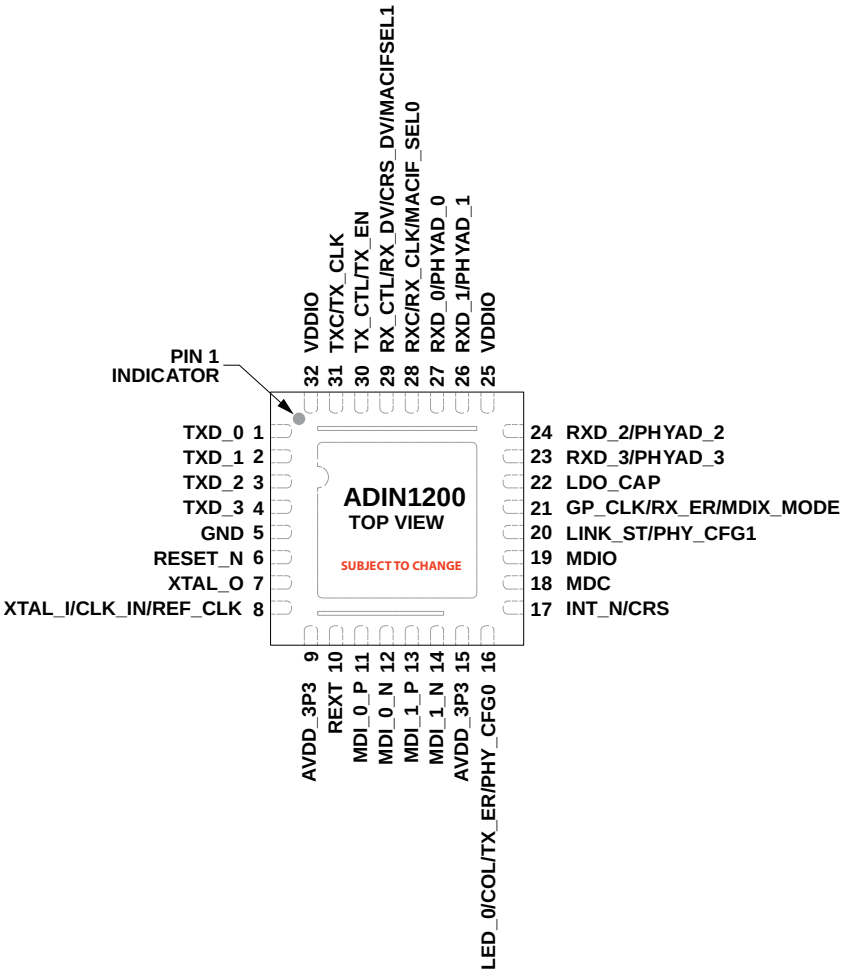
Package Type	θ_{JA}	Unit
CP-32[1]	TBD	°C/W

[1] Test Condition 1: thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. THE LFCSP HAS AN EXPOSED PAD THAT MUST BE SOLDERED TO A METAL PLATE ON THE PCB FOR MECHANICAL REASONS AND TO GND.
2. THE LFCSP ALSO HAS TWO KEEPOUT AREAS TO THE TOP AND BOTTOM OF THE EXPOSED PAD. NO PCB TRACES OR VIAS CAN BE USED IN THESE AREAS.

Figure 10. 32-ld LFCSP Pin Configuration

Table 14. Pin Function Descriptions

Pin No.	Mnemonic[1]	Description
CLOCK INTERFACE		
8	XTAL_I/CLK_IN/REF_CLK	Input for crystal/single ended 25MHz reference clock.
		REF_CLK: In RMII mode, this pin also acts as the 50 MHz RMII reference clock input.
7	XTAL_O	Second input terminal for crystal. If using a single ended reference clock on XTAL_I/CLK_IN/REF_CLK, leave XTAL_O open circuit.
MANAGEMENT INTERFACE		
19	MDIO	Management Data Input/Output synchronous to the MDC clock. This pin requires a pull-up resistor to VDDIO.
18	MDC	Management Data Clock input up to 5.5 MHz.
17	INT_N/CRS	INT_N: Management interface interrupt pin output. Active low output. A low on INT_N indicates an unmasked management interrupt. This pin requires a pull-up resistor to VDDIO.
		CRS: MII carrier sense output- indicates the presence of a carrier to MAC.
RESET		
6	RESET_N	Active low input. Hold low for >10 µs. This pin requires a pull-up resistor to AVDD_3P3.

Pin No.	Mnemonic[1]	Description
MEDIA DEPENDENT INTERFACE (MDI)		
11	MDI_0_P	Transmit/receive differential pair 0 supporting 10/100 Mb/s.
12	MDI_0_N	Transmit/receive differential pair 0 supporting 10/100 Mb/s.
13	MDI_1_P	Transmit/receive differential pair 1 supporting 10/100 Mb/s.
14	MDI_1_N	Transmit/receive differential pair 1 supporting 10/100 Mb/s.
MAC INTERFACE		
23	RXD_3/**PHYAD_3**	RXD_3: RGMII/MII receive data 3 output. See MAC Interface section.
		PHYAD_3: PHY Address hardware configuration pin.
24	RXD_2/**PHYAD_2**	RXD_2: RGMII/MII receive data 2 output. See MAC Interface section.
		PHYAD_2: PHY Address hardware configuration pin.
26	RXD_1/**PHYAD_1**	RXD_1: RGMII/RMII/MII receive data 1 output. See MAC Interface section.
		PHYAD_1: PHY Address hardware configuration pin.
27	RXD_0/**PHYAD_0**	RXD_0: RGMII/RMII/MII receive data 0 output. See MAC Interface section.
		PHYAD_0: PHY Address hardware configuration pin.
28	RXC/RX_CLK/**MACIF_SEL0**	RXC: RGMII receive clock output, 25 MHz @ 100Mbps, 2.5MHz @ 10 Mbps.
		RX_CLK : MII receive clock output, 25 MHz @ 100Mbps, 2.5MHz @ 10 Mbps.
		MACIF_SEL0: MAC interface selection hardware configuration pin. See Table 22.
29	RX_CTL/RX_DV/ CRS_DV/**MACIF_SEL1**	RX_CTL: RGMII receive control signal. This is a combination of the RX_DV and RX_ER signals using both edges of RXC.
		RX_DV: MII mode received data valid output. When asserted high, it indicates that valid data is present on RXD_[3:0] in MII mode.
		CRS_DV: RMII mode Carrier Sense/Received Data Valid signal. This is a combination of the CRS and RX_DV signals and will be asserted while the receive medium is non-idle. See RMII Interface Mode section.
		MACIF_SEL1: MAC interface selection hardware configuration pin. See Table 22.
31	TXC/TX_CLK	TXC: RGMII transmit clock input, 25 MHz @ 100 Mbps, 2.5MHz @ 10 Mbps from MAC to PHY.
		TX_CLK: MII output clock from PHY to MAC. The TX_CLK frequency is 2.5 MHz in 10BASE-T mode and 25 MHz in 100BASE-TX mode. TX_CLK has a constant phase relationship to the XTAL_I/CLK_IN clock.
4	TXD_3	RGMII/MII transmit data 3 input. See MAC Interface section.
3	TXD_2	RGMII/MII transmit data 2 input. See MAC Interface section.
2	TXD_1	RGMII/RMII/MII transmit data 1 input. See MAC Interface section.
1	TXD_0	RGMII/RMII/MII transmit data 0 input. See MAC Interface section.
30	TX_CTL/TX_EN	TX_CTL: RGMII transmit control signal. This is a combination of the TX_EN and TX_ER signals using both edges of TXC.
		TX_EN : RMII/MII mode transmit enable input from the MAC to the PHY, indicating that transmission data is available on the TXD lines.

Pin No.	Mnemonic[1]	Description
LED INTERFACE		
16	LED_0/ COL/TX_ER/ **PHY_CFG0**	LED_0: Programmable LED indicator for general purpose LED with 8 mA drive capability. The LED can be active high or active low. Recommended use is active low. The ADIN1200 automatically senses the connection of the LED during power up and reset. By default, LED_0 is on when a link is established and blinking when there is activity.
		COL: MII collision detect output – indicates a collision condition.
		TX_ER: MII transmit error detected input from the MAC to the PHY – only available by default when EEE advertisement is enabled using hardware pin configuration (see Table 15).
		PHY_CFG0: 4-level hardware configuration pin for PHY configuration. See Table 20.
OTHER PINS		
20	LINK_ST/**PHY_CFG1**	LINK_ST: General purpose output used to output link status, indicating whether or not a valid link has been established. LINK_ST is active high by default (this can be changed by software).
		PHY_CFG1: 4-level hardware configuration pin for PHY configuration. See Table 20.
21	GP_CLK/RX_ER/**MDIX_MODE**	GP_CLK: General purpose output on which PHY clocks can be made available.
		RX_ER: RMII/MII mode receive error detected output. When asserted high, it indicates that the PHY has detected a Receive Error.
		MDIX_MODE: 4-level hardware configuration pin for Auto-MDIX configuration. See Table 21.
10	REXT	External bias reference resistor. Connect a 1% 3.01kΩ resistor (1 % tolerance, 100 ppm/°C TC) to GND.
22	LDO_CAP	Internal 0.9 V digital core power supply output pin. Connect a 0.1 µF ceramic capacitor to GND as close as possible to this pin.
POWER AND GROUND PINS		
9, 15	AVDD_3P3	3.3 V power supply input for the PHY MDI interface, analog circuitry, XTAL oscillator, DLL, RESET_N and LED circuitry. Connect 0.1 µF and 0.01 µF capacitors to GND as close as possible to these pins.
25, 32	VDDIO	3.3V/2.5V/1.8V MDIO and MAC interface power supply input. Connect 0.1 µF and 0.01µF capacitors to GND as close as possible to these pins. If using 3.3 V, to minimize power supplies, VDDIO and AVDD_3P3 can be connected to the same supply.
5	GND	This pin must be connected to GND.
	EP	Exposed Pad. The LFCSP package has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to GND.
	KEEPOUT AREA	This LFCSP package includes two exposed power bars adjacent to the exposed pad at the top and bottom, shown in the package outline. These are connected to internal power rails, the area around these is a keep-out zone.

[1]In cases where a pin is shared between a functional signal(s) and a hardware pin configuration signal(s), the hardware pin configuration signal(s) is in **bold** and the pin will be referred to using the functional signal(s) name throughout the datasheet.

Table 15. Pin Function Descriptions For Each MAC Interface Option

Pin No.	Pin Name[1]	MAC Interface Pin Function[7]			
		RGMII	**MII & EEE advertisement disabled[2]**	**MII & EEE advertisement enabled[2, 5]**	**RMII**
28	RXC/RX_CLK	RXC	RX_CLK	RX_CLK	
23	RXD_3	RXD_3	RXD_3	RXD_3	
24	RXD_2	RXD_2	RXD_2	RXD_2	
26	RXD_1	RXD_1	RXD_1	RXD_1	RXD_1
27	RXD_0	RXD_0	RXD_0	RXD_0	RXD_0
29	RX_CTL/RX_DV/CRS_DV	RX_CTL	RX_DV	RX_DV	CRS_DV
21	GP_CLK[3]/RX_ER		RX_ER	RX_ER	RX_ER
16	LED_0[3]/COL/TX_ER		COL	TX_ER[4]	
17	INT_N[3]/CRS		CRS		
31	TXC/TX_CLK	TXC	TX_CLK	TX_CLK	
8	XTAL_I/CLK_IN/REF_CLK				REF_CLK[6]
4	TXD_3	TXD_3	TXD_3	TXD_3	
3	TXD_2	TXD_2	TXD_2	TXD_2	
2	TXD_1	TXD_1	TXD_1	TXD_1	TXD_1
1	TXD_0	TXD_0	TXD_0	TXD_0	TXD_0
30	TX_CTL/TX_EN	TX_CTL	TX_EN	TX_EN	TX_EN

Hardware configuration pin signal(s) have been omitted for clarity.

[2] EEE advertisement enabled/disabled using hardware pin configuration – see Hardware Configuration Pins section.

[3] These pin functions can also be reconfigured via software.

[4] Since TX_ER shares a pin with COL, this pin is grouped with the PHY output pins, when in reality, TX_ER is a PHY input pin.

[5] EEE does not support half-duplex, hence no CRS or COL pin is required.

[6] A 50MHz reference clock must be supplied on XTAL_I/CLK_IN/REF_CLK pin when using the RMII MAC interface option.

[7] Wherever the field is left blank, the pin function is the first function listed in the Pin Name column.

THEORY OF OPERATION

The ADIN1200 is a low power, robust, single port 10/100 Ethernet transceiver with industry leading latency specifications primarily designed for industrial Ethernet applications. This design integrates an Energy Efficient Ethernet PHY core plus all the associated common analog circuitry, input and output clock buffering, the management interface and sub-system registers as well as the MAC interface and control logic to manage the reset and clock control and hardware pin configuration. The ADIN1200 is available in a 5 mm x 5 mm 32-ld package. Note that the MAC Interface section must be consulted for specific information on each MAC interface configuration mode.

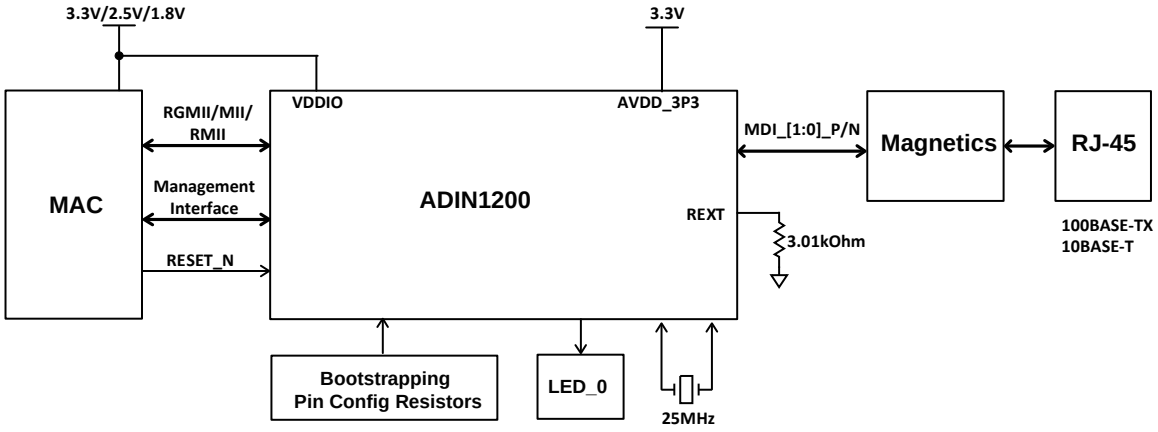


Figure 11. Basic System Block Diagram

POWER SUPPLY DOMAINS

The ADIN1200 has two power supply domains and can be supplied with a single supply if VDDIO is powered from 3.3 V.

- AVDD_3P3 is the 3.3 V analog power supply input for the PHY MDI interface, XTAL oscillator, DLL, RESET_N, and LED circuitry.
- VDDIO enables the MDIO and MAC interface voltage supply to be configured independently of the other circuitry on the ADIN1200. In most cases, RMII/MII will be operated at 3.3 V and RGMII at 2.5 V, but the MAC interface can operate at 3.3 V or 2.5 V or 1.8 V to allow maximum system flexibility depending on what is supported by the MAC.

MAC INTERFACE

The ADIN1200 provides the option of RGMII, MII or RMII MAC interface. The MAC interface can be selected using hardware configuration pins or via software. All MAC interfaces are capable of supporting 10Mbps and 100Mbps data rates.

RGMII Interface Mode

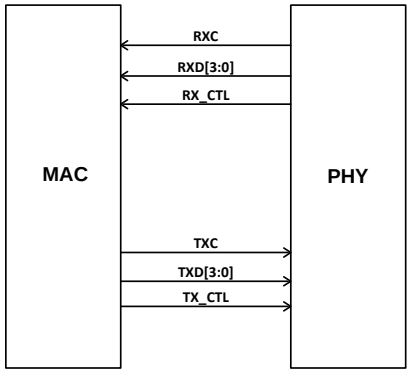


Figure 12. RGMII MAC-PHY Interface Signals

For the RX interface, the ADIN1200 generates a 25 MHz/2.5 MHz RXC signal to synchronize the RXD[3:0] receive data in100BASE-TX/10BASE-T modes respectively. The RX_CTL is a combination of the RX_DV and RX_ER signals (as described in the MII Interface Mode section) using both edges of RXC. The ADIN1200 transmits RX_DV on the positive edge of RXC and a combination (XOR function) of RX_DV and RX_ER on the negative edge of RXC.

For the TX interface, TXC is at 25 MHz and 2.5 MHz in100BASE-TX/10BASE-T modes respectively and the MAC transmits TXD[3:0] on both edges of TXC. TX_CTL is a combination of the TX_EN and TX_ER signals using both edges of TXC – TX_EN is transmitted on the positive edge of TXC and [TX_EN XOR TX_ER] is transmitted on the negative edge of TXC. Due to the fact that data is transmitted on both

edges of the clock, an accurate delay requirement of 2 ns is required on both clock edges (see Figure 5). This ensures that the delayed clock is at the centre of the data window ensuring accurate data capture. It is possible to enable this 2 ns delay on RXC only or on both RXC and TXC using hardware pin configuration settings (see Table 22). These delays can also be configured in software.

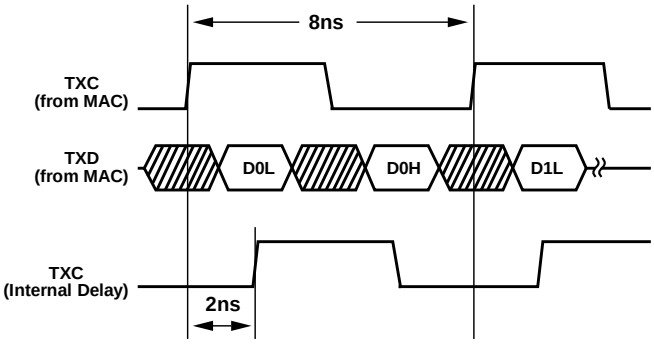


Figure 13. DLL Waveform

MII Interface Mode

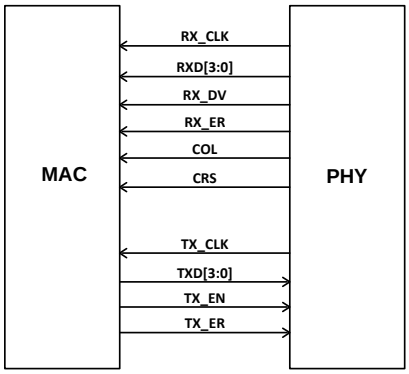


Figure 14. MII MAC-PHY Interface Signals

For the RX interface, the ADIN1200 generates a 25 MHz/2.5 MHz RX_CLK signal to synchronize the RXD[3:0] receive data in 100BASE-TX/10BASE-T modes respectively. RX_DV indicates to the MAC that there is valid data present on RXD[3:0]. RX_ER is driven high by the ADIN1200 if an error was detected in the frame that was received from the MDI side or during a false carrier event (in 100BASE-TX mode). The carrier sense output (CRS) indicates the presence of a carrier to the MAC, while the collision detect output (COL) is asserted in a collision condition.

For the TX interface, the PHY generates a 25 MHz/2.5 MHz reference clock on TX_CLK. The MAC transmits data on TXD[3:0] that is synchronized with TX_CLK. The MAC asserts TX_EN to indicate to the ADIN1200 that transmission data is available on the TXD[3:0] lines. Since TX_ER is not used in 10BASE-T mode, and is only used in 100BASE-TX mode for forward error propagation and for Energy Efficient Ethernet (EEE) Low Power Idle (LPI) request, TX_ER is not provided by default when EEE advertisement is not enabled using hardware pin configuration. However, with EEE advertisement enabled using the hardware pin configuration, the TX_ER signal is available on the LED_0 pin (see Table 15) and can be used by the MAC to request low power idle (LPI) mode.

RMII Interface Mode

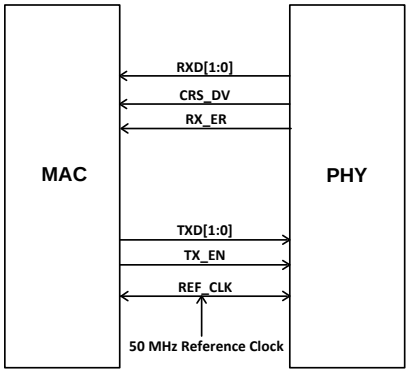


Figure 15. RMII MAC-PHY Interface Signals

A single 50 MHz reference clock (REF_CLK) is sourced from the MAC to PHY (or from an external source) for both the TX and RX interfaces.

The receive data, RXD[1:0], transitions synchronously to the reference clock, REF_CLK. The Carrier sense/Received data valid signal - CRS_DV - is a combination of the CRS and RX_DV signals and is asserted while the receive medium is non-idle. It is asserted asynchronously to REF_CLK and de-asserted synchronously. RX_ER is also synchronous to REF_CLK, and asserted when an error is detected in the received frame or when a false carrier is detected in 100BASE-TX mode. RX_ER assertion on false carrier can be disabled by software.

The MAC transmits TXD[1:0] synchronously to REF_CLK, and asserts TX_EN to indicate to the ADIN1200 that transmission data is available on the TXD[1:0] lines.

MANAGEMENT INTERFACE

The MII management interface provides a two-wire serial interface between a host processor or MAC and the ADIN1200 allowing access to control and status information in the sub-system and PHY core management registers. The interface is compatible with both IEEE Std 802.3 clause 22 and clause 45 management frame structures.

The PHY core registers at address 0x00 to 0x01F may be accessed using the interface specified under clause 22. The PHY core EMI (Extended Management Interface) registers and sub-system registers may be accessed at device address 0x1E using the interface specified under clause 45. However, for systems that do not support this interface, the registers at device address 0x1E can be accessed via registers 0x10 and 0x11 using clause 22 access.

The ADIN1200 is capable of generating an interrupt to a host processor or MAC using the INT_N pin.

MDI INTERFACE

The Media Dependent Interface (MDI) connects the ADIN1200 to the Ethernet network via a transformer as shown in Figure 8. The MDI_0_P/N are used to transmit when operating in MDI configuration and to receive when operating in MDIX configuration. The opposite is true of MDI_1_P/N in 10BASE-T and 100BASE-TX modes i.e. MDI_1_P/N are used to receive when operating in MDI configuration and to transmit when operating in MDIX-configuration. If Auto-MDIX is enabled, the ADIN1200 will automatically determine if the MDI or MDIX configuration should be used. Otherwise it will be forced to the chosen MDI or MDIX configuration.

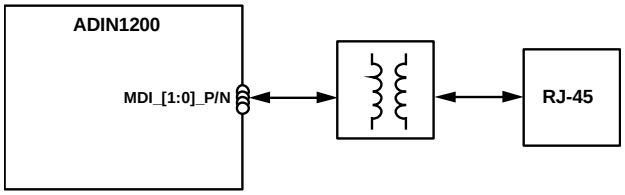


Figure 16. Media-Dependent Interface

RESET OPERATION

The ADIN1200 supports a number of resets - power-on reset, hardware reset and multiple software reset types. All of these put the ADIN1200, including the PHY core into a known state. Whenever the PHY core is reset, the MAC interface output pins (output pins with respect to the ADIN1200) are driven to a known idle state – all outputs except RXC/RX_CLK are driven low and RXC/RX_CLK is driven high.

Power-On Reset

The ADIN1200 includes power monitoring circuitry to monitor all of the supplies. At power-up the ADIN1200 is held in hardware reset until each of the supplies has crossed its minimum rising threshold value and the power is considered good. Brown out protection is provided by monitoring the supplies to detect if one or more of the supplies drops below a minimum falling threshold value and holding the part in hardware reset until the power is good again.

Hardware Reset

A hardware reset is initiated by the power-on reset circuitry or by asserting the RESET_N pin low. The pin should be brought low for a minimum of 10 µs. De-glitch circuitry is included on this pin to reject pulses shorter than approximately 1 µs.

When the RESET_N pin is de-asserted the crystal oscillator circuit is enabled and the clock is given time to stabilize. The state of the hardware configuration pins is read and latched, the digital and analog circuits are initialized and the PHY core clock multiplier unit (CMU) is reset. After 5 ms from the de-assertion of RESET_N, the management interface registers are accessible and the part can be programmed. This time is significantly shorter if a single-ended clock rather than a crystal is used and the management interface registers are accessible 3 ms after the de-assertion of RESET_N. If the ADIN1200 is configured to enter software powerdown after reset (see Table 20), the ADIN1200 will enter software powerdown mode and an interrupt will be generated to indicate a hardware reset occurred.

Following a Hardware Reset:

- The crystal oscillator circuit is enabled and time is allowed for the clock to stabilize.
- The hardware configuration pins are read and the values latched. These set the default values of the pin-dependent registers in the sub-system and PHY core registers.
- The MAC interface block is reset.
- The PHY core is reset.
- The PHY core CMU is reset.
- An interrupt to indicate a hardware reset occurred is generated depending on the pin configuration (if the ADIN1200 was configured to enter Software Powerdown mode after Reset).

Software Reset

The ADIN1200 supports a number of different software resets that reset specific circuit blocks under software control:

- Sub-System Software Reset with Pin Configuration
- Sub-System Software Reset
- PHY Core Software Reset

Sub-System Software Reset with Pin Configuration

The ADIN1200 supports a software reset capability that behaves in a very similar way to a hardware reset (see rows 1 and 2 of Table 16). A sub-system reset with pin configuration can be initiated by setting GeSftRstCfgEn (sub-system GeSftRstCfgEn register 0x1E.0xFF0D bit 0) to '1' before setting GeSftRst (sub-system GeSftRst register 0x1E.0xFF0C bit 0) to '1'. This sub-system software reset follows the same reset sequence as the power-on reset and hardware reset except that the crystal oscillator is not disabled and the clock stabilization step is skipped. The state of the hardware configuration pins is read and latched. These set the default values of the pin-dependent registers in the sub-system and PHY core registers. The MAC interface block and PHY core are reset. If a 125 MHz clock is selected as the PHY output clock the GP_CLK pin, the PHY core CMU is not reset, otherwise the CMU is reset. The main difference between this type of reset and a hardware reset is that the crystal oscillator is not disabled. Note the GeSftRstCfgEn bit is reset to its default value of zero by this type of reset.

Following a Sub-System Software Reset with Pin Configuration:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are read and the values latched. These set the default values of the pin-dependent registers in the sub-system and PHY core registers.
- The MAC interface block is reset.
- The PHY core is reset.
- The PHY core CMU is reset.
- If a 125 MHz clock is selected as the PHY output clock it is not available on the GP_CLK pin during this reset.

Sub-System Software Reset

The sub-system can be reset by setting GeSftRst (sub-system GeSftRst register 0xFF0C bit 0) to '1'. This bit is self-clearing. Setting this bit resets the sub-system and PHY core registers, the MAC interface block and the PHY core. It does not re-read the hardware configuration pins and uses previously latched values of the hardware configuration pins to set the default values of the pin-dependent registers in the sub-system and PHY core registers.

Following a Sub-System Software Reset:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are not re-read. The pin-dependent registers in the sub-system registers and PHY core registers are reset to the default values defined by the previously latched values of the hardware configuration pins.
- The MAC interface block is reset.
- The PHY core is reset.
- If a 125 MHz clock is selected as the PHY output clock the GP_CLK pin, the PHY core CMU is not reset, otherwise the CMU is reset.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin during this reset.

PHY Core Software Reset

The PHY core registers can be reset by setting SftRst (PHY core MiiControl register 0x0000 bit 15) to '1'. This bit is self-clearing. Setting this bit resets the PHY core registers, the MAC interface block and the PHY core. It does not re-read the hardware configuration pins and uses previously latched values of the hardware pins to set the default values of the pin-dependent registers in the PHY core registers. The sub-system registers are not reset to default values. This is a useful way to reset the PHY core registers to a known configuration defined by software without resetting the rest of the ADIN1200 circuitry.

Following a PHY Core Software Reset:

- The crystal oscillator circuit is not disabled during this type of reset.
- The hardware configuration pins are not re-read. The pin-dependent registers in PHY core registers are reset to the default values defined by the previously latched values of the hardware configuration pins. The sub-system registers are not reset to their default values.
- The MAC interface block is not reset.
- The PHY core is reset.
- If a 125 MHz clock is selected as the PHY output clock the GP_CLK pin, the PHY core CMU is not reset, otherwise the CMU is reset.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin during this reset.

Table 16. ADIN1200 Reset Options Summary

	Reset Type	H/W Pin Config values latched following reset?	Sub-system registers reset?	PHY core registers reset?	MAC interface block reset?	XTAL Osc disabled during reset ?	GP_CLK output (if enabled) available during reset?
1	Hardware Reset	Yes	Yes	Yes	Yes	Yes	No
2	Sub-System S/W Reset with Pin Config	Yes	Yes	Yes	Yes	No	No
3	Sub-System S/W Reset	No	Yes	Yes	Yes	No	Yes
5	PHY Core S/W Reset	No	No	Yes	No	No	Yes

POWERDOWN MODES

The ADIN1200 supports a number of powerdown modes - hardware powerdown, software powerdown, energy-detect powerdown and Energy Efficient Ethernet (EEE) low power idle (LPI) mode. The lowest power mode is hardware powerdown where the part is turned fully off and is not accessible.

- The ADIN1200 enters hardware powerdown mode when the RESET_N pin is asserted and held low. Hardware powerdown is a useful mode when operation of the ADIN1200 is not required and power is to be minimized.
- In software powerdown mode the ADIN1200 is powered down but the management interface can be accessed and the ADIN1200 can be configured. The ADIN1200 will not attempt to bring up links until enabled.
- In energy-detect powerdown mode the ADIN1200 is powered down but will still monitor the line for signal energy. Typically the ADIN1200 enters this mode when there is no cable plugged in and will remain in this mode until a remote link partner is available.
- If EEE is advertised by the local and remote PHYs an EEE link will be brought up. If there is no data to be sent, the MAC requests the ADIN1200 to enter EEE low power idle mode. When the MAC or remote PHY wishes to send data the ADIN1200 PHY wakes up within 20 μs for 100BASE-TX and can send or receive data.

Hardware Powerdown Mode

Hardware powerdown is a useful mode when operation of the ADIN1200 is not required and power is to be minimized. The ADIN1200 enters hardware powerdown mode when the RESET_N pin is asserted and held low. In this mode all analog and digital circuits are disabled, the CMU is disabled, the clocks are gated off and the only power is the leakage power of the circuits. The management interface registers are not accessible in this mode.

While in Hardware Powerdown Mode:

- All analog and digital circuits are disabled.
- The MAC interface output pins (output pins with respect to the ADIN1200) are tri-stated. Internally these pins have a weak pull-down resistor, so these outputs will be pulled low. This assumes no external pull-up resistors connected to these pins.
- All internal clocks are gated off.
- The PHY output clock (available on the GP_CLK pin) is disabled.
- The management interface registers are not accessible.

Software Powerdown Mode

Software powerdown mode is a useful mode when the part is being configured by software before links are brought up. The ADIN1200 can be configured to enter software powerdown mode after reset using the appropriate pull-up / pull-down resistors on the LINK_ST and LED_0 pins which sets the default value of SftPd (PHY core MiiControl register 0x0000 bit 11) to '1'. The ADIN1200 also enters software powerdown mode when the SftPd bit is set to 1 in software. In software powerdown mode the analog and digital circuits are in a low power state, typically the CMU is disabled[1], most clocks are gated off and the clock for the remaining digital circuitry runs at 25 MHz. Any signal or energy on the MDI pins (MDI_[1:0]_P/N) is ignored and no links will be brought up. The management interface registers are accessible and the part can be configured using software.

While in Software Powerdown Mode:

- All analog transmit and receive circuits are disabled.
- The MAC interface output pins (output pins with respect to the ADIN1200) are driven to a known idle state – all outputs except RXC/RX_CLK are driven low and RXC/RX_CLK is driven high.
- Most internal clocks are gated off.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.

The ADIN1200 exits software powerdown mode when the SftPd bit is cleared. At this point the PHY will attempt to bring up links according to its configuration. For example, if Auto-Negotiation is enabled and all speeds enabled it will advertise all speeds and start to send Auto-Negotiation link pulses.

Energy-Detect Powerdown Mode

Energy-detect powerdown mode can be enabled using the appropriate pull-up / pull-down resistors on the LINK_ST and LED_0 pins (see Table 20) or by setting NrgPdEn (PhyCtrlStatus2 register 0x15 bit 3) to '1'. When the PHY is in normal operation (not software powerdown) and energy-detect powerdown mode is enabled, the PHY will enter energy-detect powerdown mode after a number of seconds of silence on the line. This is a very low power mode in which the analog and digital circuits are in a low power state, typically the CMU is disabled[1] and most clocks are gated off. The PHY monitors the line for signal energy and sends a link pulse once every second. If signal energy is detected the PHY will exit energy-detect powerdown mode and start sending link pulses.

While in Energy-Detect Powerdown Mode:

[1] If the ADIN1200 is configured to output a 125 MHz clock on the GP_CLK pin then the CMU will be enabled and the power in this mode will be higher.

- All analog and digital circuits are disabled.
- Most internal clocks are gated off.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.
- The PHY monitors the line for signal energy.

Typically, the PHY enters energy-detect powerdown mode when the cable is unplugged and will exit this mode when a cable is plugged in and a remote link partner appears. In this mode the PHY periodically wakes up and transmits a link pulse on both MDI_0 and MDI_1 to ensure that a lock-out is avoided where both local and remote PHY are in an energy-detect powerdown mode.

Energy Efficient Ethernet Low Power Idle Mode

Energy Efficient Ethernet mode can be enabled using the appropriate pull-up / pull-down resistors on the LINK_ST and LED_0 pins (see Table 20) or by setting Eee1000Adv or Eee100Adv (EeeAdv register address 0x1E.0x8001 bit 2 or bit 1) to '1'. During link Auto-Negotiation, the local and remote PHYs advertise the speeds supported, including if they are EEE capable and the PHYs then attempt to bring up a link at the highest speed supported by both sides. If EEE is advertised by both the local and remote PHYs for the established link speed then the link is an EEE link. If there is an EEE link and if at some point in time there is no data to be sent, the MAC will request the ADIN1200 to enter EEE LPI mode which is almost as low power as energy-detect powerdown mode. The ADIN1200 wakes-up periodically to transmit refresh signals that are used by the link partner to update adaptive filters and timing circuits in order to maintain link integrity.

While in EEE LPI Mode:

- All analog and digital circuits are in a low power mode.
- Most internal clocks are gated off.
- The selected PHY output clock (if enabled) is available on the GP_CLK pin.
- The management interface registers are accessible.
- The PHY monitors the line for an LPI wake signal.

When the local or remote PHY wishes to send data the PHY initiates an LPI wake sequence and the PHYs can then start to send or receive data within 20 μs for 100BASE-TX.

STATUS LED

The ADIN1200 provides a configurable status LED. The LED can be used to indicate the speed of operation, link status, duplex mode, etc. and can be active high or active low. The recommendation is to use the LED as active low. The ADIN1200 automatically senses the connection of the LED during power up and reset, e.g. if it senses that the pin is pulled to a supply, it will configure the LED for active low operation. By default LED_0 is on when a link is established and it blinks when there is activity. The default LED operation can be overwritten in software using the PHY LED control registers, LedCtrl1, LedCtrl2 and LedCtrl3 (register addresses 0x1B, 0x1C and 0x1D). The LED_0 pin is also shared with Pin Configuration functions as defined in Table 20.

PHY OUTPUT CLOCKS

A number of internal PHY clock signals can be made available at the GP_CLK pin:

- 125 MHz free running clock
- 25 MHz clock
- 25/125 MHz recovered clock

This is configured in software. By default, the PHY clock is off. Note also that selecting the 125 MHz free running clock has an impact on power consumption, as the CMU will be powered up all the time except during reset and power up.

HARDWARE CONFIGURATION PINS

The ADIN1200 can operate in unmanaged or managed applications. In unmanaged applications, it is possible to configure the desired operation of the PHY from hardware configuration pins without any software intervention. The PHY should be configured not to enter software powerdown after reset and it will thus immediately start to attempt to bring up links as configured by the PHY_CFG[1:0] hardware configuration pins.

In managed applications, software is available to configure the PHY via the management interface. In this case, it is possible to configure the PHY to enter software powerdown after reset such that the PHY can be configured before linking is attempted.

Hardware configuration pins are pins shared with functional pins and the voltage level on the pin is sensed upon exiting from a reset. Some hardware configuration pins are multi-level sense, while others are 2-level sense. Using two resistors - R_LO and R_HI (see Figure 9) - four different voltage levels can be sensed as shown in Table 17. Only Mode 1 ('L') and Mode 4 ('H') are relevant to the 2-level sense pins and these are implemented with a 10 kOhm pull-down resistor or a 10 kOhm pull-up resistor respectively. Note that LED_0 needs to be pulled up to AVDD_3P3 rail rather than VDDIO.

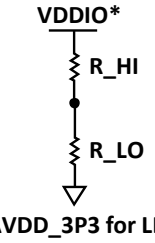


Figure 17. Hardware Configuration Pin Implementation

Note that the values listed in Table 17 assume no extra loading from circuitry external to the ADIN1200. It is likely that some configuration pins could be connected to an FPGA input which could have it's own internal pull-up/pull-down resistor. This will load the resistor divider voltage. Assuming a pull-up resistor >43 kΩ and pull-down resistor >37 kΩ, the 10kΩ resistor used in Mode 1 and Mode 4 should be replaced with a 2.5 kΩ resistor.

Table 17. Configuration modes

Mode	R_LO	R_HI	Voltage Threshold
MODE_1	10 kOhm	Open	
MODE_2	10 kOhm	56 kOhm	>0.1 x VDDIO[1]
MODE_3	56 kOhm	10 kOhm	>0.5 x VDDIO[1]
MODE_4	Open	10 kOhm	>0.9 x VDDIO[1]

[1]Note that the supply rail for LED_0 pin is AVDD_3P3 rather than VDDIO.

HARDWARE CONFIGURATION PIN FUNCTIONS

The following functions are configurable from the ADIN1200 hardware pins (see Table 8 for pin details):

- PHY Address
- Forced/Advertised PHY Speed[1]
- Software Powerdown Mode after Reset[1]
- Downspeed Enable[1]
- Energy Detect Powerdown Mode[1]
- Energy Efficient Ethernet Enable[1]
- Auto-MDIX
- MAC Interface Selection (RGMII/RMII/MII)

[1] All of these functions are available from PHY_CFG[1:0] pins.

Table 18. Hardware Configuration Pin Summary

Configuration function	Functional Pin/ Configuration Function Mnemonic	Pin Levels	Internal Pull-up/Pull-down	Default Configuration
PHYAD[3:0] Configuration	RXD_3/**PHYAD_3**	2	Pull-down	PHY Address 0x0
	RXD_2/**PHYAD_2**	2	Pull-down	
	RXD_1/**PHYAD_1**	2	Pull-down	
	RXD_0/**PHYAD_0**	2	Pull-down	
Forced/Advertised PHY Speed, Software Powerdown Mode after Reset, Downspeed Enable, Energy Detect Powerdown Mode, Energy Efficient Ethernet	LINK_ST/**PHY_CFG1**	4	None	Unknown (external resistors are required)
	LED_0/COL/TX_ER/**PHY_CFG0**	4		
Auto-MDIX	GP_CLK/RX_ER/**MDIX_MODE**	4	None	Unknown (external resistors are required)
MAC Interface Selection	RX_CTL/RX_DV/CRS_DV/**MACIF_SEL1**	2	Pull-down	RGMII RXC/TXC 2 ns delay
	RXC/RX_CLK/**MACIF_SEL0**	2	Pull-down	

PHY Address Configuration

PHY address configuration is shared with the RXD_3 to RXD_0 pins and can be configured according to Table 19. Four of the ADIN1200 pins are available for configuring the PHY address. These are two level configuration pins, which means that it is possible to configure the ADIN1200 to any of the 16 PHY addresses possible. In many applications, the default address of 0x0 is used and in that case it may not be necessary to configure these pins externally because the RXD_3 to RXD_0 pins have weak internal pull-down resistors. This assumes that no other system level circuitry attached to these nodes, such as the MAC or Ethernet switch, has internal pull-up resistors on these pins.

Table 19. PHY Address Configuration

PHY Address	PHYAD_3	PHYAD_2	PHYAD_1	PHYAD_0
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

PHY Configuration

The PHY_CFG1 and PHY_CFG0 hardware configuration pins cover a number of functions and can be configured according to Table 20:

- Forced/Advertised PHY Speed
- Software Powerdown Mode after Reset
- Downspeed Enable
- Energy Detect Powerdown (EDPD) Mode
- Energy Efficient Ethernet (EEE) Enable

The pins associated with PHY_CFG1 and PHY_CFG0 have no internal pull-up resistors so external resistors must be used to configure these functions.

Table 20. PHY Configuration

Forced/ Advertised	Speed Configuration	Other Functions Enabled[1]	PHY_CFG1	PHY_CFG0	Row No.
Advertised Speeds (Auto-Neg Enabled)	10 HD/FD & 100 HD/FD	Downspeed, EDPD and EEE	MODE_4	MODE_4	1
	10 HD/FD & 100 HD/FD		MODE_1	MODE_4	2
	10 HD/FD & 100 HD/FD	Software Powerdown Mode after Reset	MODE_3	MODE_4	3
	10 FD & 100 FD		MODE_4	MODE_3	4
	100 FD		MODE_4	MODE_1	5
Forced Speed (Auto-Neg Disabled)	10 FD		MODE_1	MODE_2	6
	100 HD		MODE_2	MODE_2	7
	100 FD		MODE_3	MODE_3	8

[1] If no function is listed in this column, then only the PHY speed is configured using this row.

Forced/Advertised PHY Speed

As outlined in Table 20, it is possible to advertise all or a subset of PHY speed capabilities, set half-duplex or full-duplex mode as well as enable/disable auto-negotiation. Auto-Negotiation is enabled for the first 5 rows in the table – i.e. in the case of Advertised Speed modes. The first three rows have the same speed configuration, however, in row 1, three other functions are also enabled - Downspeed, Energy Detect Power Down and EEE – and in row 3, the ADIN1200 will enter software powerdown mode after reset. It is also possible to configure forced speed modes where Auto-Negotiation is disabled and the speed is forced (rows 6 to 8).

Software Powerdown after Reset

If the ADIN1200 is configured so that it does not enter Software Powerdown mode after reset, the ADIN1200 will attempt to bring up links at the configured speeds and MDI/MDIX configuration once it exists reset. If the ADIN1200 is configured so that it enters Software Powerdown Mode after Reset (row 3), the ADIN1200 will wait in Software Powerdown mode until it is configured over the MDIO interface at which point, the PHY configuration can be set by software.

Downspeed Configuration

If Downspeed is enabled, the PHY will down speed to a lower speed after a number of attempts if it cannot link at the highest speed advertised. The default operation of Downspeed can be overwritten in software by writing to DnSpeedTo100En (PhyCtrl2 register, address 0x16, bit 11), DnSpeedTo10En (PhyCtrl2 register, address 0x16, bit 10) and NumSpeedRetry (PhyCtrl3 register, address 0x17, bits [12:10]).

Energy Detect Powerdown Configuration

If Energy Detect Powerdown is enabled and no energy is detected at the MDI pins, then the ADIN1200 will enter a low power mode. Thus, this mode saves power where there is no cable connected or the remote PHY is powered down.

Energy Efficient Ethernet

If Energy Efficient Ethernet is enabled and also advertised by the remote PHY, the ADIN1200 can enter a low power mode (low power idle) when no data is being transmitted by either end.

Auto MDIX Configuration

Auto-MDIX configuration mode is shared with the GP_CLK pin and can be configured according to Table 21. This pin does not have an internal pull-up resistor so external resistors must be used to set the MDI/MDIX mode.

Table 21. Auto MDIX Configuration

Configuration	MDIX_MODE
Manual MDI	MODE_1
Manual MDIX	MODE_2
Auto MDIX – Prefer MDIX	MODE_3
Auto MDIX – Prefer MDI	MODE_4

If Auto-MDIX is enabled (MODE_3 or MODE_4), the ADIN1200 will automatically determine if the MDI or MDIX configuration should be used. Otherwise, it will be forced to the chosen MDI or MDIX configuration.

If enabling Auto-MDIX, the ADIN1200 supports Auto-MDIX with a preference for MDI or MDIX. This determines which MDI/MDIX setting the auto crossover algorithm should start with. If the local and remote PHY are configured with one set to Auto MDIX – Prefer MDI and the other to Auto MDIX – Prefer MDIX then a much faster resolution of Auto MDIX will be achieved. This has the advantage of still being able to work with a mis-match of wiring and still optimizing the time to resolve Auto-MDIX.

The default operation of Auto-MDIX can be overwritten in software by writing to AutoMdiEn (PhyCtrl1 register, address 0x12, bit 10) and ManMdix (PhyCtrl1register, address 0x12, bit 9).

MAC Interface Selection

The MAC interface selection is shared with the RX_CTL/RX_DV/CRS_DV and RXC/RX_CLK pins and can be configured according to Table 22. In RGMII mode, it is possible to enable a 2 ns delay on RXC only or on both RXC and TXC. The RX_CTL/RX_DV/CRS_DV and RXC/RX_CLK pins have weak internal pull-down resistors so, by default the ADIN1200 is configured in RGMII mode with a 2 ns delay on RXC and TXC. External resistors must be used to select any of the remaining MAC interface modes.

The MAC interface selection can also be done via software (GeRgmiiCfg and GeRmiiCfg registers) with the internal 2 ns delay configured using the GeRgmiiRxldEn and GeRgmiiTxldEn bits within the GeRgmiiCfg register (address 0x1E.0xFF23, bits 1 and 2). The PHY should be put in software powerdown (setting SftPd, MiiControl register, address 0x00, bit 11) before any changes are made to the MAC interface configuration registers. As RMII mode requires a 50 MHz reference clock, software should not be used to configure the MAC interface to RMII.

Table 22. MAC Interface Selection

MAC Interface Selection	MACIF_SEL1	MACIF_SEL0
RGMII RXC/TXC 2 ns delay	L	L
RGMII RXC only 2 ns delay	H	L
MII	L	H
RMII	H	H

ON-CHIP DIAGNOSTICS

LOOPBACK MODES

The PHY core provides several loopback modes as shown in Figure 18 – All Digital loopback, External Cable loopback, Line Driver loopback and Remote loopback. These loopback modes test and verify various functional blocks within the PHY. The use of frame generators and frame checkers allow completely self-contained in-circuit testing of the digital and analog data paths within the PHY core.

The default loopback mode is All Digital loopback. This loops the data within the PHY at the analog/digital boundary. This checks correct operation of the PHY but does not require the external analog components, connections or analog supplies to be correct. In All Digital loopback it is possible to also transmit to the MDI pins which can be useful for transmit testing. By default, the LbAllDigSel bit (PhyCtrlStatus1 register , address 0x0013, bit 12) is set, which selects All Digital Loopback and the LbTxSup bit (bit 6 within the same PhyCtrlStatus1 register) is also set which suppresses the transmission of the signal to the MDI pins. Setting the PhyCtrlStatus1 register to a value of 0x1001 selects Digital Loopback with transmission to the MDI pins. The Loopback bit (MiiControl register, address 0x0000, bit 14) also needs to be set to enable All Digital loopback.

External Cable loopback verifies the full analog and digital path including the external components and cable. This requires that pair 0 and 1 are shorted together to provide an analog loopback at the end of the cable. The signal processing is adjusted so that the transmitted signal is not cancelled. Setting the LbExtEn bit (PhyCtrlStatus1 register, address 0x0013, bit 9) enables External Cable loopback.

Unlike External Cable loopback, for Line Driver loopback, the MDI pins should be left open-circuit, thereby transmitting into an unterminated connector/cable. The PHY can then operate by receiving the reflection from its own transmission. This provides similar capabilities to the External Cable loopback without the need to create any wire shorts – simply unplug the cable. Setting the LbLdSel bit (PhyCtrlStatus1 register, address 0x0013, bit 10) selects Line Driver loopback. The Loopback bit (MiiControl register, address 0x0000, bit 14) also needs to be set to enable Line Driver loopback.

Remote loopback requires a link up with a remote PHY and it loops the data received from the remote PHY back to the remote PHY. This allows a remote PHY to verify a complete link by ensuring it receives the correct data back. Setting the PhyCtrlStatus1 register to a value of 0x0241 selects Remote Loopback whereby the data received by the PHY is also sent to the MAC. Also setting the LbTxSup bit within the PhyCtrlStatus register and thereby setting the register value to 0x0341 selects Remote Loopback, whereby the data received by the PHY is not sent to the MAC. For this type of loopback, the Loopback bit (MiiControl register, address 0x0000, bit 14) should not be set.

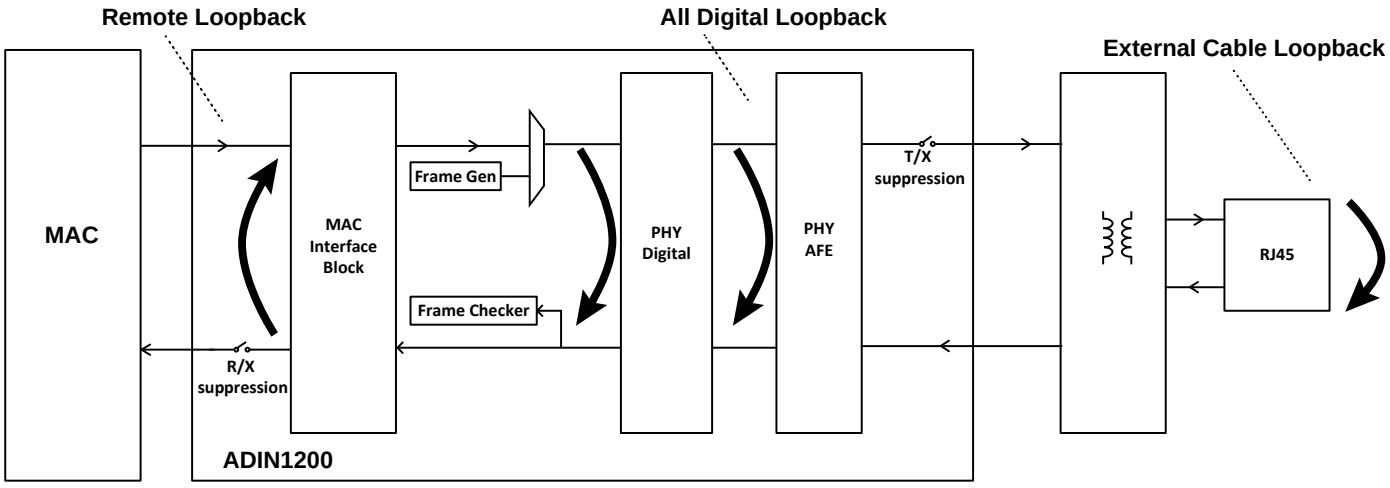


Figure 18. ADIN1200 Loopback Modes

FRAME GENERATOR AND CHECKER

The ADIN1200 can be configured to generate frames and to check received frames (see Figure 18). The frame generator and checker can be used independently to just generate frames or just check frames or can be used together to simultaneously generate frames and check frames. If frames are looped back at the remote end, the frame checker can be used to check frames generated by the ADIN1200.

When the frame generator is enabled the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator the diagnostic clock must also be enabled, (set DiagClkEn bit, PhyCtrl1 register, address 0x0012, bit 2).

The frame generator control registers configure the type of frames to be sent (random data, all ones, etc.), the frame length and the number of frames to be generated. The generation of the requested frames starts by enabling the frame generator (set FgEn bit, FgEn register, address 0x1E.0x9415, bit 0). When the generation of the frames is completed the frame generator done bit will be set (FgDone bit, FgDone register address, 0x1E.0x941E, bit 0).

The frame checker is enabled using the frame checker enable bit (set FcEn bit, FcEn register, address 0x1E.0x9403, bit 0). The frame checker can be configured to check and analyze received frames from either the MAC interface or the PHY. This is configured using the frame checker Tx select bit, (set FcTxSel bit, FcTxSel register, address 0x1E.0x9407, bit 0). The frame checker reports the number of frames received, CRC errors and various other frame errors. The frame checker frame counter and frame checker error counter registers count these events.

The frame checker counts the number of CRC errors and these are reported in the receive error counter register (RxErrCnt register, address 0x0014). To ensure synchronization between the frame checker error counter and frame checker frame counters, all of the counters are latched once the receive error counter register is read. Hence when using the frame checker, the receive error counter should be read first and then all the other frame counters and error counters should be read. A latched copy of the receive frame counter register is available in the FcFrmCntH and FcFrmCntL registers (register addresses 0x1E.0x940A and 0x1E.0x940B).

In addition to CRC errors, the frame checker counts frame length errors, frame alignment errors, symbol errors, oversized frame errors and undersized frame errors. In addition to the received frames, the frame checker counts frames with an odd number of nibbles in the frame in 100BASE-TX or 10BASE-T mode and counts frames with an odd number of nibbles in the preamble in 100BASE-TX mode. It also counts frames with a non-integer number of nibbles in 10BASE-T mode and the number of false carrier events - which is a count of the number of times the BAD SSD state is entered.

CABLE DIAGNOSTICS

The ADIN1200 has on-chip cable diagnostics capabilities. This cable analysis can be used to detect cable impairments that may be preventing the establishment of the link speed or degrading performance and can be performed both when the link is up or when the link is down.

Each time a 100BASE-TX link is brought up the ADIN1200 reports an estimate of the cable length based on the signal processing. This can be read in the cable diagnostics cable length estimate register, (CdiagCblLenEst register, address 0x1E.0x9407). This estimate is not available for a 10BASE-T link. A polarity inversion on each pair is reported in the pair polarity inversion register bits, (PolInv register address 0x001F, bits [11:10] and B10PolInv register bit (PhyStatus1 register, address 0x001A, bit 10). Pair swaps are reported in the pair swap register bit (Pair01Swap register address 0x001A, bit 11). When the link is up the signal quality on each pair is indicated in the mean square error register for each pair, (mseA/mseB/mseC/mseD registers, addresses 0x1E.0x8402:5, bits 7 – 0).

When the link is down the ADIN1200 can run cable fault detection using time domain reflectometry (TDR). By transmitting pulses and analyzing the reflections the PHY can detect cable faults like opens, shorts, cross-pair shorts, and the distance to the nearest fault. It can also determine that the pair is well terminated and does not have any faults. The remote PHY should be put in a power down state or disconnected to run cable fault detection as remote PHY link pulses may interfere with the analysis of the reflected pulses and may return a pair busy result.

The cable fault detection is automatically run on the two pairs looking at all combinations of pair faults by first putting the PHY in standby (clear LinkEn bit, PhyCtrl3 register, address 0x0017, bit 13) and then enabling the diagnostic clock (set DiagClkEn bit, PhyCtrl1 register address 0x0012, bit 2). Cable diagnostics can then be run (set CdiagRun bit, CdiagRun register, address 0x1E.0xBA1B, bit 0). The results are reported for each pair in the cable diagnostics results registers, (CdiagDtldRslts0/CdiagDtldRslts1), addresses 0x1E.0xBA1D & BA1E). The distance to the first fault for each pair is reported in the cable fault distance registers,(CdiagFltDist0/CdiagFltDist1), addresses 0x1E.0xBA21 & BA22).

REGISTER SUMMARY

The MII management interface provides a two-wire serial interface between a host processor or MAC and the ADIN1200 allowing access to control and status information in the sub-system and PHY core management registers. The interface is compatible with both IEEE Std 802.3 clause 22 and clause 45 management frame structures.

The device supplements the registers specified in IEEE Std. 802.3 with an additional set of registers that are accessed indirectly. These registers are referred to as Extended Management Interface (EMI) registers. The EMI registers may be accessed using the interface specified under clause 45. However for systems that do not support this interface an alternative access mechanism is provided using the interface specified under clause 22.

The following two sections list the PHY core and sub-system registers.

PHY CORE REGISTER SUMMARY

The PHY core registers are made up of three register groupings:

1. 0x0000 to 0x000F - IEEE standard registers
2. 0x0010 to 0x001F – Vendor specific registers
3. PHY core EMI registers at device address 0x1E

The IEEE standard registers and vendor specific registers are accessed using clause 22 access while the EMI registers are accessed using clause 45 access. The ADIN1200 supports the IEEE Clause 45 MDIO Manageable Device (MMD) registers associated with EEE. These registers are all remapped to the device address 0x1E so they are available at the same device address as the rest of the PHY extended management registers. For systems that do not support the interface specified under clause 45, the EMI registers can be accessed using clause 22 access via registers 0x0010 and 0x0011.

The default value of some of the registers are determined by the value of the hardware configuration pins which are read just after the RESET_N pin is de-asserted (see Hardware Configuration Pins section). This allows the default operation of the ADIN1200 to be configured in unmanaged applications. The default values in the tables below assume the ADIN1200 is configured as follows:

- Auto MDIX – Prefer MDI
- Auto-negotiation enabled.
- All speeds advertised.
- EEE, Energy Detect Powerdown and Downspeed disabled.
- ADIN1200 is not configured to enter software powerdown after reset.
- RGMII MAC interface selected with 2ns internal delay on RXC & TXC.

Table 23. PHY Core Register Summary

Address	Name	Description	Reset	Access
0x0000	MiiControl	MII Control Register.	0x1040	R/W
0x0001	MiiStatus	MII Status Register.	0x7949	R
0x0002	PhyId1	PHY Identifier 1 Register.	0x0283	R
0x0003	PhyId2	PHY Identifier 2 Register.	0xBC20	R
0x0004	AutonegAdv	Auto-Negotiation Advertisement Register.	0x01E1	R/W
0x0005	LpAbility	Auto-Negotiation Link Partner Base Page Ability Register.	0x0000	R
0x0006	AutonegExp	Auto-Negotiation Expansion Register.	0x0064	R
0x0007	TxNextPage	Auto-Negotiation Next Page Transmit Register.	0x2001	R/W
0x0008	LpRxNextPage	Auto-Negotiation Link Partner Received Next Page Register.	0x0000	R
0x0010	ExtRegPtr	Extended Register Pointer Register.	0x0000	R/W
0x0011	ExtRegData	Extended Register Data Register.	0x0000	R/W
0x0012	PhyCtrl1	PHY Control 1 Register.	0x0002	R/W
0x0013	PhyCtrlStatus1	PHY Control Status 1 Register.	0x1041	R/W
0x0014	RxErrCnt	Rx Error Count Register.	0x0000	R
0x0015	PhyCtrlStatus2	PHY Control Status 2 Register.	0x0000	R/W
0x0016	PhyCtrl2	PHY Control 2 Register.	0x0308	R/W
0x0017	PhyCtrl3	PHY Control 3 Register.	0x3048	R/W

Address	Name	Description	Reset	Access
0x0018	IrqMask	Interrupt Mask Register.	0x0000	R/W
0x0019	IrqStatus	Interrupt Status Register.	0x0000	R
0x001A	PhyStatus1	PHY Status 1 Register.	0x0300	R
0x001B	LedCtrl1	LED Control 1 Register.	0x0001	R/W
0x001C	LedCtrl2	LED Control 2 Register.	0x210A	R/W
0x001D	LedCtrl3	LED Control 3 Register.	0x1855	R/W
0x001F	PhyStatus2	PHY Status 2 Register.	0x03FC	R
0x8000	EeeCapability	Energy Efficient Ethernet Capability Register.	0x0006	R
0x8001	EeeAdv	Energy Efficient Ethernet Advertisement Register.	0x0000	R/W
0x8002	EeeLpAbility	Energy Efficient Ethernet Link Partner Ability Register.	0x0000	R
0x8008	EeeRslvd	Energy Efficient Ethernet Resolved Register.	0x0000	R
0x8402	MseA	Mean Square Error A Register.	0x0000	R
0x9400	RxMiiClkStopEn	Receive MII Clock Stop Enable Register.	0x0400	R/W
0x9401	PcsStatus1	PCS Status 1 Register.	0x0040	R
0x9403	FcEn	Frame Checker Enable Register.	0x0001	R/W
0x9406	FcIrqEn	Frame Checker Interrupt Enable Register.	0x0001	R/W
0x9407	FcTxSel	Frame Checker Transmit Select Register.	0x0000	R/W
0x9408	FcMaxFrmSize	Frame Checker Max Frame Size Register.	0x05F2	R/W
0x940A	FcFrmCntH	Frame Checker Count High Register.	0x0000	R
0x940B	FcFrmCntL	Frame Checker Count Low Register.	0x0000	R
0x940C	FcLenErrCnt	Frame Checker Length Error Count Register.	0x0000	R
0x940D	FcAlgnErrCnt	Frame Checker Alignment Error Count Register.	0x0000	R
0x940E	FcSymbErrCnt	Frame Checker Symbol Error Counter Register.	0x0000	R
0x940F	FcOszCnt	Frame Checker Oversized Frame Count Register.	0x0000	R
0x9410	FcUszCnt	Frame Checker Undersized Frame Count Register.	0x0000	R
0x9411	FcOddCnt	Frame Checker Odd Nibble Frame Count Register.	0x0000	R
0x9412	FcOddPreCnt	Frame Checker Odd Preamble Packet Count Register.	0x0000	R
0x9413	FcDribbleBitsCnt	Frame Checker Dribble Bits Frame Count Register.	0x0000	R
0x9414	FcFalseCarrierCnt	Frame Checker False Carrier Count Register.	0x0000	R
0x9415	FgEn	Frame Generator Enable Register.	0x0000	R/W
0x9416	FgCntrlRstrt	Frame Generator Control and Restart Register.	0x0001	R/W
0x9417	FgContModeEn	Frame Generator Continuous Mode Enable Register.	0x0000	R/W
0x9418	FgIrqEn	Frame Generator Interrupt Enable Register.	0x0000	R/W
0x941A	FgFrmLen	Frame Generator Frame Length Register.	0x006B	R/W
0x941C	FgNfrmH	Frame Generator Number of Frames High Register.	0x0000	R/W
0x941D	FgNfrmL	Frame Generator Number of Frames Low Register.	0x0100	R/W
0x941E	FgDone	Frame Generator Done Register.	0x0000	R
0xA000	LpiWakeErrCnt	LPI Wake Error Count Register.	0x0000	R
0xB412	B10TxTstMode	10BASE-T TX Test Mode Register.	0x0000	R/W
0xB413	B100TxTstMode	100BASE-TX TX Test Mode Register.	0x0000	R/W
0xBA1B	CdiagRun	Run Automated Cable Diagnostics Register.	0x0000	R/W
0xBA1C	CdiagXpairDis	Cable Diagnostics Cross Pair Fault Checking Disable Register.	0x0000	R/W
0xBA1D	CdiagDtldRslts0	Cable Diagnostics Results 0 Register.	0x0000	R
0xBA1E	CdiagDtldRslts1	Cable Diagnostics Results 1 Register.	0x0000	R
0xBA21	CdiagFltDist0	Cable Diagnostics Fault Distance Pair 0 Register.	0x00FF	R
0xBA22	CdiagFltDist1	Cable Diagnostics Fault Distance Pair 1 Register.	0x00FF	R
0xBA25	CdiagCblLenEst	Cable Diagnostics Cable Length Estimate Register.	0x00FF	R
0xBC00	LedPulStrDur	LED Pulse Stretching Duration Register.	0x0011	R/W

PHY CORE REGISTER DETAILS

MII Control Register

Address: 0x0000, Reset: 0x1040, Name: MiiControl

This address corresponds to the MII control register specified in clause 22.2.4.1 of Std 802.3. Note that the default reset value of this register is dependent on hardware configuration pins settings.

Table 24. Bit Descriptions for MiiControl

Bits	Bit Name	Description	Reset	Access
15	SftRst	Software reset bit. Note that this bit is self-clearing. Once the reset operation is complete, this bit returns to 1'b0. 1: PHY reset. 0: Normal operation.	0x0	R/W
14	Loopback	Enable/disable loopback mode. 1: Enable loopback mode. 0: Disable loopback mode.	0x0	R/W
13	SpeedSelLsb	The speed selection MSB & LSB register bits are used to configure the link speed. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 11: Reserved. 10: Reserved. 01: 100 Mb/s. 00: 10 Mb/s.	0x0	R/W
12	AutonegEn	The auto-negotiation enable bit is used to enable/disable auto-negotiation. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: Enable auto-negotiation process. 0: Disable auto-negotiation process.	0x1	R/W
11	SftPd	Software powerdown bit. Note that the default value of this register bit is configurable via hardware configuration pins. The PHYcan therefore be held in reset until initialized by software. 1: Software powerdown. 0: Normal operation.	0x0	R/W
10	Isolate	Isolate bit. 1: Electrically isolate PHY from MAC interface by setting MAC interface pins to tri-state (even if active). 0: Normal operation.	0x0	R/W
9	RestartAneg	Restart auto-negotiation bit. Note that this bit is self-clearing. Once the auto-negotiation process is restarted, this bit returns to 1'b0. 1: Restart the auto-negotiation process. 0: Normal operation.	0x0	R/W
8	DplxMode	Duplex mode bit. 1: Full duplex. 0: Half duplex.	0x0	R/W
7	Coltest	Collision test bit. 1: Enable COL signal test. 0: Disable COL signal test.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
6	SpeedSelMsb	See SpeedSelLsb bit description. 11: Reserved. 10: Reserved 01: 100 Mb/s. 00: 10 Mb/s.	0x1	R/W
5	UnidirEn	The unidirectional enable register bit is Read-only and always reads as 1'b0. Transmission from the media independent interface is only enabled when the PHY has determined that a valid link has been established.	0x0	R
[4:0]	RESERVED	Reserved.	0x0	R

MII Status Register

Address: 0x0001, Reset: 0x7949, Name: MiiStatus

This address corresponds to the MII status register specified in clause 22.2.4.2 of IEEE Std 802.3.

Table 25. Bit Descriptions for MiiStatus

Bits	Bit Name	Description	Reset	Access
15	T4Sprt	The 100BASE-T4 ability bit always reads as 1'b0 since the PHY does not support 100BASE-T4.	0x0	R
14	Fd100Sprt	The 100BASE-TX FD ability bit always reads as 1'b1 since the PHY supports 100BASE-TX Full Duplex.	0x1	R
13	Hd100Sprt	The 100BASE-TX HD ability bit always reads as 1'b1 since the PHY supports 100BASE-TX Half Duplex.	0x1	R
12	Fd10Sprt	The 10BASE-T FD ability bit always reads as 1'b1 since the PHY supports 10BASE-T Full Duplex.	0x1	R
11	Hd10Sprt	The 10BASE-T HD ability bit always reads as 1'b1 since the PHY supports 10BASE-T Half Duplex.	0x1	R
10	FdT2Sprt	The 100BASE-T2 full duplex ability bit always reads as 1'b0 since the PHY does not support 100BASE-T2.	0x0	R
9	HdT2Sprt	The 100BASE-T2 half duplex ability bit always reads as 1'b0 since the PHY does not support 100BASE-T2.	0x0	R
8	ExtStatSprt	The extended status support bit always reads as 1'b1 indicating that the PHY provides extended status information in register 0x000F.	0x1	R
7	UnidirAble	When zero, the unidirectional ability register bit indicates that the PHY can only transmit data from the media independent interface when it has determined that a valid link has been established. This bit always reads as 1'b0.	0x0	R
6	MfPreamSupAble	Management frame preamble suppression ability bit. This always reads as 1'b1 since the PHY will accept management frames with preamble suppressed.	0x1	R
5	AutonegDone	Auto-negotiation complete bit. 1: Auto-negotiation process completed. 0: Auto-negotiation process not completed.	0x0	R
4	RemFltLat	Remote fault bit. Once this bit goes high it latches high until it is unlatched by reading. 1: Remote fault condition detected. 0: No remote fault condition detected.	0x0	R
3	AutonegAble	Auto-negotiation ability bit. This bit always reads as 1'b1. 1: PHY is able to perform auto-negotiation. 0: PHY is not able to perform auto-negotiation.	0x1	R
2	LinkStatLat	Link status bit. If the link subsequently drops then this bit latches low until it is unlatched by reading. 1: Link is up. 0: Link is down.	0x0	R

Bits	Bit Name	Description	Reset	Access
1	JabberDetLat	Jabber detect bit. Once this bit goes high, it latches high until it is unlatched by reading. 1: Jabber condition detected. 0: No jabber condition detected.	0x0	R
0	ExtCapable	The extended capability bit always reads as 1'b1 since the PHY provides an extended set of capabilities.	0x1	R

PHY Identifier 1 Register

Address: 0x0002, Reset: 0x0283, Name: PhyId1

This address corresponds to the MII status register specified in clause 22.2.4.3.1 of IEEE Std 802.3 and allows 16 bits of the Organizationally Unique Identifier (OUI) to be observed.

Table 26. Bit Descriptions for PhyId1

Bits	Bit Name	Description	Reset	Access
[15:0]	PhyId1	Organizationally unique identifier bits 3 to 18.	0x283	R

PHY Identifier 2 Register

Address: 0x0003, Reset: 0xBC30, Name: PhyId2

This address corresponds to the MII status register specified in clause 22.2.4.3.1 of IEEE Std 802.3 and allows 6 bits of the OUI along with the model number and revision number to be observed.

Table 27. Bit Descriptions for PhyId2

Bits	Bit Name	Description	Reset	Access
[15:10]	PhyId2Oui	Organizationally unique identifier bits 19 to 24.	0x2F	R
[9:4]	ModelNum	Manufacturer's model number.	0x2	R
[3:0]	RevNum	Manufacturer's revision number.	0x0	R

Auto-Negotiation Advertisement Register

Address: 0x0004, Reset: 0x01E1, Name: AutonegAdv

This address corresponds to the auto-negotiation advertisement register specified in clause 28.2.4.1.3 of IEEE Std 802.3. Note that the default reset value of this register is dependent on hardware configuration pins settings.

Table 28. Bit Descriptions for AutonegAdv

Bits	Bit Name	Description	Reset	Access
15	NextPageAdv	Next page exchange occurs after the base link codewords have been exchanged. Next page exchange consists of using the normal auto-negotiation arbitration process to send next page messages. Next page transmission ends when both ends of a link segment set their next page bits to logic zero, indicating that neither has anything additional to transmit.	0x0	R/W
14	RESERVED	Reserved.	0x0	R
13	RemFltAdv	The remote fault bit provides a standard transport mechanism for the transmission of simple fault information.	0x0	R/W
12	ExtNextPageAdv	The extended next page bit indicates that the local device supports transmission of extended next pages. The use of Extended Next Page is orthogonal to the negotiated data rate, medium, or link technology.	0x0	R/W
11	ApauseAdv	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise Asymmetric PAUSE operation for full duplex links.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
10	PauseAdv	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise PAUSE operation for full duplex links.	0x0	R/W
9	T4Adv	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-T4 and always reads as 1'b0 as this technology is not supported.	0x0	R
8	Fd100Adv	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-TX full duplex. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
7	Hd100Adv	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 100BASE-TX half duplex. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
6	Fd10Adv	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 10BASE-T full duplex. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
5	Hd10Adv	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit is to advertise 10BASE-T half duplex. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W
[4:0]	SelectorAdv	Selector field is a five bit wide field, encoding 32 possible messages. This field always reads as 1'b1 indicating that the PHY only supports IEEE Std 802.3.	0x1	R/W

Auto-Negotiation Link Partner Base Page Ability Register

Address: 0x0005, Reset: 0x0000, Name: LpAbility

This address corresponds to the link partner ability register specified in clause 28.2.4.1.4 of IEEE Std 802.3.

Table 29. Bit Descriptions for LpAbility

Bits	Bit Name	Description	Reset	Access
15	LpNextPage	Link partner next page bit. Next page exchange occurs after the base link codewords have been exchanged. Next page exchange consists of using the normal auto-negotiation arbitration process to send next page messages. Next page transmission ends when both ends of a link segment set their next page bits to logic zero, indicating that neither has anything additional to transmit.	0x0	R
14	LpAck	This bit is used by the internal handshaking in auto-negotiation and should be ignored. 1 = Link partner has successfully received its link codeword 0 = Link partner has not received its link codeword	0x0	R
13	LpRemFlt	The link partner remote fault bit provides a standard transport mechanism for the transmission of simple fault information.	0x0	R
12	LpExtNextPageAble	The link partner extended next page bit indicates that the link partner supports transmission of extended next page. The use of Extended Next Page is orthogonal to the negotiated data rate, medium, or link technology.	0x0	R
11	LpApauseAble	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertised asymmetric PAUSE operation for full duplex links.	0x0	R

Bits	Bit Name	Description	Reset	Access
10	LpPauseAble	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertised PAUSE operation for full duplex links.	0x0	R
9	LpT4Able	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertised 100BASE-T4.	0x0	R
8	LpFd100Able	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertised 100BASE-TX full duplex.	0x0	R
7	LpHd100Able	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertised 100BASE-TX half duplex.	0x0	R
6	LpFd10Able	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertised 10BASE-T full duplex.	0x0	R
5	LpHd10Able	The technology ability field is a seven-bit wide field (bits 11:5 within this register) containing information indicating supported technologies specific to the selector field value. This bit indicates that the link partner advertised 10BASE-T half duplex.	0x0	R
[4:0]	LpSelector	Link partner selector field. This is a five bit wide field, encoding 32 possible messages. The value 0x1 indicates IEEE Std 802.3.	0x0	R

Auto-Negotiation Expansion Register

Address: 0x0006, Reset: 0x0064, Name: AutonegExp

This address corresponds to the auto-negotiation expansion register specified in clause 28.2.4.1.5 of IEEE Std 802.3.

Table 30. Bit Descriptions for AutonegExp

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	RxNpLocAble	The received next page location ability bit always reads as 1'b1 as received next pages are stored in register 0x0008. 1: Received Next Page storage location is specified by bit 5 (RxNpLoc). 0: Received Next Page storage location is not specified by bit 5 (RxNpLoc).	0x1	R
5	RxNpLoc	The received next page location bit always reads as 1'b1. 1: Link partner next pages are stored in register 0x0008. 0: Link partner next pages are stored in register 0x0005.	0x1	R
4	ParDetFlt	Parallel detection fault bit. Once this bit goes high it latches high until it is unlatched by reading. 1: A fault has been detected via the parallel detection function. 0: A fault has not been detected via the parallel detection function.	0x0	R
3	LpNpAble	Link partner next page ability bit. 1: Link partner is next page capable. 0: Link partner is not next page capable.	0x0	R
2	NpAble	The next page ability bit always reads as 1'b1 indicating that the PHY supports next pages. 1: Local device is next page capable. 0: Local device is not next page capable.	0x1	R

Bits	Bit Name	Description	Reset	Access
1	PageRxLat	Page received bit. Once this bit goes high it latches high until it is unlatched by reading. 1: A new page has been received. 0: A new page has not been received.	0x0	R
0	LpAutonegAble	Link partner auto-negotiation ability bit. 1: Link partner is auto-negotiation capable. 0: Link partner is not auto-negotiation capable.	0x0	R

Auto-Negotiation Next Page Transmit Register

Address: 0x0007, Reset: 0x2001, Name: TxNextPage

This address corresponds to the auto-negotiation next page transmit register specified in clause 28.2.4.1.6 of IEEE Std 802.3.

Table 31. Bit Descriptions for TxNextPage

Bits	Bit Name	Description	Reset	Access
15	NpNextPage	Next Page (NP) is used by the next page function to indicate additional next page(s) will follow, otherwise this is the last next page to be transmitted.	0x0	R/W
14	RESERVED	Reserved.	0x0	R
13	NpMsgPage	Message Page (MP) is used by the next page function to indicate this is a message page otherwise this is an unformatted page.	0x1	R/W
12	NpAck2	Acknowledge 2 (Ack2) is used by the next page function to indicate that a device has the ability to comply with the message.	0x0	R/W
11	NpToggle	Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit shall always take the opposite value of the Toggle bit in the previously exchanged link codeword.	0x0	R
[10:0]	NpCode	Message code field is an eleven bit wide field, encoding 2048 possible messages. If the message page bit is set to logic zero, then the bit encoding of the link codeword shall be interpreted as an unformatted page.	0x1	R/W

Auto-Negotiation Link Partner Received Next Page Register

Address: 0x0008, Reset: 0x0000, Name: LpRxNextPage

This address corresponds to the auto-negotiation link partner received next page register specified in clause 28.2.4.1.7 of IEEE Std 802.3.

Table 32. Bit Descriptions for LpRxNextPage

Bits	Bit Name	Description	Reset	Access
15	LpNpNextPage	Link partner Next Page (NP) is used by the next page function to indicate that the link partner will send additional next page(s), otherwise this is the last next page to be transmitted.	0x0	R
14	LpNpAck	This bit is used by the internal handshaking in auto-negotiation and should be ignored. 1 = Link partner has successfully received its link codeword 0 = Link partner has not received its link codeword	0x0	R
13	LpNpMsgPage	Link Partner Message Page (MP) is used by the next page function to indicate this is a message page otherwise this is an unformatted page.	0x0	R
12	LpNpAck2	Acknowledge 2 (Ack2) is used by the next page function to indicate that the link partner has the ability to comply with the message.	0x0	R
11	LpNpToggle	Link partner Toggle (T) is used by the arbitration function to ensure synchronization with the link partner during next page exchange. This bit shall always take the opposite value of the toggle bit in the previously exchanged link codeword.	0x0	R
[10:0]	LpNpCode	Link partner message code field is an eleven bit wide field, encoding 2048 possible messages. If the message page bit is set to logic zero, then the bit encoding of the link codeword is interpreted as an unformatted page.	0x0	R

Extended Register Pointer Register

Address: 0x0010, Reset: 0x0000, Name: ExtRegPtr

The extended register pointer and extended register data registers provide a mechanism to access the indirect access address map via directly accessible registers for cases where the station management does not support clause 45.

Table 33. Bit Descriptions for ExtRegPtr

Bits	Bit Name	Description	Reset	Access
[15:0]	ExtRegPtr	The extended register pointer and data registers provide an indirect mechanism to access Extended Management Interface (EMI) registers using normal Clause 22 access for cases where the station management does not support clause 45. The 16-bit register address should be written into the ExtRegPtr register. The EMI register can be read or written by reading or writing the ExtRegData register. An EMI register can be directly accessed using Clause 45 access.	0x0	R/W

Extended Register Data Register

Address: 0x0011, Reset: 0x0000, Name: ExtRegData

The extended register pointer and extended register data registers provide a mechanism to access the indirect access address map via directly accessible registers for cases where the station management does not support clause 45.

Table 34. Bit Descriptions for ExtRegData

Bits	Bit Name	Description	Reset	Access
[15:0]	ExtRegData	The extended register pointer and data registers provide an indirect mechanism to access EMI registers using normal Clause 22 access for cases where the station management does not support clause 45. See ExtRegPtr for further description.	0x0	R/W

PHY Control 1 Register

Address: 0x0012, Reset: 0x0002, Name: PhyCtrl1

This register provides access to various PHY control register bits, in particular for diagnostic clocking control and MDI crossover.

Table 35. Bit Descriptions for PhyCtrl1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	AutoMdiEn	The automatic MDI/MDIX resolution enable register bit allows the automatic cable crossover feature of the PHY to be controlled. Note that the default value of this register bit is configurable via a hardware configuration pin. This allows the default operation of the PHY to be configured in unmanaged applications. 1: Enable Auto MDI/MDIX. (Prefer MDI ifManMdix is 1'b0 and prefer MDIX if ManMdix is 1'b1). 0: Disable Auto MDI/MDIX.	0x0	R/W
9	ManMdix	When this bit is set and the AutoMdiEn bit is clear the PHY will operate in the MDIX configuration. In this configuration no crossover is implemented and the logical pairs of the PCS correspond to the physical pairs of the AFE. When this bit is clear and the AutoMdiEn bit is clear, the PHY will operate in the MDI configuration and will crossover the pairs. If AutoMdiEn bit is set, the ManMdix bit determines the MDI or MDIX preference option. 1: Operate in MDIX configuration. 0: Operate in MDI configuration.	0x0	R/W
[8:3]	RESERVED	Reserved.	0x0	R
2	DiagClkEn	Enable PHY diagnostics clock. This clock is required for certain diagnostic functions within the PHY, e.g. frame generator/checker. 1: Enable PHY diagnostics clock. 0: Disable PHY diagnostics clock.	0x0	R/W
[1:0]	RESERVED	Reserved.	0x2	R/W

PHY Control Status 1 Register

Address: 0x0013, Reset: 0x1041, Name: PhyCtrlStatus1

This register provides access to PHY loopback control bits.

Table 36. Bit Descriptions for PhyCtrlStatus1

Bits	Bit Name	Description	Reset	Access
[15:13]	RESERVED	Reserved.	0x0	R
12	LbAllDigSel	Setting this bit selects All Digital loopback. This loops the data within the PHY at the analog / digital boundary so that data received on the MAC Interface TXD pins is looped back to the RXD pins. This requires IEEE Loopback bit (MiiControl Register 0x0000, bit 14) to be set.	0x1	R/W
11	RESERVED	Reserved.	0x0	R
10	LbLdSel	Setting this bit selects Line Driver loopback. If this register bit is set, then every time the Loopback bit is set the PHY will enter its Line Driver loopback mode. In Line Driver loopback mode, the MDI pins should be left open in order to create a large impedance mismatch. The PHY can then operate by receiving the reflection from its own transmission.	0x0	R/W
9	LbRemoteEn	Setting this bit enables Remote loopback. This requires a link up with a remote PHY and it loops the data received from the remote PHY back to the remote PHY using all of the PHY's digital and analog circuitry.	0x0	R/W
8	IsolateRx	Setting this bit suppresses data being sent on to the MAC during loopback.	0x0	R/W
7	LbExtEn	Setting this bit enables External Cable loopback. This requires an external cable with pairs 0 and 1 shorted together to provide an analog loopback at the end of the cable. All of the PHY's digital and analog circuitry and the signal processing is adjusted so that the transmitted signal is not cancelled. The IEEE Loopback bit (MiiControl Register 0x0000, bit 14) must not be set.	0x0	R/W
6	LbTxSup	Setting this bit suppresses the transmit signal at the MDI pins in All Digital loopback.	0x1	R/W
[5:1]	RESERVED	Reserved.	0x0	R
0	LbMiiLsOk	Setting this bit sets the link status signal to OK during MII loopback.	0x1	R/W

Rx Error Count Register

Address: 0x0014, Reset: 0x0000, Name: RxErrCnt

The receive error counter register is used to access the Receive Error counter associated with the frame checker in the PHY.

Table 37. Bit Descriptions for RxErrCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	RxErrCnt	This is the Receive Error counter associated with the frame checker in the PHY. Note that this bit is self-clearing upon reading.	0x0	R

PHY Control Status 2 Register

Address: 0x0015, Reset: 0x0000, Name: PhyCtrlStatus2

This register provides access to various PHY control and status registers, in particular auto-negotiation controls and energy-detect powerdown control and status bits.

Table 38. Bit Descriptions for PhyCtrlStatus2

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	NrgPdEn	Setting this bit enables energy-detect powerdown. If there is no signal energy detected for a number of seconds the PHY will enter energy-detect powerdown mode. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: Enable energy-detect powerdown mode. 0: Disable energy-detect powerdown mode.	0x0	R/W
2	NrgPdTxEn	When this bit is set the PHY will periodically wake up when in energy-detect powerdown and will transmit a number of pulses. This is to avoid a lock-up situation where the PHYs on both ends of the line are in energy-detect powerdown mode. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: Enable periodic transmission of pulse while in energy-detect powerdown mode. 0: Disable periodic transmission of pulse while in energy-detect powerdown mode.	0x0	R/W
1	PhyInNrgPd	This status bit indicates that the PHY is in energy-detect powerdown mode. 1: PHY is in energy-detect powerdown mode. 0: PHY is not in energy-detect powerdown mode.	0x0	R
0	RESERVED	Reserved.	0x0	R/W

PHY Control 2 Register

Address: 0x0016, Reset: 0x0308, Name: PhyCtrl2

This register provides access to various PHY control registers, for control of clocking, group MDIO access, and auto-negotiation.

Table 39. Bit Descriptions for PhyCtrl2

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R/W
10	DnSpeedTo10En	Setting this bit enables downspeed to 10BASE-T. Note that Auto-negotiation must also be enabled. If the PHY is unable to bring a link up at a high speed, it will automatically drop down to 10BASE-T (assuming this speed has been advertised) if necessary. 1: Enable Downspeed to 10BASE-T. 0: Disable Downspeed to 10BASE-T.	0x0	R/W
[9:7]	RESERVED	Reserved.	0x6	R/W
6	GroupMdioEn	The group MDIO enable register bit may be used to place the PHY in group MDIO mode. In this mode the PHY will respond to any write or address operation to PHY address 5'd31 as if it was an access to its own PHY address. It is recommended that this bit be set only while performing specific sequences and then be cleared again.	0x0	R/W
[5:0]	RESERVED	Reserved.	0x8	R/W

PHY Control 3 Register

Address: 0x0017, Reset: 0x3048, Name: PhyCtrl3

This register provides access to PHY control register bits for link enable and auto-negotiation controls.

Table 40. Bit Descriptions for PhyCtrl3

Bits	Bit Name	Description	Reset	Access
[15:14]	RESERVED	Reserved.	0x0	R
13	LinkEn	Setting this bit enables linking. If linking is disabled the PHY will enter the Standby state and will not attempt to bring up links. The standby state can be used to run diagnostics, including cable diagnostics. 1: Enable linking. 0: Disable linking.	0x1	R/W
[12:10]	NumSpeedRetry	If Downspeed is enabled, this register bit specifies the number of retries the PHY should attempt to bring up a link at the advertised speed before advertising a lower speed. By default, the PHY will attempt to bring up a link 5 times (4 retries) before downspeeding.	0x4	R/W
[9:0]	RESERVED	Reserved.	0x48	R/W

Interrupt Mask Register

Address: 0x0018, Reset: 0x0000, Name: IrqMask

The interrupt mask register allows interrupts to be masked or unmasked.

Table 41. Bit Descriptions for IrqMask

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R/W
10	CblDiagIrqEn	Cable diagnostics interrupt enable bit. 1: Enable cable diagnostics interrupt. 0: Disable cable diagnostics interrupt.	0x0	R/W
9	MdioSyncIrqEn	MDIO synchronization lost interrupt enable bit. 1: Enable MDIO synchronization lost interrupt. 0: Disable MDIO synchronization lost interrupt.	0x0	R/W
8	AnStatChngIrqEn	Auto-negotiation status changed interrupt enable bit. 1: Enable auto-negotiation status changed interrupt. 0: Disable auto-negotiation status changed interrupt.	0x0	R/W
7	RESERVED	Reserved.	0x0	R/W
6	PageRxIrqEn	Auto-negotiation page received interrupt enable bit. 1: Enable auto-negotiation page received interrupt. 0: Disable auto-negotiation page received interrupt.	0x0	R/W
5	IdleErrCntIrqEn	Idle error counter saturated interrupt enable bit. 1: Enable idle error counter saturated interrupt. 0: Disable idle error counter saturated interrupt.	0x0	R/W
4	FifoOuIrqEn	MAC interface FIFO overflow/underflow interrupt enable bit. 1: Enable MAC interface FIFO overflow/underflow interrupt. 0: Disable MAC interface FIFO overflow/underflow interrupt.	0x0	R/W
3	RxStatChngIrqEn	Receive status changed interrupt enable bit. 1: Enable receive status changed interrupt. 0: Disable receive status changed interrupt.	0x0	R/W
2	LnkStatChngIrqEn	Link status changed interrupt enable bit. 1: Enable link status changed interrupt. 0: Disable link status changed interrupt.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
1	SpeedChngIrqEn	Speed changed interrupt enable bit. 1: Enable speed changed interrupt. 0: Disable speed changed interrupt.	0x0	R/W
0	HwIrqEn	When set this enables the hardware interrupt pin, INT_N and INT_N will be asserted when an interrupt is generated. 1: Enable the hardware interrupt pin, INT_N. 0: Disable the hardware interrupt pin, INT_N.	0x0	R/W

Interrupt Status Register

Address: 0x0019, Reset: 0x0000, Name: IrqStatus

The interrupt status register is used to check which interrupts have triggered since the last time it was read. Each bit will go high when the associated interrupt triggers and will then latch high until it is unlatched by reading (note that reading any of the bits in this register will unlatch all of the bits in the register). The bits of IrqStatus go high even when the associated interrupts are not enabled. However, only bits associated with enabled interrupts are considered when generating the IrqPending indication.

Table 42. Bit Descriptions for IrqStatus

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CblDiagIrqStat	If the cable diagnostics interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
9	MdioSyncIrqStat	If the MDIO synchronization lost interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
8	AnStatChngIrqStat	If the auto-negotiation status changed interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
7	RESERVED	Reserved.	0x0	R
6	PageRxIrqStat	If the auto-negotiation page received interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
5	IdleErrCntIrqStat	If the idle error counter saturated interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
4	FifoOuIrqStat	If the MAC Interface RGMII transmit FIFO overflow/underflow interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
3	RxStatChngIrqStat	If the receive status changed interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
2	LnkStatChngIrqStat	If the link status changed interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
1	SpeedChngIrqStat	If the speed changed interrupt status bit is '1', this indicates that the associated interrupt triggered since last read. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R
0	IrqPending	If the interrupt pending status bit is '1', this indicates that an interrupt has occurred and is pending. Note that once this bit goes high it latches high until it is unlatched by reading.	0x0	R

PHY Status 1 Register

Address: 0x001A, Reset: 0x0300, Name: PhyStatus1

This register provides access to various PHY status registers.

Table 43. Bit Descriptions for PhyStatus1

Bits	Bit Name	Description	Reset	Access
15	PhyInStndby	A '1' indicates that the PHY is in standby state and will not attempt to bring up links. The standby state can be used to run diagnostics including cable diagnostics.	0x0	R
14	Reserved	Reserved	0x0	R
13	ParDetFltStat	Parallel detection fault status bit. A '1' indicates that a fault has occurred in the parallel detection process. This bit is a copy of ParDetFlt, (AutonegExp register, address 0x0006, bit 4). Reading the ParDetFltStat bit does not clear ParDetFlt.	0x0	R
12	AutonegStat	Auto-negotiation status bit. A '1' indicates that Auto-negotiation has completed. This bit is a copy of AutonegDone, (MiiStatus register, address 0x0001, bit 5). Reading the AutonegStat bit does not clear AutonegDone.	0x0	R
11	Pair01Swap	A '1' indicates that pairs 0 and 1 have been swapped.	0x0	R
10	B10PolInv	A '1' indicates that the polarity of the 10BASE-T signal has been inverted.	0x0	R
[9:7]	HcdTech	This field indicates the resolved technology after the link has been established. 111: Reserved. 110: Reserved. 101: Reserved 100: Reserved . 011: Speed resolved to 100BASE-TX full duplex. 010: Speed resolved to 100BASE-TX half duplex. 001: Speed resolved to 10BASE-T full duplex. 000: Speed resolved to 10BASE-T half duplex.	0x6	R
6	LinkStat	A '1' indicates that the relevant technology dependent link_status signal is OK (i.e. when the link is up).	0x0	R
5	TxEnStat	A '1' indicates that Transmit Enable (TX_EN) is asserted.	0x0	R
4	RxDvStat	A '1' indicates that Receive Data Valid (RX_DV) is asserted.	0x0	R
3	ColStat	A '1' indicates that Collision (COL) is asserted.	0x0	R
2	AutonegSup	A '1' indicates that both the local and remote PHYs support auto-negotiation.	0x0	R
1	LpPauseAdv	A '1' indicates that the link partner has advertised Pause. The link partner pause advertisement bit indicates that the link partner advertised support for pause operation on full duplex links. This bit provides the same information as LpPauseAble.	0x0	R
0	LpApauseAdv	A '1' indicates that the link partner has advertised Asymmetric Pause. The link partner asymmetric pause advertisement bit indicates that the link partner advertised support for asymmetric pause operation on full duplex links. This bit provides the same information as LpApauseAble.	0x0	R

LED Control 1 Register

Address: 0x001B, Reset: 0x0001, Name: LedCtrl1

This register provides access to various PHY LED control register bits.

Table 44. Bit Descriptions for LedCtrl1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R/W
10	LedAExtCfgEn	Enable extended configuration set for LED_0 pin. See also LedACfg, (LedCtrl2 register, address 0x001C, bits 3:0). 1: Enable extended configuration set for LED_0 pin. 0: Disable extended configuration set for LED_0 pin.	0x0	R/W
[9:8]	RESERVED	Reserved.	0x0	R
[7:4]	LedPatPauseDur	Internal LED pattern pause duration for LED_0. After the blink pattern is driven out to the LED_0 pin, the last bit is held for a duration specified by the LED pattern pause duration register field. This duration is the value of LED tick duration (e.g. the time for each bit) multiplied by the value of the LED pattern pause duration register field. Also see, LedPat register field, (LedCtrl3 register, address 0x001D, bits 7:0) and the LedPatTickDur register field, (LedCtrl3 register, address 0x001D, bits 13:8). The default blink is a 0.5s ON and 0.5s OFF pattern.	0x0	R/W
[3:2]	LedPulStrDurSel	This bit field selects the duration of the pulse stretching. 11: User-programmable. In this case the duration of the pulse stretching is programmable by the LedPulStrDur register (address 0x1E.0xBC00, bits 5:0). 10: 102 ms. 01: 64 ms. 00: 32 ms.	0x0	R/W
1	LedOeN	LED active low output enable register bit. 1: Disable LED outputs. 0: Enable LED outputs.	0x0	R/W
0	LedPulStrEn	Setting this bit enables pulse stretching for transmit, receive or collision LED events so that very short duration events are visible. The LED pulse stretching enable register indicates that the PHY should stretch any pulses indicating transmit, receive or collision. Without stretching these pulses may be too short to cause a LED to light.	0x1	R/W

LED Control 2 Register

Address: 0x001C, Reset: 0x210A, Name: LedCtrl2

This register provides access to various PHY LED control register bits.

Table 45. Bit Descriptions for LedCtrl2

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x210	R/W
[3:0]	LedACfg	LED_0 configuration, bits 3:0. Bit 4 is from LedAExtCfgEn, (LedCtrl1 register, address 0x001B, bit 10). This configures LED_0, selecting one of 32 possible configuration functions according to the settings below. The default setting is ON if link up and blink on activity. 11111: On if 10BASE-T link, blink if 100BASE-TX link. 11110: On if 10BASE-T link, 11101: On if 100BASE-TX link, blink if 10BASE-T link. 11100: On if 100BASE-TX link 11011: blink if 10BASE-T link. 11010: Blink if transmit. 11001: Blink on activity. 11000: Reserved 10111: Reserved 10110: Reserved 10101: Reserved 10100: Reserved 10011: On if 100BASE-TX link, blink on activity. 10010: On if 10BASE-T link, blink on activity. 10001: Reserved 10000: On if 10BASE-T or 100BASE-TX link. 01111: Off. 01110: On. 01101: Blink. 01100: On if full duplex link, blink on collision. 01011: On if link, blink if receiving. 01010: On if link, blink on activity. 01001: On if collision. 01000: On if full duplex link. 00111: On if activity (transmitting or receiving). 00110: On if receiving. 00101: On if transmitting. 00100: On if link up. 00011: blink if 100BASE-TX. 00010: Reserved 00001: Reserved 00000: Reserved	0xA	R/W

LED Control 3 Register

Address: 0x001D, Reset: 0x1855, Name: LedCtrl3

This register provides access to various PHY LED control register bits.

Table 46. Bit Descriptions for LedCtrl3

Bits	Bit Name	Description	Reset	Access
[15:14]	LedPatSel	The LedPatSel register field is always 2'b00. This accesses the LED_0 blink pattern registers via the LedPat, LedPatTickDur and LedPatPauseDur register fields. 11: Reserved. 10: Reserved. 01: Reserved. 00: Read/write access to LED_0 blink pattern registers.	0x0	R/W
[13:8]	LedPatTickDur	Each bit in the blink pattern register field (LedPat) is driven to the corresponding LED pin and held for the duration specified in this 6-bit LED pattern duration register. The duration is the value of this register plus 1 multiplied by 8, e.g. 8 ms, 16 ms, … 504 ms. The value 63 has a special meaning of a 1 ms tick duration. Also see, the LedPatPauseDur register field, (LedCtrl1 register, address 0x001B, bits 7:4). The default blink is a 0.5 s ON and 0.5 s OFF pattern.	0x18	R/W
[7:0]	LedPat	The internal LED pattern register for LED_0 can be read or written via this field. The LedPatSel field selects which set of internal blink pattern registers for LED_0 is accessed. The default value of the LED pattern register is 0x55 and is thus an alternating 0/1 pattern. (LedCtrl1 register, address 0x001B, bits 7:4). The default blink is a 0.5s ON and 0.5s OFF pattern.	0x55	R/W

PHY Status 2 Register

Address: 0x001F, Reset: 0x03FC, Name: PhyStatus2

This register provides access to various PHY status register bits.

Table 47. Bit Descriptions for PhyStatus2

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	Pair1PolInv	A '1' indicates that the polarity on pair 1 has been inverted.	0x0	R
10	Pair0PolInv	A '1' indicates that the polarity on pair 0 has been inverted.	0x0	R
[9:0]	RESERVED	Reserved.	0x1FE	R

Energy Efficient Ethernet Capability Register

Address: 0x8000, Reset: 0x0006, Name: EeeCapability

This address corresponds to the EEE capability register specified in clause 45.2.3.9 of IEEE Std 802.3, which, in the IEEE standard is at MMD register address 3.20. This register is used to indicate the capability of the PCS to support EEE functions for each PHY type.

Table 48. Bit Descriptions for EeeCapability

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	Eee10GKrSprt	The 10GBASE-KR EEE capability bit always reads as 1'b0. 1: EEE is supported for 10GBASE-KR. 0: EEE is not supported for 10GBASE-KR.	0x0	R
5	Eee10GKx4Sprt	The 10GBASE-KX4 EEE capability bit always reads as 1'b0. 1: EEE is supported for 10GBASE-KX4. 0: EEE is not supported for 10GBASE-KX4.	0x0	R

Bits	Bit Name	Description	Reset	Access
4	Eee1000KxSprt	The 1000BASE-KX EEE capability bit always reads as 1'b0. 1: EEE is supported for 1000BASE-KX. 0: EEE is not supported for 1000BASE-KX.	0x0	R
3	Eee10GSprt	The 10GBASE-T EEE capability bit always reads as 1'b0. 1: EEE is supported for 10GBASE-T. 0: EEE is not supported for 10GBASE-T.	0x0	R
2	Eee1000Sprt	The 1000BASE-T EEE capability bit always reads as 1'b1. 1: EEE is supported for 1000BASE-T. 0: EEE is not supported for 1000BASE-T.	0x1	R
1	Eee100Sprt	The 100BASE-TX EEE capability bit always reads as 1'b1. 1: EEE is supported for 100BASE-TX. 0: EEE is not supported for 100BASE-TX.	0x1	R
0	RESERVED	Reserved.	0x0	R

Energy Efficient Ethernet Advertisement Register

Address: 0x8001, Reset: 0x0000, Name: EeeAdv

This address corresponds to the EEE advertisement register specified in clause 45.2.7.13 of Std 802.3, which in the IEEE standard is at MMD register address 7.60. This register is used to define the EEE advertisement during auto-negotiation. The reset value of this register is 0x0000 except where the hardware configuration pins are set to enable EEE - in this case, the reset value is 0x0006.

Table 49. Bit Descriptions for EeeAdv

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	Eee10GKrAdv	The 10GBASE-KR EEE advertisement bit always reads as 1'b0. 1: Advertise that the 10GBASE-KR has EEE capability. 0: Do not advertise that the 10GBASEKR has EEE capability.	0x0	R
5	Eee10GKx4Adv	The 10GBASE-KX4 EEE advertisement bit always reads as 1'b0. 1: Advertise that the 10GBASE-KX4 has EEE capability. 0: Do not advertise that the 10GBASEKX4 has EEE capability.	0x0	R
4	Eee1000KxAdv	The 1000BASE-KX EEE advertisement bit always reads as 1'b0. 1: Advertise that the 1000BASE-KX has EEE capability. 0: Do not advertise that the 1000BASEKX has EEE capability.	0x0	R
3	Eee10GAdv	The 10GBASE-T EEE advertisement bit always reads as 1'b0. 1: Advertise that the 10GBASE-T has EEE capability. 0: Do not advertise that the 10GBASE-T has EEE capability.	0x0	R
2	Eee1000Adv	The default value of the 1000BASE-T EEE advertisement register bit is dependent on the hardware configuration pins settings. When EEE is enabled by these pins, the default value is 1'b1 and when disabled, the default value is 1'b0. 1: Advertise that the 1000BASE-T has EEE capability. 0: Do not advertise that the 1000BASE-T has EEE capability.	0x0	R/W
1	Eee100Adv	The default value of the 100BASE-TX EEE advertisement register bit is dependent on the hardware configuration pins settings. When EEE is enabled by these pins, the default value is 1'b1 and when disabled, the default value is 1'b0. 1: Advertise that the 100BASE-TX has EEE capability. 0: Do not advertise that the 100BASETX has EEE capability.	0x0	R/W
0	RESERVED	Reserved.	0x0	R

Energy Efficient Ethernet Link Partner Ability Register

Address: 0x8002, Reset: 0x0000, Name: EeeLpAbility

This address corresponds to the EEE link partner ability register specified in clause 45.2.7.14 of Std 802.3, which in the IEEE standard is at MMD register address 7.61. This register reflects the link partner's EEE advertisement during auto-negotiation.

Table 50. Bit Descriptions for EeeLpAbility

Bits	Bit Name	Description	Reset	Access
[15:7]	RESERVED	Reserved.	0x0	R
6	LpEee10GKrAble	Link partner 10GBASE-KR EEE ability bit. 1: Link partner is advertising EEE capability for 10GBASE-KR. 0: Link partner is not advertising EEE capability for 10GBASE-KR.	0x0	R
5	LpEee10GKx4Able	Link partner 10GBASE-KX4 EEE ability bit. 1: Link partner is advertising EEE capability for 10GBASE-KX4. 0: Link partner is not advertising EEE capability for 10GBASE-KX4.	0x0	R
4	LpEee1000KxAble	Link partner 1000BASE-KX EEE ability bit. 1: Link partner is advertising EEE capability for 1000BASE-KX. 0: Link partner is not advertising EEE capability for 1000BASE-KX.	0x0	R
3	LpEee10GAble	Link partner 10GBASE-T EEE ability bit. 1: Link partner is advertising EEE capability for 10GBASE-T. 0: Link partner is not advertising EEE capability for 10GBASE-T.	0x0	R
2	LpEee1000Able	Link partner 1000BASE-T EEE ability bit. 1: Link partner is advertising EEE capability for 1000BASE-T. 0: Link partner is not advertising EEE capability for 1000BASE-T.	0x0	R
1	LpEee100Able	Link partner 100BASE-TX EEE ability bit. 1: Link partner is advertising EEE capability for 100BASE-TX. 0: Link partner is not advertising EEE capability for 100BASE-TX.	0x0	R
0	RESERVED	Reserved.	0x0	R

Energy Efficient Ethernet Resolved Register

Address: 0x8008, Reset: 0x0000, Name: EeeRslvd

This register indicates whether or not the resolved technology after the link has been established is EEE capable.

Table 51. Bit Descriptions for EeeRslvd

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	EeeRslvd	This bit indicates that the resolved technology after the link has been established is EEE capable. This is a vendor specific register bit. 1: Resolved technology is EEE capable. 0: Resolved technology is not EEE capable.	0x0	R

Mean Square Error A Register

Address: 0x8402, Reset: 0x0000, Name: MseA

This register is an indication of signal quality and is a measure of the mean square error on dimension A.

Table 52. Bit Descriptions for MseA

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	MseA	This register is an indication of signal quality when a 100BASE-TX link is up and is a measure of the mean square error on dimension A.	0x0	R

Receive MII Clock Stop Enable Register

Address: 0x9400, Reset: 0x0400, Name: RxMiiClkStopEn

This register contains the Clock stop enable bit specified in clause 45.2.3.1.4 of IEEE Std 802.3 which in the IEEE standard is at MMD register address 3.0 bit 10.

Table 53. Bit Descriptions for RxMiiClkStopEn

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	RxMiiClkStopEn	If this bit is set then the PHY may stop the receive xMII clock while it is signaling LPI otherwise it shall keep the clock active. 1: The PHY may stop the clock during LPI. 0: Clock not stoppable.	0x1	R/W
[9:0]	RESERVED	Reserved.	0x0	R

PCS Status 1 Register

Address: 0x9401, Reset: 0x0040, Name: PcsStatus1

The bits contained in this register correspond to the bits in the PCS status 1 register specified in clause 45.2.3.2 of IEEE Std 802.3, which in the IEEE standard is at MMD register address 3.1 bits 11 to 8 and 6.

Table 54. Bit Descriptions for PcsStatus1

Bits	Bit Name	Description	Reset	Access
[15:12]	RESERVED	Reserved.	0x0	R
11	TxLpiRcvd	The transmit LPI received bit is a latched version of TxLpi. Once it goes high it latches high until it is unlatched by reading. 1: Tx PCS has received LPI. 0: LPI not received.	0x0	R
10	RxLpiRcvd	The receive LPI received bit is a latched version of RxLpi. Once it goes high it latches high until it is unlatched by reading. 1: Rx PCS has received LPI. 0: LPI not received.	0x0	R
9	TxLpi	Transmit LPI bit. 1: Tx PCS is currently receiving LPI. 0: PCS is not currently receiving LPI.	0x0	R
8	RxLpi	Receive LPI bit. 1: Rx PCS is currently receiving LPI. 0: PCS is not currently receiving LPI.	0x0	R
7	RESERVED	Reserved.	0x0	R
6	TxMiiClkStopCpbl	The transmit xMII clock stop capable bit always reads as 1'b1. 1: The MAC may stop the clock during LPI. 0: Clock not stoppable.	0x1	R
[5:0]	RESERVED	Reserved.	0x0	R

Frame Checker Enable Register

Address: 0x9403, Reset: 0x0001, Name: FcEn

This register is used to enable the frame checker. The frame checker analyzes the received frames from either the MAC interface or the PHY (see FcTxSel register address 0x1E.0x9407, bit 0) to report the number of frames received, CRC errors and various other frame errors. The frame checker frame and error counter registers count these events.

Table 55. Bit Descriptions for FcEn

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FcEn	When set this register bit enables the frame checker.	0x1	R/W

Frame Checker Interrupt Enable Register

Address: 0x9406, Reset: 0x0001, Name: FcIrqEn

This register is used to enable the frame checker interrupt. An interrupt is generated when a receive error occurs. The frame checker/generator interrupt should be enabled in the Interrupt Mask Register - set FcFgIrqEn bit (IrqMask register, address 0x0018, bit 7). The interrupt status can be read via the FcFgIrqStat bit (IrqStatus register, address 0x0019, bit 7).

Table 56. Bit Descriptions for FcIrqEn

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FcIrqEn	When set, this register bit enables the frame checker interrupt.	0x1	R/W

Frame Checker Transmit Select Register

Address: 0x9407, Reset: 0x0000, Name: FcTxSel

This register is used to select the transmit side or receive side for frames to be checked. If set, frames received on the MAC interface to be transmitted are checked. This can be used to verify that correct data is received over the MAC interface and is also useful if remote loopback is enabled (set LbRemoteEn bit in PhyCtrlStatus1 register address 0x0013, bit 9) as it can be used to check the received data after it is looped back at the MAC interface.

Table 57. Bit Descriptions for FcTxSel

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FcTxSel	When set, this register bit indicates that the frame checker should check frames received to be transmitted by the PHY. 1: Check frames from the MAC I/F to be transmitted by the PHY. 0: Check frames received by the PHY from the remote end.	0x0	R/W

Frame Checker Max Frame Size Register

Address: 0x9408, Reset: 0x05F2, Name: FcMaxFrmSize

This register specifies the max frame size. Frames longer than this are counted as oversized frames.

Table 58. Bit Descriptions for FcMaxFrmSize

Bits	Bit Name	Description	Reset	Access
[15:0]	FcMaxFrmSize	This register field specifies the max frame size. Received frames that are longer than this are counted as oversized frames. Note, this frame length excludes the preamble and Start Frame Delimiter.	0x5F2	R/W

Frame Checker Count High Register

Address: 0x940A, Reset: 0x0000, Name: FcFrmCntH

This register is a latched copy of bits 31:16 of the 32-bit receive frame counter register. When the receive error counter (RxErrCnt register address 0x0014) is read, the receive frame counter register is latched. A copy of the receive frame counter register is latched when RxErrCnt is read so that the error count and receive frame count are synchronized.

Table 59. Bit Descriptions for FcFrmCntH

Bits	Bit Name	Description	Reset	Access
[15:0]	FcFrmCntH	Bits 31:16 of latched copy of the number of received frames.	0x0	R

Frame Checker Count Low Register

Address: 0x940B, Reset: 0x0000, Name: FcFrmCntL

This register is a latched copy of bits 15:0 of the 32-bit receive frame counter register. When the receive error counter (RxErrCnt register address 0x0014) is read, the receive frame counter register is latched. A copy of the receive frame counter register is latched when RxErrCnt is read so that the error count and receive frame count are synchronized.

Table 60. Bit Descriptions for FcFrmCntL

Bits	Bit Name	Description	Reset	Access
[15:0]	FcFrmCntL	Bits 15:0 of latched copy of the number of received frames.	0x0	R

Frame Checker Length Error Count Register

Address: 0x940C, Reset: 0x0000, Name: FcLenErrCnt

This register is a latched copy of the frame length error counter register. This is a count of received frames with lengthError status. When the receive error counter (RxErrCnt register address 0x0014) is read, the frame length error counter register is latched, this ensures that the frame length error count and receive frame count are synchronized.

Table 61. Bit Descriptions for FcLenErrCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcLenErrCnt	Latched copy of the frame length error counter.	0x0	R

Frame Checker Alignment Error Count Register

Address: 0x940D, Reset: 0x0000, Name: FcAlgnErrCnt

This register is a latched copy of the frame alignment error counter register. This is a count of received frames with alignmentError status. When the receive error counter counter (RxErrCnt register address 0x0014) is read, the alignment error counter register is latched, this ensures that the frame alignment error count and receive frame count are synchronized.

Table 62. Bit Descriptions for FcAlgnErrCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcAlgnErrCnt	Latched copy of the frame alignment error counter.	0x0	R

Frame Checker Symbol Error Counter Register

Address: 0x940E, Reset: 0x0000, Name: FcSymbErrCnt

This register is a latched copy of the symbol error counter register. This is a count of received frames with both RX_ER and RX_DV set. When the receive error counter (RxErrCnt register address 0x0014) is read, the symbol error counter register is latched, this ensures that the symbol error count and receive frame count are synchronized.

Table 63. Bit Descriptions for FcSymbErrCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcSymbErrCnt	Latched copy of the symbol error counter.	0x0	R

Frame Checker Oversized Frame Count Register

Address: 0x940F, Reset: 0x0000, Name: FcOszCnt

This register is a latched copy of the oversized frame error counter register. This is a count of received frames with a length greater than specified in frame checker max frame size (FcMaxFrmSize register address 0x1E.0x9407). When the receive error counter (RxErrCnt register, address 0x0014) is read, the oversized frame error counter register is latched, this ensures that the oversized frame error count and receive frame count are synchronized.

Table 64. Bit Descriptions for FcOszCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcOszCnt	Latched copy of the oversized frame error counter.	0x0	R

Frame Checker Undersized Frame Count Register

Address: 0x9410, Reset: 0x0000, Name: FcUszCnt

This register is a latched copy of the undersized frame error counter register. This is a count of received frames with a length less than 64 bytes. When the receive error counter (RxErrCnt register address 0x0014) is read, the undersized frame error counter register is latched, this ensures that the undersized frame error count and receive frame count are synchronized.

Table 65. Bit Descriptions for FcUszCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcUszCnt	Latched copy of the undersized frame error counter.	0x0	R

Frame Checker Odd Nibble Frame Count Register

Address: 0x9411, Reset: 0x0000, Name: FcOddCnt

This register is a latched copy of the odd nibble frame counter register. This is a count of received frames with an odd number of nibbles in the frame in 100BASE-TX or 10BASE-T mode. When the receive error counter (RxErrCnt register address 0x0014) is read, the odd nibble frame counter register is latched, this ensures that the odd nibble frame count and receive frame count are synchronized.

Table 66. Bit Descriptions for FcOddCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcOddCnt	Latched copy of the odd nibble counter.	0x0	R

Frame Checker Odd Preamble Packet Count Register

Address: 0x9412, Reset: 0x0000, Name: FcOddPreCnt

This register is a latched copy of the odd preamble packet counter register. This is a count of received frames with an odd number of number of nibbles in the preamble in 100BASE-TX mode. When the receive error counter (RxErrCnt register address 0x0014) is read, the odd preamble packet counter register is latched, this ensures that odd preamble packet count and receive frame count are synchronized.

Table 67. Bit Descriptions for FcOddPreCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcOddPreCnt	Latched copy of the odd preamble packet counter.	0x0	R

Frame Checker Dribble Bits Frame Count Register

Address: 0x9413, Reset: 0x0000, Name: FcDribbleBitsCnt

This register is a latched copy of the dribble bits frame counter register. This is a count of received frames with a non-integer number of nibbles in 10BASE-T mode. When the receive error counter (RxErrCnt register address 0x0014) is read, the dribble bits frame counter register is latched, this ensures that dribble bits frame count and receive frame count are synchronized.

Table 68. Bit Descriptions for FcDribbleBitsCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcDribbleBitsCnt	Latched copy of the dribble bits frame counter.	0x0	R

Frame Checker False Carrier Count Register

Address: 0x9414, Reset: 0x0000, Name: FcFalseCarrierCnt

This register is a latched copy of the false carrier events counter register. This is a count of the number of times the BAD SSD state is entered. When the receive error counter (RxErrCnt register address 0x0014) is read, the false carrier events counter register is latched, this ensures that false carrier events count and receive frame count are synchronized.

Table 69. Bit Descriptions for FcFalseCarrierCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	FcFalseCarrierCnt	Latched copy of the false carrier events counter.	0x0	R

Frame Generator Enable Register

Address: 0x9415, Reset: 0x0000, Name: FgEn

This register is used to enable the frame generator. When the frame generator is enabled the source of data for the PHY comes from the frame generator and not the MAC interface. To use the frame generator the diagnostic clock must also be enabled - set DiagClkEn bit (PhyCtrl1 register, address 0x0012, bit 2).

Table 70. Bit Descriptions for FgEn

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FgEn	When set, this register bit enables the built-in frame generator.	0x0	R/W

Frame Generator Control and Restart Register

Address: 0x9416, Reset: 0x0001, Name: FgCntrlRstrt

This register provides frame generator control and restart functions.

Table 71. Bit Descriptions for FgCntrlRstrt

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
3	FgRstrt	When set, this register bit restarts the frame generator. This bit is self-clearing.	0x0	R/W
[2:0]	FgCntrl	This register field controls the frame generator in accordance with the following encoding: 111: Reserved. 110: Reserved. 101: Data field decrementing from 255 (decimal) to 0. 100: Alternative 0x55 in the MAC Client Data frame field. 011: All ones in the MAC Client Data frame field. 010: All zeros in the MAC Client Data frame field. 001: Random number in the MAC Client Data frame field. 000: No frames after completion of current frame.	0x1	R/W

Frame Generator Continuous Mode Enable Register

Address: 0x9417, Reset: 0x0000, Name: FgContModeEn

This register is used to put the frame generator into continuous mode. The default mode of operation is burst mode, where the number of frames generated is specified by the FgNfrmH and FgNfrmL registers (register addresses 0x1E.0x941C and 0x1E.0x941D).

Table 72. Bit Descriptions for FgContModeEn

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FgContModeEn	This register bit is used to put the frame generator into continuous or burst mode. 1: Frame generator operates in continuous mode. In this mode the frame generator keeps generating frames indefinitely. 0: Frame generator operates in burst mode. In this mode the frame generator generates a single burst of frames and then stops. The number of frames in the burst is determined by the FgNfrmH and FgNfrmL registers.	0x0	R/W

Frame Generator Interrupt Enable Register

Address: 0x9418, Reset: 0x0000, Name: FgIrqEn

This register is used to enable the frame generator interrupt. An interrupt is generated when the requested number of frames has been generated. The frame checker/generator interrupt should be enabled in the IrqMask register - set FcFgIrqEn bit (register address 0x0018, bit 7). The interrupt status can be read via the IrqStatus register - FcFgIrqStat bit (register address 0x0019, bit 7).

Table 73. Bit Descriptions for FgIrqEn

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FgIrqEn	When set, this register bit indicates that the frame generator should generate an interrupt when it has transmitted the programmed number of frames. 1: Enable the frame generator interrupt. 0: Disable the frame generator interrupt.	0x0	R/W

Frame Generator Frame Length Register

Address: 0x941A, Reset: 0x006B, Name: FgFrmLen

This register specifies the MAC client data field frame length in bytes. In addition to the data field, 6 bytes are added for the source address, 6 bytes for the destination address, 2 bytes for the length field and 4 bytes for the FCS. The total frame length is the data field length plus 18.

Table 74. Bit Descriptions for FgFrmLen

Bits	Bit Name	Description	Reset	Access
[15:0]	FgFrmLen	The data field frame length in bytes.	0x6B	R/W

Frame Generator Number of Frames High Register

Address: 0x941C, Reset: 0x0000, Name: FgNfrmH

This register is bits 31:16 of a 32-bit register that specifics the number of frames to be generated each time the frame generator is enabled or restarted.

Table 75. Bit Descriptions for FgNfrmH

Bits	Bit Name	Description	Reset	Access
[15:0]	FgNfrmH	Bits 31:16 of the number of frames to be generated.	0x0	R/W

Frame Generator Number of Frames Low Register

Address: 0x941D, Reset: 0x0100, Name: FgNfrmL

This register is bits 15:0 of a 32-bit register that specifics the number of frames to be generated each time the frame generator is enabled or restarted.

Table 76. Bit Descriptions for FgNfrmL

Bits	Bit Name	Description	Reset	Access
[15:0]	FgNfrmL	Bits 15:0 of the number of frames to be generated.	0x100	R/W

Frame Generator Done Register

Address: 0x941E, Reset: 0x0000, Name: FgDone

This register is used to indicate that the frame generator has completed the generation of the number of frames requested in the FgNfrmH and FgNfrmL registers (register addresses 0x1E.0x941C and 0x1E.0x941D respectively).

Table 77. Bit Descriptions for FgDone

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	FgDone	This bit reads as 1'b1 to indicate that the generation of frames has completed. Once set this bit goes high it latches high until it is unlatched by reading.	0x0	R

LPI Wake Error Count Register

Address: 0xA000, Reset: 0x0000, Name: LpiWakeErrCnt

This address corresponds to the EEE wake error counter register specified in clause 45.2.3.10 of IEEE Std 802.3, which in the IEEE standard is at MMD register address 3.22.

Table 78. Bit Descriptions for LpiWakeErrCnt

Bits	Bit Name	Description	Reset	Access
[15:0]	LpiWakeErrCnt	This register field counts wake time faults where the PHY fails to complete its normal wake sequence within the time required. This field will self-clear upon reading.	0x0	R

10BASE-T TX Test Mode Register

Address: 0xB412, Reset: 0x0000, Name: B10TxTstMode

This register provides the ability to transmit a 10BASE-T test signal.

Table 79. Bit Descriptions for B10TxTstMode

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	B10TxTstMode	The PHY provides the ability to transmit a 10BASE-T test signal consisting of either a 5MHz or a 10MHz square wave. 111: Reserved. 110: Reserved. 101: Reserved. 100: Transmit 5MHz square wave on dimension 1. 011: Transmit 5MHz square wave on dimension 0. 010: Transmit 10MHz square wave on dimension 1. 001: Transmit 10MHz square wave on dimension 0. 000: 10BASE-T test mode disabled.	0x0	R/W

100BASE-TX TX Test Mode Register

Address: 0xB413, Reset: 0x0000, Name: B100TxTstMode

This register provides the ability to transmit a 100BASE-TX test signal.

Table 80. Bit Descriptions for B100TxTstMode

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	B100TxTstMode	The PHY provides the ability to transmit a 100BASE-TX test signal which cycles continuously through the valid MLT3 signal levels - zero, positive, zero, negative and so on. Each transmit level may be held for either 16ns (short dwell time) or 112ns (long dwell time). The MLT3 transmit test waveform with a 16 ns dwell time can be used to measure duty cycle distortion as specified in clause 9.1.8 of ANSI Std X3.263. The MLT3 transmit test waveform with a 112 ns dwell time can be used to measure waveform overshoot, amplitude symmetry and rise/fall times as specified in clauses 9.1.3, 9.1.4 and 9.1.6 of ANSI Std X3.263. 111: Reserved. 110: Reserved. 101: Reserved. 100: Transmit MLT3 test waveform, 112 ns dwell time on dimension 1. 011: Transmit MLT3 test waveform, 112 ns dwell time on dimension 0. 010: Transmit MLT3 test waveform, 16 ns dwell time on dimension 1. 001: Transmit MLT3 test waveform, 16 ns dwell time on dimension 0. 000: 100BASE-TX test mode disabled.	0x0	R/W

Run Automated Cable Diagnostics Register

Address: 0xBA1B, Reset: 0x0000, Name: CdiagRun

This register is used to start the automated running of cable diagnostics and to return results in the cable diagnostic results registers.

Table 81. Bit Descriptions for CdiagRun

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CdiagRun	When set, this register bit starts an automatic cable diagnostics run. This should be run with the PHY in standby - clear LinkEn bit (PhyCtrl3 register, address 0x0017, bit 13). This bit self clears when the cable diagnostics is completed.	0x0	R/W

Cable Diagnostics Cross Pair Fault Checking Disable Register

Address: 0xBA1C, Reset: 0x0000, Name: CdiagXpairDis

This register allows the checking of cross pair faults in the cable diagnostics to be disabled.

Table 82. Bit Descriptions for CdiagXpairDis

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	CdiagXpairDis	When set, this register bit disables cross pair fault checking. 1: Disable cross pair fault checking. 0: Enable cross pair fault checking.	0x0	R/W

Cable Diagnostics Results 0 Register

Address: 0xBA1D, Reset: 0x0000, Name: CdiagDtldRslts0

This register provides cable diagnostics results for pair 0.

Table 83. Bit Descriptions for CdiagDtldRslts0

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CdiagRslt0Bsy	When set, this register bit indicates pair 0 is busy. This bit indicates that there was unknown activity on pair 0 during cable diagnostics.	0x0	R
[9:8]	RESERVED	Reserved.	0x0	R
7	CdiagRslt0Xsim1	When set, this register bit indicates that there is a significant impedance cross pair short between pair 0 and pair 1.	0x0	R
6	CdiagRslt0Sim	When set, this register bit indicates that there is a significant impedance mismatch on pair 0.	0x0	R
[5:4]	RESERVED	Reserved.	0x0	R
3	CdiagRslt0Xshrt1	When set, this register bit indicates that there is a cross pair short between pair 0 and pair 1.	0x0	R
2	CdiagRslt0Shrt	When set, this register bit indicates that there is a short on pair 0.	0x0	R
1	CdiagRslt0Opn	When set, this register bit indicates that there is an open on pair 0.	0x0	R
0	CdiagRslt0Gd	When set, this register bit indicates that pair 0 is well terminated.	0x0	R

Cable Diagnostics Results 1 Register

Address: 0xBA1E, Reset: 0x0000, Name: CdiagDtldRslts1

This register provides cable diagnostics results for pair 1.

Table 84. Bit Descriptions for CdiagDtldRslts1

Bits	Bit Name	Description	Reset	Access
[15:11]	RESERVED	Reserved.	0x0	R
10	CdiagRslt1Bsy	When set, this register bit indicates pair 1 is busy. This bit indicates that there was unknown activity on pair 1 during cable diagnostics.	0x0	R
[9:8]	RESERVED	Reserved.	0x0	R
7	CdiagRslt1Xsim0	When set, this register bit indicates that there is a significant impedance cross pair short between pair 1 and pair 0.	0x0	R
6	CdiagRslt1Sim	When set, this register bit indicates that there is a significant impedance mismatch on pair 1.	0x0	R
[5:4]	RESERVED	Reserved.	0x0	R
3	CdiagRslt1Xshrt0	When set, this register bit indicates that there is a cross pair short between pair 1 and pair 0.	0x0	R
2	CdiagRslt1Shrt	When set, this register bit indicates that there is a short on pair 1.	0x0	R
1	CdiagRslt1Opn	When set, this register bit indicates that there is an open on pair 1.	0x0	R
0	CdiagRslt1Gd	When set, this register bit indicates that pair 1 is well terminated.	0x0	R

Cable Diagnostics Fault Distance Pair 0 Register

Address: 0xBA21, Reset: 0x00FF, Name: CdiagFltDist0

This register provides the distance to the first fault on pair 0.

Table 85. Bit Descriptions for CdiagFltDist0

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CdiagFltDist0	This register field provides the distance to the first fault on pair 0 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Fault Distance Pair 1 Register

Address: 0xBA22, Reset: 0x00FF, Name: CdiagFltDist1

This register provides the distance to the first fault on pair 1.

Table 86. Bit Descriptions for CdiagFltDist1

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CdiagFltDist1	This register field provides the distance to the first fault on pair 1 in meters. A value of 0xFF indicates an unknown result.	0xFF	R

Cable Diagnostics Cable Length Estimate Register

Address: 0xBA25, Reset: 0x00FF, Name: CdiagCblLenEst

This register provides an estimate of the cable length in meters based on the signal processing and is estimated during link establishment for 100BASE-TX =

Table 87. Bit Descriptions for CdiagCblLenEst

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x0	R
[7:0]	CdiagCblLenEst	This register field provides a cable length estimate in meters. A value of 0xFF indicates an unknown result.	0xFF	R

LED Pulse Stretching Duration Register

Address: 0xBC00, Reset: 0x0011, Name: LedPulStrDur

When the LedPulStrDurSel register field in the LedCtrl1 register (address 0x001B, bits [3:2]) is set to 2'b11, the LedPulStrDur register determines the LED pulse stretching duration.

Table 88. Bit Descriptions for LedPulStrDur

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
[5:0]	LedPulStrDur	When the LedPulStrDurSel register field in the LedCtrl1 register (address 0x001B, bits [3:2]) is set to 2'b11, the LedPulStrDur register field determines the LED pulse stretching duration. Multiply the value specified by 8 to determine the duration in ms.	0x11	R/W

SUB-SYSTEM REGISTER SUMMARY

The sub-system registers are accessible at device address 0x1E using clause 45 access. For systems that do not support the interface specified under clause 45, these registers can be accessed using clause 22 access via registers 0x0010 and 0x0011.

The default value of some of the registers are determined by the value of the hardware configuration pins which are read just after the RESET_N pin is de-asserted (see Hardware Configuration Pins section). This allows the default operation of the ADIN1200 to be configured in unmanaged applications. The default values in the tables below assume the ADIN1300 is configured with auto-negotiation enabled, all speeds advertised and the ADIN1200 is not configured to enter software powerdown after reset.

Table 89. Sub-System Register Summary

Address	Name	Description	Reset	Access
0xFF0C	GeSftRst	Sub-System Software Reset Register.	0x0000	R/W
0xFF0D	GeSftRstCfgEn	Sub-System Software Reset Configuration Enable Register.	0x0000	R/W
0xFF1F	GeClkCfg	Sub-System Clock Configuration Register.	0x0000	R/W
0xFF23	GeRgmiiCfg	Sub-System RGMII Configuration Register.	0x0E07	R/W
0xFF24	GeRmiiCfg	Sub-System RMII Configuration Register.	0x0116	R/W
0xFF3C	GeLnkStatInvEn	Sub-System Link Status Invert Enable Register.	0x0000	R/W
0xFF3D	GeIoGpClkOrCntrl	Sub-System GP_CLK Pin Over-ride Control Register.	0x0000	R/W
0xFF3E	GeIoGpOutOrCntrl	Sub-System LINK_ST Pin Over-ride Control Register.	0x0000	R/W
0xFF3F	GeIoIntNOrCntrl	Sub-System INT_N Pin Over-ride Control Register.	0x0000	R/W
0xFF41	GeIoLedAOrCntrl	Sub-System LED_0 Pin Over-ride Control Register.	0x0000	R/W

SUB-SYSTEM REGISTER DETAILS

Sub-System Software Reset Register

Address: 0xFF0C, Reset: 0x0000, Name: GeSftRst

The soft reset register is used to reset the sub-system.

Table 90. Bit Descriptions for GeSftRst

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GeSftRst	The sub-system can be reset by setting GeSftRst to '1'. The sub-system behavior depends on the setting of the GeSftRstCfgEn register. When the GeSftRstCfgEn bit is set, the sub-system will request a new set of hardware configuration pin settings from the chip during the software reset sequence. When GeSftRstCfgEn is clear the previously stored hardware configuration pin settings will simply be reloaded into the corresponding management registers.	0x0	R/W

Sub-System Software Reset Configuration Enable Register

Address: 0xFF0D, Reset: 0x0000, Name: GeSftRstCfgEn

In the event of a software reset using GeSftRst, the sub-system behavior depends on the setting of this register bit.

Table 91. Bit Descriptions for GeSftRstCfgEn

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GeSftRstCfgEn	In the event of a sub-system software reset using GeSftRst, the sub-system behavior depends on the setting of the GeSftRstCfgEn register bit. 1: When the GeSftRstCfgEn bit is set, the sub-system will request a new set of hardware configuration pin settings from the chip during the software reset sequence. 0: When GeSftRstCfgEn is clear the previously stored hardware configuration pin settings will simply be reloaded into the corresponding management registers.	0x0	R/W

Sub-System Clock Configuration Register

Address: 0xFF1F, Reset: 0x0000, Name: GeClkCfg

This register allows the sub-system output clock configuration to be controlled.

Table 92. Bit Descriptions for GeClkCfg

Bits	Bit Name	Description	Reset	Access
[15:6]	RESERVED	Reserved.	0x0	R
5	GeClkRcvr125En	When this register bit is set, the125 MHz PHY recovered clock (or PLL clock) is driven at the GP_CLK pin.	0x0	R/W
4	GeClkFree125En	When this register bit is set the 125 MHz PHY free running clock is driven at the GP_CLK pin.	0x0	R/W
3	Reserved	Reserved	0x0	R/W
2	GeClkHrtRcvrEn	The PHY provides a digital recovered heartbeat clock. This clock is sourced either from the 25 MHz reference clock or the 125 MHz recovered clock depending on the mode that the PHY is in and on the settings of certain registers. Setting GeClkHrtRcvrEn causes the sub-system to request the chip to drive the digital recovered heartbeat clock at the GP_CLK pin.	0x0	R/W
1	GeClkHrtFreeEn	The PHY provides a digital free-running heartbeat clock. This clock is sourced either from the 25 MHz reference clock or the 125 MHz free running clock depending on the mode that the PHY is in and on the settings of certain registers. Setting GeClkHrtFreeEn causes the sub-system to request the chip to drive the digital free-running heartbeat clock at the GP_CLK pin.	0x0	R/W
0	GeClk25En	When this register bit is set, the 25 MHz reference clock from the crystal oscillator is driven at the GP_CLK pin.	0x0	R/W

Sub-System RGMII Configuration Register

Address: 0xFF23, Reset: 0x0E07, Name: GeRgmiiCfg

This register allows the MAC interface RGMII configuration to be controlled.

Table 93. Bit Descriptions for GeRgmiiCfg

Bits	Bit Name	Description	Reset	Access
[15:9]	RESERVED	Reserved.	0x7	R
[8:6]	GeRgmiiRxSel	This field allows the RGMII R/X clock delay to be specified in terms of the DLL unit delay (Tu = 200 ps). 111: 10 x Tu + 400ps. 110: 9 x Tu + 400ps. 101: Reserved. 100: Reserved. 011: Reserved. 010: 7 x Tu + 400ps. 001: 6 x Tu + 400ps. 000: 8 x Tu + 400ps.	0x0	R/W
[5:3]	GeRgmiiGtxSel	This field allows the RGMII T/X clock delay to be specified in terms of the DLL unit delay (Tu = 200 ps). 111: 10 x Tu + 400ps. 110: 9 x Tu + 400ps. 101: Reserved. 100: Reserved. 011: Reserved.	0x0	R/W

Bits	Bit Name	Description	Reset	Access
		010: 7 x Tu + 400ps. 001: 6 x Tu + 400ps. 000: 8 x Tu + 400ps.		
2	GeRgmiiRxIdEn	Enable/disable R/X clock internal 2 ns delay in RGMII mode. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: Enable R/X clock internal 2 ns delay in RGMII mode. 0: Disable R/X clock internal 2 ns delay in RGMII mode.	0x1	R/W
1	GeRgmiiTxIdEn	Enable/disable T/X clock internal 2 ns delay in RGMII mode. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. 1: Enable T/X clock internal 2 ns delay in RGMII mode. 0: Disable T/X clock internal 2 ns delay in RGMII mode.	0x1	R/W
0	GeRgmiiEn	This bit selects the RGMII MAC interface mode. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications.	0x1	R/W

Sub-System RMII Configuration Register

Address: 0xFF24, Reset: 0x0116, Name: GeRmiiCfg

This register allows the MAC interface RMII configuration to be controlled.

Table 94. Bit Descriptions for GeRmiiCfg

Bits	Bit Name	Description	Reset	Access
[15:8]	RESERVED	Reserved.	0x1	R
7	GeRmiiFifoRst	This bit allows the RMII FIFO to be reset.	0x0	R/W
[6:4]	GeRmiiFifoDpth	This field allows the RMII R/X FIFO depth to be selected. 111: Reserved. 110: Reserved. 101: +/- 24 bits. 100: +/- 20 bits. 011: +/- 16 bits. 010: +/- 12 bits. 001: +/- 8 bits. 000: +/- 4 bits.	0x1	R/W
3	GeRmiiTxdChkEn	This bit determines whether or not TXD[1:0] is monitored to detect the start of a frame. It allows connecting the RMII R/X CRS_DV to the RMII TX_EN signal. This would allow an RX to TX RMII pin loopback for media converter applications. This is something that it is not supported in the RMII spec.	0x0	R/W
2	GeRmiiCrsEn	This bit determines whether or not CRS is encoded in the CRS_DV output signal. This would allow an RX to TX RMII pin loopback for media converter applications. This is something that it is not supported in the RMII spec.	0x1	R/W
1	GeRmiiBadSsdRxErEn	This bit determines whether or not the RX_ER output signal is asserted when a False Carrier (Bad SSD) is detected. When cleared RX_ER will only be asserted in case of a symbol error during a frame.	0x1	R/W
0	GeRmiiEn	This bit selects the RMII MAC interface mode. Note that the default value of this register bit is configurable via hardware configuration pins. This allows the default operation of the PHY to be configured in unmanaged applications. As RMII mode requires a 50 MHz reference clock, the RMII interface must be configured from the hardware configuration pins and not from software.	0x0	R/W

Sub-System Link Status Invert Enable Register

Address: 0xFF3C, Reset: 0x0000, Name: GeLnkStatInvEn

This register allows the link status output signal on the LINK_ST pin, to be inverted, meaning that link up would be indicated by setting LINK_ST low.

Table 95. Bit Descriptions for GeLnkStatInvEn

Bits	Bit Name	Description	Reset	Access
[15:1]	RESERVED	Reserved.	0x0	R
0	GeLnkStatInvEn	When set to 1, this bit enables the link status output signal on the LINK_ST pin, to be inverted, meaning that link up would be indicated by setting LINK_ST low.	0x0	R/W

Sub-System GP_CLK Pin Over-ride Control Register

Address: 0xFF3D, Reset: 0x0000, Name: GeIoGpClkOrCntrl

This register allows the default function of the GP_CLK pin to be overridden.

Table 96. Bit Descriptions for GeIoGpClkOrCntrl

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	GeIoGpClkOrCntrl	This register field allows the default function of the GP_CLK pin to be overridden. 111: PHY clock selected by the registers in the GeClkCfg register. 110: RX_ER. 101: COL. 100: CRS. 011: RX Start Of Packet indication. 010: TX Start Of Packet indication. 001: Link Status. 000: Default function. The default function is RX_ER when the PHY is configured for MII or RMII MAC interface. In all other cases, the default function is GP_CLK.	0x0	R/W

Sub-System LINK_ST Pin Over-ride Control Register

Address: 0xFF3E, Reset: 0x0000, Name: GeIoGpOutOrCntrl

This register allows the default function of the LINK_ST pin to be overridden.

Table 97. Bit Descriptions for GeIoGpOutOrCntrl

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	GeIoGpOutOrCntrl	This register field allows the default function of the LINK_ST pin to be overridden. 111: Link Status. 110: Reserved. 101: COL. 100: CRS. 011: RX Start Of Packet indication. 010: TX Start Of Packet indication. 001: Link Status. 000: Default function - Link Status.	0x0	R/W

Sub-System INT_N Pin Over-ride Control Register

Address: 0xFF3F, Reset: 0x0000, Name: GeIoIntNOrCntrl

This register allows the default function of the INT_N pin to be overridden.

Table 98. Bit Descriptions for GeIoIntNOrCntrl

Bits	Bit Name	Description	Reset	Access
[15:3]	RESERVED	Reserved.	0x0	R
[2:0]	GeIoIntNOrCntrl	This register field allows the default function of the INT_N pin to be overridden. 111: INT_N. 110: TX_ER. 101: COL. 100: CRS. 011: RX Start Of Packet indication. 010: TX Start Of Packet indication. 001: Link Status. 000: Default function - INT_N. The default function when configured for MII MAC interface with EEE advertisement disabled from hardware pin configuration, is CRS. In all other cases the pin function is INT_N.	0x0	R/W

Sub-System LED_0 Pin Over-ride Control Register

Address: 0xFF41, Reset: 0x0000, Name: GeIoLedAOrCntrl

This register allows the default function of the LED_0 pin to be overridden.

Table 99. Bit Descriptions for GeIoLedAOrCntrl

Bits	Bit Name	Description	Reset	Access
[15:4]	RESERVED	Reserved.	0x0	R
[3:0]	GeIoLedAOrCntrl	This register field allows the default function of the LED_0 pin to be overridden. 1111: LED_0. 1110: LED_0. 1101: LED_0. 1100: LED_0. 1011: LED_0. 1010: LED_0. 1001: Reserved. 1000: Reserved. 0111: LED_0. 0110: TX_ER. 0101: COL. 0100: CRS. 0011: RX Start Of Packet indication. 0010: TX Start Of Packet indication. 0001: Link Status. 0000: Default function - LED_0. When configured for MII MAC interface with EEE advertisement disabled from the hardware configuration pins, the default function is COL. When configured for MII MAC interface with EEE advertisement enabled from the hardware pin configuration, the default function is TX_ER. In all other cases, the default is LED_0.	0x0	R/W

APPLICATIONS INFORMATION

SUPPLY DECOUPLING

It is recommended to decouple the AVDD_3P3 and DVDD_0P9 supply pins with 0.1 µF in parallel with 0.01 µF capacitors to ground. Place decoupling capacitors as close to the relevant pins as possible.

LAYOUT GUIDELINES FOR LFCSP PACKAGE

The LFCSP package has an exposed pad that must be soldered to a metal plate on the PCB for mechanical reasons and to GND. The package also has two keepout areas to the top and bottom of the exposed pad. No pcb traces or vias can be used in these areas.

For thermal impedance performance, use of a JEDEC 2S2P board with a 4x4 array of thermal vias beneath the exposed GND pad is required.

COMPONENT RECOMMENDATIONS

Crystal

The typical connection for an external crystal is shown in Figure 21. To ensure minimum current consumption and to minimize stray capacitances, connections between the crystal, capacitors, and ground should be made as close to the ADIN1200 as possible. Consult individual crystal vendors for recommended load information and crystal performance specifications.

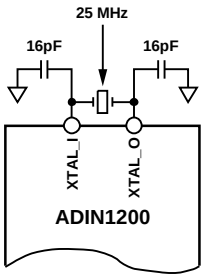


Figure 19. Crystal Oscillator Connection

Table 100. Crystal Specifications

Parameter	Min	Typ	Max	Unit
Frequency		25		MHz
Frequency tolerance	-30		+30	ppm
ESR		20-100		Ohm
Load capacitance		10		pF
Output drive level		200		µW

External Clock Input

If using a single ended reference clock on XTAL_I/CLK_IN/REF_CLK, leave XTAL_O open circuit. This clock should be a unipolar 2.5 V 25MHz sinewave or square-wave signal. In the case of using the RMII MAC interface, a single 50 MHz reference clock (REF_CLK) is required. This could be sourced from the MAC or from an external source.

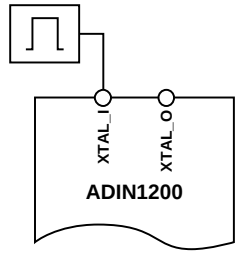


Figure 20. External Clock Connection

Magnetics

Galvanic isolation is necessary between any two point-to-point communication nodes in applications using the Ethernet protocol to transmit/receive data. Magnetic coupling between the PHY and the RJ45 is the most common way of achieving this isolation. Such magnetics can be discrete or integrated into what is known as a MagJack RJ45 connector.

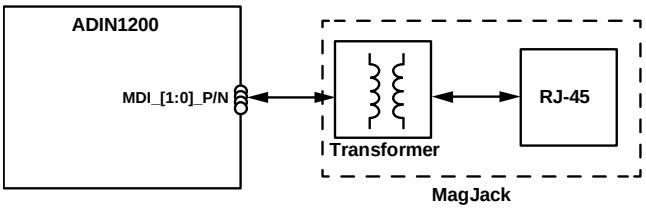
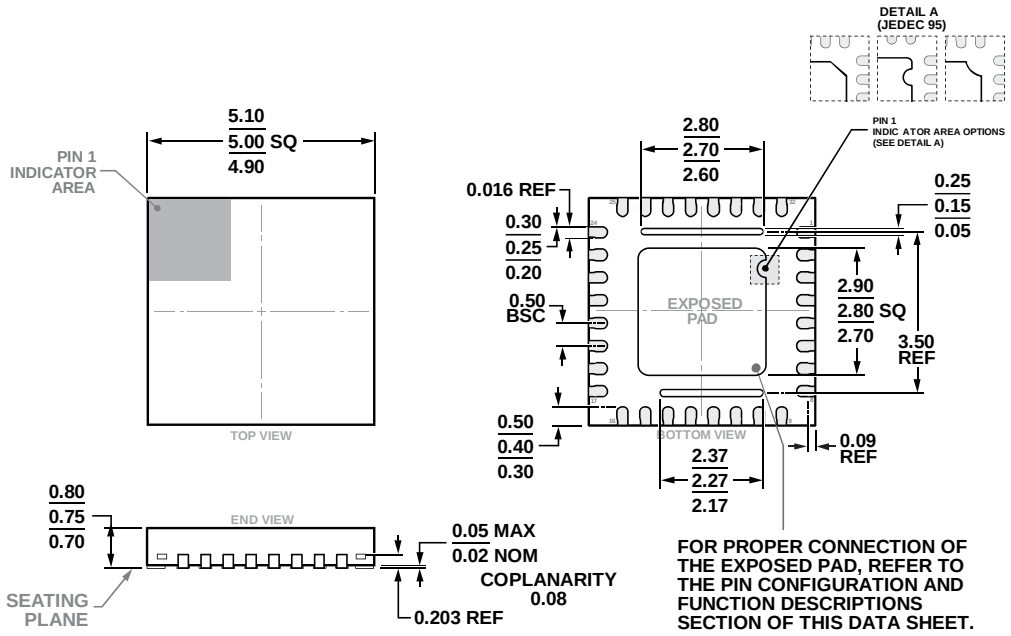


Figure 21. Magnetics Connection

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WHHD-2

Figure 22. 32-Lead Lead Frame Chip Scale Package [LFSCP]
5 mm x 5 mm Body and 0.75 mm Package Height
(CP-32-31)
Dimensions shown in millimeters

PR21561-0-8/19(PrH)