Polyphase Multifunction Energy Metering IC

Silicon Anomaly

ADE7854/ADE7858/ADE7868/ADE7878

This anomaly list describes the known issues with the ADE7854, ADE7858, ADE7868, and ADE7878 silicon identified by the version register (Address 0xE707) being equal to 2, to 4, and to 5.

Analog Devices, Inc., is committed, through future silicon revisions, to continuously improve silicon functionality. Analog Devices tries to ensure that these future silicon revisions remain compatible with your present software/systems by implementing the recommended workarounds outlined here.

ADE7854/ADE7858/ADE7868/ADE7878 FUNCTIONALITY ISSUES

Silicon Revision Identifier	Chip Marking	Silicon Status	Anomaly Sheet	No. of Reported Issues
Version = 2	ADE7854ACPZ ADE7858ACPZ ADE7868ACPZ ADE7878ACPZ	Released	Rev. A	4 (er001, er002, er003, er004)
Version = 4	ADE7854ACPZ ADE7858ACPZ ADE7868ACPZ ADE7878ACPZ	Released	Rev. B	1 (er005)
Version = 5	ADE7854ACPZ ADE7858ACPZ ADE7868ACPZ ADE7878ACPZ	Released	Rev. C	1 (er005)

FUNCTIONALITY ISSUES

Table 1. Offset RMS Registers Cannot be Set to Negative Values [er001, Version = 2 Silicon]

Background	When the AIRMSOS, AVRMSOS, BIRMSOS, BVRMSOS, CIRMSOS, CVRMSOS, and NIRMSOS registers are set to a negative value, for sufficiently small inputs, the argument of the square root used in the rms data path may become negative. In this case, the corresponding AIRMS, AVRMS, BIRMS, BVRMS, CIRMS, or CVRMS rms register is automatically set to 0.
Issue	Negative values for the AIRMSOS, AVRMSOS, BIRMSOS, BVRMSOS, CIRMSOS, CVRMSOS, and NIRMSOS registers are not supported in the silicon version identified by the version register being equal to 2.
Workaround	Do not use negative values for the AIRMSOS, AVRMSOS, BIRMSOS, BVRMSOS, CIRMSOS, CVRMSOS, and NIRMSOS registers. If further details on this issue are required, please use the following website to submit your query: www.analog.com/en/content/technical_support_page/fca.html.
Related Issues	None.

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Table 2. Values Written to the CF1DEN, CF2DEN, CF3DEN, SAGLVL, and ZXTOUT Registers May Not Be Immediately Used By ADE7854, ADE7858, ADE7868, ADE7878 [er002, Version = 2 Silicon]

Background	Usually, the CF1DEN, CF2DEN, CF3DEN, SAGLVL, and ZXTOUT registers initialize immediately after power-up or after a hardware/software reset. After the RUN register is set to 1, the energy-to-frequency converter (for CF1DEN, CF2DEN, and CF3DEN), the phase voltage sag detector (for SAGLVL), and the zero-crossing timeout circuit (for ZXTOUT) use these values immediately.
Issue	After the CF1DEN register is initialized with a new value after power-up or a hardware/software reset, the new value may be delayed and, therefore, not immediately available for use by the energy-to-frequency converter. It is, however, used by the converter after the first high-to-low transition is triggered at t the CF1 pin using the CF1DEN default value (0x0). CF2DEN and CF3DEN registers present similar behavior at the CF2 and CF3 pins, respectively. CF1DEN, CF2DEN and CF3DEN above behavior has been corrected in Version = 4 silicon. After the SAGLVL register is initialized with a new value after power-up or a hardware or software reset, the new value may be delayed and not available for immediate use by the phase voltage sag detector. However, it is used by the detector after at least one phase voltage rises above 10% of the full-scale input at the phase voltage ADCs. After the ZXTOUT register is initialized with a new value after power-up or a hardware or software reset, the new value may be delayed and not available for immediate use by the zero-crossing timeout circuit. However, the circuit does use the new value after at least one phase voltage rises above 10% of the full-scale input at the phase voltage ADCs.
Workaround	If the behavior outlined in the Issue row does not conflict with the meter specification, then the new values of the CF1DEN, CF2DEN, CF3DEN, SAGLVL, and ZXTOUT registers may be written one time only. If the behavior is not acceptable, write the new value into the CF1DEN, CF2DEN, and CF3DEN registers eight consecutive times. This ensures the probability of the new value not being considered immediately by the energy-to-frequency converter becomes lower than 0.2 ppm. Usually, at least one of the phase voltages is greater than 10% of full scale after power-up or after a hardware/software reset. If this cannot be guaranteed, then the SAGLVL and ZXTOUT registers should also be written eight consecutive times to reduce the probability of not being considered immediately by the phase voltage sag detector and zero-crossing timeout circuit.
Related Issues	None.

Table 3. The Read-Only RMS Registers May Show the Wrong Value [er003, Version = 2 Silicon]

Background	The read-only rms registers (AVRMS, BVRMS, CVRMS, AIRMS, BIRMS, CIRMS, and NIRMS) can be read without restrictions at any time.
Issue	The fixed function DSP of ADE7854, ADE7858, ADE7868, and ADE7878 computes all the powers and rms values in a loop with a period of 125 µs (8 kHz frequency). If two rms registers are accessed (read) consecutively, the value of the second register may be corrupted. Consequently, the apparent power computed during that 125 µs cycle is also corrupted. The rms calculation recovers in the next 125 µs cycle, and all the rms and apparent power values compute correctly. The issue appears independent of the communication type, SPI or I^2C, when the time between the start of two consecutive rms readings is lower than 265 µs. The issue affects only the rms registers; all of the other registers of ADE7854, ADE7858, ADE7868, and ADE7878 can be accessed without any restrictions.
Workaround	The rms registers can be read one at a time with at least 265 µs between the start of the readings. DREADY interrupt at the $\overline{IRQ0}$ pin can be used to time one rms register reading every three consecutive DREADY interrupts. This ensures 375 µs between the start of the rms readings. Alternatively, the rms registers can be read interleaved with readings of other registers that are not affected by this restriction as long as the time between the start of two consecutive rms register readings is 265 µs.
Related Issues	None.

Table 4. To Obtain Best Accuracy Performance, Internal Setting Must Be Changed [er004, Version = 2 Silicon]

Background	Internal default settings provide best accuracy performance for ADE7854, ADE7858, ADE7868, and ADE7878.
Issue	It was found that if a different setting is used, the accuracy performance can be improved.
Workaround	To enable a new setting for this internal register, execute two consecutive 8-bit register write operations: The first write operation: 0xAD is written to Address 0xE7FE. The second write operation: 0x01 is written to Address 0xE7E2. The write operations must be executed consecutively without any other read/write operation in between. As a verification that the value was captured correctly, a simple 8-bit read of Address 0xE7E2 should show the 0x01 value.
Related Issues	None.

Table 5. Values Written to the SAGLVL and ZXTOUT Registers May Not Be Immediately Used by ADE7854, ADE7858, ADE7868, and ADE7878 [er005, Version = 4 and Version = 5 Silicons]

Background	Usually, the SAGLVL and ZXTOUT registers initialize immediately after power-up or after a hardware/software reset. After the run register is set to 1, the phase voltage sag detector (for SAGLVL), and the zero-crossing timeout circuit (for ZXTOUT) use these values immediately.
Issue	After the SAGLVL register is initialized with a new value after power-up or a hardware or software reset, the new value may be delayed and not available for immediate use by the phase voltage sag detector. However, it is used by the detector after at least one phase voltage rises above 10% of the full-scale input at the phase voltage ADCs. After the ZXTOUT register is initialized with a new value after power-up or a hardware or software reset, the new value may be delayed and not available for immediate use by the zero-crossing timeout circuit. However, the circuit does use the new value after at least one phase voltage rises above 10% of the full-scale input at the phase voltage ADCs.
Workaround	Usually, at least one of the phase voltages is greater than 10% of full scale after power-up or after a hardware/software reset. If this cannot be guaranteed, then the SAGLVL and ZXTOUT registers should be written eight consecutive times to reduce the probability of not being considered immediately by the phase voltage sag detector and zero-crossing timeout circuit below 0.2 ppm.
Related Issues	None.

SECTION 1. ADE7854/ADE7858/ADE7868/ADE7878 FUNCTIONALITY ISSUES

Reference Number	Description	Status
er001	Offset rms registers cannot be set to negative values.	Identified
er002	Values written to the CF1DEN, CF2DEN, CF2DEN, SAGLVL, and ZXTOUT registers may not be immediately used by ADE7854, ADE7858, ADE7868, and ADE7878.	Identified
er003	The read-only rms registers may show the wrong value.	Identified
er004	To obtain best accuracy performance, internal setting must be changed.	Identified
er005	Values written to the SAGLVL and ZXTOUT registers may not be immediately used by ADE7854, ADE7858, ADE7868, and ADE7878.	Identified

NOTES

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