Integrated LCD Grayscale Generator

ADD8502

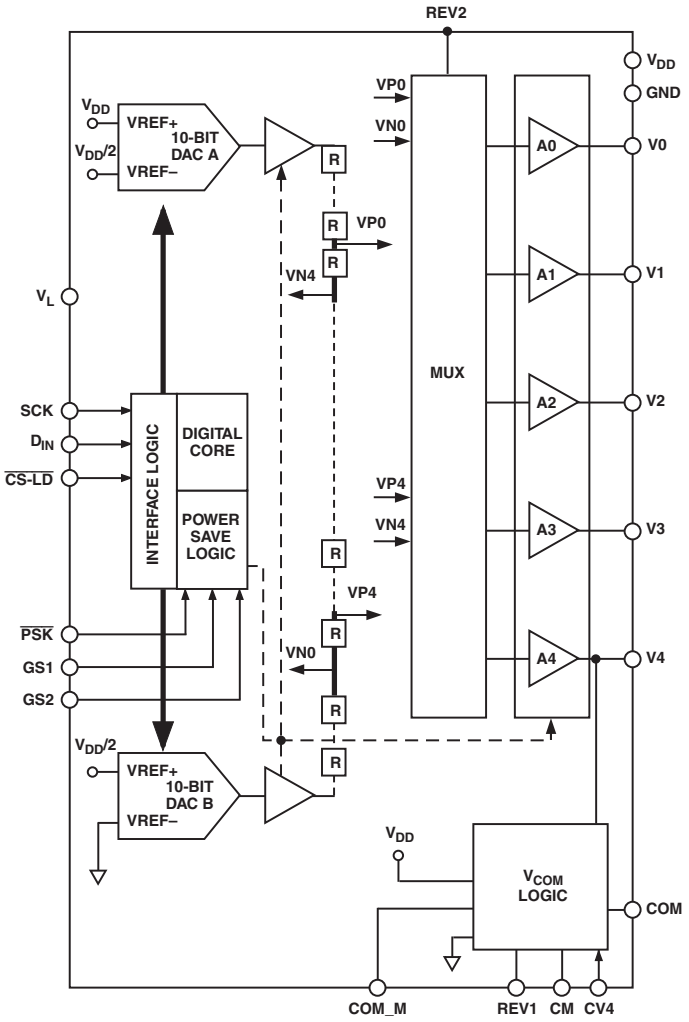
FEATURES

Two Mask Programmable Sets of Five Reference Levels
Dual 10-Bit DACs for Flicker Offset and Range Adjustment
Integrated V_{COM} Switching
Single-Supply Operation: 5.0 V
Low Supply Current: 300 μA
Global Power Save Mode: 1 μA Max
Fast Settling Time for Load Change: 20 μs
Stable with 20 nF/100 Ω Loads
CMOS/TTL Input Levels

APPLICATIONS

Color TFT Cell Phones
Color TFT PDAs

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADD8502 is an integrated, high accuracy, programmable grayscale generator. Two sets of five output reference voltages are mask programmed to 0.2% resolution. The outputs switch between the two sets of five levels. The reference levels are selected from a 512 tap resistor network using a via mask.

ADD8502 includes two serially addressable, 10-bit digital-to-analog converters (DACs) and five fast, low current buffers. The dual DACs set the endpoint voltages applied to the resistor network to adjust for flicker and range. The two power save modes can reduce the total current to less than 1 μA and feature fast recovery time from Shutdown/Sleep Mode. The ADD8502 accepts CMOS or TTL inputs for all controls, including the common drive circuit levels.

ADD8502 operates over the industrial temperature range from –40°C to +85°C and is available in a space-saving 24-lead 4 mm × 4 mm frame chip scale package.

REV. 0

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ADD8502–SPECIFICATIONS (@ V_{DD} = 5.0 V, −40°C ≤ T_A ≤ +85°C, unless otherwise noted.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SYSTEM ACCURACY						
V_{OUT} Error				3	20	mV
Swing Error[1]		$(V_{Pn} - V_{Nn}) - (V_{Pi} - V_{Ni})$		1	17	mV
Mean Error[2]		$(V_{Pn} + V_{Nn})/2 - (V_{Pi} + V_{Ni})/2)$		3	21	mV
Mean Error between Adjacent Channels[3]				3	21	mV
Mean Error between V0 and V4[4]				3	25	mV
DAC ACCURACY						
Resolution				10		Bits
Differential Nonlinearity	DNL			±0.25		LSB
Integral Nonlinearity[5]	INL			±0.5		LSB
Offset Error				±0.4		% of FSR
Gain Error				±0.15		% of FSR
OUTPUT CHARACTERISTICS						
Output Current	I_{OUT}	$(V_{DD} - 1\ V)$		25		mA
Short Circuit Current	I_{SC}	Short to Ground		60		mA
Output Leakage Current in High-Z Mode	$I_{LEAKAGE}$	High-Z Mode		0.01	1.0	µA
Slew Rate	SR	R_L = 100 kΩ		1.25		V/µs
Settling Time to 1%	t_S	V0 to V4 Step Size		8	12	µs
Slew Rate[5]	SR	L_D =100 Ω Series 16 nF		0.7		V/µs
Settling Time to 1%[5]	t_S	V0 to V4 Step Size		8	12	µs
Phase Margin	ϕo			67		Degrees
V_{COM} SWITCHES ACTIVE IMPEDANCE						
COM to V_{DD}	Z	See Table IV		25	50	Ω
COM to GND	Z			25	50	Ω
COM to COM_M	Z	I = 20 mA		25	50	Ω
COM to V4	Z			25	50	Ω
MASK PROGRAMMABLE RESISTOR CHAIN						
Resistor Matching	R_{MATCH}	Any Two Segments between 512 Resistor String		1		%
POWER SUPPLY						
Supply Voltage	V_{DD}		4.5	5	5.5	V
Supply Current	I_{SY}	V_{DD} = 5 V; No Load	190	270	400	µA
Shutdown Supply Current	I_{SY-GLB}	Full Shutdown Mode		0.2	1	µA
Sleep Supply Current	$I_{SY-GS1-3}$	Mid 3 Buffers Shutdown	140	175	210	µA
Shutdown Recovery Time		Global PD to 1%		23	30	µs
Sleep Recovery Time		V1–V3 Off to 1%		10	15	µs
LOGIC SUPPLY						
Logic Input Voltage Level	V_L		2.3	3.3	5.5	V
Logic Input Current	I_{VL}			0.01	1	µA
DIGITAL I/O						
Digital Input High Voltage	V_{IH}		$V_L \times 0.7$			V
Digital Input Low Voltage	V_{IL}				$V_L \times 0.3$	V
Digital Input Current	I_{IN}	GND ≤ V_{IN} ≤ 5.5 V			±1	µA
Digital Input Capacitance	C_{IN}				10	pF

NOTES

[1]Swing error is a comparison of measured V_{OUT} step versus theoretical V_{OUT} step. Theoretical values can be found on the Mask Tap Point Option sheet.

[2]Mean error is measured V_{OUT} mean versus theoretical V_{OUT} mean (see Figure 3).

[3]Mean errors between two adjacent channels versus theoretical (see Figure 3).

[4]Mean errors between V0 and V4 versus theoretical (see Figure 3).

[5]Slew rate and settling time are measured between the output resistor and the capacitor (see Figure 1).

Specifications subject to change without notice.

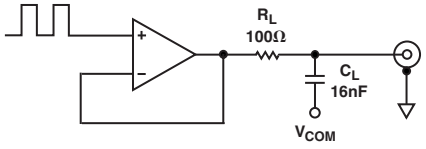

Figure 1. Slew Rate Diagram

Table I. Serial Data Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
SCK Cycle Time	t_1	100			ns
SCK High Time	t_2	45			ns
SCK Low Time	t_3	45			ns
$\overline{\text{CS-LD}}$ Setup Time	t_4	20			ns
Data Setup Time	t_5	5			ns
Data Hold Time	t_6	5			ns
LSB SCK High to $\overline{\text{CS-LD}}$ High	t_7	5			ns
Minimum $\overline{\text{CS-LD}}$ High Time	t_8	10			ns
SCK to $\overline{\text{CS-LD}}$ Active Edge Setup Time	t_9	5			ns
$\overline{\text{CS-LD}}$ High to SCK Positive Edge	t_{10}	10			ns
SCK Frequency (Square Wave)				10	MHz

NOTES
[1]All input signals are specified with rise/fall time –5 ns (10% to 90% of V_{DD}) and timed from a voltage level of $(V_S + V_{IH})/2$.
[2]See Figure 2.

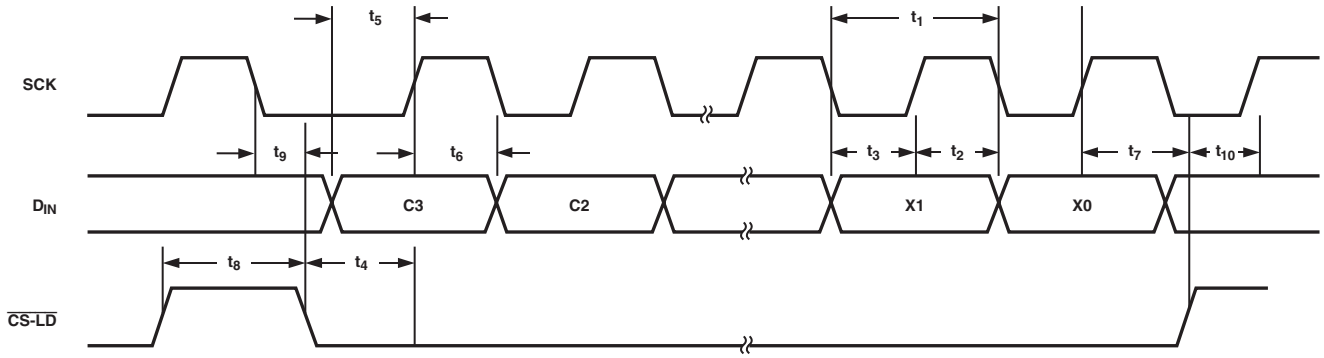

Figure 2. Serial Write Interface

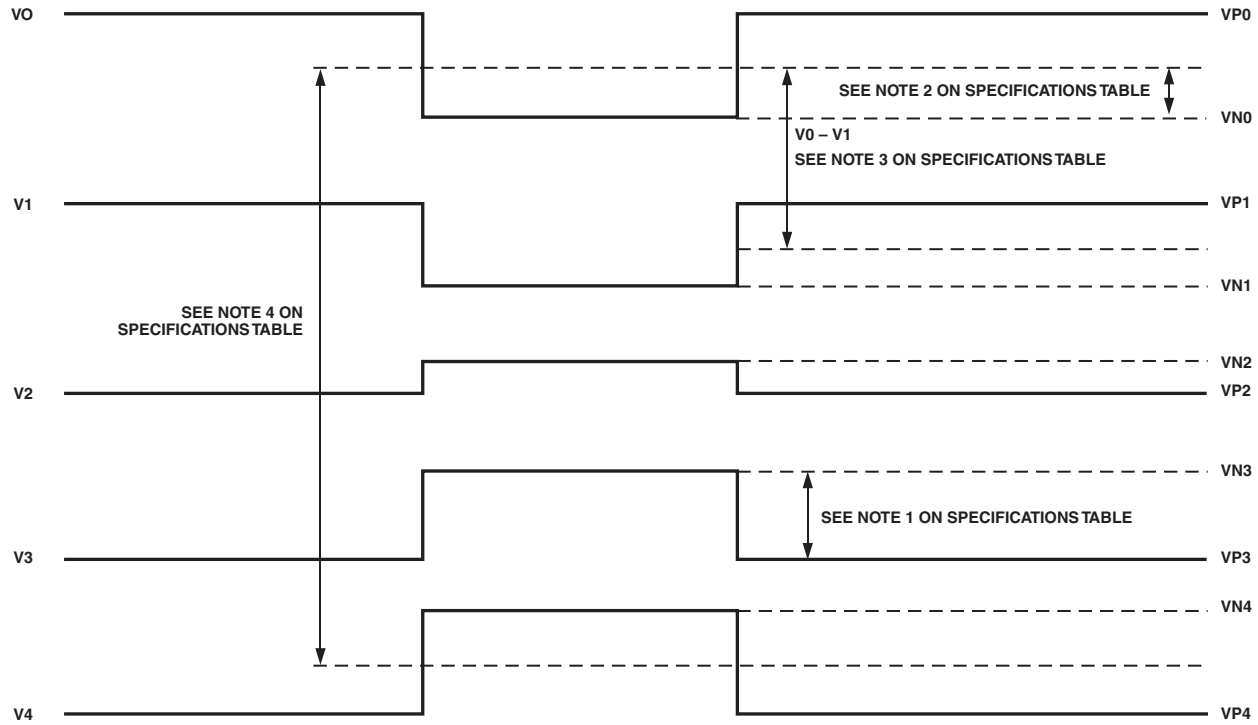

Figure 3. Output Wave Form Diagram