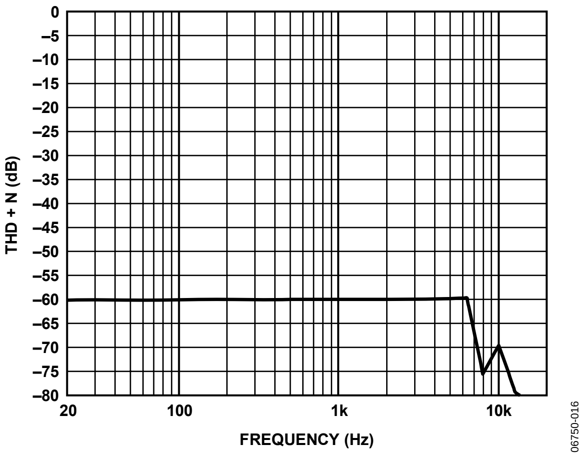


Figure 17. THD + N vs. Frequency, 1 W, 15 V, 8 Ω

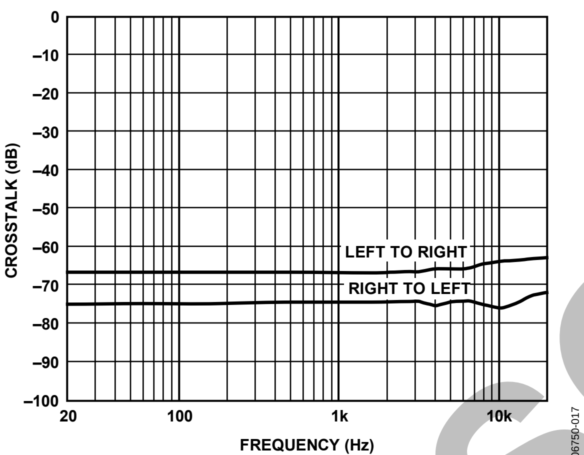


Figure 18. Crosstalk, 0 dBFS, 15 V, 8 Ω

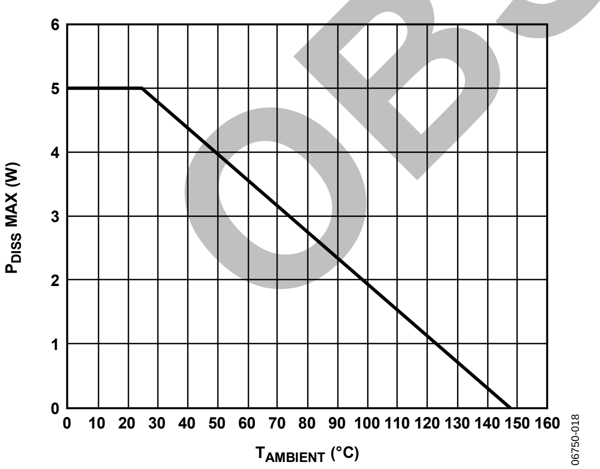


Figure 19. Power Dissipation vs. Ambient Temperature

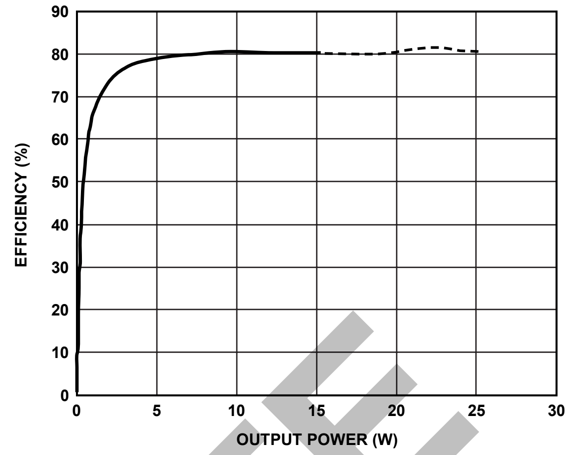


Figure 20. Efficiency vs .Output Power, 15 V, 4 Ω

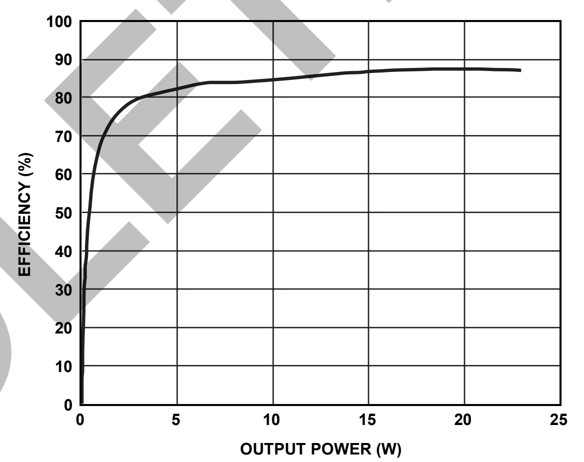


Figure 21. Efficiency vs. Output Power, 15 V, 6 Ω

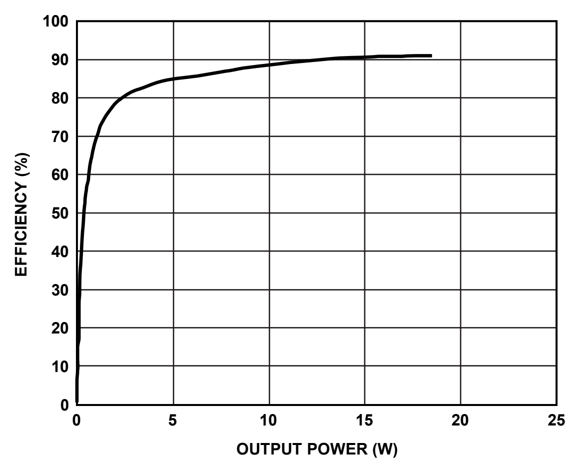


Figure 22. Efficiency vs. Output Power, 15 V, 8 Ω

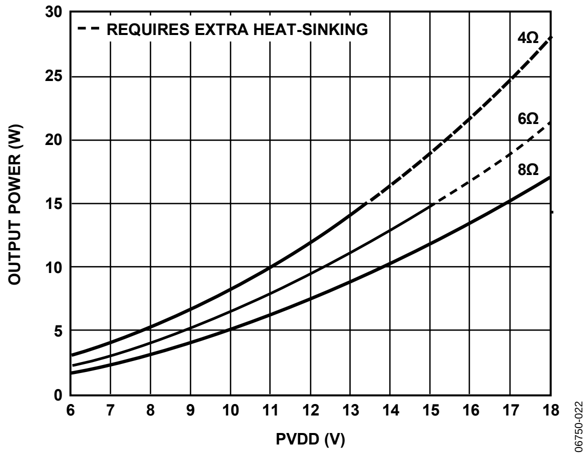


Figure 23. Output Power vs. PVDD, 40 dB THD + N

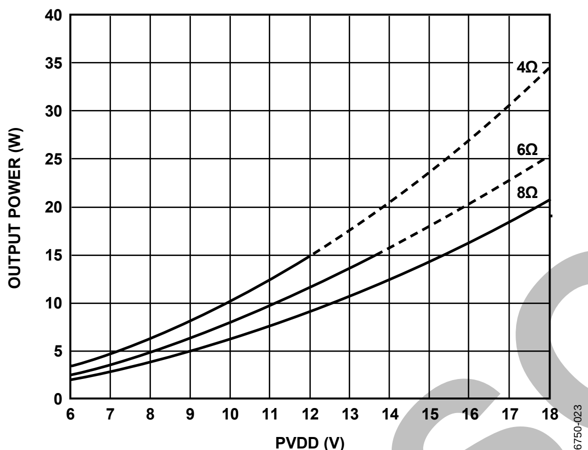


Figure 24. Output Power vs. PVDD, 20 dB THD + N

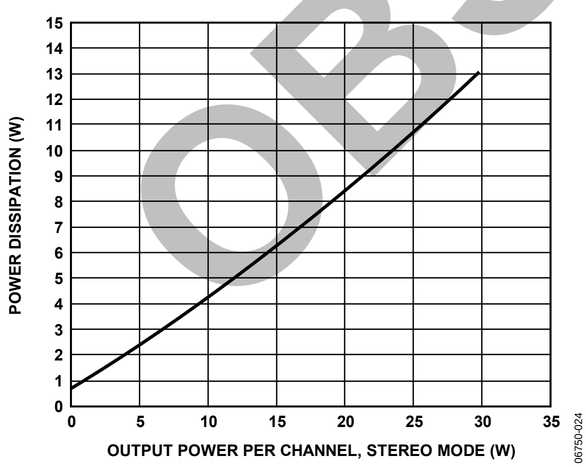


Figure 25. Power Dissipation vs. Output Power, 4 Ω

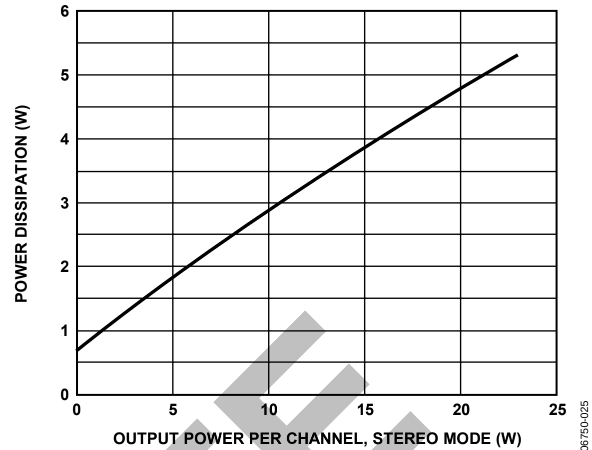


Figure 26. Power Dissipation vs. Output Power, 6 Ω

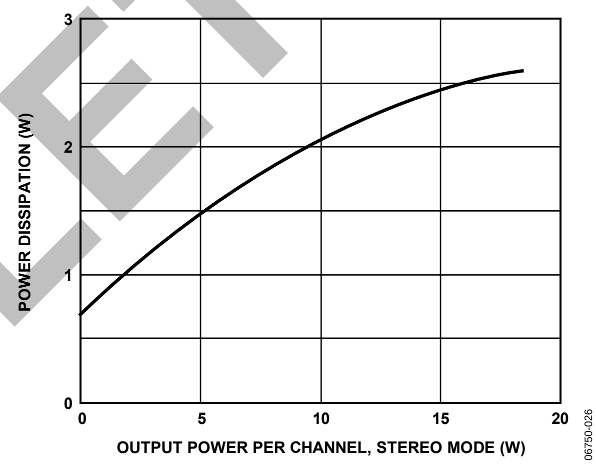


Figure 27. Power Dissipation vs. Output Power, 8 Ω

THEORY OF OPERATION

OVERVIEW

The ADAU1513 is a 2-channel integrated power stage designed to accept the logic level PWM inputs. The PWM inputs are amplified, low-pass filtered using a simple passive LC network, and then can be used to drive the speaker loads. The power stage has built-in circuits for overtemperature, overcurrent, short-circuit, and undervoltage protection.

POWER STAGE

The 2-channel ADAU1513 power stage comprises a total of eight half bridges. Each half bridge is made up of PMOS and NMOS devices. The gate drive for the respective FETs is generated internally and does not need a special gate drive supply or bootstrap capacitor compared to all NMOS stages. This simplifies the high-side driver design and requires less external components.

PROTECTION CIRCUITS

The ADAU1513 includes comprehensive protection circuits. It includes thermal warning, thermal overheat, and overcurrent or short-circuit protection on the outputs. The ERR and OTW outputs are open drain, requiring external pull-up resistors. The outputs are capable of sinking 10 mA. The open-drain outputs are useful in multichannel applications where more than one ADAU1513 are used. The error outputs of multiple ADAU1513s can be OR'ed to simplify the system design. The logic outputs of the error flags ease the system design using a microcontroller.

The power stage does not consist of protection in case PWM input stays high continuously. In such a case, the output produces dc and it is possible to damage the speaker. To prevent this, ensure that the modulator is switching whenever the power stage is turned on.

THERMAL PROTECTION

Thermal protection in the ADAU1513 is categorized into two error flags: one as thermal warning and the other as thermal shutdown. When the device junction temperature reaches near 135°C (±5°C) the ADAU1513 outputs a thermal warning error flag by pulling OTW (Pin 10) low. This flag can be used by the microcontroller in the system as an indication to the user or can be used to lower the input level to the amplifier to prevent the thermal shutdown. The device continues operation until shutdown temperature is reached.

When the device junction temperature exceeds 150°C the device outputs an error flag by pulling the ERR (Pin 9) low. This error flag is latched. To restore the operation, MUTE (Pin 16) needs to be toggled to low and then to high again.

OVERCURRENT PROTECTION

The overcurrent protection in the ADAU1513 is set internally at 5 A peak output current. The device protects the output devices against excessive output current by pulling the ERR (Pin 9) low. This error flag is latched type. To restore the normal operation, MUTE (Pin 16) needs to be toggled to low and then to high again. The error flag is useful for the microcontroller in the system to indicate an abnormal operation and to initiate the audio MUTE sequence. The device senses the short-circuit condition on the outputs after the LC filter. Typical short-circuit conditions include shorting of the output load and shorting to either PVDD or GND.

UNDERVOLTAGE PROTECTION

The ADAU1513 has an undervoltage protection circuit that senses the undervoltage on PVDD. When the PVDD supply goes below the operating threshold, the output FETs are turned to a high-Z condition. Also, the device issues an error flag by pulling the ERR pin low. This condition is latched. To restore the operation, MUTE (Pin 16) needs to be toggled to low and then to high again.

AUTOMATIC RECOVERY FROM PROTECTIONS

In certain applications, it is desired for the amplifier to recover itself from thermal protection without the need for system microcontroller intervention.

The ADAU1513 thermal protection circuit issues two error signals for this purpose: one thermal warning (OTW) and the other thermal shutdown (ERR).

With these two error signals, there are two options for using the protections:

- Option 1: Using OTW
- Option 2: Using ERR

The following sections provide further details of these two options.

Option 1: Using OTW

The OTW pin is pulled low when the die temperature reaches 130°C to 135°C This pin can be wired to the MUTE pin using an RC circuit as shown in Figure 28.

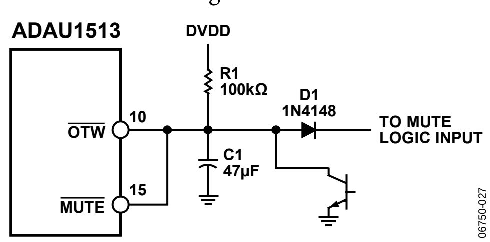


Figure 28. Option 1 Schematic for Autorecovery

The low logic level on OTW also pulls down the MUTE pin. The bridge is shut down and, therefore, starts cooling or the die temperature starts reducing. When it reaches 120°C, the OTW signal starts going high. While this pin is tied to a capacitor with a resistor pulled to DVDD, the voltage on this pin starts rising slowly towards DVDD. When it reaches the input logic high threshold, MUTE is deasserted and the amplifier starts functioning again. This cycle repeats itself depending on the input signal conditions and the temperature of the die. This option allows part operation that is safely below the shutdown temperature of 150°C and allows the amplifier to recover itself without the need for microcontroller intervention.

Option 2: Using $\overline{\text{ERR}}$

Option 2 is similar to Option 1 if the $\overline{\text{ERR}}$ pin can be tied to $\overline{\text{MUTE}}$ instead of $\overline{\text{OTW}}$. See the circuit in Figure 29.

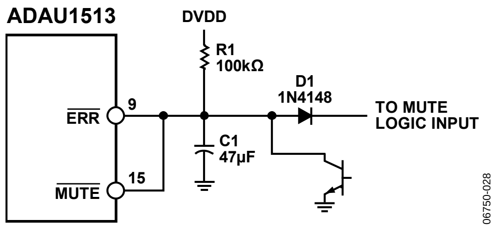


Figure 29. Option 2 Schematic for Autorecovery

In this case, the part goes into shutdown mode due to any of the error-generating events like output overcurrent, overtemperature, missing PVDD or DVDD, or clock loss. The part recovers itself based on the same circuit operation in Figure 28.

However, if the part goes into error mode due to overtemperature, then the device would have reached its maximum limit of 150°C (15°C to 20°C higher than Option 1). If it goes into error mode due to an overcurrent from a short circuit on the speaker outputs, then the part will keep itself recycling on and off until the short circuit is removed.

It is possible that, with this operation, the part is subjected to a much higher temperature and current stress continuously. This, in turn, reduces the part's reliability in the long term. Therefore, using Option 1 for autorecovery from the thermal protection and using the system microcontroller to indicate to the user of an error condition is recommended.

$\overline{\text{MUTE}}$ AND $\overline{\text{STDN}}$

The $\overline{\text{MUTE}}$ and $\overline{\text{STDN}}$ are 3.3 V logic-compatible inputs used to control the turn-on/turn-off for ADAU1513.

The $\overline{\text{STDN}}$ input is active low when the $\overline{\text{STDN}}$ pin is pulled low and the device is in its energy-saving mode. The power stage is in high-Z state. The high logic level input on the $\overline{\text{STDN}}$ pin will wake up the device. The logic circuits are running internally but the power stage is still in high-Z state.

When the $\overline{\text{MUTE}}$ pin is pulled high, the power stage is active and starts responding to PWM inputs. The low level on the $\overline{\text{MUTE}}$ pin disables the power stage and is recommended to be used to mute the audio output. See the Power-Up/Power-Down Sequence section for more details.

POWER-UP/POWER-DOWN SEQUENCE

Figure 30 shows the recommended power-up sequence for the ADAU1513.

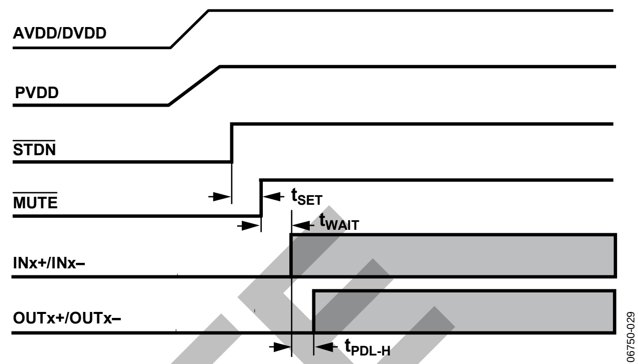


Figure 30. Recommended Power-Up Sequence

The ADAU1513 does not have any pop-and-click suppression circuits; therefore, care must be taken during the power-up. The power stage stays in Hi-Z on power-up. However, it is recommended to ensure that $\overline{\text{STDN}}$ and $\overline{\text{MUTE}}$ are held low during initial power-up. First, $\overline{\text{STDN}}$ should be pulled high followed by $\overline{\text{MUTE}}$ to turn on the power stage. The power stage turns on after the $\overline{\text{MUTE}}$ signal is pulled high and responds to PWM inputs after a small propagation delay of 200 µs.

The special turn-on sequence may be necessary depending on the PWM used to prevent the turn-on pop or click. However, if the ADAV4201 processor is used, the processor has a built-in special turn-on PWM sequence. The processor sends a unique PWM input start sequence that ensures soft turn-on.

If another modulator is used, care must be taken to ensure that the modulator has built-in pop-and-click suppression. Also, because the power stage does not track the PWM inputs, it is recommended to use the system microcontroller to ensure that the modulator is ready to send the PWM sequence before turning on the power stage.

Similarly, for muting the amplifier, it may be necessary to supply a special muting PWM sequence for minimum pop and click. The ADAV4201 processor has a built-in feature that takes care of this need. If any other modulator is used, care must be taken during muting of the power stage.

The system microcontroller can be used to handle the mute/unmute of the power stage as well as a modulator.

The error outputs of the power stage should be connected to the microcontroller port. This error flag can be used to inform the modulator that the power stage is shut down and to mute the PWM inputs. On removal of the error condition, the microcontroller should initiate an unmute sequence to minimize pop and click while power stage is turning on/turning off.

The ADAU1513 uses three separate supplies: AVDD (3.3 V analog for internal reference), DVDD (3.3 V digital for control logic and clock oscillator), and PVDD (9 V to 18 V power stage and level shifter). Separate pins are provided for the AVDD, DVDD, and PVDD supply connections, as well AGND, DGND, and PGND.

In addition, the ADAU1513 incorporates a built-in undervoltage lockout logic on DVDD as well as PVDD. This helps detect undervoltage operation and eliminates the need to have an external mechanism to sense the supplies.

The ADAU1513 monitors the DVDD and PVDD supply voltages and prevents the power stage from turning on if either of the supplies are not present or below the operating threshold. Therefore, if DVDD is missing or below the operating threshold, for example, the power stage will not turn on, even if the PVDD is present or vice versa.

Because this protection is only present on DVDD and PVDD and not on AVDD, shorting both AVDD and DVDD externally or generating AVDD and DVDD from one power source is recommended. This ensures both AVDD and DVDD supplies are tracking each other and avoids the need to monitor the sequence with respect to PVDD. This also ensures minimal pop and click during power-up.

When using separate AVDD and DVDD supplies, ensure that both supplies are stable before unmuting or turning on the power stage.

During power-up, it is recommended to keep $\overline{\text{STDN}}$ and $\overline{\text{MUTE}}$ low to ensure that the power stage stays in high-Z mode.

Similarly, during shutdown, pulling $\overline{\text{MUTE}}$ to logic low before pulling $\overline{\text{STDN}}$ down is recommended. However, where a fault event occurs, the power stage will shut down to protect the part. In this case, depending on the signal level, there is some pop at the speaker.

During shutdown of the power supplies to reduce power consumption, it is highly recommended to mute the amplifier first, followed by pulling $\overline{\text{STDN}}$ low before shutting down any of the supplies. After MUTE is pulled low, the power supplies can be shut down in the following order: PVDD, DVDD, then AVDD. Where AVDD and DVDD are generated from a single source, ensure that PVDD is tuned off before DVDD and AVDD, and after issuing $\overline{\text{MUTE}}$ and $\overline{\text{STDN}}$.

APPLICATIONS INFORMATION

Refer to the application schematic in Figure 31 for details on connections and component values. For details on the PWM modulator part, refer to the ADAV4201 data sheet.

For applications with PVDD > 15 V, add components R1 and R2 = 10 Ω typical, C5 and C6 = 680 pF typical, and D1 through D8 = CRS01/02.

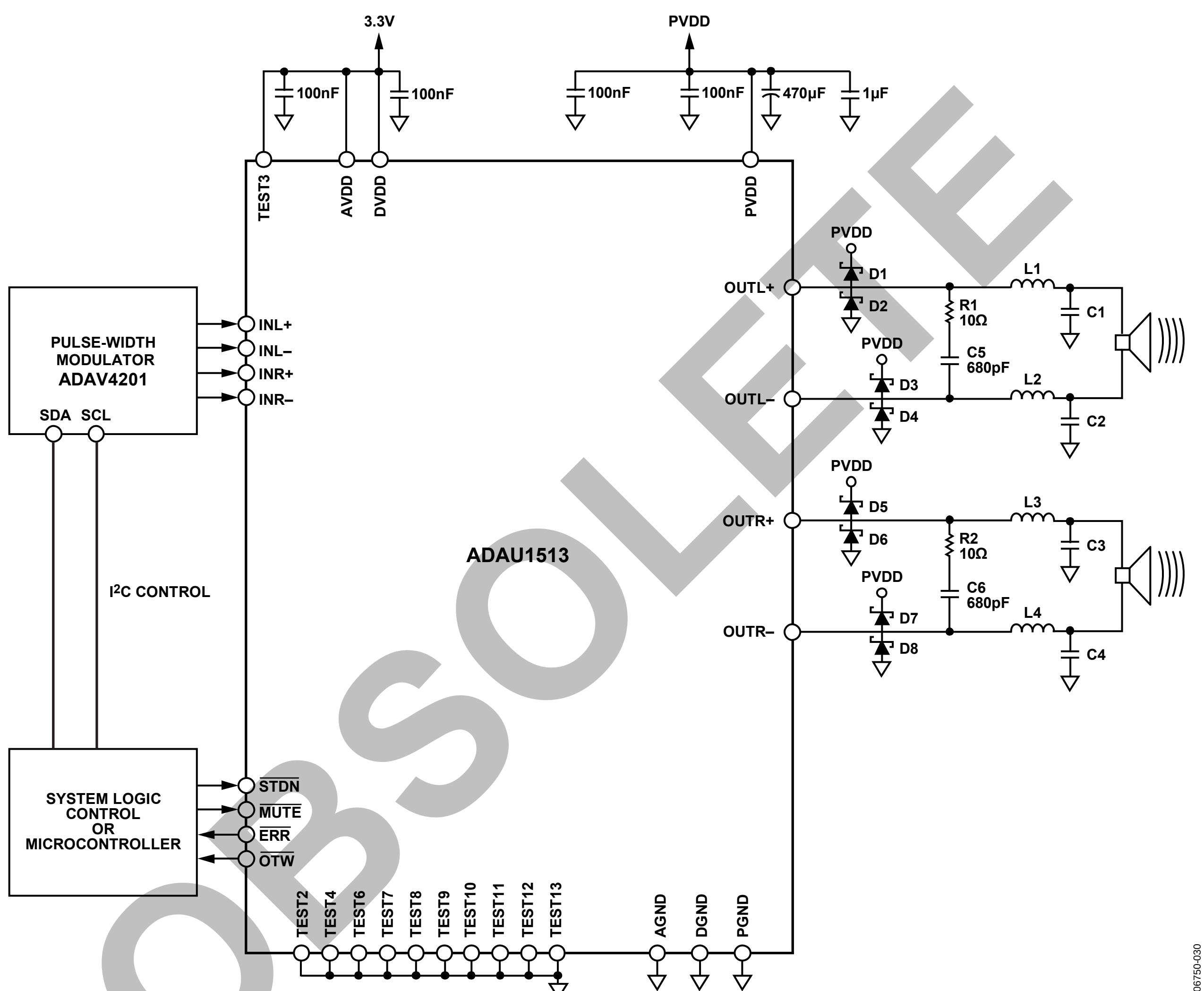
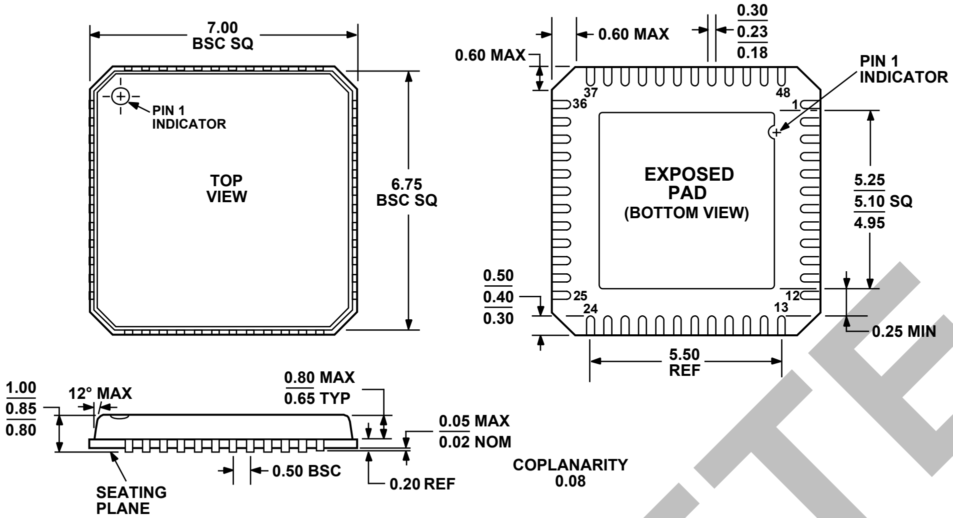


Figure 31. Application Schematic

Table 8. Suggested Low-Pass Filter Values

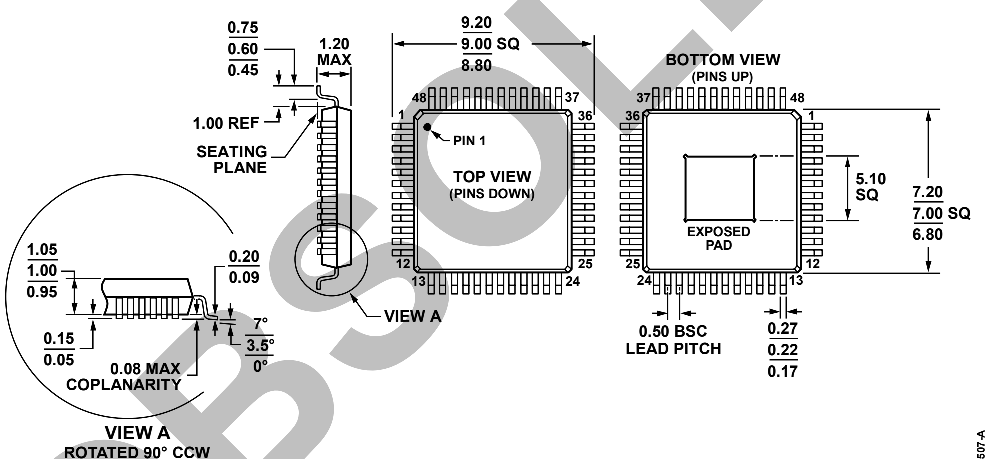
Load Impedance (Ω)	Inductance L1 to L4 (µH)	Capacitance C1 to C4 (µF)
4	10	1.5
6	15	1
8	22	0.68

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VKKD-2

Figure 32. 48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
7 mm × 7 mm Body, Very Thin Quad
(CP-48-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-026-ABC

Figure 33. 48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]
(SV-48-5)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADAU1513ACPZ[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-48-1
ADAU1513ACPZ-RL[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 13" Tape and Reel	CP-48-1
ADAU1513ACPZ-RL7[1]	−40°C to +85°C	48-Lead Lead Frame Chip Scale Package [LFCSP_VQ], 7" Tape and Reel	CP-48-1
ADAU1513ASVZ[1]	−40°C to +85°C	48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP]	SV-48-5
ADAU1513ASVZ-RL[1]	−40°C to +85°C	48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP], 13" Tape and Reel	SV-48-5
ADAU1513ASVZ-RL7[1]	−40°C to +85°C	48-Lead Thin Quad Flat Package, Exposed Pad [TQFP_EP], 7" Tape and Reel	SV-48-5

[1] Z = RoHS Compliant Part.

D06750-0-5/07(0)