

### FEATURES

- Single supply operation: 4.5 V to 30 V
- Dual supply operation:  $\pm 2.25$  V to  $\pm 15$  V
- Low offset voltage: 4  $\mu$ V maximum
- Input offset voltage drift: 0.05  $\mu$ V/ $^{\circ}$ C maximum
- High gain: 130 dB minimum
- High PSRR: 120 dB minimum
- High CMRR: 130 dB minimum
- Input common-mode range includes lower supply rail
- Rail-to-rail output
- Low supply current: 0.95 mA maximum

### APPLICATIONS

- Electronic weigh scale
- Pressure and position sensors
- Strain gage amplifiers
- Medical instrumentation
- Thermocouple amplifiers

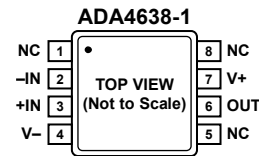
### GENERAL DESCRIPTION

The [ADA4638-1](#) is a high voltage, high precision, zero-drift amplifier featuring rail-to-rail output swing. It is guaranteed to operate from 4.5 V to 30 V single supply or  $\pm 2.25$  V to  $\pm 15$  V dual supplies while consuming less than 0.95 mA of supply current at  $\pm 5$  V.

With an offset voltage of 4  $\mu$ V, offset drift less than 0.05  $\mu$ V/ $^{\circ}$ C, no 1/f noise, and input voltage noise of only 1.2  $\mu$ V p-p (0.1 Hz to 10 Hz), the [ADA4638-1](#) is suited for high precision applications where large error sources cannot be tolerated. Pressure sensors, medical equipment, and strain gage amplifiers benefit greatly from nearly zero drift over the wide operating temperature range. Many applications can take advantage of the rail-to-rail output swing provided by the [ADA4638-1](#) to maximize the signal-to-noise ratio (SNR).

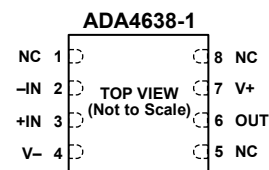
The [ADA4638-1](#) is specified for the extended industrial ( $-40^{\circ}$ C to  $+125^{\circ}$ C) temperature range and is available in 8-lead LFCSP (3 mm  $\times$  3 mm) and SOIC packages.

### PIN CONFIGURATIONS



- NOTES  
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.

Figure 1. 8-Lead SOIC



- NOTES  
1. NC = NO CONNECT. DO NOT CONNECT TO THIS PIN.  
2. IT IS RECOMMENDED THAT THE EXPOSED PAD BE CONNECTED TO V-.

Figure 2. 8-Lead LFCSP

Table 1. Analog Devices, Inc., Zero-Drift Op Amp Portfolio

Operating Voltage	Type	Product	Offset Voltage ( $\mu$ V) Max	Offset Voltage Drift ( $\mu$ V/ $^{\circ}$ C) Max
30 V	Single	<a href="#">ADA4638-1</a>	4.5	0.08
16 V	Single	<a href="#">AD8638</a>	9	0.06
	Dual	<a href="#">AD8639</a>	9	0.06
5 V	Single	<a href="#">ADA4528-1</a>	2.5	0.015
		<a href="#">AD8628</a>	5	0.02
		<a href="#">AD8538</a>	13	0.1
		<a href="#">ADA4051-1</a>	15	0.1
	Dual	<a href="#">AD8629</a>	5	0.02
		<a href="#">AD8539</a>	13	0.1
		<a href="#">ADA4051-2</a>	15	0.1
Quad	<a href="#">AD8630</a>	5	0.02	

#### Rev. 0

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**REVISION HISTORY**

**10/11—Revision 0: Initial Version**

## SPECIFICATIONS

## ELECTRICAL CHARACTERISTICS—30 V OPERATION

$V_S = 30\text{ V}$ ,  $V_{CM} = V_{SY}/2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; SOIC		0.5	4.5	$\mu\text{V}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; LFCSP			12.5	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; SOIC			14.5	$\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; LFCSP			0.1	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		45	90	$\text{pA}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			500	$\text{pA}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		25	105	$\text{pA}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			170	$\text{pA}$
Input Voltage Range			0		27	$\text{V}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 27\text{ V}$	130	142		$\text{dB}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	130			$\text{dB}$
Open-Loop Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $V_O = 1\text{ V to } 29\text{ V}$	140	165		$\text{dB}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	140			$\text{dB}$
Input Resistance, Common Mode	$R_{INCM}$			330		$\text{G}\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			4		$\text{pF}$
Input Capacitance, Common Mode	$C_{INCM}$			9		$\text{pF}$
OUTPUT CHARACTERISTICS						
Output Voltage High	$V_{OH}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$	29.90	29.92		$\text{V}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	29.85			$\text{V}$
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$	29.50	29.58		$\text{V}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	29.35			$\text{V}$
Output Voltage Low	$V_{OL}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$		50	60	$\text{mV}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			95	$\text{mV}$
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$		235	270	$\text{mV}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			445	$\text{mV}$
Short-Circuit Current	$I_{SC}$			$\pm 38$		$\text{mA}$
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_v = +1$		220		$\Omega$
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 4.5\text{ V to } 30\text{ V}$	120	143		$\text{dB}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120			$\text{dB}$
Supply Current/Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$		0.85	1.05	$\text{mA}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			1.25	$\text{mA}$
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_v = +1$		1.5		$\text{V}/\mu\text{s}$
Overload Recovery Time		$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_v = -100$		8		$\mu\text{s}$
Settling Time to 0.1%	$t_s$	$V_{IN} = 5\text{ V step}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_v = -1$		4		$\mu\text{s}$
Unity-Gain Crossover	UGC	$V_{IN} = 30\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_v = +1$		1.3		$\text{MHz}$
Phase Margin	$\Phi_M$	$V_{IN} = 30\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_v = +1$		69		Degrees
Gain-Bandwidth Product	GBP	$V_{IN} = 30\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_v = +100$		1.5		$\text{MHz}$
-3 dB Closed-Loop Bandwidth	$f_{-3dB}$	$V_{IN} = 30\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_v = +1$		2.5		$\text{MHz}$
NOISE PERFORMANCE						
Voltage Noise	$e_n$ p-p	$f = 0.1\text{ Hz to } 10\text{ Hz}$		1.2		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		66		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.1		$\text{pA}/\sqrt{\text{Hz}}$

**ELECTRICAL CHARACTERISTICS—10 V OPERATION**

$V_S = 10\text{ V}$ ,  $V_{CM} = V_{SY}/2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

Table 3.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; SOIC $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; LFCSP		0.1	4	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; SOIC $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; LFCSP			9 12 0.05 0.08	$\mu\text{V}$ $\mu\text{V}$ $\mu\text{V}/^\circ\text{C}$ $\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	50	pA
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	80	pA
Input Voltage Range			0		7	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }7\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	130	155		dB
Open-Loop Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $V_O = 1\text{ V to }9\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	130	160		dB
Input Resistance, Common Mode	$R_{INCM}$			250		G $\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			4		pF
Input Capacitance, Common Mode	$C_{INCM}$			9		pF
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $R_L = 2\text{ k}\Omega$ to $V_{CM}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	9.96 9.95 9.85 9.75	9.97		V V V V
Output Voltage Low	$V_{OL}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ $R_L = 2\text{ k}\Omega$ to $V_{CM}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		20	25 40 90 145	mV mV mV mV
Short-Circuit Current	$I_{SC}$			$\pm 22$		mA
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = +1$		300		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 4.5\text{ V to }30\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120	143		dB
Supply Current/Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.8	0.95 1.15	mA mA
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +1$		1.5		V/ $\mu\text{s}$
Overload Recovery Time		$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = -100$		14		$\mu\text{s}$
Settling Time to 0.1%	$t_s$	$V_{IN} = 2\text{ V step}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = -1$		3		$\mu\text{s}$
Unity-Gain Crossover	UGC	$V_{IN} = 30\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +1$		1.1		MHz
Phase Margin	$\Phi_M$	$V_{IN} = 30\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +1$		67		Degrees
Gain Bandwidth Product	GBP	$V_{IN} = 30\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +100$		1.4		MHz
-3 dB Closed-Loop Bandwidth	$f_{-3dB}$	$V_{IN} = 30\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +1$		1.9		MHz
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n$ p-p	$f = 0.1\text{ Hz to }10\text{ Hz}$		1.2		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		66		nV/ $\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.1		pA/ $\sqrt{\text{Hz}}$

**ELECTRICAL CHARACTERISTICS—5 V OPERATION**

$V_S = 5\text{ V}$ ,  $V_{CM} = V_{SY}/2\text{ V}$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

**Table 4.**

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
<b>INPUT CHARACTERISTICS</b>						
Offset Voltage	$V_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; SOIC		1	13	$\mu\text{V}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; LFCSP			18	$\mu\text{V}$
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; SOIC			21	$\mu\text{V}/^\circ\text{C}$
		$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ; LFCSP			0.05	$\mu\text{V}/^\circ\text{C}$
Input Bias Current	$I_B$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30	90	$\text{pA}$
Input Offset Current	$I_{OS}$	$-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		60	170	$\text{pA}$
					200	$\text{pA}$
Input Voltage Range			0		3	$\text{V}$
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to }3\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	118	140		$\text{dB}$
Open-Loop Gain	$A_{VO}$	$R_L = 10\text{ k}\Omega$ , $V_O = 0.5\text{ V to }+4.5\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	118	150		$\text{dB}$
			125			$\text{dB}$
Input Resistance, Common Mode	$R_{INCM}$			75		$\text{G}\Omega$
Input Capacitance, Differential Mode	$C_{INDM}$			4		$\text{pF}$
Input Capacitance, Common Mode	$C_{INCM}$			9		$\text{pF}$
<b>OUTPUT CHARACTERISTICS</b>						
Output Voltage High	$V_{OH}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.98	4.984		$\text{V}$
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.97			$\text{V}$
			4.90	4.92		$\text{V}$
			4.87			$\text{V}$
Output Voltage Low	$V_{OL}$	$R_L = 10\text{ k}\Omega$ to $V_{CM}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		7.5	10	$\text{mV}$
		$R_L = 2\text{ k}\Omega$ to $V_{CM}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		37	45	$\text{mV}$
					70	$\text{mV}$
Short-Circuit Current	$I_{SC}$			$\pm 22$		$\text{mA}$
Closed-Loop Output Impedance	$Z_{OUT}$	$f = 1\text{ MHz}$ , $A_V = +1$		340		$\Omega$
<b>POWER SUPPLY</b>						
Power Supply Rejection Ratio	PSRR	$V_S = 4.5\text{ V to }30\text{ V}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	120	143		$\text{dB}$
			120			$\text{dB}$
Supply Current/Amplifier	$I_{SY}$	$I_O = 0\text{ mA}$ $-40^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.8	0.95	$\text{mA}$
					1.15	$\text{mA}$
<b>DYNAMIC PERFORMANCE</b>						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +1$		1.5		$\text{V}/\mu\text{s}$
Overload Recovery Time		$R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = -100$		22		$\mu\text{s}$
Settling Time to 0.1%	$t_s$	$V_{IN} = 1\text{ V step}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = -1$		3		$\mu\text{s}$
Unity-Gain Crossover	UGC	$V_{IN} = 20\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +1$		1.0		$\text{MHz}$
Phase Margin	$\Phi_M$	$V_{IN} = 20\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +1$		64		Degrees
Gain Bandwidth Product	GBP	$V_{IN} = 20\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +100$		1.3		$\text{MHz}$
-3 dB Closed-Loop Bandwidth	$f_{-3dB}$	$V_{IN} = 20\text{ mV p-p}$ , $R_L = 10\text{ k}\Omega$ , $C_L = 20\text{ pF}$ , $A_V = +1$		1.8		$\text{MHz}$
<b>NOISE PERFORMANCE</b>						
Voltage Noise	$e_n\text{ p-p}$	$f = 0.1\text{ Hz to }10\text{ Hz}$		1.2		$\mu\text{V p-p}$
Voltage Noise Density	$e_n$	$f = 1\text{ kHz}$		70		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	$i_n$	$f = 1\text{ kHz}$		0.015		$\text{pA}/\sqrt{\text{Hz}}$

## ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	33 V
Input Voltage <sup>1</sup>	$\pm V_{SY}$
Input Current	$\pm 10$ mA
Differential Input Voltage	$\pm V_{SY}$
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +125°C
Junction Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

<sup>1</sup> Input voltage should always be limited to less than 30 V.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL RESISTANCE

$\theta_{JA}$  is specified for a device soldered on a 4-layer JEDEC standard board with zero airflow. For LFCSP packages, the exposed pad is soldered to the board.

Table 6. Thermal Resistance

Package Type	$\theta_{JA}$	$\theta_{JC}$	Unit
8-Lead SOIC	120	45	°C/W
8-Lead LFCSP	75	12	°C/W

## ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# TYPICAL PERFORMANCE CHARACTERISTICS

T<sub>A</sub> = 25°C, unless otherwise noted.

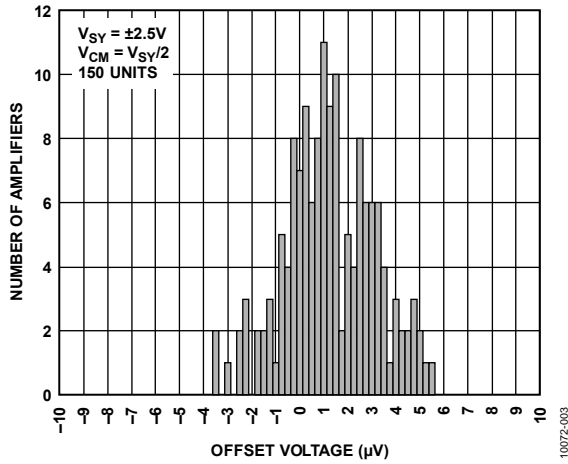


Figure 3. Input Offset Voltage Distribution

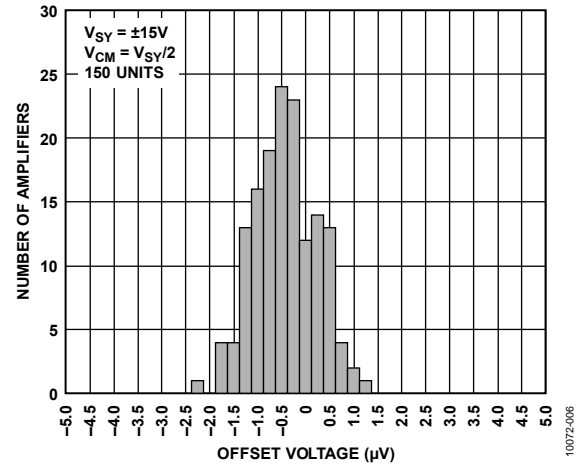


Figure 6. Input Offset Voltage Distribution

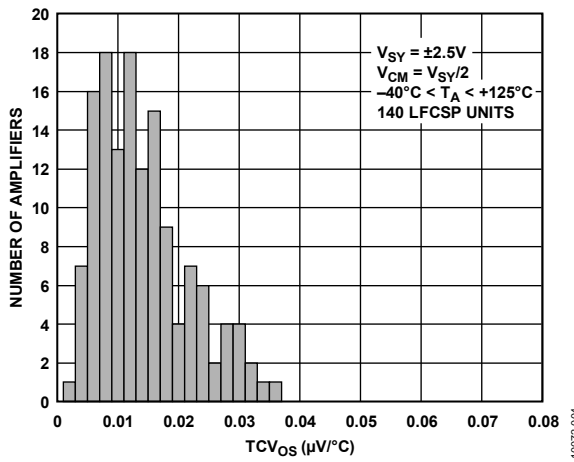


Figure 4. Input Offset Voltage Drift Distribution

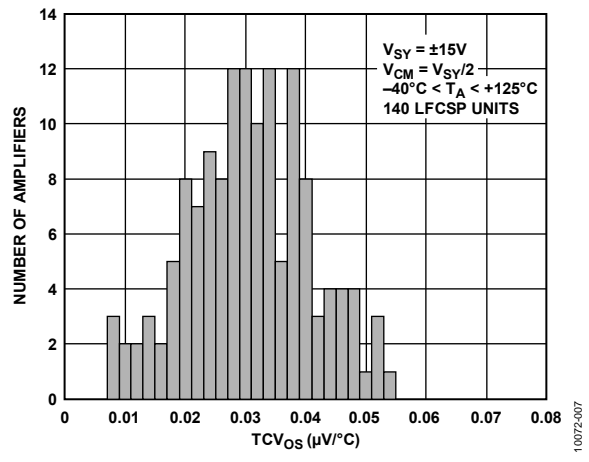


Figure 7. Input Offset Voltage Drift Distribution

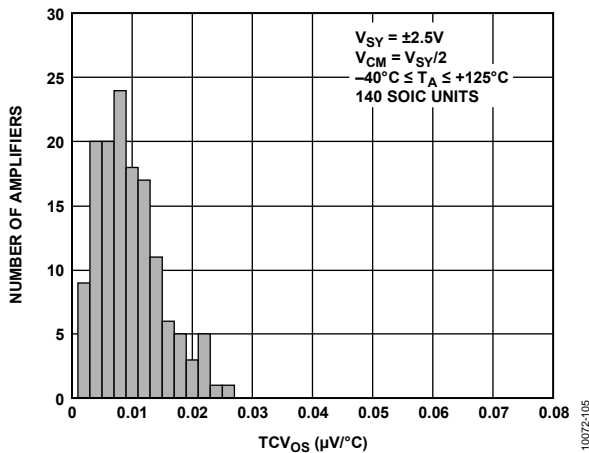


Figure 5. Input Offset Voltage Drift Distribution

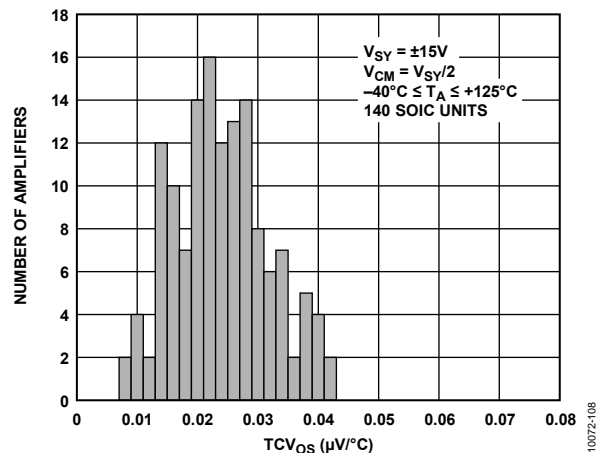


Figure 8. Input Offset Voltage Drift Distribution

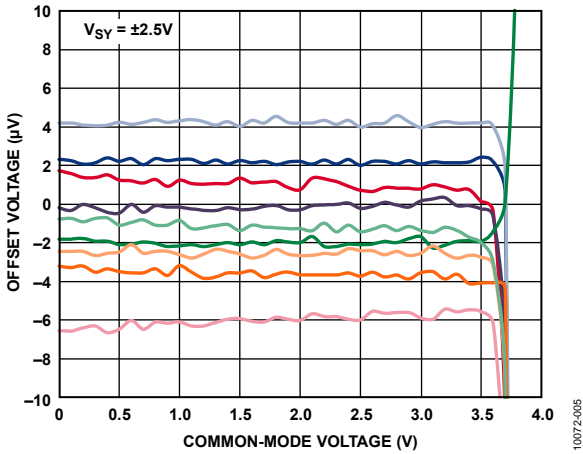


Figure 9. Input Offset Voltage vs. Common-Mode Voltage

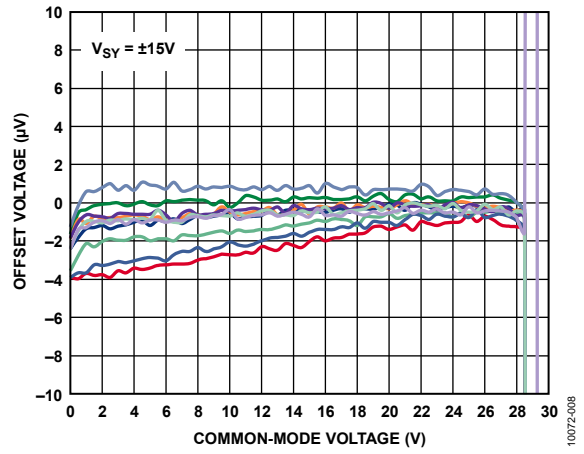


Figure 12. Input Offset Voltage vs. Common-Mode Voltage

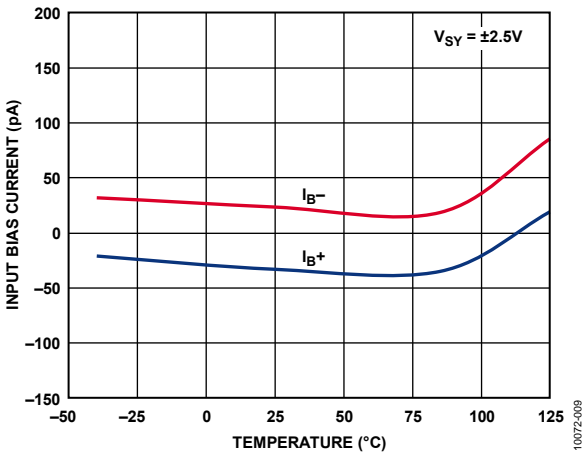


Figure 10. Input Bias Current vs. Temperature

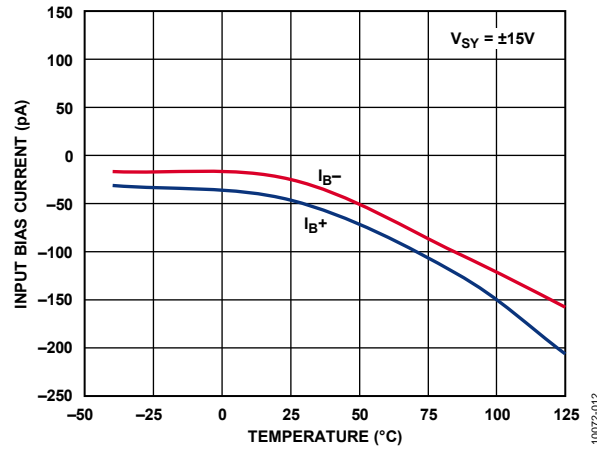


Figure 13. Input Bias Current vs. Temperature

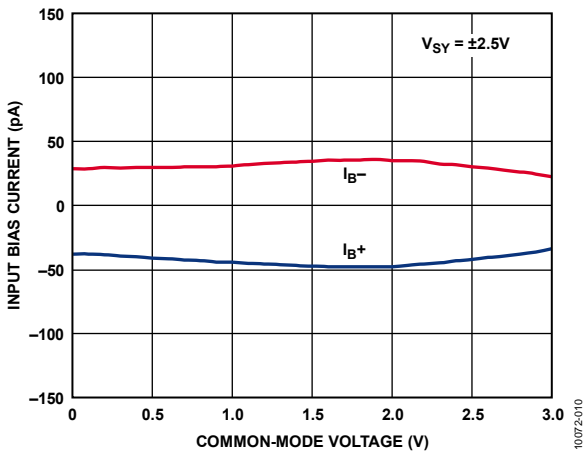


Figure 11. Input Bias Current vs. Common-Mode Voltage

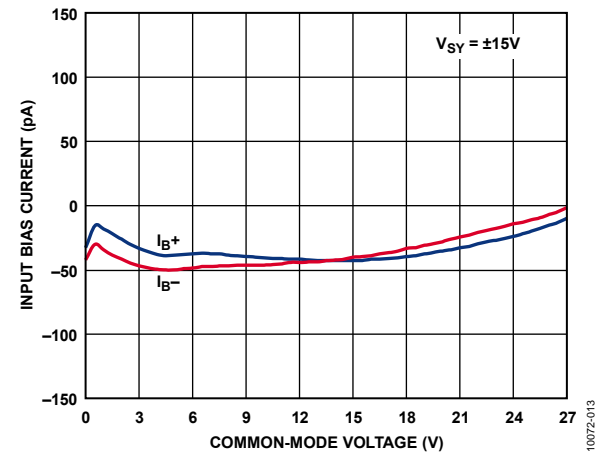


Figure 14. Input Bias Current vs. Common-Mode Voltage



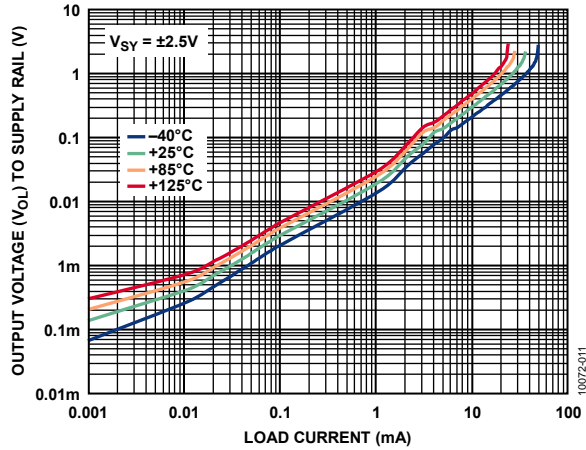


Figure 15. Output Voltage ( $V_{OL}$ ) to Supply Rail vs. Load Current

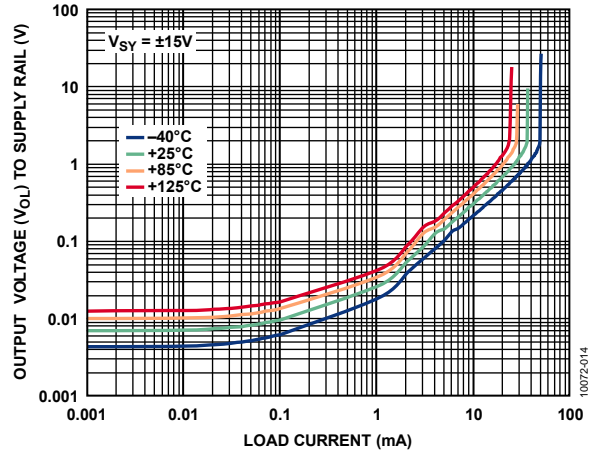


Figure 18. Output Voltage ( $V_{OL}$ ) to Supply Rail vs. Load Current

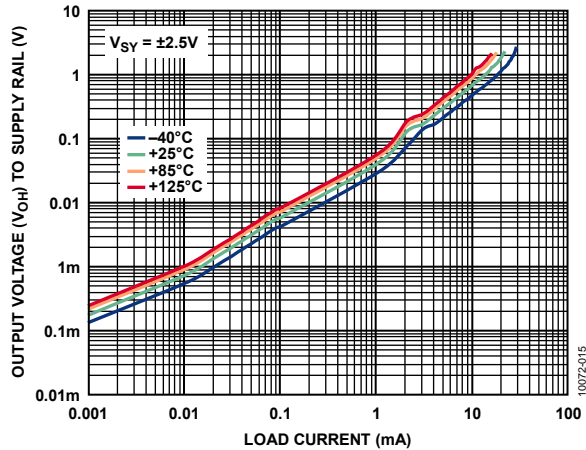


Figure 16. Output Voltage ( $V_{OH}$ ) to Supply Rail vs. Load Current

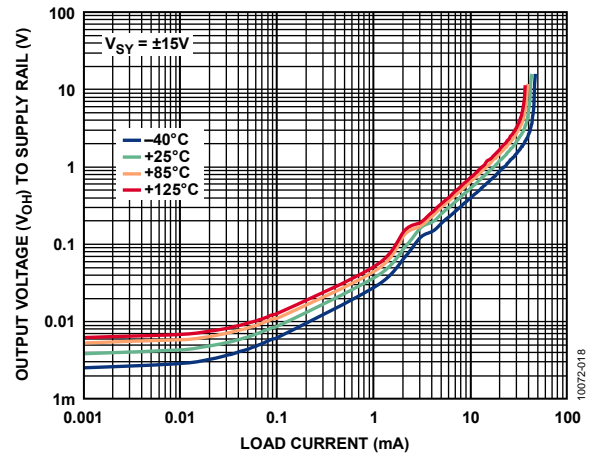


Figure 19. Output Voltage ( $V_{OH}$ ) to Supply Rail vs. Load Current

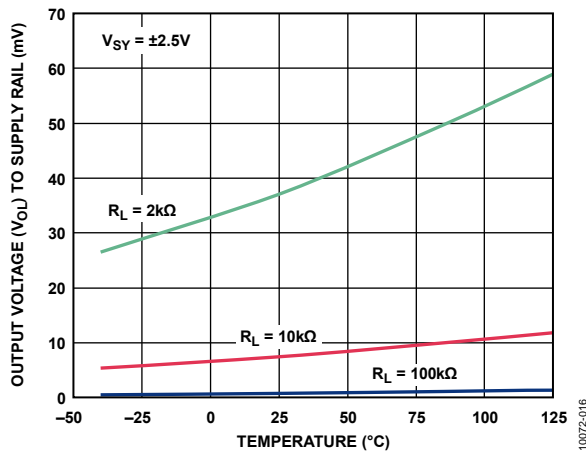


Figure 17. Output Voltage ( $V_{OL}$ ) to Supply Rail vs. Temperature

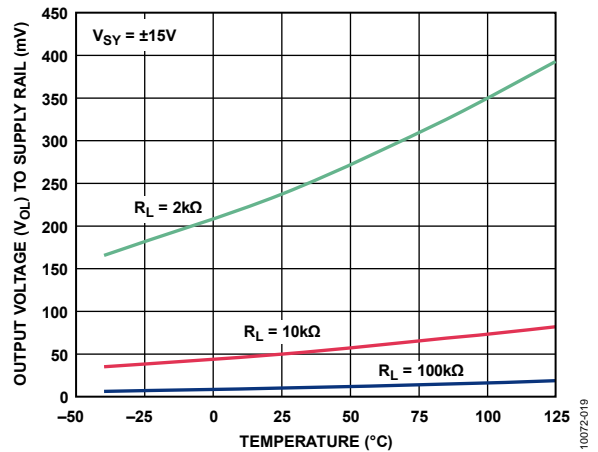


Figure 20. Output Voltage ( $V_{OL}$ ) to Supply Rail vs. Temperature

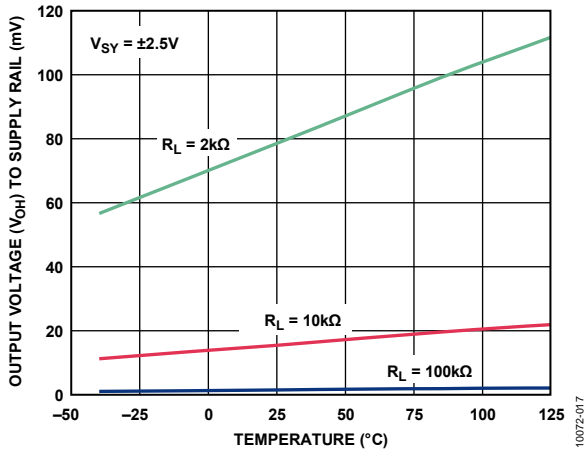


Figure 21. Output Voltage ( $V_{OH}$ ) to Supply Rail vs. Temperature

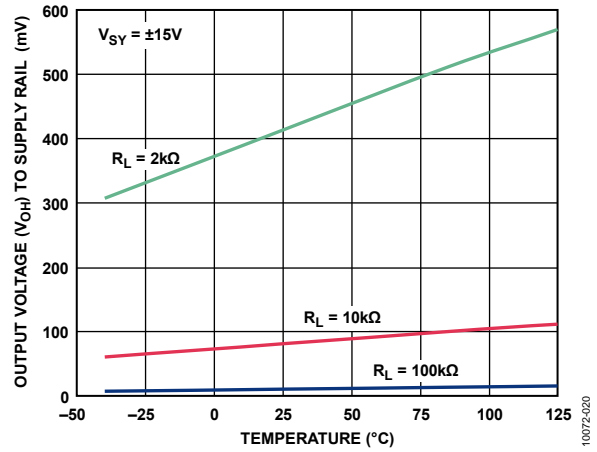


Figure 24. Output Voltage ( $V_{OH}$ ) to Supply Rail vs. Temperature

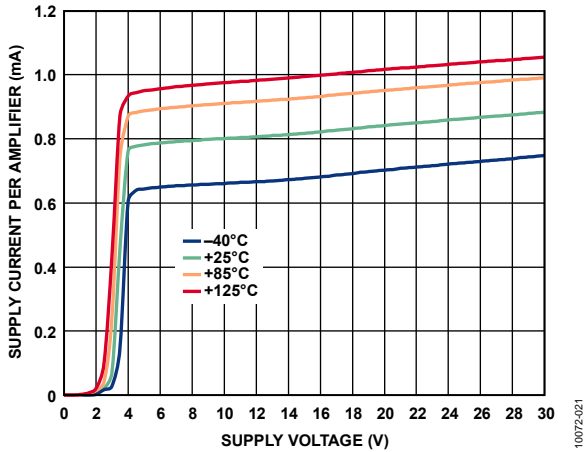


Figure 22. Supply Current vs. Supply Voltage

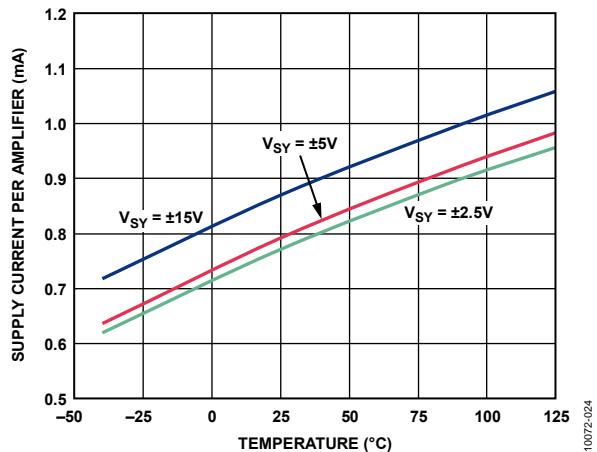


Figure 25. Supply Current vs. Temperature

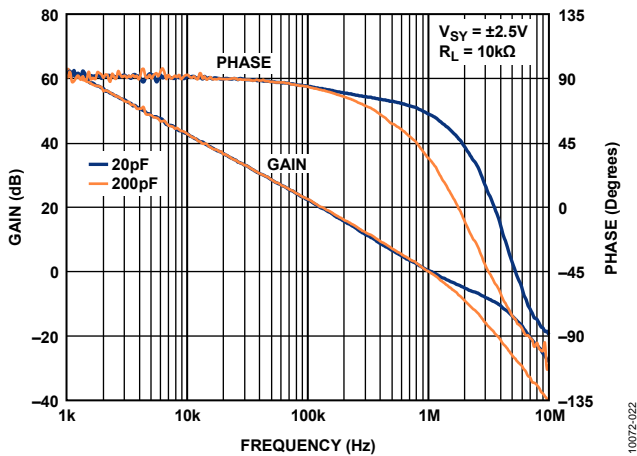


Figure 23. Open-Loop Gain and Phase vs. Frequency

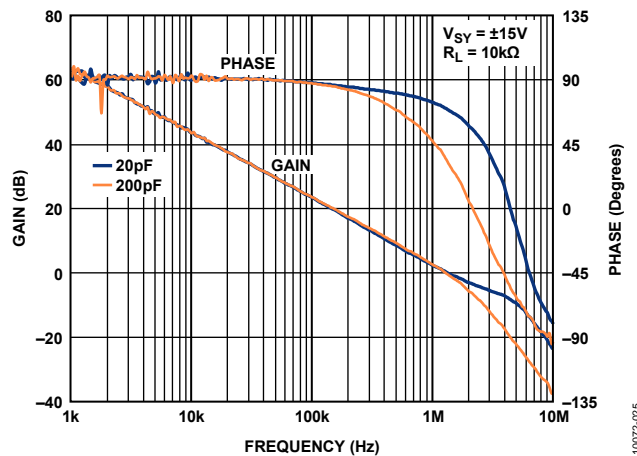


Figure 26. Open-Loop Gain and Phase vs. Frequency

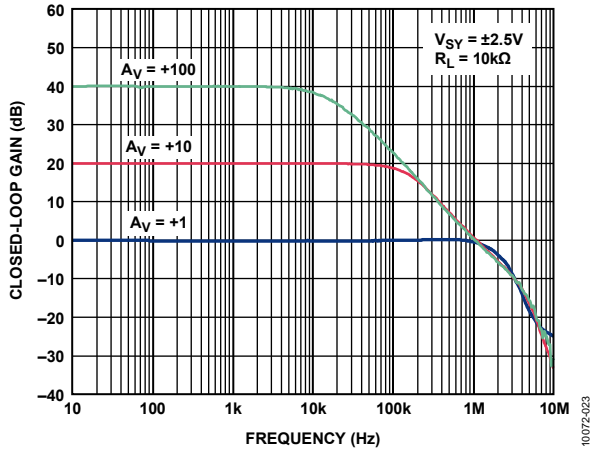


Figure 27. Closed-Loop Gain vs. Frequency

10072-023

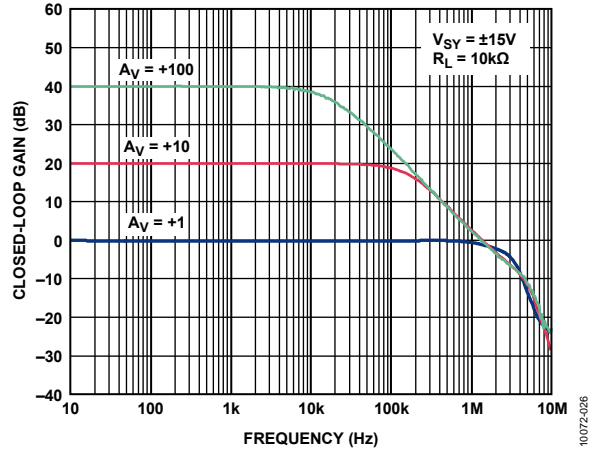


Figure 30. Closed-Loop Gain vs. Frequency

10072-026

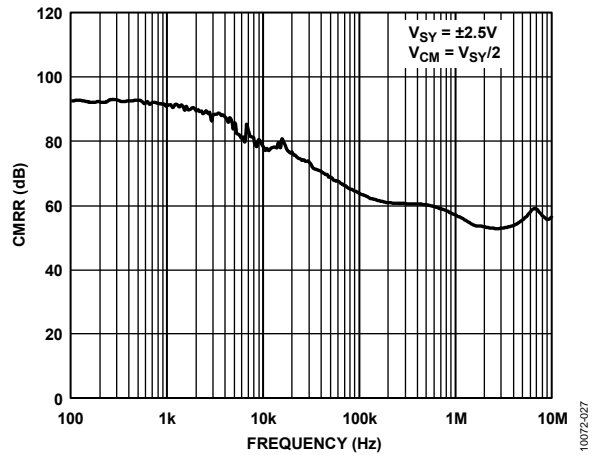


Figure 28. CMRR vs. Frequency

10072-027

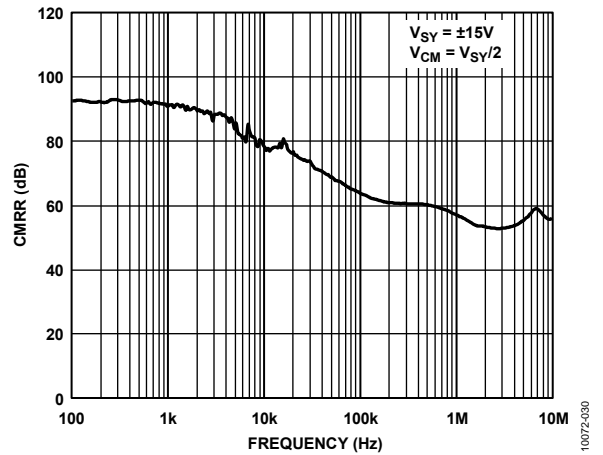


Figure 31. CMRR vs. Frequency

10072-030

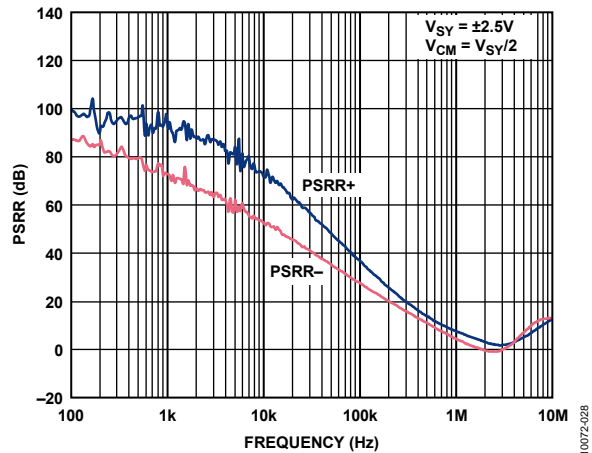


Figure 29. PSRR vs. Frequency

10072-028

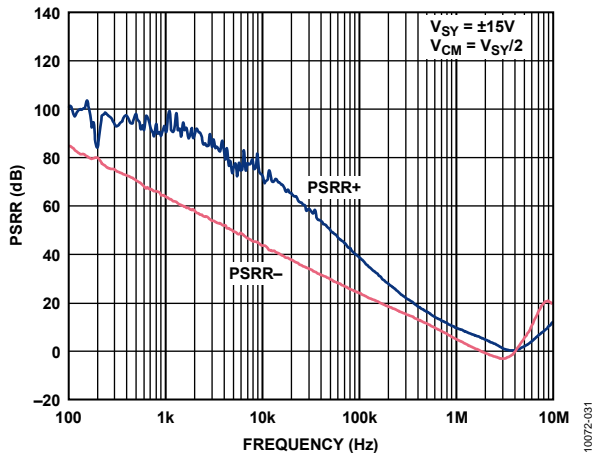


Figure 32. PSRR vs. Frequency

10072-031

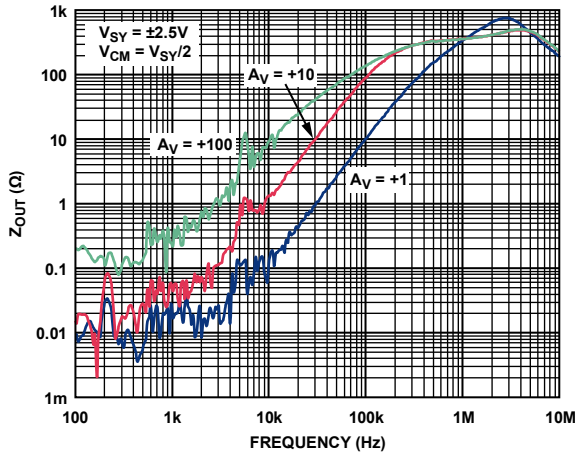


Figure 33. Closed-Loop Output Impedance vs. Frequency

10072-029

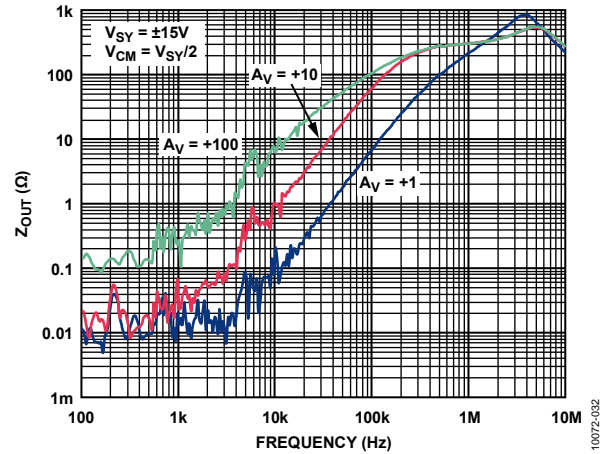


Figure 36. Closed-Loop Output Impedance vs. Frequency

10072-032

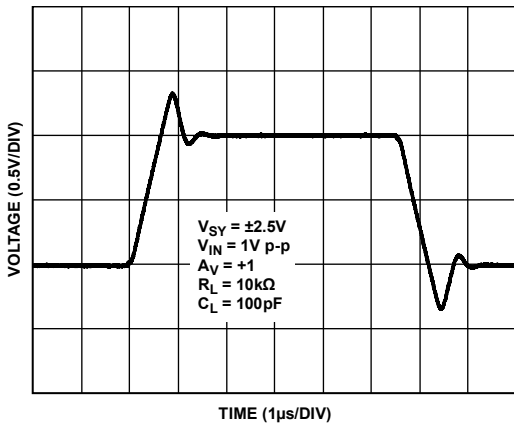


Figure 34. Large Signal Transient Response

10072-033

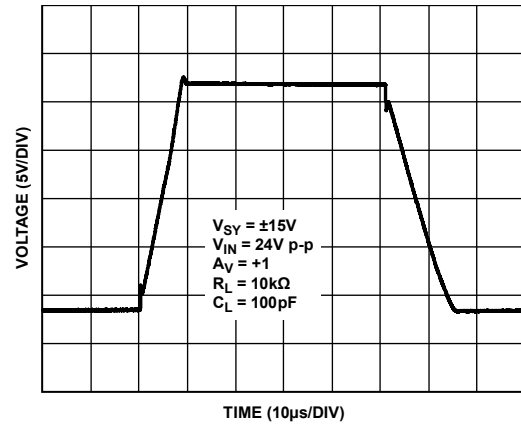


Figure 37. Large Signal Transient Response

10072-036

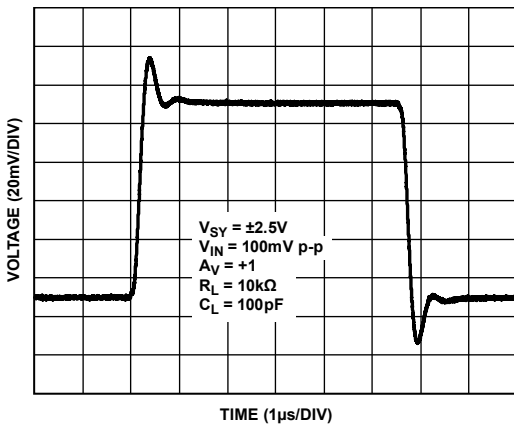


Figure 35. Small Signal Transient Response

10072-034

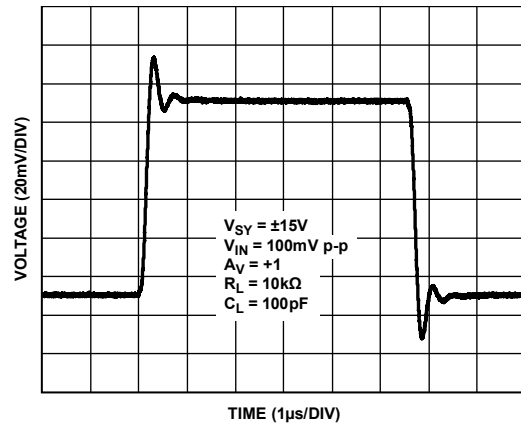


Figure 38. Small Signal Transient Response

10072-037

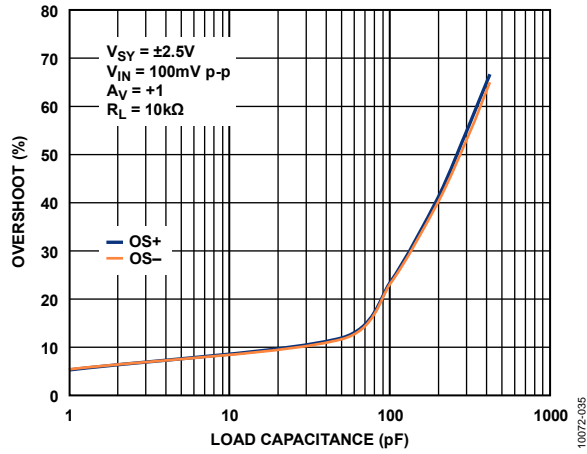


Figure 39. Small Signal Overshoot vs. Load Capacitance

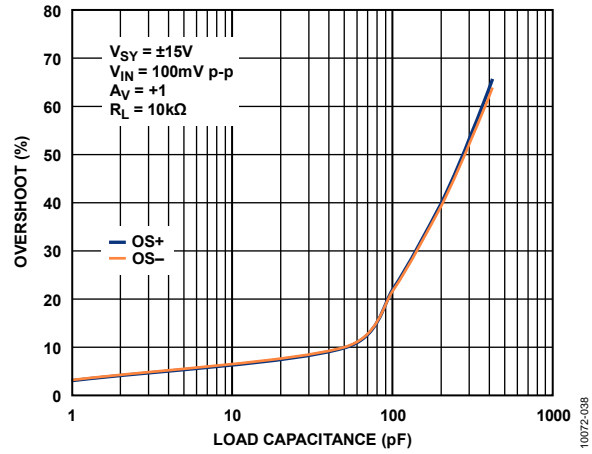


Figure 42. Small Signal Overshoot vs. Load Capacitance

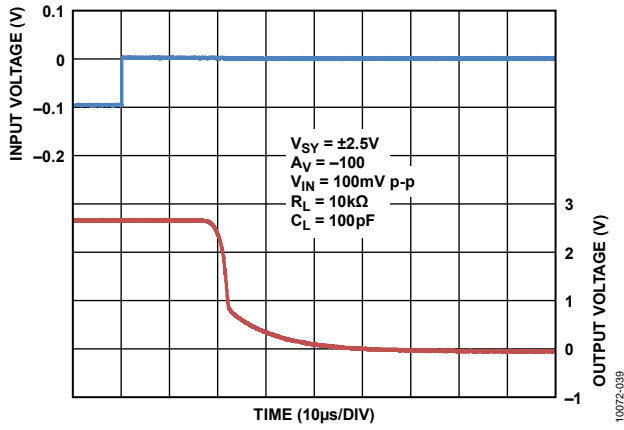


Figure 40. Positive Overload Recovery

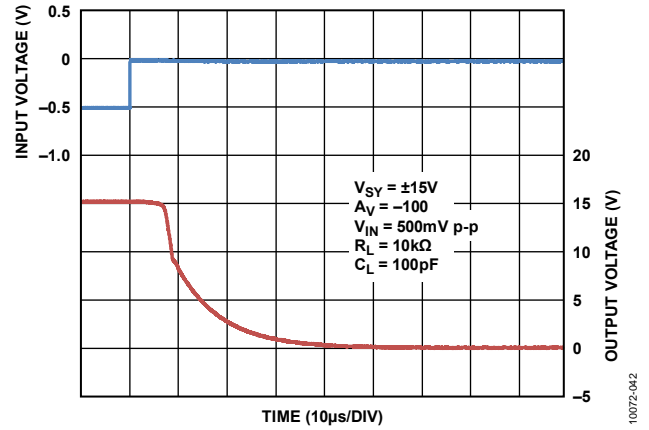


Figure 43. Positive Overload Recovery

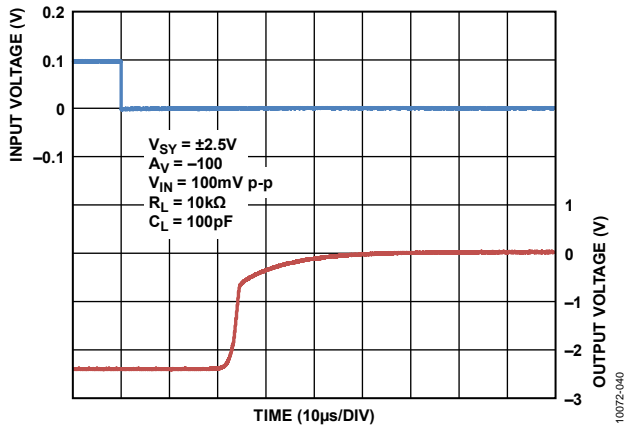


Figure 41. Negative Overload Recovery

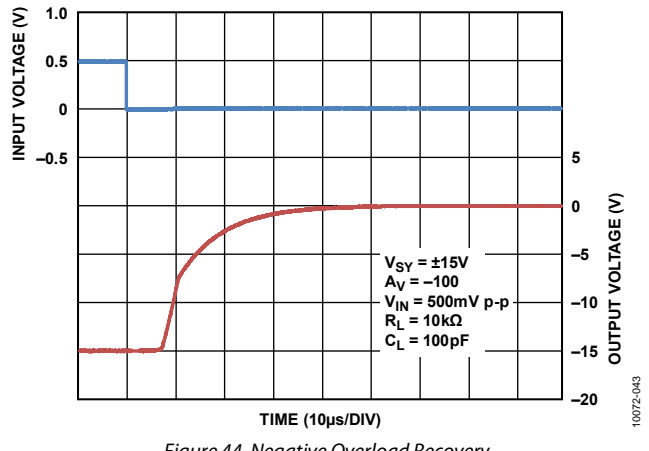


Figure 44. Negative Overload Recovery

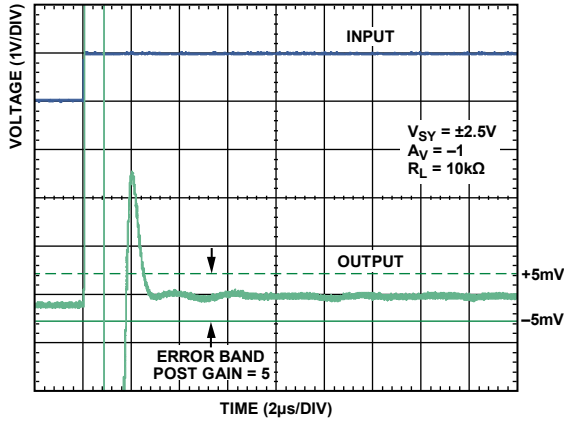


Figure 45. Positive Settling Time to 0.1%

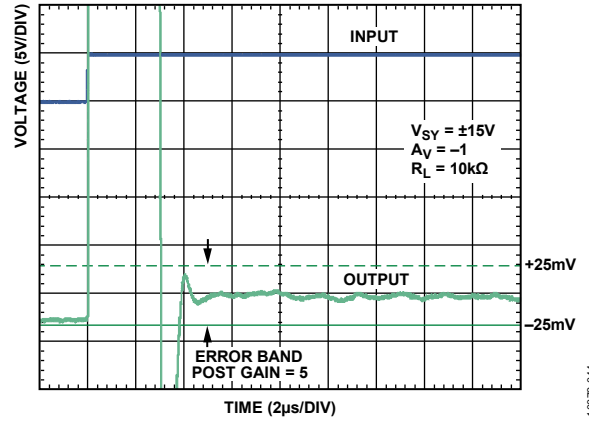


Figure 48. Positive Settling Time to 0.1%

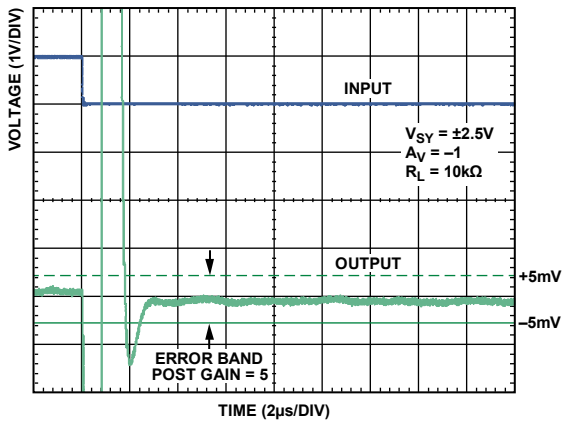


Figure 46. Negative Settling Time to 0.1%

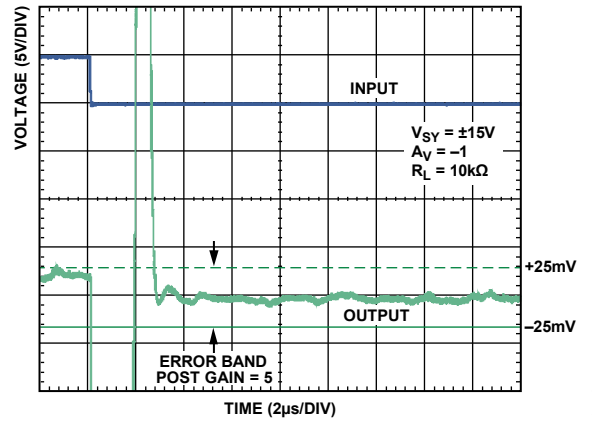


Figure 49. Negative Settling Time to 0.1%

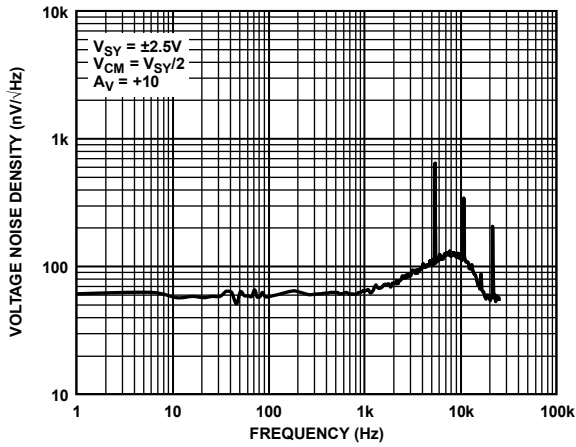


Figure 47. Voltage Noise Density vs. Frequency

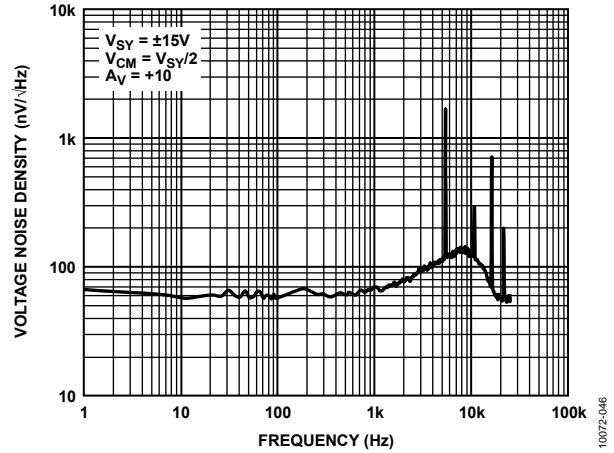


Figure 50. Voltage Noise Density vs. Frequency

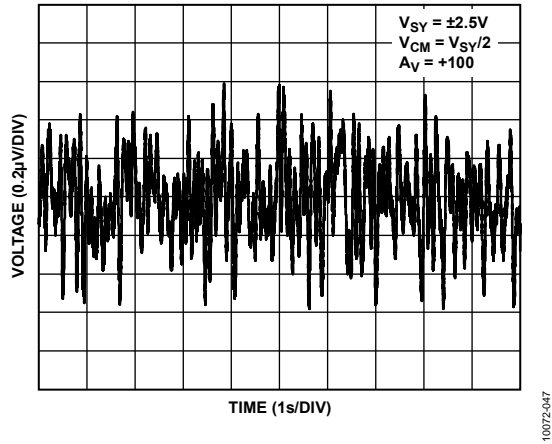


Figure 51. 0.1 Hz to 10 Hz Noise

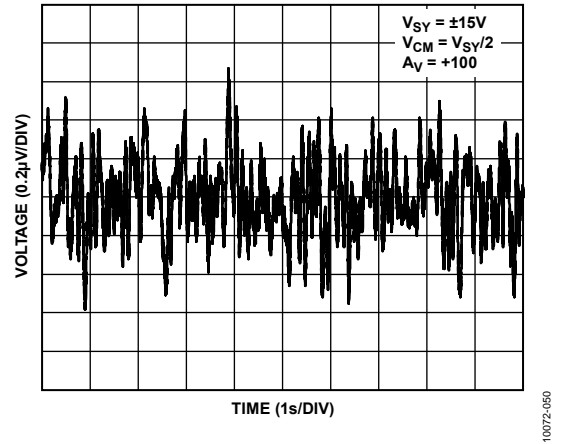


Figure 54. 0.1 Hz to 10 Hz Noise

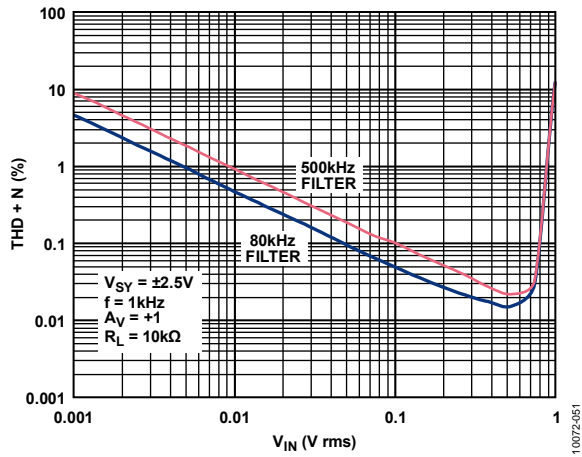


Figure 52. THD + N vs. Amplitude

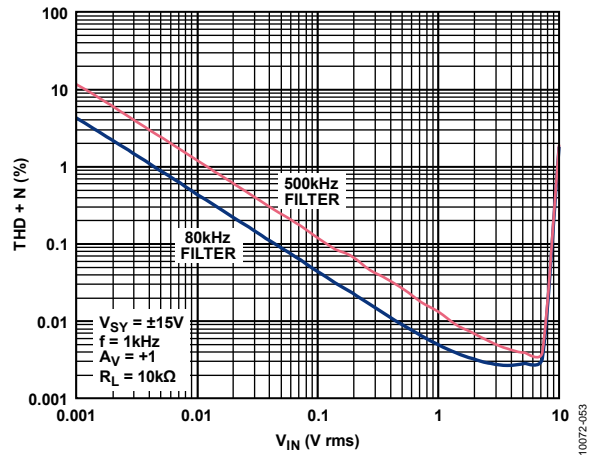


Figure 55. THD + N vs. Amplitude

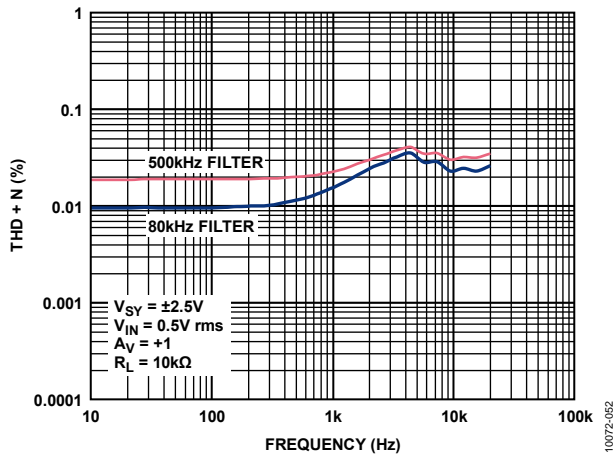


Figure 53. THD + N vs. Frequency

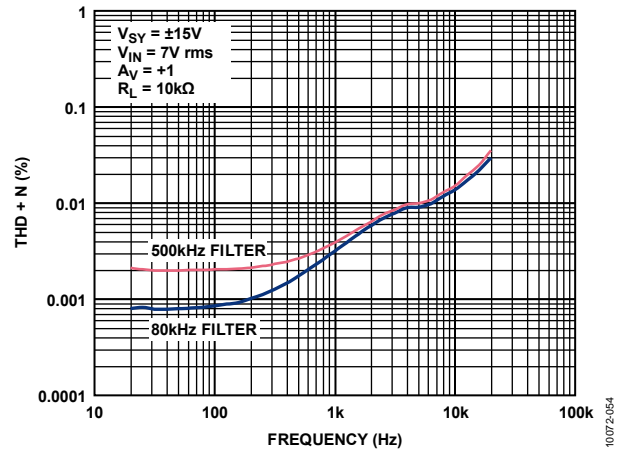


Figure 56. THD + N vs. Frequency

## APPLICATIONS INFORMATION

The [ADA4638-1](#), with its wide supply voltage range of 4.5 V to 30 V, is a precision, rail-to-rail output, zero-drift operational amplifier that features a patented combination of auto-zeroing and chopping technique. This unique topology allows the [ADA4638-1](#) to maintain its low offset voltage over a wide temperature range and over its operating lifetime. This amplifier offers ultralow input offset voltage of 4.5  $\mu\text{V}$  maximum and an input offset voltage drift of 80 nV/ $^{\circ}\text{C}$  maximum. Offset voltage errors due to common-mode voltage swings and power supply variations are also corrected by the auto-zeroing and chopping technique, resulting in a superb typical CMRR figure of 142 dB and a PSRR figure of 143 dB at a  $\pm 15$  V supply voltage. With ultrahigh dc accuracy and no 1/f noise component, the [ADA4638-1](#) is ideal for high gain amplification of low level signals in dc or low frequency applications without the risk of excessive output voltage errors.

## DIFFERENTIATION

Traditionally, zero-drift amplifiers are designed using either the auto-zeroing or chopping technique. Each technique has its benefits and drawbacks. Auto-zeroing usually results in low noise energy at the auto-zeroing frequency, at the expense of higher low frequency noise due to aliasing of wideband noise into the auto-zeroed frequency band. Chopping results in lower low frequency noise at the expense of larger noise energy at the chopping frequency. The [ADA4638-1](#) uses both auto-zeroing and chopping in a patented ping-pong arrangement to obtain lower low frequency noise together with lower energy at the chopping and auto-zeroing frequencies, maximizing the signal-to-noise ratio for the majority of applications. The relatively high chopping frequency of 16 kHz and auto-zeroing frequency of 8 kHz simplifies filter requirements for a wide, useful bandwidth.





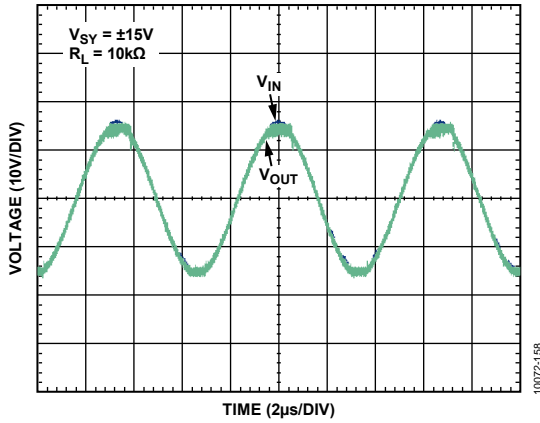


Figure 58. No Phase Reversal

**NOISE CONSIDERATIONS**

**1/f Noise**

1/f noise, also known as pink noise or flicker noise, is inherent in semiconductor devices and increases as frequency decreases. At low frequency, 1/f noise is a major noise contributor and causes a significant output voltage offset when amplified by the noise gain of the circuit. However, the ADA4638-1 eliminates the 1/f noise internally, thus making it an excellent choice for dc or low frequency high precision applications. The 0.1 Hz to 10 Hz voltage noise is only 1.2 µV p-p at ±15 V of supply voltage.

The low frequency 1/f noise appears as a slow varying offset to the ADA4638-1 and is greatly reduced by the combination of auto-zeroing and chopping technique. This allows the ADA4638-1 to have a much lower noise at dc and low frequency in comparison to standard low noise amplifiers that are susceptible to 1/f noise. Figure 47 and Figure 50 show the voltage noise density of the ADA4638-1 with no 1/f noise.

**COMPARATOR OPERATION**

Op amps are designed to operate in a closed-loop configuration with feedback from its output to its inverting input. Figure 59 shows the ADA4638-1 configured as a voltage follower with an input voltage, which is kept at midpoint of the power supplies. A1 and A2 indicate the placement of ammeters to measure supply currents. I<sub>SY+</sub> refers to the current flowing into the positive supply pin of the op amp, and I<sub>SY-</sub> refers to the current flowing out of the negative supply pin of the op amp. From Figure 60, as expected in normal operating condition, the current flowing into the op amp is equivalent to the current flowing out of the op amp, where I<sub>SY+</sub> = I<sub>SY-</sub>.

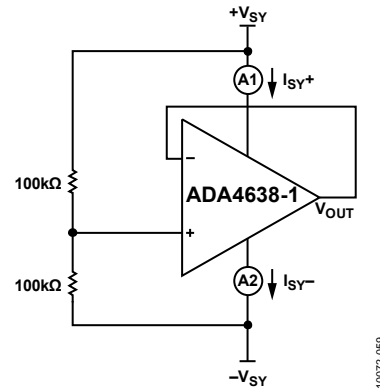


Figure 59. Voltage Follower

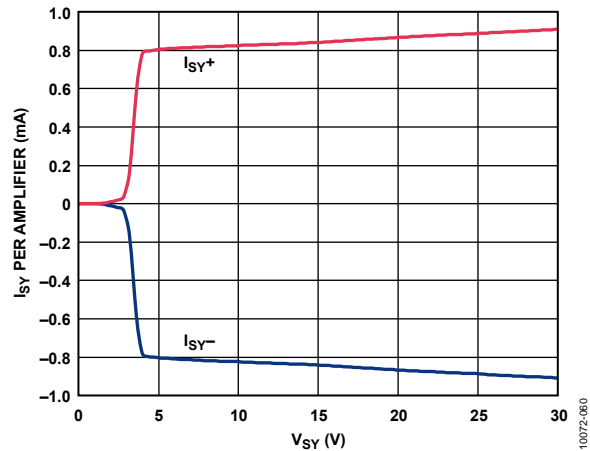


Figure 60. Supply Current vs. Supply Voltage (Voltage Follower)

In contrast to op amps, comparators are designed to work in an open-loop configuration and to drive logic circuits. Although op amps are different from comparators, occasionally an unused section of a dual op amp is used as a comparator to save board space and cost; however, this is not recommended.

Figure 61 and Figure 62 show the ADA4638-1 configured as a comparator, with resistors R<sub>IN1</sub> and R<sub>IN2</sub> in series with the input pins.

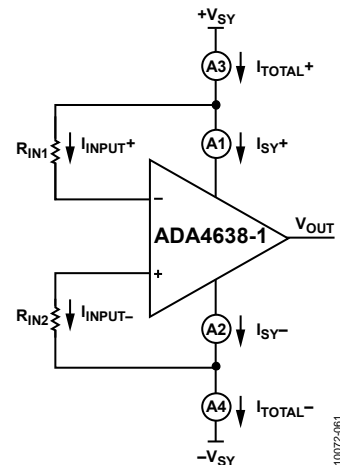


Figure 61. Comparator A

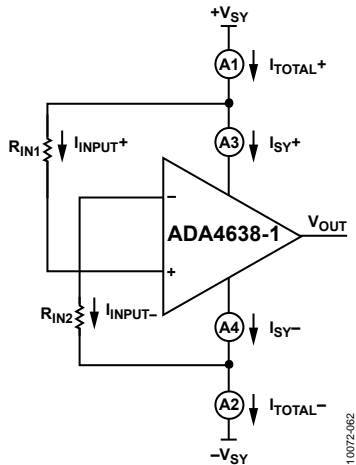


Figure 62. Comparator B

Figure 63 and Figure 64 show the total supply current of the system,  $I_{TOTAL}$ , and the actual currents,  $I_{SY}$ , that flow into and out of the supply pins of the ADA4638-1. With  $R_{IN1} = R_{IN2} = 100\text{ k}\Omega$  and supply voltage of 30 V, the total supply current of the system is 800  $\mu\text{A}$  to 900  $\mu\text{A}$ .

With smaller input series resistors, total supply current of the system increases much more. Figure 65 and Figure 66 show the supply currents with  $R_{IN1} = R_{IN2} = 0\ \Omega$ . The total current of the system increases to 10 mA.

$$I_{TOTAL} = I_{SY} + I_{INPUT}$$

Note that, at 30 V of supply voltage, 8 mA to 9 mA of current flows through the input pins. This is undesirable. The ADA4638-1 is not recommended to be used as a comparator. If absolutely necessary, place resistors in series with the inputs of the amplifier to limit input current to less than 10 mA.

For more details on op amps as comparators, refer to the AN-849 Application Note, *Using Op Amps as Comparators*.

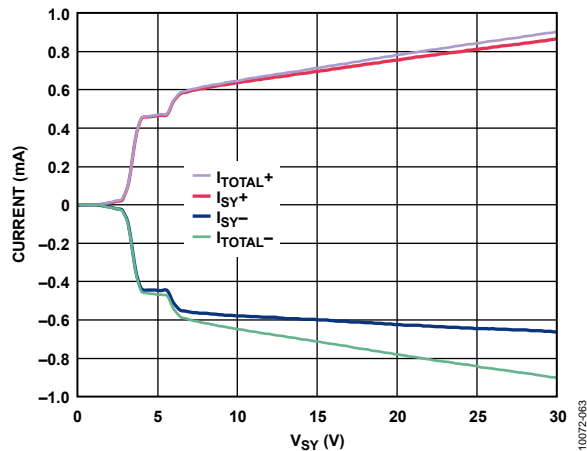


Figure 63. Supply Current vs. Supply Voltage (Comparator A,  $R_{IN1} = R_{IN2} = 100\text{ k}\Omega$ )

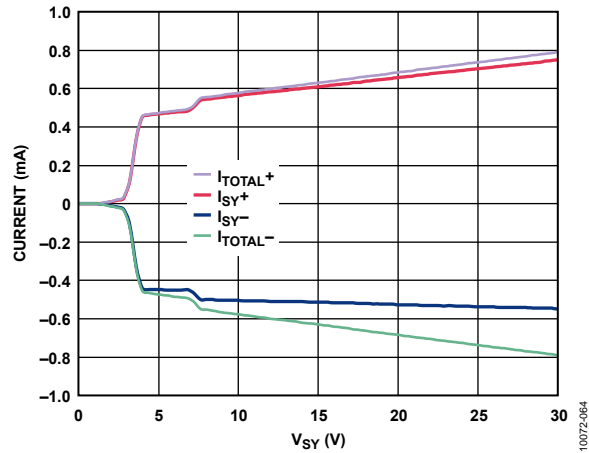


Figure 64. Supply Current vs. Supply Voltage (Comparator B,  $R_{IN1} = R_{IN2} = 100\text{ k}\Omega$ )

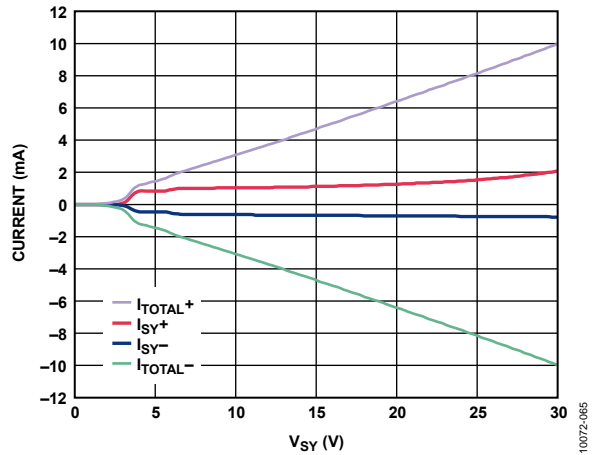


Figure 65. Supply Current vs. Supply Voltage (Comparator A,  $R_{IN1} = R_{IN2} = 0\text{ k}\Omega$ )

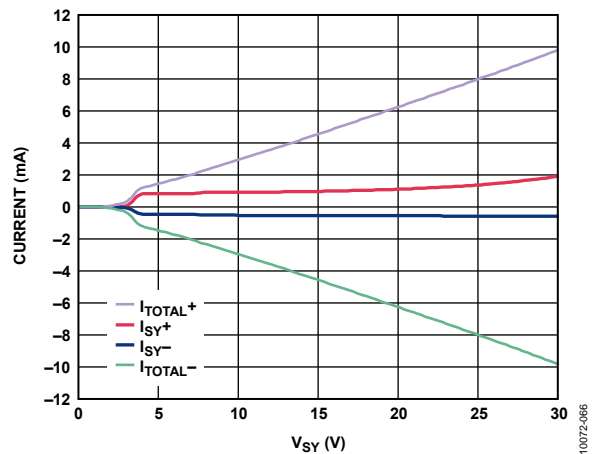
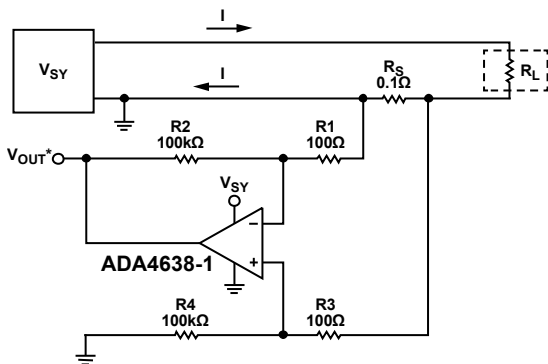


Figure 66. Supply Current vs. Supply Voltage (Comparator B,  $R_{IN1} = R_{IN2} = 0\text{ k}\Omega$ )

**PRECISION LOW-SIDE CURRENT SHUNT SENSOR**

Many applications require the sensing of signals near the positive or negative rails. Current shunt sensors are one such application and are mostly used for feedback control systems. They are also used in a variety of other applications, including power metering, battery fuel gauging and feedback controls in electrical power steering. In such application, it is desirable to use a shunt with very low resistance to minimize series voltage drop. This not only minimizes wasted power, but also allows the measurement of high currents while saving power. A typical shunt may be 100 mΩ. At a measured current of 1 A, the voltage produced from the shunt is 100 mV, and the amplifier error sources are not critical. However, at low measured current in the 1 mA range, the 100 μV generated across the shunt demands a very low offset voltage and drift amplifier to maintain absolute accuracy. The unique attributes of a zero-drift amplifier provides a solution. The ADA4638-1, with its input common-mode voltage that includes the lower supply rail, can be used for implementing low-side current shunt sensors.

Figure 67 shows a low-side current sensing circuit using the ADA4638-1. The ADA4638-1 is configured as a difference amplifier with a gain of 1000. Although the ADA4638-1 has high common-mode rejection, the CMR of the system is limited by the external resistors. Therefore, the key to high CMR for the system are resistors that are well matched from both the resistive ratio and relative drift, where  $R1/R2 = R3/R4$ . The resistors are important in determining the performance over manufacturing tolerances, time, and temperature.



\* $V_{OUT} = \text{AMPLIFIER GAIN} \times \text{VOLTAGE ACROSS } R_S$   
 $= 1000 \times R_S \times I$   
 $= 100 \times I$

Figure 67. Low-Side Current Sensing Circuit

**PRINTED CIRCUIT BOARD LAYOUT**

The ADA4638-1 is a high precision device with ultralow offset voltage and offset voltage drift. Therefore, care must be taken in the design of the printed circuit board (PCB) layout to achieve optimum performance of the ADA4638-1 at board level.

To avoid leakage currents, keep the surface of the board clean and free of moisture. Coating the board surface creates a barrier to moisture accumulation and reduces parasitic resistance on the board.

Properly bypassing the power supplies and keeping the supply traces short minimizes power supply disturbances caused by output current variation. Connect bypass capacitors as close as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. It is recommended that signal traces be kept at a distance of at least 5 mm from supply lines to minimize coupling.

A potential source of offset error is the Seebeck voltage on the circuit board. The Seebeck voltage occurs at the junction of two dissimilar metals and is a function of the temperature of the junction. The most common metallic junctions on a circuit board are solder-to-board trace and solder-to-component lead. Figure 68 shows a cross section of a surface-mount component soldered to a PCB. A variation in temperature across the board (where  $T_{A1} \neq T_{A2}$ ) causes a mismatch in the Seebeck voltages at the solder joints thereby resulting in thermal voltage errors that degrade the performance of the ultralow offset voltage of the ADA4638-1.

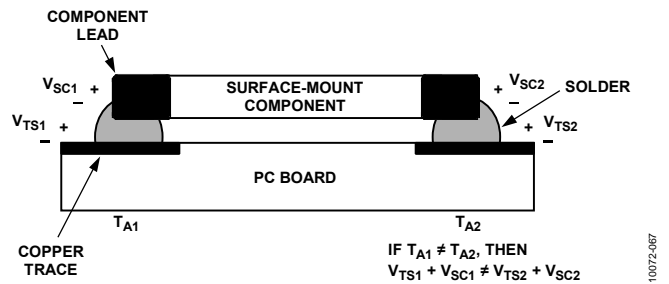
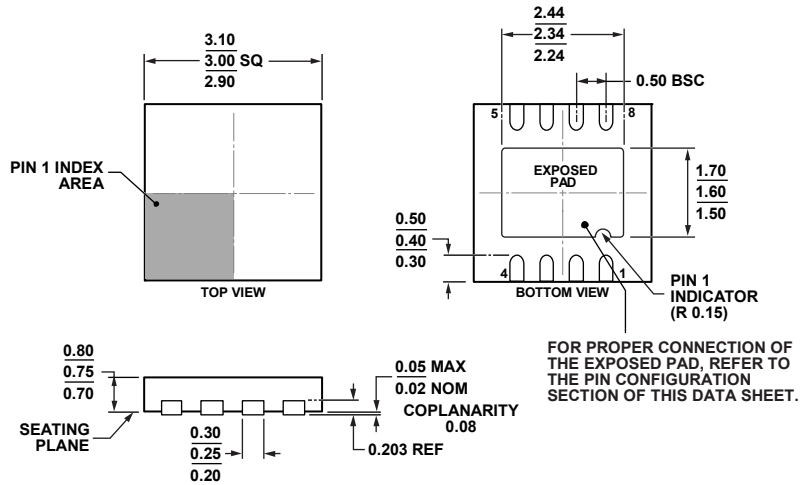


Figure 68. Mismatch in Seebeck Voltages Causes Seebeck Voltage Error

To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Where possible, the input signal paths should contain matching numbers and types of components to match the number and type of thermocouple junctions. For example, dummy components, such as zero value resistors, can be used to match the thermoelectric error source (real resistors in the opposite input path). Place matching components in close proximity and orient them in the same manner to ensure equal Seebeck voltages, thus cancelling thermal errors. Additionally, use leads that are of equal length to keep thermal conduction in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

It is highly recommended to use a ground plane. A ground plane helps distribute heat throughout the board, maintains a constant temperature across the board, and reduces EMI noise pickup.

OUTLINE DIMENSIONS

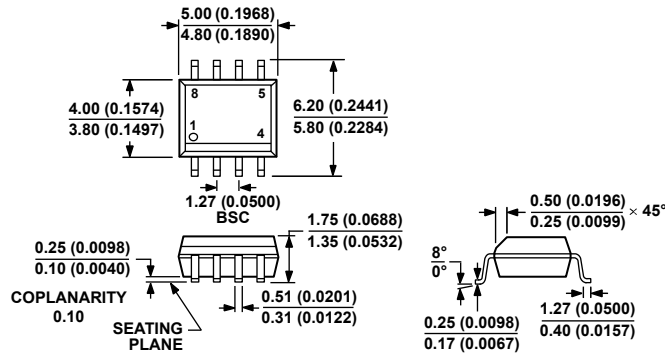


COMPLIANT TO JEDEC STANDARDS MO-229-WEED

Figure 69. 8-Lead Lead Frame Chip Scale Package [LFCSP\_WD]  
3 mm × 3 mm Body, Very Very Thin, Dual Lead  
(CP-8-11)

Dimensions shown in millimeters

01-24-2011-B



COMPLIANT TO JEDEC STANDARDS MS-012-AA

CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 70. 8-Lead Standard Small Outline Package [SOIC\_N]  
Narrow Body  
(R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

Model <sup>1</sup>	Temperature Range	Package Description	Package Option	Branding
ADA4638-1ACPZ-R7	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-11	A2W
ADA4638-1ACPZ-RL	-40°C to +125°C	8-Lead Lead Frame Chip Scale Package [LFCSP_WD]	CP-8-11	A2W
ADA4638-1ARZ	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4638-1ARZ-R7	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	
ADA4638-1ARZ-RL	-40°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8	

<sup>1</sup> Z = RoHS Compliant Part.

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