FEATURES

- Low offset voltage: 60 µV maximum at 25°C (8-lead and 14-lead SOIC)
- Low offset voltage drift: 1 µV/°C maximum (8-lead and 14-lead SOIC)
- Low input bias current: 1 nA maximum at 25°C
- Low voltage noise density: 8 nV/√Hz typical at 1 kHz
- Large signal voltage gain (Av0): 100 dB minimum over full supply voltage and operating temperature
- Input overvoltage protection to 32 V above and below the supply voltage rail
- Integrated EMI filter
  - 70 dB typical rejection at 1000 MHz
  - 90 dB typical rejection at 2400 MHz
- Rail-to-rail output swing
- Low supply current: 500 µA typical per amplifier
- Wide bandwidth
  - Gain bandwidth product (Av = 100): 3.5 MHz typical
  - Unity-gain crossover (Av = 1): 3.5 MHz typical
  - −3 dB bandwidth (Av = 1): 6 MHz typical
- Dual-supply operation
  - Specified at ±5 V to ±15 V, operates over ±2.5 V to ±18 V
- Unity-gain stable
- No phase reversal
- Long-term offset voltage drift (10,000 hours): 2 µV typical
- Temperature hysteresis: 2 µV typical

APPLICATIONS

- Wireless base station control circuits
- Optical network control circuits
- Instrumentation
- Sensors and controls
  - Thermocouples, RTDs, strain gages, shunt current measurements

GENERAL DESCRIPTION

The ADA4177-1 single-channel, ADA4177-2 dual-channel, and ADA4177-4 quad-channel amplifiers feature low offset voltage (2 µV typical) and drift (1 µV/°C maximum), low input bias current, low noise, and low current consumption (500 µA typical). Outputs are stable with capacitive loads of more than 1000 pF with no external compensation.

The inputs of the ADA4177-1/ADA4177-2/ADA4177-4 feature outstanding precision amplifier robustness, providing input protection against signal excursions 32 V beyond either supply, as well as 70 dB of rejection for electromagnetic interference (EMI) at 1000 MHz.

Applications for these amplifiers include sensor signal conditioning (such as thermocouples, resistor thermal detectors (RTDs), and strain gages), process control front-end amplifiers, and precision diode power measurement in optical and wireless transmission systems.

The ADA4177-1/ADA4177-2/ADA4177-4 operate over the −40°C to +125°C industrial temperature range. The ADA4177-1/ADA4177-2 are available in an 8-lead SOIC package and an 8-lead MSOP package. The ADA4177-4 is available in a 14-lead TSSOP and a 14-lead SOIC package.

![PIN CONNECTION DIAGRAM](image)

![Figure 1. ADA4177-2, for Additional Packages and Models, See the Pin Configurations and Function Descriptions Section](image)

![Figure 2. Overvoltage Current Limiting, Voltage Follower Configuration](image)

### Table 1. Evolution of Protected Input Op Amps by Generation

<table>
<thead>
<tr>
<th>Gen. 1, OVP (10 V)</th>
<th>Gen. 2, OVP (25 V)</th>
<th>Gen. 3, OVP (32 V)</th>
<th>Gen. 4 EMI Filters</th>
<th>Gen. 5, OVP (32 V) + EMI</th>
</tr>
</thead>
<tbody>
<tr>
<td>OP191</td>
<td>ADA4091-2</td>
<td>ADA4096-2</td>
<td>AD8657</td>
<td>ADA4177-1</td>
</tr>
<tr>
<td>OP291</td>
<td>ADA4091-4</td>
<td>ADA4096-4</td>
<td>AD8659</td>
<td>ADA4177-2</td>
</tr>
<tr>
<td>OP491</td>
<td>ADA4092-4</td>
<td>ADA4096-4</td>
<td>AD8546</td>
<td>ADA4177-4</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>AD8548</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ADA661-2</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>ADA666-2</td>
<td></td>
</tr>
</tbody>
</table>

1 Gen. means generation.
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SPECIFICATIONS

ELECTRICAL CHARACTERISTICS, ±5 V

V_{SV} = ±5.0 V, V_{CM} = 0 V, T_A = 25°C, unless otherwise noted.

### Table 2.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>V_{OS}</td>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>2</td>
<td>60</td>
<td>120</td>
<td>µV</td>
</tr>
<tr>
<td>8-Lead SOIC and 14-Lead SOIC</td>
<td></td>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>3</td>
<td>120</td>
<td>200</td>
<td>µV</td>
</tr>
<tr>
<td>8-Lead MSOP</td>
<td></td>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>3</td>
<td>150</td>
<td>300</td>
<td>µV</td>
</tr>
<tr>
<td>14-Lead TSSOP</td>
<td></td>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>3</td>
<td>150</td>
<td>300</td>
<td>µV</td>
</tr>
<tr>
<td>Offset Voltage Matching</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8-Lead SOIC</td>
<td></td>
<td></td>
<td>40</td>
<td>µV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8-Lead MSOP</td>
<td></td>
<td></td>
<td>110</td>
<td>µV</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Voltage Drift</td>
<td>ΔV_{OS}/ΔT</td>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>1</td>
<td>µV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8-Lead SOIC and 14-Lead SOIC</td>
<td></td>
<td></td>
<td>1.6</td>
<td>µV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>8-Lead MSOP and 14-Lead TSSOP</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>I_{B}</td>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>−1</td>
<td>−0.4</td>
<td>+1</td>
<td>nA</td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>I_{OS}</td>
<td>−0.75 +0.1 +0.75</td>
<td>−2</td>
<td>+2</td>
<td>+2</td>
<td>nA</td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>5 V &lt; V_{CM} &lt; 37 V</td>
<td>12</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>−37 V &lt; V_{CM} &lt; −5 V</td>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>10</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>CMRR</td>
<td></td>
<td>5 V &lt; V_{CM} &lt; 37 V</td>
<td>122</td>
<td>130</td>
<td>dB</td>
</tr>
<tr>
<td>−37 V &lt; V_{CM} &lt; −5 V</td>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>A_{V0}</td>
<td>R_L = 2 kΩ, V_{OUT} = −4.5 V to +4.5 V</td>
<td>108</td>
<td>110</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>R_L = 10 kΩ, V_{OUT} = −4.5 V to +4.5 V</td>
<td>115</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>C_{INDM}</td>
<td>Differential mode</td>
<td>1</td>
<td>pF</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C_{CM}</td>
<td>8</td>
<td>pF</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td>R_{DIFF}</td>
<td>Differential mode</td>
<td>4</td>
<td>MΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td>R_{CM}</td>
<td>100</td>
<td>GΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OUTPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>V_{OH}</td>
<td>I_{LOAD} = 1 mA</td>
<td>4.95</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>4.90</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>4.80</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>4.75</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Low</td>
<td>V_{OL}</td>
<td>I_{LOAD} = 1 mA</td>
<td>−4.95</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>−4.90</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>−4.80</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>−40°C &lt; T_A &lt; +125°C</td>
<td>−4.75</td>
<td>V</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Current</td>
<td>I_{OUT}</td>
<td>V_{DROPOUT} &lt; 1 V</td>
<td>25</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Short-Circuit Current</td>
<td>I_{SC}</td>
<td>T_A = 25°C</td>
<td>36</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sourcing</td>
<td>48</td>
<td>mA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sinking</td>
<td>Z_{OUT}</td>
<td>f = 1 kHz, A_{V0} = 1</td>
<td>0.11</td>
<td>Ω</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Conditions/Comments</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>-----------------------------------------</td>
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<td>------------------------------------------</td>
<td>-------</td>
<td>------</td>
<td>-------</td>
<td>------</td>
</tr>
<tr>
<td><strong>POWER SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>$V_S = \pm 2.5\ V \text{ to } \pm 18\ V$</td>
<td>125</td>
<td>145</td>
<td>120</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40^\circ\ C &lt; T_A &lt; +125^\circ\ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current per Amplifier</td>
<td>$I_{SY}$</td>
<td>$V_{OUT} = 0\ V$</td>
<td>500</td>
<td>560</td>
<td>600</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40^\circ\ C &lt; T_A &lt; +125^\circ\ C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>DYNAMIC PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>$R_L = 2\ k\Omega$</td>
<td>1.5</td>
<td></td>
<td></td>
<td>V/µs</td>
</tr>
<tr>
<td>Settling Time</td>
<td>$t_s$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>To 0.1%</td>
<td></td>
<td>$V_{IN} = 1\ V\ \text{step}, R_L = 2\ k\Omega, A_v = -1$</td>
<td>1.8</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>To 0.01%</td>
<td></td>
<td>$V_{IN} = 1\ V\ \text{step}, R_L = 2\ k\Omega, A_v = -1$</td>
<td>3.5</td>
<td></td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>GBP</td>
<td>$V_{IN} = 10\ mV\ \text{p-p}, R_L = 2\ k\Omega, A_v = 100$</td>
<td>3.5</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Unity-Gain Crossover</td>
<td>UGC</td>
<td>$V_{IN} = 10\ mV\ \text{p-p}, R_L = 2\ k\Omega, A_v = 1$</td>
<td>3.5</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>$-3\ dB$ Closed-Loop Bandwidth</td>
<td>$f_{-3\ dB}$</td>
<td>$V_{IN} = 10\ mV\ \text{p-p}, R_L = 2\ k\Omega, A_v = 1$</td>
<td>6</td>
<td></td>
<td></td>
<td>MHz</td>
</tr>
<tr>
<td>Total Harmonic Distortion Plus Noise</td>
<td>THD + N</td>
<td>$V_{IN} = 1\ V\ \text{rms}, R_L = 2\ k\Omega, A_v = +1, f = 1\ kHz$</td>
<td>0.003</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>EMI Rejection of $+INx$</td>
<td>EMIRR</td>
<td>$V_{IN} = 200\ mV\ \text{p-p}$</td>
<td>70</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>$f = 1000\ MHz$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$f = 2400\ MHz$</td>
<td></td>
<td></td>
<td>90</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td><strong>NOISE PERFORMANCE</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Noise</td>
<td>$e_{n\ \text{p-p}}$</td>
<td>$0.1\ Hz \text{ to } 10\ Hz$</td>
<td>175</td>
<td></td>
<td></td>
<td>nV\ \text{p-p}</td>
</tr>
<tr>
<td>Voltage Noise Density</td>
<td>$e_n$</td>
<td>$f = 10\ Hz$</td>
<td>10</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 1\ kHz$</td>
<td>8</td>
<td></td>
<td></td>
<td>nV/√Hz</td>
</tr>
<tr>
<td>Current Noise Density</td>
<td>$i_n$</td>
<td>$f = 1\ kHz$</td>
<td>0.2</td>
<td></td>
<td></td>
<td>pA/√Hz</td>
</tr>
</tbody>
</table>

1 All inputs are stressed to 32 V beyond supplies for 500 ms. See Figure 71 for the typical input bias current vs. the input voltage over the overvoltage protected input range.
### ELECTRICAL CHARACTERISTICS, ±15 V

$V_{SV} = ±15\, V$, $V_{CM} = 0\, V$, $T_A = 25°C$, unless otherwise noted.

#### Table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>INPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Offset Voltage</td>
<td>$V_{OS}$</td>
<td>8-Lead SOIC and 14-Lead SOIC $-40°C &lt; T_A &lt; +125°C$</td>
<td>2</td>
<td>60</td>
<td>120</td>
<td>µV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-Lead MSOP $-40°C &lt; T_A &lt; +125°C$</td>
<td>3</td>
<td>120</td>
<td>200</td>
<td>µV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>14-Lead TSSOP $-40°C &lt; T_A &lt; +125°C$</td>
<td>3</td>
<td>150</td>
<td>300</td>
<td>µV</td>
</tr>
<tr>
<td>Offset Voltage Matching</td>
<td></td>
<td>8-Lead SOIC</td>
<td>4</td>
<td></td>
<td>40</td>
<td>µV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-Lead MSOP</td>
<td></td>
<td></td>
<td>110</td>
<td>µV</td>
</tr>
<tr>
<td>Offset Voltage Drift</td>
<td>$\Delta V_{OS}/\Delta T$</td>
<td>8-Lead SOIC and 14-Lead SOIC $-40°C &lt; T_A &lt; +125°C$</td>
<td></td>
<td></td>
<td>1</td>
<td>µV/°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>8-Lead MSOP and 14-Lead TSSOP</td>
<td></td>
<td></td>
<td>1.6</td>
<td>µV/°C</td>
</tr>
<tr>
<td>Input Bias Current</td>
<td>$I_B$</td>
<td></td>
<td>$-1$</td>
<td>$-0.3$</td>
<td>$+1$</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Offset Current</td>
<td>$I_{OS}$</td>
<td></td>
<td>$-0.75$</td>
<td>$+0.1$</td>
<td>$+0.75$</td>
<td>nA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Voltage Range</td>
<td>$I_{VR}$</td>
<td></td>
<td>$-13.5$</td>
<td></td>
<td>$+13.5$</td>
<td>V</td>
</tr>
<tr>
<td>Overvoltage Current Limit$^1$</td>
<td>$I_{OVP}$</td>
<td>$15, V &lt; V_{CM} &lt; 47, V$</td>
<td>12</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-47, V &lt; V_{CM} &lt; -15, V$</td>
<td>10</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio</td>
<td>$CMRR$</td>
<td>$V_{CM} = -13.5, V$ to $+13.5, V$</td>
<td>128</td>
<td>130</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td></td>
<td></td>
<td>125</td>
<td>dB</td>
</tr>
<tr>
<td>Large Signal Voltage Gain</td>
<td>$A_{VO}$</td>
<td>$R_L = 2, k\Omega$, $V_{OUT} = -14.2, V$ to $+14.2, V$</td>
<td>110</td>
<td>114</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td></td>
<td></td>
<td>103</td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = 10, k\Omega$, $V_{OUT} = -14.5, V$ to $+14.5, V$</td>
<td>118</td>
<td>120</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td></td>
<td></td>
<td>110</td>
<td>dB</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>$C_{INDM}$</td>
<td>Differential mode</td>
<td>1</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$C_{INCM}$</td>
<td>Common mode</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Resistance</td>
<td>$R_{DIFF}$</td>
<td>Differential mode</td>
<td>4</td>
<td></td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_{CM}$</td>
<td>Common mode</td>
<td>130</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>OUTPUT CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Voltage</td>
<td>$V_{OH}$</td>
<td>$I_{LOAD} = 1, mA$</td>
<td>14.95</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td>14.90</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{LOAD} = 7, mA$</td>
<td>14.80</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td>14.75</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{LOAD} = 1, mA$</td>
<td></td>
<td></td>
<td>$-14.95$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td></td>
<td></td>
<td>$-14.90$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{LOAD} = 7, mA$</td>
<td></td>
<td></td>
<td>$-14.80$</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40°C &lt; T_A &lt; +125°C$</td>
<td></td>
<td></td>
<td>$-14.75$</td>
<td>V</td>
</tr>
<tr>
<td>Output Current</td>
<td>$I_{OUT}$</td>
<td>$V_{DROPOUT} &lt; 1, V$</td>
<td>25</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Short-Circuit Current</td>
<td>$I_{SC}$</td>
<td>$T_A = 25°C$</td>
<td>53</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Sourcing</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65</td>
<td>mA</td>
</tr>
<tr>
<td>Sinking</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>65</td>
<td>mA</td>
</tr>
<tr>
<td>Closed-Loop Output Impedance</td>
<td>$Z_{OUT}$</td>
<td>$f = 1, kHz$, $A_{V} = 1$</td>
<td>0.08</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>Parameter</td>
<td>Symbol</td>
<td>Test Conditions/Comments</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>-----------</td>
<td>--------</td>
<td>--------------------------</td>
<td>-----</td>
<td>-----</td>
<td>-----</td>
<td>------</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>PSRR</td>
<td>$V_S = \pm 2.5\ V \text{ to } \pm 18\ V$</td>
<td>125</td>
<td>145</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40^\circ C &lt; T_A &lt; +125^\circ C$</td>
<td>120</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Supply Current per Amplifier</td>
<td>$I_{SY}$</td>
<td>$V_{OUT} = 0\ V$</td>
<td>500</td>
<td>580</td>
<td>$\mu A$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$-40^\circ C &lt; T_A &lt; +125^\circ C$</td>
<td>620</td>
<td>$\mu A$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Dynamic Performance**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Slew Rate</td>
<td>SR</td>
<td>$R_L = 2\ k\Omega$</td>
<td>1.5</td>
<td>V/$\mu s$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Settling Time</td>
<td>$t_s$</td>
<td>$V_{IN} = 10\ V\ p-p, R_L = 2\ k\Omega, A_V = -1$</td>
<td>5.5</td>
<td>$\mu s$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 10\ V\ p-p, R_L = 2\ k\Omega, A_V = -1$</td>
<td>7.5</td>
<td>$\mu s$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Gain Bandwidth Product</td>
<td>GBP</td>
<td>$V_{IN} = 10\ mV\ p-p, R_L = 2\ k\Omega, A_V = 100$</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Unity-Gain Crossover</td>
<td>UGC</td>
<td>$V_{IN} = 10\ mV\ p-p, R_L = 2\ k\Omega, A_V = 1$</td>
<td>3.5</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$-3\ dB$ Closed-Loop Bandwidth</td>
<td>$f_{-3\ dB}$</td>
<td>$V_{IN} = 10\ mV\ p-p, R_L = 2\ k\Omega, A_V = 1$</td>
<td>6</td>
<td>MHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion Plus Noise</td>
<td>THD + N</td>
<td>$V_{IN} = 1\ V\ rms, A_V = +1, R_L = 2\ k\Omega, f = 1\ kHz$</td>
<td>0.002</td>
<td>%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>EMI Rejection of $+INx$</td>
<td>EMIRR</td>
<td>$V_{IN} = 200\ mV\ p-p$</td>
<td>70</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 1000\ MHz$</td>
<td>90</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 2400\ MHz$</td>
<td>dB</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Noise Performance**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Noise</td>
<td>$e_n, p-p$</td>
<td>0.1 Hz to 10 Hz</td>
<td>175</td>
<td>nV p-p</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Voltage Noise Density</td>
<td>$e_n$</td>
<td>$f = 10\ Hz$</td>
<td>10</td>
<td>nV/$\sqrt{Hz}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f = 1\ kHz$</td>
<td>8</td>
<td>nV/$\sqrt{Hz}$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Noise Density</td>
<td>$i_n$</td>
<td>$f = 1\ kHz$</td>
<td>0.2</td>
<td>pA/$\sqrt{Hz}$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Multiple Amplifiers Channel Separation**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$C_s$</td>
<td>$f = 1\ kHz$</td>
<td>127</td>
<td>dB</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 All inputs are stressed to 32 V beyond supplies for 500 ms. See Figure 74 for the typical input bias current vs. the input voltage over the overvoltage protected input range.
ABSOLUTE MAXIMUM RATINGS

Table 4.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage</td>
<td>36 V</td>
</tr>
<tr>
<td>Input Voltage</td>
<td>$V_{SY} \pm 32$ V</td>
</tr>
<tr>
<td>Differential Input Voltage</td>
<td>$\pm V_{SV}$</td>
</tr>
<tr>
<td>Output Short-Circuit Duration to GND</td>
<td>See the Maximum Power Dissipation section</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>$-65^\circ$ to $+150^\circ$</td>
</tr>
<tr>
<td>Operating Temperature Range</td>
<td>$-40^\circ$ to $+125^\circ$</td>
</tr>
<tr>
<td>Junction Temperature Range</td>
<td>$-65^\circ$ to $+150^\circ$</td>
</tr>
<tr>
<td>Lead Temperature, Soldering (10 sec)$^1$</td>
<td>300°C</td>
</tr>
<tr>
<td>Electrostatic Discharge (ESD)</td>
<td></td>
</tr>
<tr>
<td>Human Body Model (HBM)$^2$</td>
<td>4 kV</td>
</tr>
<tr>
<td>Field Induced Charged Device Model (FICDM)$^3$</td>
<td>1250 V</td>
</tr>
<tr>
<td>Machine Model (MM)</td>
<td>200 V</td>
</tr>
</tbody>
</table>

1 IPC/JEDEC J-STS-020D applicable standard.
2 ESDA/JEDEC JS-001-2011 applicable standard.
3 JESD22-C101 (ESD FICDM standard of JEDEC) applicable standard.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

MAXIMUM POWER DISSIPATION

The ADA4177-1/ADA4177-2/ADA4177-4 can drive a short-circuit output current of up to 65 mA. However, the usable output load current drive is limited by the maximum power dissipation allowed by the device package. The absolute maximum junction temperature is 150°C (see Table 4). The junction temperature can be estimated as follows:

$$T_J = P_D \times \theta_{JA} + T_A$$

where:

- $T_J$ is the die junction temperature.
- $P_D$ is the power dissipated in the package.
- $\theta_{JA}$ is the thermal resistance of the package.
- $T_A$ is the ambient temperature.

The power dissipated in the package ($P_D$) is the sum of the quiescent power dissipation and the power dissipated by the output stage transistor. It is calculated as follows:

$$P_D = (V_{SY} \times I_{SY}) + (V_{SY} - V_{OUT}) \times I_{LOAD}$$

where:

- $V_{SY}$ is the power supply rail.
- $I_{SY}$ is the quiescent current.
- $V_{OUT}$ is the output of the amplifier.
- $I_{LOAD}$ is the output load.

Do not exceed the 150°C maximum junction temperature for the device. Exceeding the junction temperature limit can cause degradation in the parametric performance or even destroy the device. Refer to [Technical Article MS-2251, Data Sheet Intricacies—Absolute Maximum Ratings and Thermal Resistances](#), for more information.

THERMAL RESISTANCE

Thermal resistance between junction and ambient ($\theta_{JA}$) is specified for the worst case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 5. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta_{JA}$</th>
<th>$\theta_{JC}$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-Lead MSOP</td>
<td>190</td>
<td>44</td>
<td>°C/W</td>
</tr>
<tr>
<td>8-Lead SOIC</td>
<td>158</td>
<td>43</td>
<td>°C/W</td>
</tr>
<tr>
<td>14-Lead TSSOP</td>
<td>240</td>
<td>43</td>
<td>°C/W</td>
</tr>
<tr>
<td>14-Lead SOIC</td>
<td>115</td>
<td>36</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
Table 6. ADA4177-1 Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 5, 8</td>
<td>NIC</td>
<td>Not Internally Connected.</td>
</tr>
<tr>
<td>2</td>
<td>−IN</td>
<td>Inverting Input Channel.</td>
</tr>
<tr>
<td>3</td>
<td>+IN</td>
<td>Noninverting Input Channel.</td>
</tr>
<tr>
<td>4</td>
<td>V−</td>
<td>Negative Supply Voltage.</td>
</tr>
<tr>
<td>6</td>
<td>OUT</td>
<td>Output Channel.</td>
</tr>
<tr>
<td>7</td>
<td>V+</td>
<td>Positive Supply Voltage.</td>
</tr>
</tbody>
</table>
Table 7. **ADA4177-2 Pin Function Descriptions**

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT A</td>
<td>Output Channel A.</td>
</tr>
<tr>
<td>2</td>
<td>−IN A</td>
<td>Inverting Input Channel A.</td>
</tr>
<tr>
<td>3</td>
<td>+IN A</td>
<td>Noninverting Input Channel A.</td>
</tr>
<tr>
<td>4</td>
<td>V−</td>
<td>Negative Supply Voltage.</td>
</tr>
<tr>
<td>5</td>
<td>+IN B</td>
<td>Noninverting Input Channel B.</td>
</tr>
<tr>
<td>6</td>
<td>−IN B</td>
<td>Inverting Input Channel B.</td>
</tr>
<tr>
<td>7</td>
<td>OUT B</td>
<td>Output Channel B.</td>
</tr>
<tr>
<td>8</td>
<td>V+</td>
<td>Positive Supply Voltage.</td>
</tr>
</tbody>
</table>
Table 8. ADA4177-4 Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>OUT A</td>
<td>Output Channel A.</td>
</tr>
<tr>
<td>2</td>
<td>−IN A</td>
<td>Inverting Input Channel A.</td>
</tr>
<tr>
<td>3</td>
<td>+IN A</td>
<td>Noninverting Input Channel A.</td>
</tr>
<tr>
<td>4</td>
<td>V+</td>
<td>Positive Supply Voltage.</td>
</tr>
<tr>
<td>5</td>
<td>+IN B</td>
<td>Noninverting Input Channel B.</td>
</tr>
<tr>
<td>6</td>
<td>−IN B</td>
<td>Inverting Input Channel B.</td>
</tr>
<tr>
<td>7</td>
<td>OUT B</td>
<td>Output Channel B.</td>
</tr>
<tr>
<td>8</td>
<td>OUT C</td>
<td>Output Channel C.</td>
</tr>
<tr>
<td>9</td>
<td>−IN C</td>
<td>Inverting Input Channel C.</td>
</tr>
<tr>
<td>10</td>
<td>+IN C</td>
<td>Noninverting Input Channel C.</td>
</tr>
<tr>
<td>11</td>
<td>V−</td>
<td>Negative Supply Voltage.</td>
</tr>
<tr>
<td>12</td>
<td>+IN D</td>
<td>Noninverting Input Channel D.</td>
</tr>
<tr>
<td>13</td>
<td>−IN D</td>
<td>Inverting Input Channel D.</td>
</tr>
<tr>
<td>14</td>
<td>OUT D</td>
<td>Output Channel D.</td>
</tr>
</tbody>
</table>
TYPICAL PERFORMANCE CHARACTERISTICS

Ambient temperature (T_a) = 25°C unless otherwise noted.

Figure 9. Input Offset Voltage (V_os) Distribution, V_S = ±5 V, 8-Lead SOIC

Figure 10. Input Offset Voltage (V_os) Distribution, V_S = ±5 V, 8-Lead MSOP

Figure 11. Input Offset Voltage (V_os) Distribution, V_S = ±5 V, 14-Lead SOIC

Figure 12. Input Offset Voltage (V_os) Distribution, V_S = ±15 V, 8-Lead SOIC

Figure 13. Input Offset Voltage (V_os) Distribution, V_S = ±15 V, 8-Lead MSOP

Figure 14. Input Offset Voltage (V_os) Distribution, V_S = ±15 V, 14-Lead SOIC
Figure 15. Input Offset Voltage ($V_{OS}$) Distribution, $V_{SY} = \pm 5\, V$, 14-Lead TSSOP

Figure 16. Input Offset Voltage ($V_{OS}$) vs. Temperature, $V_{SY} = \pm 5\, V$, 8-Lead SOIC and 14-Lead SOIC

Figure 17. Input Offset Voltage ($V_{OS}$) vs. Temperature, $V_{SY} = \pm 5\, V$, 8-Lead MSOP and 14-Lead TSSOP

Figure 18. Input Offset Voltage ($V_{OS}$) Distribution, $V_{SY} = \pm 15\, V$, 14-Lead TSSOP

Figure 19. Input Offset Voltage ($V_{OS}$) vs. Temperature, $V_{SY} = \pm 15\, V$, 8-Lead SOIC and 14-Lead SOIC

Figure 20. Input Offset Voltage ($V_{OS}$) vs. Temperature, $V_{SY} = \pm 15\, V$, 8-Lead MSOP and 14-Lead TSSOP
Figure 21. Temperature Coefficient of Offset Voltage (TCVOS), $V_{SY} = \pm 5\, \text{V}$, 8-Lead SOIC and 14-Lead SOIC

Figure 22. Temperature Coefficient of Offset Voltage (TCVOS), $V_{SY} = \pm 5\, \text{V}$, 8-Lead MSOP and 14-Lead TSSOP

Figure 23. Input Offset Voltage ($V_{OS}$) vs. Common-Mode Voltage ($V_{CM}$), $V_{SY} = \pm 5\, \text{V}$

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THEORY OF OPERATION
The ADA4177-1/ADA4177-2/ADA4177-4 are precision, bipolar op amps that integrate both input overvoltage protection (OVP) and input EMI filtering while maintaining a low 2 nA maximum bias current and a rail-to-rail output operation. Figure 84 shows a conceptual schematic of the main amplifier that uses super beta, bipolar input transistors and bias current cancellation to minimize the input bias current. The inputs are cascoded to protect the super beta input devices from damage during overvoltage conditions. The cascoded inputs feed into an active load that makes up the primary gain stage. A buffered transconductance (g_m) stage converts a differential voltage to a differential current to drive the output stage. The rail-to-rail output can swing to 50 mV maximum (for example, the guaranteed room temperature limit for V_off is 14.95 V when the positive supply is 15 V) with a 1 mA load at 25°C.

Figure 84. Conceptual Schematic
APPLICATIONS INFORMATION
ACTIVE OVERVOLTAGE PROTECTION

The ADA4177-1/ADA4177-2/ADA4177-4 use active overvoltage protection to protect the devices from damage when the inputs are driven to a voltage up to 32 V above the positive supply voltage or 32 V below the negative supply voltage. The ADA4177-1/ADA4177-2/ADA4177-4 not only protect the input from damage, but they also reduce the input noise.

Common Protection Methods
Add an External Series Input Resistor

When an op amp does not have input overvoltage protection, moving the input voltage above or below the supply voltage can cause excessive input current, which can damage the op amp. To avoid this, add a series resistor at the input. To protect the op amp from a 30 V transient beyond either rail, limit the input current to 5 mA, and add a 6 kΩ series resistor to the input. However, a trade-off of adding the series resister is its added thermal noise. The 6 kΩ series resistor exhibits 10 nV/√Hz of thermal noise, which adds quadrature thermal noise from the resistor with the op amp noise.

\[
N_{\text{TOTAL}} = \sqrt{N_{\text{OP AMP}}^2 + N_{\text{RESISTOR}}^2}
\]

where:
- \(N_{\text{TOTAL}}\) is the total noise.
- \(N_{\text{OP AMP}}\) is the op amp noise.
- \(N_{\text{RESISTOR}}\) is the thermal noise generated by the resistor.

When the additional thermal noise from the series resistor is added to the thermal noise (8 nV/√Hz) of the ADA4177-1/ADA4177-2/ADA4177-4, the 6 kΩ series resistor brings the total thermal noise to 12 nV/√Hz, which is a 70% increase in thermal noise. Figure 85 shows how noise from the additional source resistance adds to the total noise at the amplifier input; the higher the source resistance, the higher the total noise. Because the ADA4177-1/ADA4177-2/ADA4177-4 have integrated input protection for overvoltage conditions, the noise trade-off is avoided.

Add External Clamping Diodes

Precision op amps have a low VOS and a high common-mode rejection ratio (CMRR). Both of these characteristics simplify system calibration and minimize dynamic error. To maintain these specifications in the presence of ESD events, bipolar op amps often have internal clamp diodes and small limiting resistors in series with their inputs; however, these do not address fault conditions where the inputs exceed the rails. In these cases, the system designer commonly adds clamping diodes (D1 and D2) along with a series resistor (\(R_{\text{OVP}}\)), shown in Figure 86.

If the signal source at \(V_{\text{IN}}\) is driven to one diode voltage beyond the op amp supplies, the fault current is limited by \(R_{\text{OVP}}\). Schottky diodes have a low forward knee voltage of 200 mV less than a typical small signal diode. Therefore, all overvoltage currents are shunted through the external diodes (D1 and D2). The reverse leakage current for a typical Schottky diode is extremely variable with the reverse voltage level. Therefore, as the noninverting input of the op amp swings, the D1 and D2 leakage currents do not match, and the differences pass through \(R_{\text{OVP}}\), creating a voltage drop. The voltage drop on \(R_{\text{OVP}}\) appears as a variation in \(V_{\text{OS}}\), which can drastically reduce the CMRR performance. Because the ADA4177-1/ADA4177-2/ADA4177-4 have integrated input protection during overvoltage conditions, the degradation in performance is avoided.

Input Protection Circuit

The ADA4177-1/ADA4177-2/ADA4177-4 inputs provide overvoltage protection without the trade-offs encountered in the common design methods. The conceptual schematic of the input is shown in Figure 87.
J1A, J1B, J2A, and J2B are depletion mode junction field effect transistors (JFETs) that replace the series resistance in the conventional protection scheme. Under normal operation, the input bias current of the ADA4177-1/ADA4177-2/ADA4177-4 flows through the J1A and J2A transistors without pinching off the channel. To achieve excellent noise performance, J1A and J2A must have a low on resistance ($R_{\text{DS(ON)}}$) of approximately 300 Ω.

When either input exceeds the rail by more than a diode, large currents flow through either J1A or J2A, which causes the channels to pinch off and effectively raises their resistance. Figure 88 shows the positive overvoltage and negative overvoltage characteristics as the FET channel pinches.

**Figure 88.** Input Bias Current During Positive and Negative Overvoltage, $V_{SV} = \pm 15\,\text{V}$, Voltage Follower Configuration

Figure 89 shows how the JFET effective resistance increases exponentially as shown by the measurements at 2 V, 20 V, and 40 V overvoltage. As the overvoltage increases from 2 V to 40 V, the resistance increases from 300 Ω to 3.5 kΩ (a factor of 11).

**Figure 89.** Overvoltage vs. Input Voltage ($V_{IN}$), Voltage Follower Configuration

**LIMITING OVERVOLTAGE CURRENT OUT OF THE POSITIVE SUPPLY PIN**

Because the positive power supply of the system can be incapable of sinking the large overvoltage current of 8 mA (see Figure 88), care was taken to divide down this current into the positive rail during an overvoltage event. As shown in Figure 90, Q1L is a lateral PNP transistor that serves two purposes. First, the emitter base acts as a clamping diode to route the overvoltage current away from the $V+$ pin and to the $V-$ pin. Second, it divides down this current via the beta of Q1L. At an emitter current of 8 mA, the beta of Q1L is approximately 8, which reduces the current injected into the positive supply by a factor of 8.

**Figure 90.** Overvoltage Protection Circuitry

Figure 91 shows the positive and negative supply currents when the input voltage exceeds the supply voltages (and overvoltage condition). The current at the $V+$ terminal does not reverse direction during an overvoltage event because the current is directed to $V-$ via the collector of Q1L.

**Figure 91.** Supply Current vs. Input Differential, Circuit Configured at Unity Gain with $V+=+15\,\text{V}$ and $V-=−15\,\text{V}$

If negative overvoltage transients are expected, ensure that the negative voltage source driving $V-$ can handle sourcing current without forcing current into the device and causing the supply voltage to change.
EMI PROTECTION
The ADA4177-1/ADA4177-2/ADA4177-4 inputs are also protected from high frequency EMI. In an op amp with no EMI protection, signals not within the bandwidth of the op amp couple into sensitive amplifier inputs and become rectified as they travel through the amplifier, eventually appearing as ac feedthrough on top of a dc offset. When an input filter is not provided, these offsets can be quite large. These offsets are referred to as the electromagnetic interference rejection ratio (EMIRR). The amplifier EMIRR is defined as

\[ EMIRR = 20 \times \log \left( \frac{100 \text{ mV}}{\Delta V_{OS}} \right) \]

where:
100 mV is generally the peak-to-peak input used for the test.
\( \Delta V_{OS} \) is the change in the op amp offset as a result of the input signal.

Figure 92 shows the input EMI protection of the ADA4177-1/ADA4177-2/ADA4177-4.

SELF HEATING
During an overvoltage condition, the ADA4177-1/ADA4177-2/ADA4177-4 dissipate heat according to the thermal resistance (\( \theta_{JA} \)) of the package it is in, which, in turn, heats up the die. Ensure that the specified operating junction temperature does not exceed 150°C for device protection. Extended overtemperature exposure can cause some operating specifications to shift outside of their guaranteed limits.

As shown in Figure 88, the ADA4177-1/ADA4177-2/ADA4177-4 inputs sink by approximately 8 mA at 15 V overvoltage. In that condition, the ADA4177-1/ADA4177-2/ADA4177-4 dissipate 120 mW of power. If the package has a \( \theta_{JA} \) of 100°C/W, the junction temperature rises by approximately 12°C over the ambient temperature of the package and junction. In such a case, derate the ambient operating temperature by 12°C (125°C minus 12°C) for an absolute maximum operating temperature of 113°C.

When the junction temperature exceeds the absolute maximum junction temperature of 150°C, add an additional series resistance to the inputs to further decrease the overvoltage current. Figure 93 shows the maximum operating temperature vs. the continuous overvoltage at \( \theta_{JA} = 150^\circ\text{C/W} \).

Figure 93. Maximum Operating Temperature vs. Continuous Overvoltage for One Input and Two Inputs (\( \theta_{JA} = 150^\circ\text{C/W} \))

USING THE ADA4177-1/ADA4177-2/ADA4177-4 AS A COMPARATOR

The ADA4177-1/ADA4177-2/ADA4177-4 can be used as a comparator as long as relatively small input impedance can be tolerated. That is, the input differential pair is diode clamped but the overvoltage protection circuitry limits the differential. Figure 94 shows the input current vs. the input differential voltage with ±15 V supplies.

Figure 94. Input Current vs. Input Differential with ±15 V Supplies
Figure 95 shows the input and output of a comparator circuit referenced to ground using the ADA4177-1/ADA4177-2/ADA4177-4. The supply voltages are ±5 V. The −INx input is grounded and a positive input is stepped to ±1 V. Both the positive and negative recovery is approximately 4 µs.

![Figure 95. ADA4177-1/ADA4177-2/ADA4177-4 Used as a Comparator with ±5 V Supplies and a ±1 V Input Step, Voltage Follower Configuration](image)

**OUTPUT PHASE REVERSAL**

Phase reversal is defined as a change in polarity in the amplifier transfer function. Many op amps exhibit phase reversal when the voltage applied to the input is greater than the maximum common-mode voltage. In some instances, this phase reversal can cause permanent damage to the amplifier. In feedback loops, it can result in system lockups or equipment damage. The ADA4177-1/ADA4177-2/ADA4177-4 are immune to phase reversal problems even at input voltages beyond the power supply settings.

![Figure 96. Output Showing No Phase Reversal in Overvoltage Condition](image)

**PROPER PRINTED CIRCUIT BOARD (PCB) LAYOUT**

The ADA4177-1/ADA4177-2/ADA4177-4 are high precision devices. To ensure optimum performance at the PCB level, take care in the design of the board layout.

To avoid leakage currents, maintain a clean and moisture free board surface. Coating the surface creates a barrier to moisture accumulation and reduces parasitic resistance on the board.

Keeping supply traces short and properly bypassing the power supplies minimizes the power supply disturbances caused by the output current variation, such as when driving an ac signal into a heavy load. Connect bypass capacitors as closely as possible to the device supply pins. Stray capacitances are a concern at the outputs and the inputs of the amplifier. Keep the signal traces at least 5 mm from supply lines to minimize coupling.

A variation in temperature across the PCB can cause a mismatch in the Seebeck voltages at solder joints and other points where dissimilar metals are in contact, resulting in thermal voltage errors. To minimize these thermocouple effects, orient resistors so that heat sources warm both ends equally. Ensure, where possible, that input signal paths contain matching numbers and types of components, to match the number and type of thermocouple junctions. For example, dummy components such as zero value resistors can be used to match real resistors in the opposite input path. Place matching components in close proximity to each other, and orient them in the same manner. Ensure that leads are of equal length so that thermal conduction is in equilibrium. Keep heat sources on the PCB as far away from amplifier input circuitry as is practical.

The use of a ground plane is highly recommended. A ground plane reduces EMI noise and maintains a constant temperature across the circuit board.

**LONG-TERM DRIFT**

The stability of a precision signal path over its lifetime or between calibration procedures is dependent on the long-term stability of the analog components in the path, such as op amps, references, and data converters. To help system designers predict the long-term drift of circuits that use the ADA4177-1/ADA4177-2/ADA4177-4, Analog Devices measured the offset voltage of multiple units for 10,000 hours (more than 13 months) using a high precision measurement system, including an ultrastable oil bath. To replicate real-world system performance, the devices under test (DUTs) were soldered onto an FR4 PCB using a standard reflow profile (as defined in the JEDEC J-STD-020D standard), as opposed to testing them in sockets. This manner of testing is important because expansion and contraction of the PCB can apply stress to the integrated circuit (IC) package and contribute to shifts in the offset voltage.
The ADA4177-1/ADA4177-2/ADA4177-4 have extremely low long-term drift, as shown in Figure 97. The red, blue, and green traces show sample units. Note that the ADA4177-1/ADA4177-2/ADA4177-4 have a mean drift over 10,000 hours of less than 2 µV, or 2% of their maximum specified offset voltage of 60 µV at room temperature.

In the three full cycles, the offset hysteresis is typically only 2 µV, or less than 2% of its 120 µV maximum offset voltage over the full operating temperature range. The histogram in Figure 99 shows that the hysteresis is larger when the device is cycled through only a half cycle, from room temperature to hot 125°C and back to room temperature.

### TEMPERATURE HYSTERESIS

In addition to stability over time as described in the Long-Term Drift section, it is useful to know the temperature hysteresis, that is, the stability vs. cycling of temperature. Hysteresis is an important parameter because it tells the system designer how closely the signal returns to its starting amplitude after the ambient temperature changes and subsequent return to room temperature. Figure 98 shows the change in input offset voltage as the temperature cycles three times from room temperature to +125°C to −40°C and back to room temperature. The dotted line is an initial preconditioning cycle to eliminate the original temperature induced offset shift from exposure to production solder reflow temperatures.

The histogram in Figure 99 shows the temperature hysteresis of the offset voltage over three full cycles and over three half cycles.
OUTLINE DIMENSIONS

**Figure 100. 8-Lead Mini Small Outline Package (MSOP) (RM-8)**

Dimensions shown in millimeters

**Figure 101. 8-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-8)**

Dimensions shown in millimeters and (inches)
Figure 102. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)
Dimensions shown in millimeters

Figure 103. 14-Lead Standard Small Outline Package [SOIC_N] Narrow Body (R-14)
Dimensions shown in millimeters and (inches)
## ORDERING GUIDE

<table>
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</tr>
</thead>
<tbody>
<tr>
<td>ADA4177-1ARMZ</td>
<td>−40°C to +125°C</td>
<td>8-Lead Mini Small Outline Package [MSOP]</td>
<td>RM-8</td>
<td>A3E</td>
</tr>
<tr>
<td>ADA4177-1ARMZ-R7</td>
<td>−40°C to +125°C</td>
<td>8-Lead Mini Small Outline Package [MSOP]</td>
<td>RM-8</td>
<td>A3E</td>
</tr>
<tr>
<td>ADA4177-1ARZ</td>
<td>−40°C to +125°C</td>
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<td>R-8</td>
<td>A3E</td>
</tr>
<tr>
<td>ADA4177-1ARZ-R7</td>
<td>−40°C to +125°C</td>
<td>8-Lead Standard Small Outline Package [SOIC_N]</td>
<td>R-8</td>
<td>A3E</td>
</tr>
<tr>
<td>ADA4177-1ARZ-RL</td>
<td>−40°C to +125°C</td>
<td>8-Lead Standard Small Outline Package [SOIC_N]</td>
<td>R-8</td>
<td>A3E</td>
</tr>
<tr>
<td>ADA4177-2ARMZ</td>
<td>−40°C to +125°C</td>
<td>8-Lead Mini Small Outline Package [MSOP]</td>
<td>RM-8</td>
<td>A36</td>
</tr>
<tr>
<td>ADA4177-2ARMZ-R7</td>
<td>−40°C to +125°C</td>
<td>8-Lead Mini Small Outline Package [MSOP]</td>
<td>RM-8</td>
<td>A36</td>
</tr>
<tr>
<td>ADA4177-2ARZ</td>
<td>−40°C to +125°C</td>
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<td>R-8</td>
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</tr>
<tr>
<td>ADA4177-2ARZ-R7</td>
<td>−40°C to +125°C</td>
<td>8-Lead Standard Small Outline Package [SOIC_N]</td>
<td>R-8</td>
<td>A36</td>
</tr>
<tr>
<td>ADA4177-4ARUZ</td>
<td>−40°C to +125°C</td>
<td>14-Lead Thin Shrink Small Outline Package [TSSOP]</td>
<td>RU-14</td>
<td></td>
</tr>
<tr>
<td>ADA4177-4ARUZ-R7</td>
<td>−40°C to +125°C</td>
<td>14-Lead Thin Shrink Small Outline Package [TSSOP]</td>
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<td></td>
</tr>
<tr>
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<td></td>
</tr>
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<td>−40°C to +125°C</td>
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<td></td>
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<td>−40°C to +125°C</td>
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<td></td>
</tr>
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<td>ADA4177-4ARZ-RL</td>
<td>−40°C to +125°C</td>
<td>14-Lead Standard Small Outline Package [SOIC_N]</td>
<td>R-14</td>
<td></td>
</tr>
</tbody>
</table>

1 Z = RoHS Compliant Part.