internally by the serial port controller by decrementing from the specified address. For LSB-first format, the specified address is a beginning address or the least significant address in the current cycle. Remaining register addresses for multiple byte data transfers are generated internally by the serial port controller by incrementing from the specified address.

MSB/LSB TRANSFERS

The serial port can support both MSB-first and LSB-first data formats. This functionality is controlled by Register 0x00, Bit 6. The default is Logic 0, which is MSB-first format.

When using MSB-first format (LSBFIRST = 0), the instruction and data bit must be written from MSB to LSB. Multibyte data transfers in MSB-first format start with an instruction byte that includes the register address of the most significant data byte. Subsequent data bytes are loaded into sequentially lower address locations. In MSB-first mode, the serial port internal address generator decrements for each byte of the multibyte data transfer.

When using LSB-first format (LSBFIRST = 1), the instruction and data bit must be written from LSB to MSB. Multibyte data transfers in LSB-first format start with an instruction byte that includes the register address of the least significant data byte. Subsequent data bytes are loaded into sequentially higher address locations. In LSB-first mode, the serial port internal address generator increments for each byte of the multibyte data transfer.

Use of a single-byte transfer when changing the serial port data format is recommended to prevent unexpected device behavior.

SERIAL INTERFACE PORT PIN DESCRIPTIONS

Chip Select Bar (CSB)

Active low input starts and gates a communication cycle. It allows more than one device to be used on the same serial communication lines. CSB must stay low during the entire communication cycle. Incomplete data transfers are aborted anytime the CSB pin goes high. SDO and SDIO pins go to a high impedance state when this input is high.

Serial Clock (SCLK)

The serial clock pin is used to synchronize data to and from the device and to run the internal state machines. The maximum frequency of SCLK is 40 MHz. All data input is registered on the rising edge of SCLK. All data is driven out on the falling edge of SCLK.

Serial Data I/O (SDIO)

Data is always written into the device on this pin. However, SDIO can also function as a bidirectional data output line. The configuration of this pin is controlled by Register 0x00, Bit 7. The default is Logic 0, which configures the SDIO pin as unidirectional.

Serial Data Out (SDO)

Data is read from this pin for protocols that use separate lines for transmitting and receiving data. The configuration of this pin is controlled by Register 0x00, Bit 7. If this bit is set to a Logic 1, the SDO pin does not output data and is set to a high impedance state.

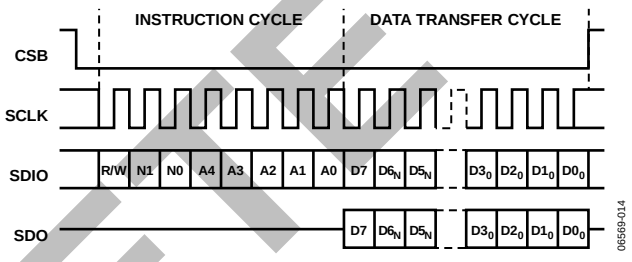

Figure 23. Serial Register Interface—MSB First

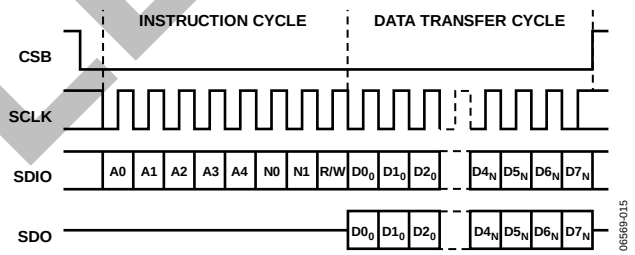

Figure 24. Serial Register Interface Timing—LSB First

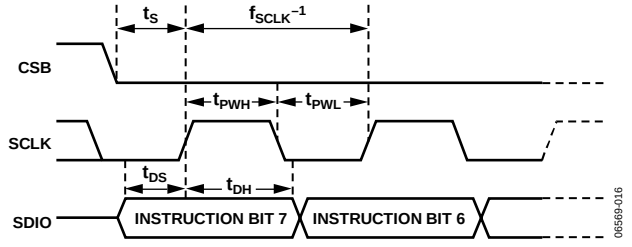

Figure 25. Timing Diagram for SPI Register Write

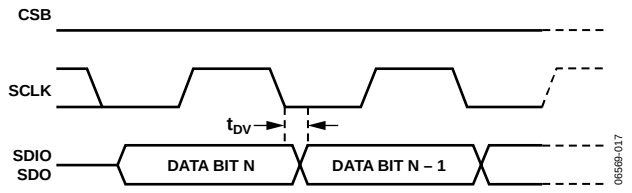

Figure 26. Timing Diagram for SPI Register Read

SPI REGISTER MAP

Reading any register returns previously written values for all defined register bits, unless otherwise noted. Change serial port configuration or execute software reset in single byte instruction only to avoid unexpected device behavior.

Table 14.

Register Name	Address	Default	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Control	0x00	0x00	SDIODIR	LSBFIRST	SWRESET					
Data Control	0x02	0x00	DATTYPE	ONEPORT		INVDCO				
Power Down	0x03	0x00	PD_DCO		PD_AUX2	PD_AUX1	PD_BIAS	PC_CLK	PD_DAC2	PD_DAC1
DAC Mode Select	0x0A	0x00					DAC1MOD<1:0>		DAC2MOD<1:0>	
DAC1 Gain LSB	0x0B	0xF9	DAC1FSC<7:0>							
DAC1 Gain MSB	0x0C	0x01							DAC1FSC<9:8>	
AUX DAC1 LSB	0x0D	0x00	AUXDAC1<7:0>							
AUX DAC1 MSB	0x0E	0x00	AUX1PIN	AUX1DIR					AUXDAC1<9:8>	
DAC2 Gain LSB	0x0F	0xF9	DAC2FSC<7:0>							
DAC2 Gain MSB	0x10	0x01							DAC2FSC<9:8>	
AUX DAC2 LSB	0x11	0x00	AUXDAC2<7:0>							
AUX DAC2 MSB	0x12	0x00	AUX2PIN	AUX2DIR					AUXDAC2<9:8>	

SPI REGISTER DESCRIPTIONS

Table 15.

Register	Address	Bit	Name	Description
SPI Control	0x00	7	SDIODIR	0, operate SPI in 4-wire mode, SDIO pin operates as an input only
				1, operate SPI in 3-wire mode, SDIO pin operates as a bidirectional I/O line
		6	LSBFIRST	0, LSBFIRST off, SPI serial data mode is MSB to LSB
				1, LSBFIRST on, SPI serial data mode is LSB to MSB
		5	SWRESET	0, resume normal operation following software RESET
				1, software RESET; loads default values to all registers (except Register 0x00)
Data Control	0x02	7	DATTYPE	0, DAC input data is twos complement binary format
				1, DAC input data is unsigned binary format
		6	ONEPORT	0, normal two port input mode
				1, optional single port input mode, interleaved data received on Port 1 only
		4	INVDCO	1, inverts data clock output signal
Power Down	0x03	7	PD_DCO	1, power down data clock output
		5	PD_AUX2	1, power down AUX2 DAC
		4	PD_AUX1	1, power down AUX1 DAC
		3	PD_BIAS	1, power down reference voltage bias circuit
		2	PD_CLK	1, power down DAC clock input circuit
		1	PD_DAC2	1, power down DAC2 analog output
		0	PD_DAC1	1, power down DAC1 analog output
DAC Mode Select	0x0A	3:2	DAC1MOD<1:0>	00, selects normal mode, DAC1
				01, selects mix mode, DAC1
				10, selects return-to-zero mode, DAC1
		1:0	DAC2MOD<1:0>	00, selects normal mode, DAC2
				01, selects mix mode, DAC2
				10, selects return-to-zero mode, DAC2
DAC1 Gain	0x0B	7:0	DAC1FSC<7:0>	DAC1 full-scale 10-bit adjustment word
	0x0C	1:0	DAC1FSC<9:8>	0x03FF, sets full-scale current to the maximum value of 31.66 mA
				0x01F9, sets full-scale current to the nominal value of 20.0 mA
				0x0000, sets full-scale current to the minimum value of 8.64 mA
AUX DAC1	0x0D	7:0	AUXDAC1<7:0>	Auxiliary DAC1 10-bit output current adjustment word
	0x0E	1:0	AUXDAC1<9:8>	0x03FF, sets output current magnitude to 2.0 mA
				0x0200, sets output current magnitude to 1.0 mA
				0x0000, sets output current magnitude to 0.0 mA
		7	AUX1PIN	1, AUX1P output pin is active
				0, AUX1N output pin is active
		6	AUX1DIR	0, configures AUX1 DAC output to source current
				1, configures AUX1 DAC output to sink current
DAC2 Gain	0x0F	7:0	DAC2FSC<7:0>	DAC2 full-scale 10-bit adjustment word
	0x10	1:0	DAC2FSC<9:8>	0x03FF, sets full-scale current to the maximum value of 31.66 mA
				0x01F9, sets full-scale current to the nominal value of 20.0 mA
				0x0000, sets full-scale current to the minimum value of 8.64 mA
AUX DAC2	0x11	7:0	AUXDAC2<7:0>	Auxiliary DAC2 10-bit output current adjustment word
	0x12	1:0	AUXDAC2<9:8>	0x03FF, sets output current magnitude to 2.0 mA
				0x0200, sets output current to 1.0 mA
				0x0000, sets output current to 0.0 mA
		7	AUX2PIN	1, AUX2P output pin is active
				0, AUX2N output pin is active
		6	AUX2DIR	0, configures AUX2 DAC output to source current
				1, configures AUX2 DAC output to sink current

DIGITAL INPUTS AND OUTPUTS

The AD9741/AD9743/AD9745/AD9746/AD9747 can operate in two data input modes: dual-port mode and single-port mode. For the default dual-port mode (ONEPORT = 0), each DAC receives data from a dedicated input port. In single-port mode (ONEPORT = 1), however, both DACs receive data from Port 1. In single-port mode, DAC1 and DAC2 data is interleaved and the IQSEL input is used to steer data to the correct DAC.

In single-port mode, when the IQSEL input is high, Port 1 data is delivered to DAC1 and when IQSEL is low, Port 1 data is delivered to DAC2. The IQSEL input should always coincide and be time-aligned with the other data bus signals. In single-port mode, minimum setup and hold times apply to the IQSEL input as well as to the input data signals. In dual-port mode, the IQSEL input is ignored.

In dual-port mode, the data must be delivered at the sample rate (up to 250 MSPS). In single-port mode, data must be delivered at twice the sample rate. Because the data inputs function only up to 250 MSPS, it is only practical to operate the DAC clock at up to 125 MHz in single-port mode.

In both dual-port and single-port modes, a data clock output (DCO) signal is available as a fixed time base with which to stimulate data from an FPGA. This output signal always operates at the sample rate. It may be inverted by asserting the INVDCO bit.

INPUT DATA TIMING

With most DACs, signal-to-noise ratio (SNR) is a function of the relationship between the position of the clock edges and the point in time at which the input data changes. The AD9741/AD9743/AD9745/AD9746/AD9747 are rising edge triggered and thus exhibit greater SNR sensitivity when the data transition is close to this edge.

The specified minimum setup and hold times define a window of time, within each data period, where the data is sampled correctly. Generally, users should position data to arrive relative to the DAC clock and well beyond the minimum setup and minimum hold times. This becomes increasingly more important at increasingly higher sample rates.

DUAL-PORT MODE TIMING

The timing diagram for the dual-port mode is shown in Figure 27.

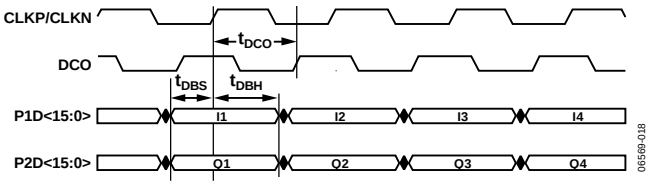

Figure 27. Data Interface Timing, Dual-Port Mode

In Figure 27, data samples for DAC1 are labeled Ix and data samples for DAC2 are labeled Qx. Note that the differential DAC clock input is shown in a logical sense (CLKP/CLKN). The data clock output is labeled DCO.

Setup and hold times are referenced to the positive transition of the DAC clock. Data should arrive at the input pins such that the minimum setup and hold times are met. Note that the data clock output has a fixed time delay from the DAC clock and may be a more convenient signal to use to confirm timing.

SINGLE-PORT MODE TIMING

The single-port mode timing diagram is shown in Figure 28.

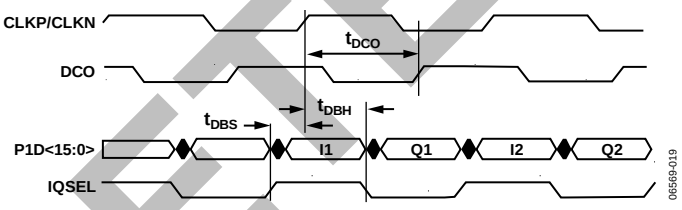

Figure 28. Data Interface Timing, Single-Port Mode

In single-port mode, data for both DACs is received on the Port 1 input bus. Ix and Qx data samples are interleaved and arrive twice as fast as in dual-port mode. Accompanying the data is the IQSEL input signal, which steers incoming data to its respective DAC. When IQSEL is high, data is steered to DAC1 and when IQSEL is low, data is steered to DAC2. IQSEL should coincide as well as be time-aligned with incoming data.

SPI PORT, RESET, AND PIN MODE

In general, when the AD9741/AD9743/AD9745/AD9746/AD9747 are powered up, an active high pulse applied to the RESET pin should follow. This insures the default state of all control register bits. In addition, once the RESET pin goes low, the SPI port can be activated, so CSB should be held high.

For applications without a controller, the AD9741/AD9743/AD9745/AD9746/AD9747 also support pin mode operation, which allows some functional options to be pin, selected without the use of the SPI port. Pin mode is enabled anytime the RESET pin is held high. In pin mode, the four SPI port pins take on secondary functions, as shown in Table 16.

Table 16. SPI Pin Functions (Pin Mode)

Pin Name	Pin Mode Description
SCLK	ONEPORT (Register 0x02, Bit 6), bit value (1/0) equals pin state (high/low)
SDIO	DATTYPE (Register 0x02, Bit 7), bit value (1/0) equals pin state (high/low)
CSB	Enable Mix Mode, if CSB is high, Register 0x0A is set to 0x05 putting both DAC1 and DAC2 into mix mode
SDO	Enable full power-down, if SDO is high, Register 0x03 is set to 0xFF

In pin mode, all register bits are reset to their default values with the exception of those that are controlled by the SPI pins.

Note also that the RESET pin should be allowed to float and must be pulled low. Connect an external 10 kΩ resistor to DVSS. This avoids unexpected behavior in noisy environments.

DRIVING THE DAC CLOCK INPUT

The DAC clock input requires a low jitter drive signal. It is a PMOS differential pair powered from the CVDD18 supply. Each pin can safely swing up to 800 mV p-p at a common-mode voltage of about 400 mV. Though these levels are not directly LVDS-compatible, CLKP and CLKN can be driven by an ac-coupled, dc-offset LVDS signal, as shown in Figure 29.

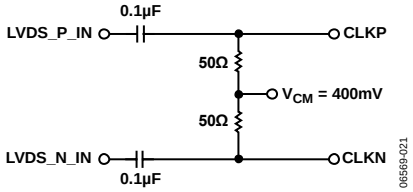

Figure 29. LVDS DAC Clock Drive Circuit

Using a CMOS or TTL clock is also acceptable for lower sample rates. It can be routed through an LVDS translator and then ac-coupled as described previously, or alternatively, it can be transformer-coupled and clamped, as shown in Figure 30.

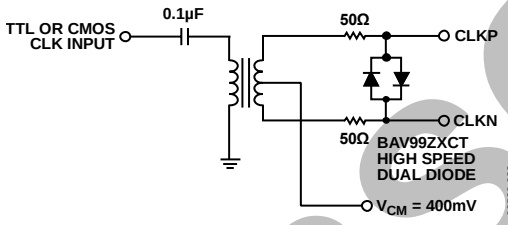

Figure 30. TTL or CMOS DAC Clock Drive Circuit

If a sine wave signal is available, it can be transformer-coupled directly to the DAC clock inputs, as shown in Figure 31.

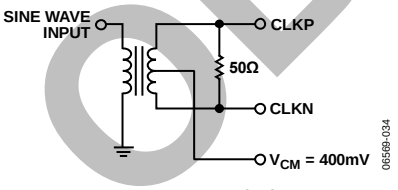

Figure 31. Sine Wave DAC Clock Drive Circuit

The 400 mV common-mode bias voltage can be derived from the CVDD18 supply through a simple divider network, as shown in Figure 32.

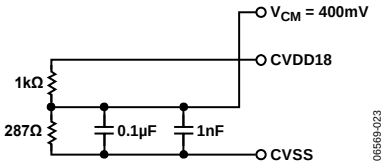

Figure 32. DAC Clock VCM Circuit

It is important to use CVDD18 and CVSS for any clock bias circuit as noise that is coupled onto the clock from another power supply is multiplied by the DAC input signal and degrades performance.

FULL-SCALE CURRENT GENERATION

The full-scale currents on DAC1 and DAC2 are functions of the current drawn through an external resistor connected to the FSADJ pin (Pin 54). The required value for this resistor is 10 kΩ. An internal amplifier sets the current through the resistor to force a voltage equal to the band gap voltage of 1.2 V. This develops a reference current in the resistor of 120 µA.

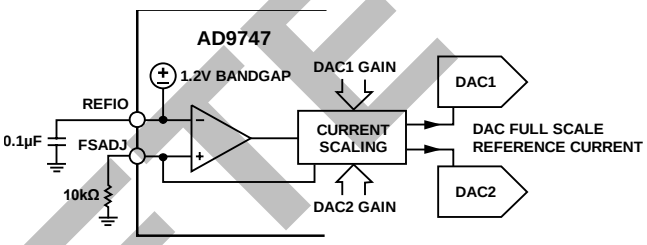

Figure 33. Reference Circuitry

REFIO (Pin 55) should be bypassed to ground with a 0.1 µF capacitor. The band gap voltage is present on this pin and can be buffered for use in external circuitry. The typical output impedance is near 5 kΩ. If desired, an external reference can be connected to REFIO to overdrive the internal reference.

Internal current mirrors provide a means for adjusting the DAC full-scale currents. The gain for DAC1 and DAC2 can be adjusted independently by writing to the DAC1FSC<9:0> and DAC2FSC<9:0> register bits. The default value of 0x01F9 for the DAC gain registers gives an I_{FS} of 20 mA, where I_{FS} equals

$$I_{FS} = \frac{1.2\text{ V}}{10{,}000} \times \left(72 + \left(\frac{3}{16} \times DAC\,\text{n}\,FSC\right)\right)$$

The full-scale output current range is 8.6 mA to 31.7 mA for register values 0x000 to 0x3FF.

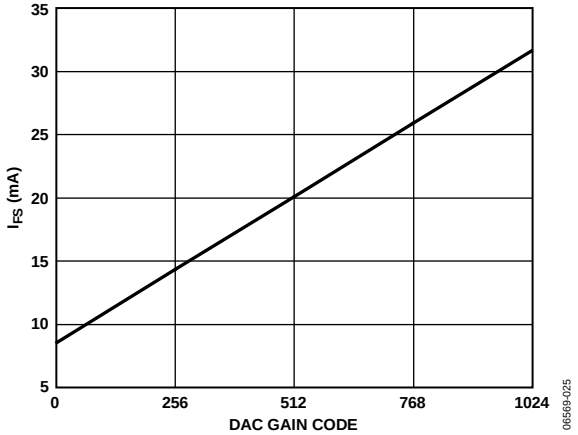

Figure 34. I_{FS} vs. DAC Gain Code

DAC TRANSFER FUNCTION

Each DAC output of the AD9741/AD9743/AD9745/AD9746/AD9747 drives complementary current outputs I_{OUTP} and I_{OUTN}. I_{OUTP} provides a near full-scale current output (I_{FS}) when all bits are high. For example,

$$DAC\ CODE = 2^N - 1$$

where:
N = 8-/10-/12-/14-/16-bits (for AD9741/AD9743/AD9745/AD9746/AD9747 respectively), and I_{OUTN} provides no current.

The current output appearing at I_{OUTP} and I_{OUTN} is a function of both the input code and I_{FS} and can be expressed as

$$I_{OUTP} = (DAC\ DATA/2^N) \times I_{FS} \quad (1)$$

$$I_{OUTN} = ((2^N - 1) - DAC\ DATA)/2^N \times I_{FS} \quad (2)$$

where $DAC\ DATA$ = 0 to $2^N - 1$ (decimal representation).

The two current outputs typically drive a resistive load directly or via a transformer. If dc coupling is required, I_{OUTP} and I_{OUTN} should be connected to matching resistive loads (R_{LOAD}) that are tied to analog common (AVSS). The single-ended voltage output appearing at the I_{OUTP} and I_{OUTN} pins is

$$V_{OUTP} = I_{OUTP} \times R_{LOAD} \quad (3)$$

$$V_{OUTN} = I_{OUTN} \times R_{LOAD} \quad (4)$$

Note that to achieve the maximum output compliance of 1 V at the nominal 20 mA output current, R_{LOAD} must be set to 50 Ω. Also note that the full-scale value of V_{OUTP} and V_{OUTN} should not exceed the specified output compliance range to maintain specified distortion and linearity performance.

There are two distinct advantages to operating the AD9741/AD9743/AD9745/AD9746/AD9747 differentially. First, differential operation helps cancel common-mode error sources associated with I_{OUTP} and I_{OUTN}, such as noise, distortion, and dc offsets. Second, the differential code dependent current and subsequent output voltage (V_{DIFF}) is twice the value of the single-ended voltage output (V_{OUTP} or V_{OUTN}), providing 2× signal power to the load.

$$V_{DIFF} = (I_{OUTP} - I_{OUTN}) \times R_{LOAD} \quad (5)$$

ANALOG MODES OF OPERATION

The AD9741/AD9743/AD9745/AD9746/AD9747 utilize a proprietary quad-switch architecture that lowers the distortion of the DAC output by eliminating a code dependent glitch that occurs with conventional dual-switch architectures. But whereas this architecture eliminates the code dependent glitches, it creates a constant glitch at a rate of 2 × f_{DAC}. For communications systems and other applications requiring good frequency domain performance, this is seldom problematic.

The quad-switch architecture also supports two additional modes of operation; mix mode and return-to-zero (RZ) mode. The waveforms of these two modes are shown in Figure 35. In mix mode, the output is inverted every other half clock cycle. This effectively chops the DAC output at the sample rate. This chopping has the effect of frequency shifting the sinc roll-off from dc to f_{DAC}. Additionally, there is a second subtle effect on the output spectrum. The shifted spectrum is shaped by a second sinc function with a first null at 2 × f_{DAC}. The reason for this shaping is that the data is not continuously varying at twice the clock rate, but is simply repeated.

In RZ mode, the output is set to midscale on every other half clock cycle. The output is similar to the DAC output in normal mode except that the output pulses are half the width and half the area. Because the output pulses have half the width, the sinc function is scaled in frequency by 2 and has a first null at 2 × f_{DAC}. Because the area of the pulses is half that of the pulses in normal mode, the output power is half the normal mode output power.

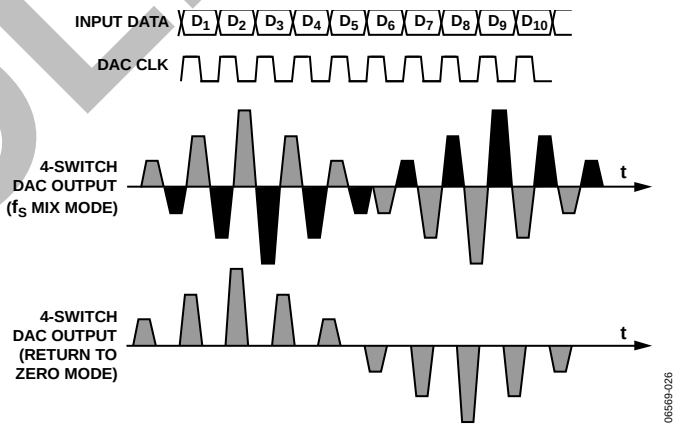

Figure 35. Mix Mode and RZ Mode DAC Waveforms

The functions that shape the output spectrums for normal mode, mix mode, and RZ mode, are shown in Figure 36. Switching between the modes reshapes the sinc roll off inherent at the DAC output. This ability to change modes in the AD9741/AD9743/AD9745/AD9746/AD9747 makes the parts suitable for direct IF applications. The user can place a carrier anywhere in the first three Nyquist zones depending on the operating mode selected. The performance and maximum amplitude in all three zones are impacted by this sinc roll off depending on where the carrier is placed, as shown in Figure 36.

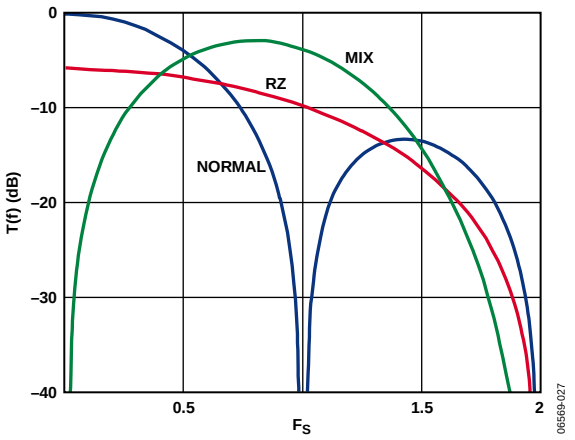

Figure 36. Transfer Function for Each Analog Operating Mode

AUXILIARY DACS

Two auxiliary DACs are provided on the AD9741/AD9743/AD9745/AD9746/AD9747. A functional diagram is shown in Figure 37. The auxiliary DACs are current output devices with two output pins, AUXP and AUXN. The active pin can be programmed to either source or sink current. When either sinking or sourcing, the full-scale current magnitude is 2 mA. The available compliance range at the auxiliary DAC outputs depends on whether the output is configured to a sink or source current. When sourcing current, the compliance voltage is 0 V to 1.6 V, but when sinking current, the output compliance voltage reduces to 0.8 V to 1.6 V. Either output can be used, but only one output of the auxiliary DAC (P or N) is active at any time. The inactive pin is always in a high impedance state (>100 kΩ).

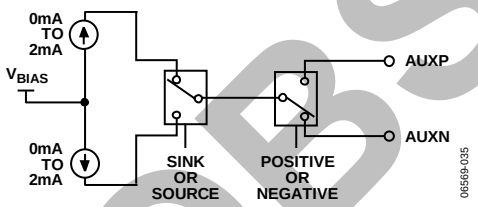

Figure 37. Auxiliary DAC Functional Diagram

In a single side band transmitter application, the combination of the input referred dc offset voltage of the quadrature modulator and the DAC output offset voltage can result in local oscillator (LO) feedthrough at the modulator output, which degrades system performance. The auxiliary DACs can be used to remove the dc offset and the resulting LO feedthrough. The circuit configuration for using the auxiliary DACs for performing dc offset correction depends on the details of the DAC and modulator interface. An example of a dc-coupled configuration with low-pass filtering is outlined in the Power Dissipation section.

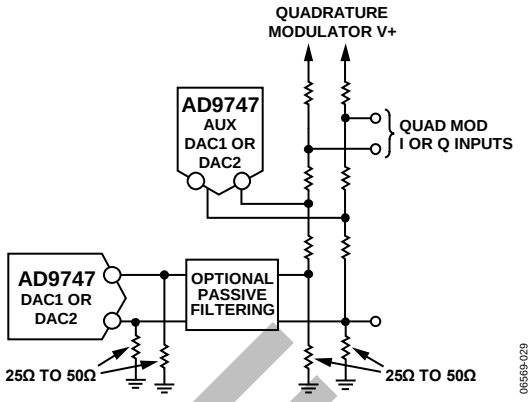

Figure 38. DAC DC Coupled to Quadrature Modulator with Passive DC Shift

POWER DISSIPATION

Figure 39 shows the power dissipation and current draw of the AD9741/AD9743/AD9745/AD9746/AD9747. It shows that the devices have a quiescent power dissipation of about 190 mW. Most of this comes from the AVDD33 supply. Total power dissipation increases about 50% as the clock rate is increased to the maximum clock rate of 250 MHz.

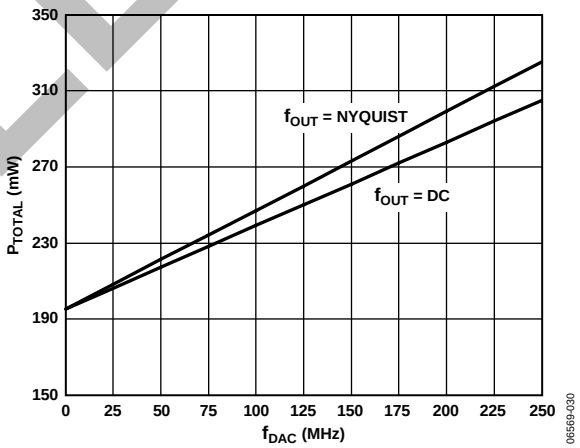

Figure 39. AD9747 Power Dissipation vs. f_{DAC}

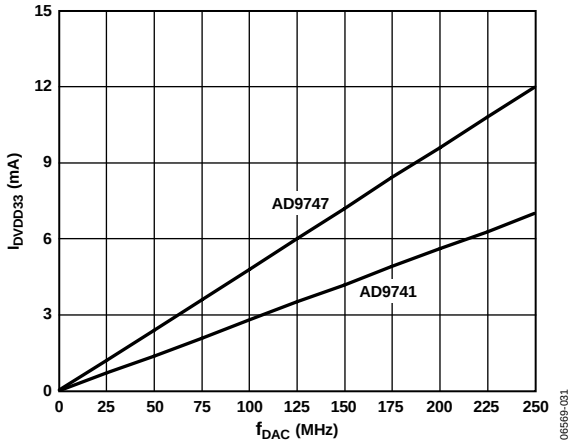

Figure 40. DVDD33 Current vs. f_{DAC}

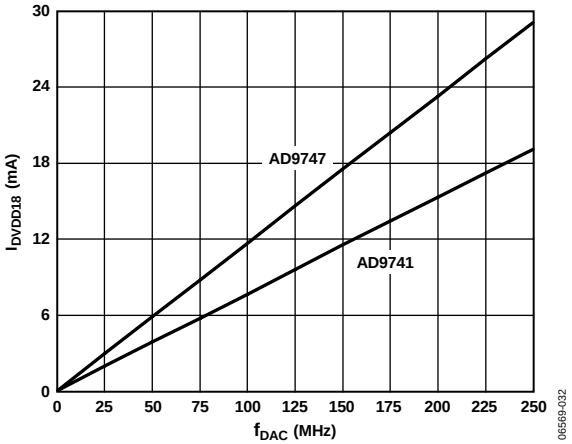

Figure 41. DVDD18 Current vs. f_{DAC}

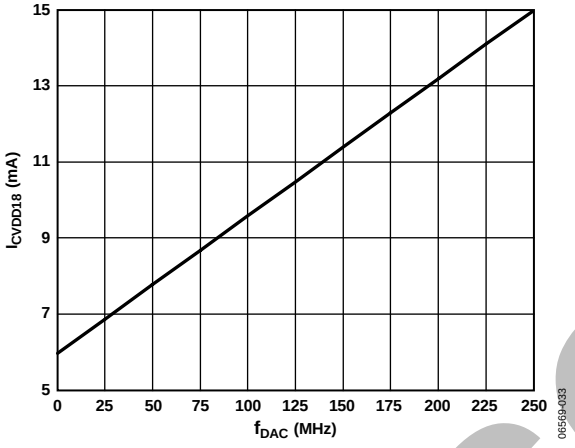

Figure 42. CVDD18 Current vs. f_{DAC}

Figure 43 shows the power consumption for each power supply domain as well as the total power consumption. Individual bars within each group display the power in full active mode (blue) vs. power for five increasing levels of power-down.

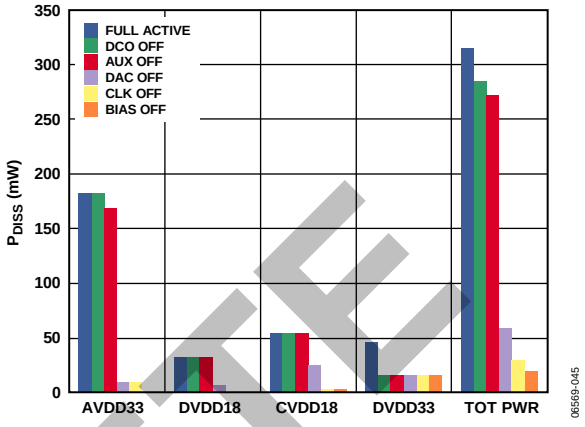

Figure 43. Power Dissipation vs. Power-Down Mode

The overall power consumption is dominated by AVDD33 and significant power savings can be achieved simply by disabling the DAC outputs. Also, disabling the DAC outputs is a significant way to conserve power and still maintain a fast wake-up time. Full power-down disables all circuitry for minimum power consumption. Note, however, that even in full power-down, there is a small power draw (25 mW) due to incoming data activity. To lower power consumption to near zero, all incoming data activity must be halted.

OUTLINE DIMENSIONS

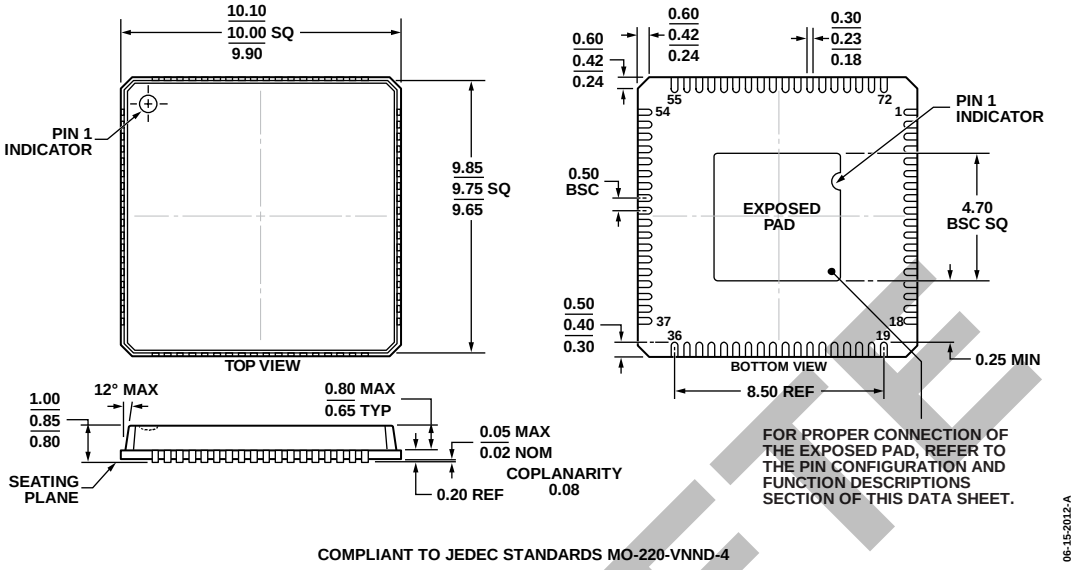

Figure 44. 72-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
10 mm × 10 mm, Very Thin Quad
(CP-72-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD9741BCPZ	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9741BCPZRL	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9743BCPZ	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9743BCPZRL	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9745BCPZ	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9745BCPZRL	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9746BCPZ	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9746BCPZRL	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9747BCPZ	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9747BCPZRL	−40°C to +85°C	72-Lead LFCSP_VQ	CP-72-1
AD9741-DPG2-EBZ		Evaluation Board	
AD9743-DPG2-EBZ		Evaluation Board	
AD9745-DPG2-EBZ		Evaluation Board	
AD9746-DPG2-EBZ		Evaluation Board	
AD9747-DPG2-EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

D06569-0-1/14(B)