ULTRALOW NOISE PERFORMANCE
2.9 nV/√Hz at 10 kHz
0.38 μV p-p, 0.1 Hz to 10 Hz
6.9 fA/√Hz Current Noise at 1 kHz

EXCELLENT AC PERFORMANCE
12.5 V/μs Slew Rate
20 MHz Gain Bandwidth Product
THD = 0.0002% @ 1 kHz
Internally Compensated for Gains of +5 (or –4) or Greater

EXCELLENT DC PERFORMANCE
0.5 mV Max Offset Voltage
250 pA Max Input Bias Current
2000 V/mV Min Open Loop Gain
Available in Tape and Reel in Accordance with EIA-481A Standard

APPLICATIONS
Sonar
Photodiode and IR Detector Amplifiers
Accelerometers
Low Noise Preamplifiers
High Performance Audio

PRODUCT DESCRIPTION
The AD745 is an ultralow noise, high-speed, FET input operational amplifier. It offers both the ultralow voltage noise and high speed generally associated with bipolar input op amps and the very low input currents of FET input devices. Its 20 MHz bandwidth and 12.5 V/μs slew rate makes the AD745 an ideal amplifier for high-speed applications demanding low noise and high dc precision. Furthermore, the AD745 does not exhibit an output phase reversal.

The AD745 also has excellent dc performance with 250 pA maximum input bias current and 0.5 mV maximum offset voltage.

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier where low level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains. The AD745 is available in two performance grades. The AD745J and AD745K are rated over the commercial temperature range of 0°C to 70°C, and are available in the 16-lead SOIC package.

Analog Devices, Inc., 2002
### AD745—SPECIFICATIONS
#### AD745 ELECTRICAL CHARACTERISTICS (@ +25°C and ±15 V dc, unless otherwise noted.)

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<th>Typ</th>
<th>Max</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<td>Initial Offset</td>
<td>$T_{\text{MIN}}$ to $T_{\text{MAX}}$</td>
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<td>0.1</td>
<td>0.5</td>
<td>mV</td>
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<td>vs. Temp.</td>
<td>$T_{\text{MIN}}$ to $T_{\text{MAX}}$</td>
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<td>1.5</td>
<td>2</td>
<td>1.0</td>
<td>mV</td>
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<tr>
<td>vs. Supply (PSRR)</td>
<td>12 V to 18 V²</td>
<td>90</td>
<td>96</td>
<td>100</td>
<td>106</td>
<td>dB</td>
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<td></td>
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<td>vs. Supply (PSRR)</td>
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<td>98</td>
<td>105</td>
<td>105</td>
<td>dB</td>
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<td>INPUT BIAS CURRENT³</td>
<td>Either Input</td>
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<td>400</td>
<td>150</td>
<td>250</td>
<td>pA</td>
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<td>120</td>
<td>MHz</td>
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<tr>
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<td>600</td>
<td>250</td>
<td>400</td>
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<td>200</td>
<td>30</td>
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<td>150</td>
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<td>@ $T_{\text{MAX}}$</td>
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<td></td>
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<tr>
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<td>Gain BW, Small Signal</td>
<td>$G = -4$</td>
<td>20</td>
<td>20</td>
<td>kHz</td>
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<td>Full Power Response</td>
<td>$V_{O} = 20$ V p-p</td>
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<td>120</td>
<td>kHz</td>
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<td>12.5</td>
<td>µs</td>
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<td>Settling Time to 0.01%</td>
<td>$G = -4$</td>
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<td>5</td>
<td>µs</td>
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<td>Total Harmonic Distortion⁴</td>
<td>f = 1 kHz</td>
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<td>0.0002</td>
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<td>INPUT IMPEDANCE</td>
<td>Differential</td>
<td>$1 \times 10^{10}$Ω</td>
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<td>100</td>
<td>ΩpF</td>
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<td>Common Mode</td>
<td>$3 \times 10^{11}$Ω</td>
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<td>100</td>
<td>ΩpF</td>
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<tr>
<td>INPUT VOLTAGE RANGE</td>
<td>Differential⁵</td>
<td>$V_{\text{CM}} = \pm 10$ V</td>
<td>±20</td>
<td>±10.7</td>
<td>±20</td>
<td>±10.7</td>
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<tr>
<td>Common-Mode Voltage</td>
<td>$V_{\text{CM}} = \pm 10$ V</td>
<td>±13.3</td>
<td>+12</td>
<td>±13.3</td>
<td>+12</td>
<td>V</td>
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<tr>
<td>Over Max Operating Range⁶</td>
<td>$V_{\text{CM}} = \pm 10$ V</td>
<td>−10</td>
<td>+12</td>
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<td>+12</td>
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<tr>
<td>Common-Mode</td>
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<td>95</td>
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<td>102</td>
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<td>Rejection Ratio</td>
<td>$T_{\text{MIN}}$ to $T_{\text{MAX}}$</td>
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<td>88</td>
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<td>88</td>
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<td>INPUT VOLTAGE NOISE</td>
<td>f = 0.1 to 10 Hz</td>
<td>0.38</td>
<td>0.38</td>
<td>0.38</td>
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<td>µV p-p</td>
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<tr>
<td>f = 10 Hz</td>
<td>5.5</td>
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<td>nV/√Hz</td>
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<tr>
<td>f = 100 Hz</td>
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<td>6.9</td>
<td>fA/√Hz</td>
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<td>$V_{O} = \pm 10$ V</td>
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<td>4000</td>
<td>2000</td>
<td>4000</td>
<td>V/mV</td>
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<td>$R_{\text{LOAD}} \geq 2$ kΩ</td>
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<td>1200</td>
<td>800</td>
<td>1200</td>
<td>V/mV</td>
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<td>OUTPUT CHARACTERISTICS</td>
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<td>$R_{\text{LOAD}} \geq 600$ Ω</td>
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<td>+13, −12</td>
<td>+13.6, −12.6</td>
<td>V</td>
<td></td>
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<tr>
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<td>$R_{\text{LOAD}} \geq 2$ kΩ</td>
<td>+12, −10</td>
<td>+12, −10</td>
<td>+13.8, −13.1</td>
<td>V</td>
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<td>Short Circuit</td>
<td>20</td>
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<td>20</td>
<td>40</td>
<td>mA</td>
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<tr>
<td>POWER SUPPLY</td>
<td>Rated Performance</td>
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<td>Operating Range</td>
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<td>±15</td>
<td>±15</td>
<td>V</td>
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<td>Quiescent Current</td>
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<td>±4.8</td>
<td>±18</td>
<td>±4.8</td>
<td>±18</td>
<td>V</td>
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<td></td>
<td></td>
<td>8</td>
<td>10.0</td>
<td>8</td>
<td>10.0</td>
<td>mA</td>
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<tr>
<td>TRANSISTOR COUNT</td>
<td># of Transistors</td>
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<td>50</td>
<td>50</td>
<td>50</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>

**NOTES**

¹ Input offset voltage specifications are guaranteed after five minutes of operation at $T_{A} = 25^\circ$C.

² Test conditions: $+V_{S} = 15$ V, $–V_{S} = 12$ V to 18 V and $+V_{S} = 12$ V to +18 V, $–V_{S} = 15$ V.

³ Bias current specifications are guaranteed maximum at either input after five minutes of operation at $T_{A} = 25^\circ$C. For higher temperature, the current doubles every 10°C.

⁴ Gain = −4, $R_{L} = 2$ kΩ, $C_{L} = 10$ pF.

⁵ Defined as voltage between inputs, such that neither exceeds $\pm 10$ V from common.

⁶ The AD745 does not exhibit an output phase reversal when the negative common-mode limit is exceeded.

All min and max specifications are guaranteed.

Specifications subject to change without notice.
**CAUTION**

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD745 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

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**ABSOLUTE MAXIMUM RATINGS**

- Supply Voltage: ±18 V
- Internal Power Dissipation: 1.2 W
- Input Voltage: ±V$_S$
- Output Short-Circuit Duration: Indefinite
- Differential Input Voltage: +V$_S$ and -V$_S$
- Storage Temperature Range (R): -65°C to +125°C
- Operating Temperature Range (AD745J/K): 0°C to 70°C
- Lead Temperature Range (Soldering 60 sec): 300°C

**NOTES**

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

2. 16-Pin Plastic SOIC Package: $\theta$$_{JA}$ = 100°C/W, $\theta$$_{JC}$ = 30°C/W

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**ESD SUSCEPTIBILITY**

An ESD classification per method 3015.6 of MIL-STD-883C has been performed on the AD745, which is a class 1 device. Using an IMCS 5000 automated ESD tester, the two null pins will pass at voltages up to 1,000 volts, while all other pins will pass at voltages exceeding 2,500 volts.

**ORDERING GUIDE**

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<th>Temperature Range</th>
<th>Package Option*</th>
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<td>R-16</td>
</tr>
<tr>
<td>AD745KR-16</td>
<td>0°C to 70°C</td>
<td>R-16</td>
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*R = Small Outline IC.
AD745 – Typical Performance Characteristics (@ +25°C, V3 = ±15 V, unless otherwise noted.)

**TPC 1. Input Voltage Swing vs. Supply Voltage**

**TPC 2. Output Voltage Swing vs. Supply Voltage**

**TPC 3. Output Voltage Swing vs. Load Resistance**

**TPC 4. Quiescent Current vs. Supply Voltage**

**TPC 5. Input Bias Current vs. Temperature**

**TPC 6. Output Impedance vs. Frequency**

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TPC 22a. Gain of 5 Follower, 16-Lead Package Pinout

TPC 22b. Gain of 5 Follower Large Signal Pulse Response

TPC 22c. Gain of 5 Follower Small Signal Pulse Response

TPC 23a. Gain of 4 Inverter, 16-Lead Package Pinout

TPC 23b. Gain of 4 Inverter Large Signal Pulse Response

TPC 23c. Gain of 4 Inverter Small Signal Pulse Response
OP AMP PERFORMANCE JFET VERSUS BIPOLAR
The AD745 offers the low input voltage noise of an industry standard bipolar opamp without its inherent input current errors. This is demonstrated in Figure 3, which compares input voltage noise vs. input source resistance of the OP37 and the AD745 opamps. From this figure, it is clear that at high source impedance the low current noise of the AD745 also provides lower total noise. It is also important to note that with the AD745 this noise reduction extends all the way down to low source impedances. The lower dc current errors of the AD745 also reduce errors due to offset and drift at high source impedances (Figure 4).

The internal compensation of the AD745 is optimized for higher gains, providing a much higher bandwidth and a faster slew rate. This makes the AD745 especially useful as a preamplifier, where low-level signals require an amplifier that provides both high amplification and wide bandwidth at these higher gains.

The 0.1 Hz to 10 Hz noise is typically 0.38 µV p-p. The user should pay careful attention to several design details to optimize low frequency noise performance. Random air currents can generate varying thermocouple voltages that appear as low frequency noise. Therefore, sensitive circuitry should be well shielded from air flow. Keeping absolute chip temperature low also reduces low frequency noise in two ways: first, the low frequency noise is strongly dependent on the ambient temperature and increases above 25°C. Second, since the gradient of temperature from the IC package to ambient is greater, the noise generated by random air currents, as previously mentioned, will be larger in magnitude. Chip temperature can be reduced both by operation at reduced supply voltages and by the use of a suitable clip-on heat sink, if possible.

Low frequency current noise can be computed from the magnitude of the dc bias current

\[ I_n = \sqrt{2qI_B\Delta f} \]

and increases below approximately 100 Hz with a 1/f power spectral density. For the AD745 the typical value of current noise is 6.9 fA/√Hz at 1 kHz. Using the formula:

\[ I_n = \sqrt{4kT/R\Delta f} \]

to compute the Johnson noise of a resistor, expressed as a current, one can see that the current noise of the AD745 is equivalent to that of a 3.45 × 10^8 Ω source resistance.

At high frequencies, the current noise of a FET increases proportionately to frequency. This noise is due to the “real” part of the gate input impedance, which decreases with frequency. This noise component usually is not important, since the voltage noise of the amplifier impressed upon its input capacitance is an apparent current noise of approximately the same magnitude.

In any FET input amplifier, the current noise of the internal bias circuitry can be coupled externally via the gate-to-source capacitances and appears as input current noise. This noise is totally correlated at the inputs, so source impedance matching will tend to cancel out its effect. Both input resistance and input capacitance should be balanced whenever dealing with source capacitances of less than 300 pF in value.

LOW NOISE CHARGE AMPLIFIERS
As stated, the AD745 provides both low voltage and low current noise. This combination makes this device particularly suitable in applications requiring very high charge sensitivity, such as capacitive accelerometers and hydrophones. When dealing with a high source capacitance, it is useful to consider the total input charge uncertainty as a measure of system noise.

Charge (Q) is related to voltage and current by the simply stated fundamental relationships:

\[ Q = CV \quad \text{and} \quad I = \frac{dQ}{dt} \]

As shown, voltage, current and charge noise can all be directly related. The change in open circuit voltage (ΔV) on a capacitor will equal the combination of the change in charge (ΔQ/C) and the change in capacitance with a built-in charge (Q/ΔC).
Figures 5 and 6 show two ways to buffer and amplify the output of a charge output transducer. Both require the use of an amplifier that has a very high input impedance, such as the AD745. Figure 5 shows a model of a charge amplifier circuit. Here, amplification depends on the principle of conservation of charge at the input of amplifier A1, which requires that the charge on capacitor CS be transferred to capacitor CF, thus yielding an output voltage of \( \Delta Q/CF \). The amplifiers input voltage noise will appear at the output amplified by the noise gain \( (1 + (CS/CF)) \) of the circuit.

![Figure 5. A Charge Amplifier Circuit](image)

The second circuit, Figure 6, is simply a high impedance follower with gain. Here, the noise gain \( (1 + (R1/R2)) \) is the same as the gain from the transducer to the output. Resistor RB, in both circuits, is required as a dc bias current return.

There are three important sources of noise in these circuits. Amplifiers A1 and A2 contribute both voltage and current noise, while resistor RB contributes a current noise of:

\[
\tilde{N} = \sqrt{4kT/R} \Delta f
\]

where:

- \( k \) = Boltzman’s Constant = 1.381 \times 10^{-23} Joules/Kelvin
- \( T \) = Absolute Temperature, Kelvin (0°C = 273.2 Kelvin)
- \( \Delta f \) = Bandwidth – in Hz (Assuming an Ideal “Brick Wall” Filter)

This must be root-sum-squared with the amplifier’s own current noise.

Figure 5 shows that these two circuits have an identical frequency response and the same noise performance (provided that \( C_s/C_F = R_1/R_2 \)). One feature of the first circuit is that a “T” network is used to increase the effective resistance of RB and improve the low frequency cutoff point by the same factor.

![Figure 6. Model for A High Z Follower with Gain](image)

However, this does not change the noise contribution of RB which, in this example, dominates at low frequencies. The graph of Figure 8 shows how to select an RB large enough to minimize this resistor’s contribution to overall circuit noise. When the equivalent current noise of RB ((\( \sqrt{4kT/R} \)) equals the noise of \( I_B(\sqrt{2qI_B}) \), there is diminishing return in making RB larger.

![Figure 8. Graph of Resistance vs. Input Bias Current Where the Equivalent Noise \( \sqrt{4kT/R} \), Equals the Noise of the Bias Current \( I_B(\sqrt{2qI_B}) \)](image)
HOW CHIP PACKAGE TYPE AND POWER DISSIPATION AFFECT INPUT BIAS CURRENT

As with all JFET input amplifiers, the input bias current of the AD745 is a direct function of device junction temperature, $I_B$, approximately doubling every $10^\circ$C. Figure 9 shows the relationship between bias current and junction temperature for the AD745. This graph shows that lowering the junction temperature will dramatically improve $I_B$.

![Figure 9. Input Bias Current vs. Junction Temperature](image)

The dc thermal properties of an IC can be closely approximated by using the simple model of Figure 10 where current represents power dissipation, voltage represents temperature, and resistors represent thermal resistance (in °C/watt).

![Figure 10. Device Thermal Model](image)

From this model $T_J = T_A + \theta_{JA} P_{IN}$. Therefore, $I_B$ can be determined in a particular application by using Figure 9 together with the published data for $\theta_{JA}$ and power dissipation. The user can modify $\theta_{JA}$ by use of an appropriate clip-on heat sink such as the Aavid #5801. Figure 11 shows bias current versus supply voltage with $\theta_{JA}$ as the third variable. This graph can be used to predict bias current after $\theta_{JA}$ has been computed. Again bias current will double for every $10^\circ$C.

![Figure 11. Input Bias Current vs. Supply Voltage for Various Values of $\theta_{JA}$](image)

REduced POWER SUPPLY OPERATION FOR LOWER $I_B$

Reduced power supply operation lowers $I_B$ in two ways: first, by lowering both the total power dissipation and, second, by reducing the basic gate-to-junction leakage (Figure 11). Figure 13 shows a 40 dB gain piezoelectric transducer amplifier, which operates without an ac coupling capacitor, over the $-40^\circ$C to $+85^\circ$C temperature range. If the optional coupling capacitor, $C_1$, is used, this circuit will operate over the entire $-55^\circ$C to $+125^\circ$C temperature range.

![Figure 13. A Piezoelectric Transducer](image)
Two of the most popular charge-out transducers are hydrophones and accelerometers. Precision accelerometers are typically calibrated for a charge output (pC/g).* Figures 14 and 15 show two ways in which to configure the AD745 as a low noise charge amplifier for use with a wide variety of piezoelectric accelerometers. The input sensitivity of these circuits will be determined by the value of capacitor C1 and is equal to:

\[ \Delta V_{OUT} = \frac{\Delta Q_{OUT}}{C1} \]

The ratio of capacitor C1 to the internal capacitance (C_T) of the transducer determines the noise gain of this circuit \((1 + C_T/C1)\). The amplifiers voltage noise will appear at its output amplified by this amount. The low frequency bandwidth of these circuits will be dependent on the value of resistor R1. If a “T” network is used, the effective value is: \(R1 (1 + R2/R3)\).

* \(pC = \text{Picocoulombs} \)

\(g = \text{Earth's Gravitational Constant}\)

\[\begin{align*}
R1 & = 110 \text{M} \\
C1 & = 1250 \text{pF} \\
C_T & = \text{Transducer's internal capacitance} \\
R4 & = 18 \text{M} \\
C3 & = 2.2 \mu \text{F} \\
R5 & = 1 \text{M} \\
R6 & = 1 \text{M} \\
R7 & = 1 \text{M} \\
R2 & = 9 \text{k} \\
R3 & = 1 \text{k} \\
C_C & = \text{Optional DC blocking capacitor}
\end{align*}\]

A dc servo loop (Figure 15) can be used to assure a dc output \(<10 \text{ mV}\), without the need for a large compensating resistor when dealing with bias currents as large as 100 nA. For optimal low frequency performance, the time constant of the servo loop \((R4C2 = R5C3)\) should be:

\[\text{Time Constant} \geq 10 R1 \left(1 + \frac{R2}{R3}\right)C1\]

A LOW NOISE HYDROPHONE AMPLIFIER

Hydrophones are usually calibrated in the voltage-out mode. The circuit of Figures 16 can be used to amplify the output of a typical hydrophone. If the optional ac coupling capacitor C_C is used, the circuit will have a low frequency cutoff determined by an RC time constant equal to:

\[\text{Time Constant} \geq 10 R1 \frac{1}{2\pi C_C \times 100 \Omega}\]

where the dc gain is 1 and the gain above the low frequency cutoff \((1/(2\pi C_C(100 \Omega)))\) is equal to \((1 + R2/R3)\). The circuit of Figure 17 uses a dc servo loop to keep the dc output at 0 V and to maintain full dynamic range for \(I_B\)'s up to 100 nA. The time constant of R7 and C1 should be larger than that of R1 and C_T for a smooth low frequency response.

![Figure 14. A Basic Accelerometer Circuit](image)

![Figure 15. An Accelerometer Circuit Employing a DC Servo Amplifier](image)

A dc servo loop (Figure 15) can be used to assure a dc output \(<10 \text{ mV}\), without the need for a large compensating resistor when dealing with bias currents as large as 100 nA. For optimal low frequency performance, the time constant of the servo loop \((R4C2 = R5C3)\) should be:

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![Figure 16. A Low Noise Hydrophone Amplifier](image)

The transducer shown has a source capacitance of 7500 pF. For smaller transducer capacitances \((\leq 300 \text{ pF})\), lowest noise can be achieved by adding a parallel RC network \((R4 = R1, C1 = C_T)\) in series with the inverting input of the AD745.

![Figure 17. A Hydrophone Amplifier Incorporating a DC Servo Loop](image)
DESIGN CONSIDERATIONS FOR I-TO-V CONVERTERS

There are some simple rules of thumb when designing an I-V converter where there is significant source capacitance (as with a photodiode) and bandwidth needs to be optimized. Consider the circuit of Figure 18. The high frequency noise gain \((1 + C_S/C_L)\) is usually greater than five, so the AD745, with its higher slew rate and bandwidth is ideally suited to this application.

Here both the low current and low voltage noise of the AD745 can be taken advantage of, since it is desirable in some instances to have a large RF (which increases sensitivity to input current noise) and, at the same time, operate the amplifier at high noise gain.

**Figure 18. A Model for an I-to-V Converter**

In this circuit, the \(R_F C_S\) time constant limits the practical bandwidth over which flat response can be obtained, in fact:

\[
f_B = \frac{f_C}{2 \pi R_F C_S}
\]

where:

- \(f_B\) = signal bandwidth
- \(f_C\) = gain bandwidth product of the amplifier

With \(C_L = 1/(2 \pi R_F C_S)\) the net response can be adjusted to provide a two pole system with optimal flatness that has a corner frequency of \(f_B\). Capacitor \(C_L\) adjusts the damping of the circuit’s response. Note that bandwidth and sensitivity are directly traded off against each other via the selection of \(R_F\). For example, a photodiode with \(C_S = 300\ pF\) and \(R_F = 100\ \Omega\) will have a maximum bandwidth of 360 kHz when capacitor \(C_L = 4.5\ pF\).

Conversely, if only a 100 kHz bandwidth were required, then the maximum value of \(R_F\) would be 360 \(\Omega\) and that of capacitor \(C_L\) still \(4.5\ pF\).

In either case, the AD745 provides impedance transformation, the effective transresistance, i.e., the I/V conversion gain, may be augmented with further gain. A wideband low noise amplifier such as the AD829 is recommended in this application.

This principle can also be applied to use the AD745 in a high performance audio application. Figure 19 shows that an I-V converter of a high performance DAC, here the AD1862, can be designed to take advantage of the low voltage noise of the AD745 (2.9 nV/\(\sqrt{Hz}\)) as well as the high slew rate and bandwidth provided by decompensation. This circuit, with component values shown, has a 12 dB/octave rolloff at 728 kHz, with a passband ripple of less than 0.001 dB and a phase deviation of less than 2 degrees @ 20 kHz.

**Figure 19. A High Performance Audio DAC Circuit**

An important feature of this circuit is that high frequency energy, such as clock feedthrough, is shunted to common via a high quality capacitor and not the output stage of the amplifier, greatly reducing the error signal at the input of the amplifier and subsequent opportunities for intermodulation distortions.

**Figure 20. RTI Noise Voltage vs. Input Capacitance**

**BALANCING SOURCE IMPEDANCES**

As mentioned previously, it is good practice to balance the source impedances (both resistive and reactive) as seen by the inputs of the AD745. Balancing the resistive components will optimize dc performance over temperature because balancing will mitigate the effects of any bias current errors. Balancing input capacitance will minimize ac response errors due to the amplifier’s input capacitance and, as shown in Figure 20, noise performance will be optimized. Figure 21 shows the required external components for noninverting (A) and inverting (B) configurations.
Figure 40. Optional External Components for Balancing Source Impedances

OUTLINE DIMENSIONS
Dimensions shown in inches and (mm).

16-Lead SOIC (R) Package

Revision History

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