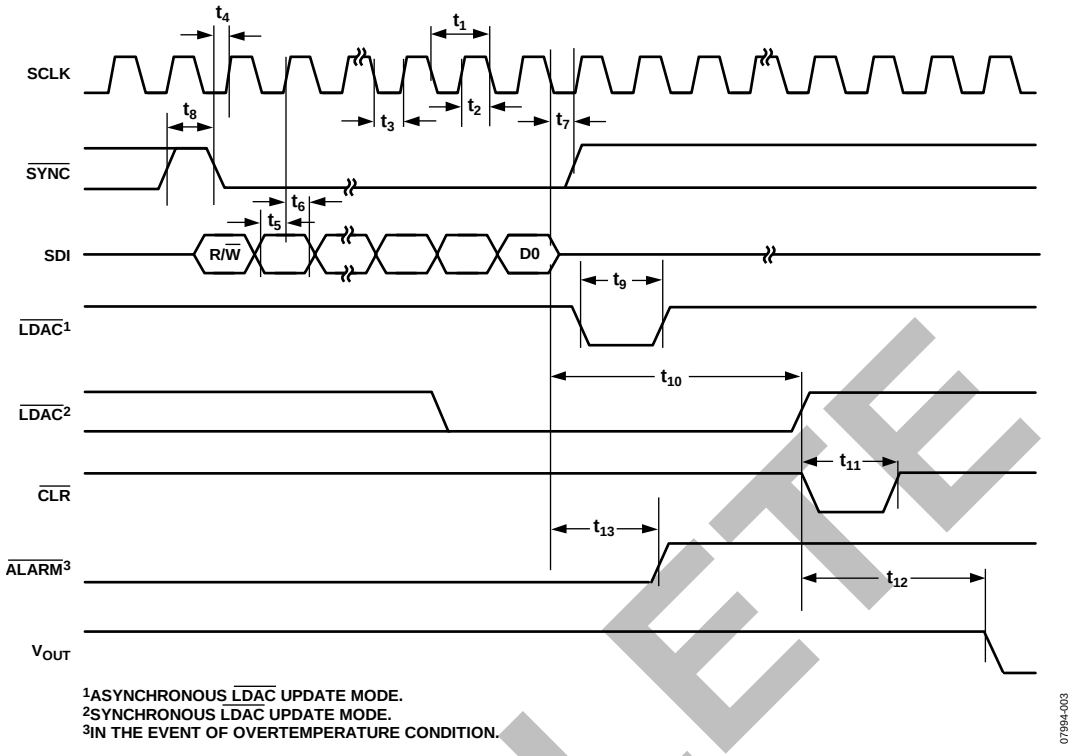

Figure 3. Write Timing Diagram

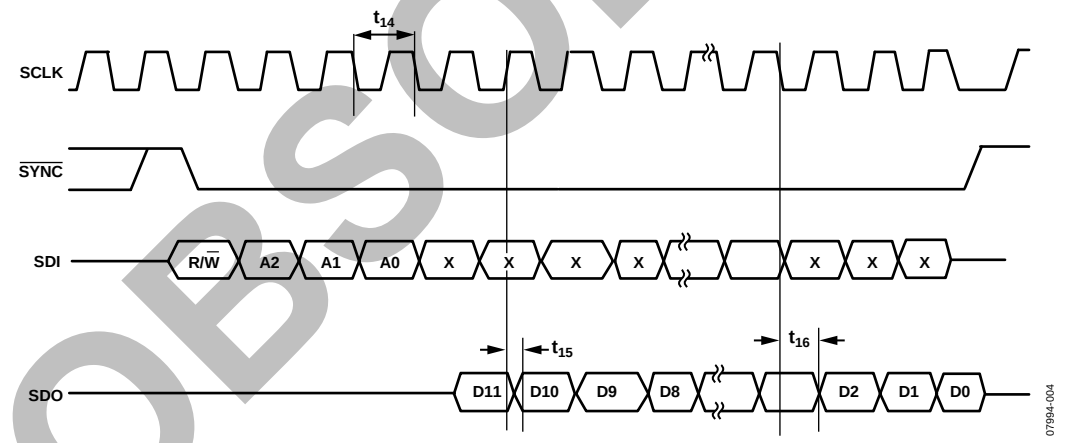

Figure 4. Read Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

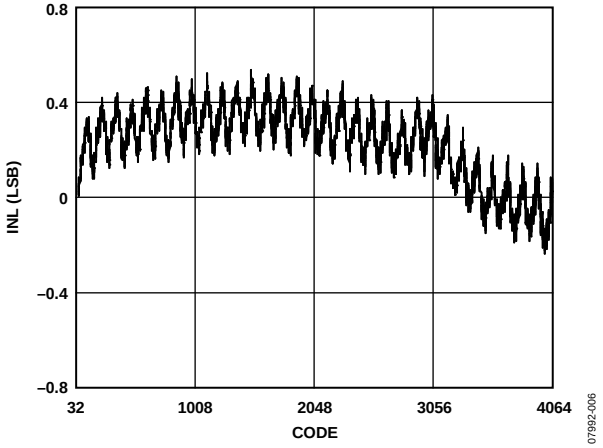

Figure 6. Typical INL

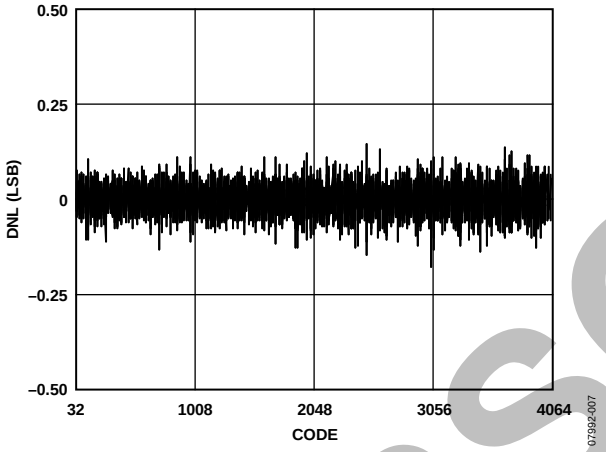

Figure 7. Typical DNL

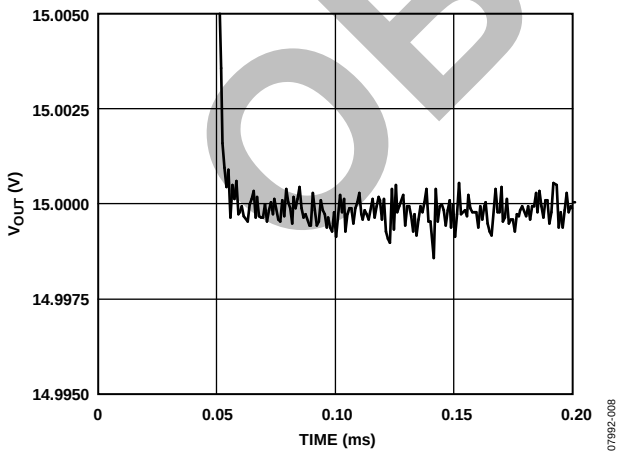

Figure 8. Output Settling Time (High to Low)

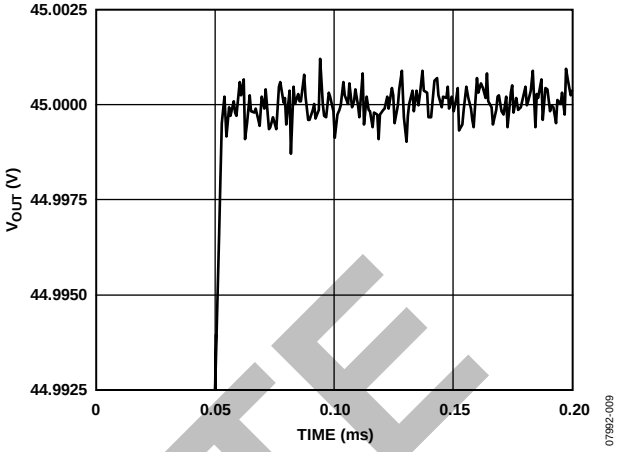

Figure 9. Output Settling Time (Low to High)

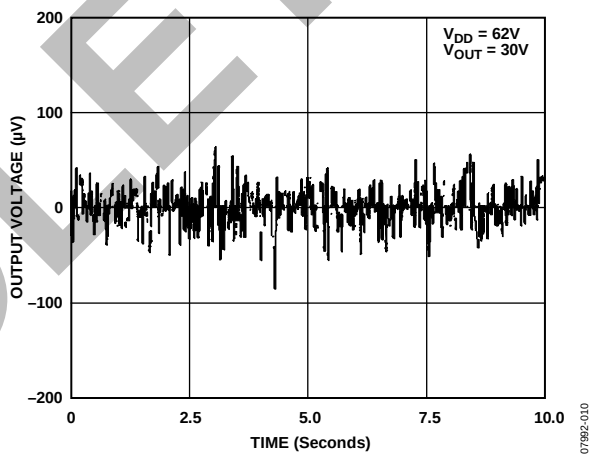

Figure 10. Output Noise

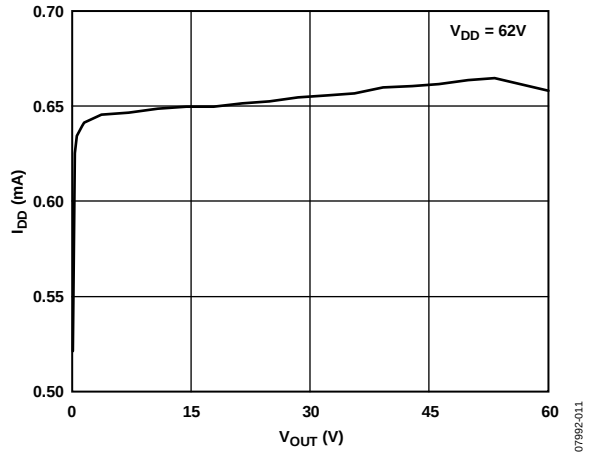

Figure 11. I_{DD} vs. V_{OUT}

SERIAL INTERFACE

The AD5501 has a serial interface (SYNC, SCLK, SDI, and SDO), which is compatible with SPI standards, as well as with most DSPs. The AD5501 allows writing of data, via the serial interface, to the input and control registers. The DAC register is not directly writeable or readable.

The input shift register is 16 bits wide (see Table 8). The 16-bit word consists of one read/write (R/W) control bit, followed by three address bits and 12 DAC data bits. Data is loaded MSB first.

WRITE MODE

To write to a register, the R/W bit should be 0. The three address bits in the input register (see Table 9) then determine the register to update. The address bits (A2 to A0) should be 001 to write to the DAC input register or 111 to write to the control register. Data is clocked into the selected register during the remaining 12 clocks of the same frame. Figure 3 shows a timing diagram of a typical AD5501 write sequence. The write sequence begins by bringing the SYNC line low. Data on the SDI line is clocked into the 16-bit shift register on the rising edge of SCLK. On the 16th falling clock edge, the last data bit is clocked in and the programmed function is executed (that is, a change in the selected DAC input register or a change in the mode of operation). The AD5501 does not require a continuous SCLK and dynamic power can be saved by transmitting clock pulses during a serial write only. At this stage, the SYNC line can be kept low or be brought high. In either case, it must be brought high for a minimum of 20 ns before the next write sequence for a falling edge of SYNC to initiate the next write sequence. Operate all interface pins close to the supply rails to minimize power consumption in the digital input buffers.

READ MODE

The AD5501 allows data readback via the serial interface from the DAC input register and the control register. To read back a register, it is first necessary to tell the AD5501 that a readback is required. This is achieved by setting the R/W bit to 1. The three address bits then determine the register from which data is to be read back. Data from the selected register is clocked out of the SDO pin on the next 12 clocks of the same frame.

The SDO pin is normally three-stated but becomes driven on the rising edge of the fifth clock pulse. The pin remains driven until the data from the register has been clocked out or the SYNC pin is returned high. Figure 4 shows the timing requirements during a read operation. Note that due to timing requirements of t_{14} (110 ns), the maximum speed of the SPI interface during a read operation should not exceed 9 MHz.

WRITING TO THE CONTROL REGISTER

The control register is written when Bits[DB14:DB12] are 1. The control register sets the power-up state of the DAC output. A write to the control register must be followed by another write operation. The second write operation can be a write to a DAC input register or a NOP write. Figure 17 shows some typical combinations.

Table 8. Input Register Bit Map

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
R/W	A2	A1	A0	Data											

Table 9. Input Register Bit Functions

Bit	Description			
R/W	Indicates a read from or a write to the addressed register.			
A2, A1, A0	These bits determine if the input register or the control register is to be accessed.			
	A2	**A1**	**A0**	**Function**
	0	0	0	NOP[1]
	0	0	1	DAC input register
	0	1	0	Reserved
	0	1	1	Reserved
	1	0	0	Reserved
	1	0	1	Reserved
	1	1	0	Reserved
	1	1	1	Control register
D11:D0	Data bits.			

[1] No operation command

Table 10. Control Register Functions Bit Map

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0[1]
R/$\overline{W}$	1	1	1	0	0	0	0	0	C6	C5	C4	C3	C2	C1	C0

[1] Read only bit. This bit should be 0 when writing to the control register

Table 11. Control Register Function Bit Descriptions

Bit No.	Bit Name	Description
DB0	C0	C0 = 0: the device is not in thermal shutdown mode. C0 = 1: the thermal shutdown mode is activated.
DB1	C1	C1 = 0: reserved. This bit should be 0 when writing to the control register.
DB2	C2	C2 = 0: DAC channel power-down (default). C2 = 1: DAC channel power-up.
DB[3:5]	C3 to C5	C3 to C5 = 0: reserved. These bits should be 0 when writing to the control register.
DB6	C6	C6 = 0: output connected to AGND through a 20 kΩ resistor. C6 = 1: output is three-stated (default).

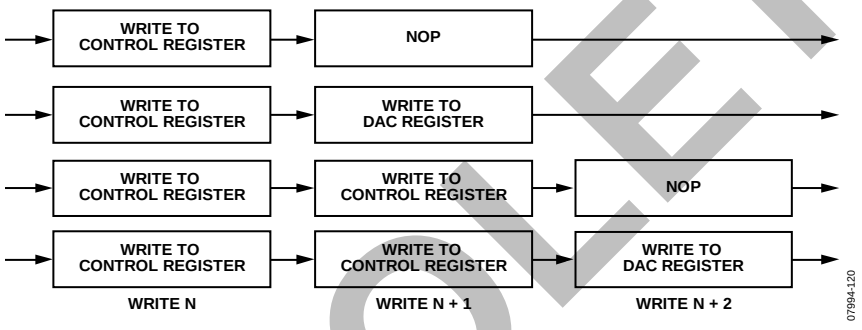

Figure 17. Control Register Write Sequences

INTERFACING EXAMPLES

The SPI interface of the AD5501 is designed to allow it to be easily connected to industry-standard DSPs and microcontrollers. Figure 18 shows how the AD5501 can be connected to the Analog Devices, Inc., Blackfin® DSP. The Blackfin has an integrated SPI port that can be connected directly to the SPI pins of the AD5501. Programmable input/output pins are also available and can be used to read or set the state of the digital input or output pins associated with the interface.

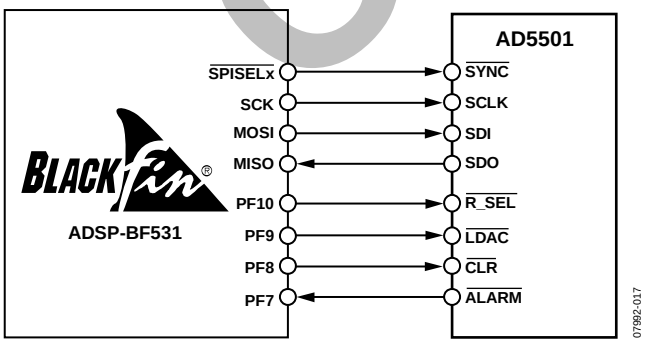

Figure 18. Interfacing to a Blackfin DSP

The Analog Devices ADSP-21065L is a floating point DSP with two serial ports (SPORTs). Figure 19 shows how one SPORT can be used to control the AD5501. In this example, the transmit frame synchronization (TFS) pin is connected to the receive frame synchronization (RFS) pin. The transmit and receive clocks (TCLK and RCLK) are also connected together. The user can write to the AD5501 by writing to the transmit register. When a read operation is performed, the data is clocked out of the AD5501 on the last 12 SCLKs. The DSP receive interrupt can be used to indicate when the read operation is complete.

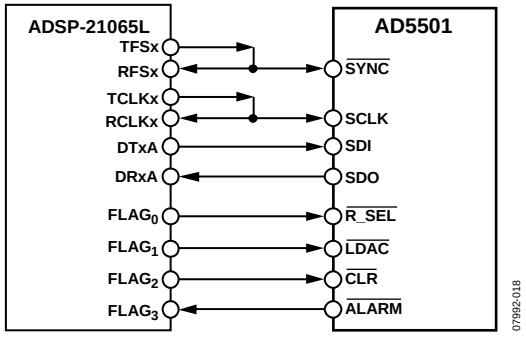

Figure 19. Interfacing to an ADSP-21065L DSP

OUTLINE DIMENSIONS

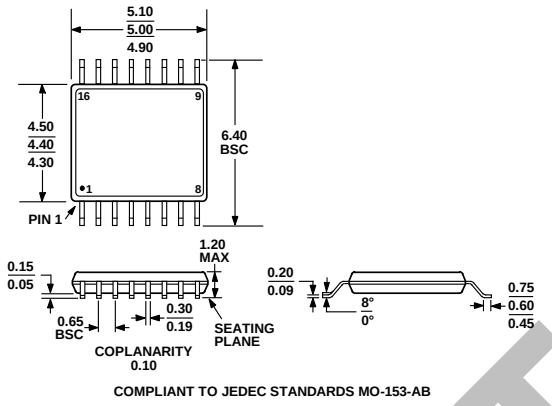

Figure 20. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5501BRUZ	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
AD5501BRUZ-REEL	−40°C to +105°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
EVAL-AD5501EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

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