12-Bit Successive Approximation
High Accuracy A/D Converters

AD5210 Series

FEATURES
True 12-Bit Operation: ±1/2LSB max Nonlinearity
Totally Adjustment-Free
Guaranteed No Missing Codes Over the Specified
Temperature Range
Hermetically-Sealed Package
Standard Temperature Range: -25°C to +85°C
Extended Temperature Range: -55°C to +125°C
Serial and Parallel Outputs
Monolithic DAC with Scaling Resistors for Stability
Low Chip Count for High Reliability
Industry Standard Pin Out
Small 24-Pin DIP

GENERAL DESCRIPTION
The AD52XX series devices are 12-bit successive approximation
analog-to-digital converters. The hybrid design utilizes MSI
digital, linear monolithic chips and active laser trimming of
high-stability thin-film resistors to provide a totally adjustment
free converter—no potentiometers are required for calibration.

The innovative design of the AD52XX series devices incorporates
a monolithic 12-bit feedback DAC for reduced chip
count and higher reliability. The exceptional temperature
coefficients of the monolithic DAC guarantees ±1/2LSB line-
arity over the entire operating temperature range of -25°C
to +85°C for the BD grade and -55°C to +125°C for the
TD grade.

The AD52XX series converters are available in 2 input voltage
ranges: ±5V (AD521X1) and ±10V (AD52X2/AD52X5).
The converters are available either complete with an internal
buried zener reference or with the option of an external
reference for improved absolute accuracy.

The AD52XX series converters are available in two per-
formance grades; the “B” is specified from -25°C to +85°C
and the “T” is specified from -55°C to +125°C. All units are
available in a 24-pin hermetically sealed ceramic DIP.

The Serial Output function is no longer supported on the
AD5212 after date code 9622.

The Serial Output function is no longer supported on the
AD5215 after date code 9618.

PRODUC'T HIGHLIGHTS
1. The AD52XX series devices are laser trimmed at the factory
to provide a totally adjustment free converter—no potenti-
ometers are required for 12-bit performance.
2. A monolithic 12-bit feedback DAC is used for reduced chip
count and higher reliability.
3. The AD52XX series directly replaces other devices of this
type with significant increases in performance.
4. The devices offer true 12-bit accuracy and exhibits no
missing codes over the entire operating temperature range.
5. The fast conversion rate of the AD5210 series makes it an
excellent choice for applications requiring high system
throughput rates.

REV. A

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# SPECIFICATIONS
(typical @ +25°C, ±15V and +5V unless otherwise noted)

<table>
<thead>
<tr>
<th>INPUT RANGE</th>
<th>INPUT IMPEDANCE</th>
<th>AD52X1B</th>
<th>AD52X1T</th>
<th>AD52X2B</th>
<th>AD52X2T</th>
<th>AD52X5B</th>
<th>AD52X5T</th>
</tr>
</thead>
<tbody>
<tr>
<td>-5V to +5V</td>
<td>5.0kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>-10V to +10V</td>
<td>10.0kΩ</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>REFERENCE</td>
<td>Internal</td>
<td>⋆</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>RESOLUTION</td>
<td>12 Bits</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
</tr>
<tr>
<td>LINEARITY ERROR, MAX</td>
<td>±1/2LSB</td>
<td></td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
</tr>
<tr>
<td>No Missing Codes T&lt;sub&gt;min&lt;/sub&gt; to T&lt;sub&gt;max&lt;/sub&gt;</td>
<td>Guaranteed</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
<td>⋆</td>
</tr>
<tr>
<td>ZERO ERROR, MAX</td>
<td>±1LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ZERO ERROR, MAX T&lt;sub&gt;min&lt;/sub&gt; to T&lt;sub&gt;max&lt;/sub&gt;</td>
<td>±2LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ABSOLUTE ACCURACY, MAX</td>
<td>±2LSB</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ABSOLUTE ACCURACY, MAX T&lt;sub&gt;min&lt;/sub&gt; to T&lt;sub&gt;max&lt;/sub&gt;</td>
<td>±0.4% of FSR&lt;sup&gt;2&lt;/sup&gt;</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>±0.1% of FSR&lt;sup&gt;2&lt;/sup&gt;</td>
</tr>
<tr>
<td>CONVERSION TIME, MAX</td>
<td>Clock = 1MHz (5210 Series)</td>
<td>13μs</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**LOGIC RATINGS**

Input Logic Commands
- Logic “0” 0.8V max
- Logic “1” +2.0V min
- Loading 0.5TTL Load

CLOCK INPUT PULSE WIDTH
100ns min

**OUTPUT LOGIC**

Logic “0” 0.4V max
Logic “1” 3.6V (2.4 min)

FANOUT - HIGH 8TTL Loads
FANOUT - LOW 2TTL Loads

**POWER SUPPLY REQUIREMENTS**

V<sub>LOGIC</sub> +5V ±10%
V<sub>CC</sub> +15V ±10%
V<sub>DD</sub> −15V ±10%

**OPERATING CURRENT**

V<sub>LOGIC</sub> 25mA (68mA max)
V<sub>CC</sub> 10mA (35mA max)
V<sub>DD</sub> 20mA (28mA max)
V<sub>REF</sub> 0.5mA

**POWER SUPPLY REJECTION**

V<sub>CC</sub> ±0.005%/%/max
V<sub>DD</sub> ±0.005%/%/max

**POWER CONSUMPTION**

575mW (1000mW max)

**OPERATING TEMPERATURE RANGE**

-25°C to +85°C
-55°C to +125°C

**NOTES**

* Same specifications as AD52X1/X2B.
** Same specifications as AD52X1/X2T.
*** Same specifications as AD52X5B.
1 Other input ranges are available, consult factory.
2 FSR is Full Scale Range and is equal to the peak to peak input signal.
Specifications subject to change without notice.
ABSOLUTE MAXIMUM RATINGS

- Storage Temperature: -65°C to +150°C
- Positive Supply: +18V
- Negative Supply: -18V
- Logic Supply: 0 to +7V
- Analog Input: ±25V
- Digital Outputs: Logic Supply
- Digital Inputs: +5.5V
- Reference Supply: -15V

*DIVIDER ADDED FOR EXTERNAL REFERENCE MODELS ONLY.

**Figure 1. Burn In Circuit**

**Figure 2. Pin Designations**

AD52XX SERIES ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model</th>
<th>Linearity</th>
<th>Absolute Accuracy</th>
<th>Temperature Range</th>
<th>Conversion Time</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD521**BD</td>
<td>1/2LSB</td>
<td>2LSB</td>
<td>-25°C to +85°C</td>
<td>13μs</td>
<td>DH-24C</td>
</tr>
<tr>
<td>AD521**1D</td>
<td>1/2LSB</td>
<td>2LSB</td>
<td>-55°C to +125°C</td>
<td>13μs</td>
<td>DH-24C</td>
</tr>
</tbody>
</table>

**Insert number according to desired input voltage range as shown in Table II.**

OUTLINE DIMENSIONS

24-Lead Side Brazed Ceramic DIP for Hybrid (DH-24C)

Dimensions shown in inches and (millimeters)

NOTES
1. INDEX AREA: A NOTCH OR A LEAD ONE IDENTIFICATION MARK IS LOCATED ADJACENT TO LEAD ONE.
2. DIMENSION SHALL BE MEASURED FROM THE SEATING PLANE TO THE BASE PLANE.
3. THE BASIC PIN SPACING IS 0.100" (2.54 mm) BETWEEN CENTERLINES.
4. APPLIES TO ALL FOUR CORNERS.
5. THE DIMENSION SHALL BE MEASURED AT THE CENTERLINE OF THE LEADS.
6. TWENTY TWO SPACES.
7. CONTROLLING DIMENSIONS ARE IN INCHES; MILLIMETER DIMENSIONS (IN PARENTHESES) ARE ROUNDED-OFF INCH EQUIVALENTS FOR REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.
THEORY OF OPERATION

On receipt of a CONVERT START command, the AD52XX converts the voltage as its analog input into an equivalent 12-bit binary number. This conversion is accomplished as follows: the 12-bit successive-approximation register (SAR) has its 12-bit outputs connected both to the device bit output pins and to the corresponding bit inputs of the feedback DAC. The analog input is successively compared to the feedback DAC output, one bit at a time (MSB first, LSB last). The decision to keep or reject each bit is then made at the completion of each bit comparison period, depending on the state of the comparator at that time.

TIMING

The timing diagram is shown in Figure 3. A conversion is initiated by holding the start convert low during a rising edge of the clock. The start convert transition must occur at a minimum of 25ns prior to the clock transition. The end of conversion (E.O.C.) signal will be set simultaneously with the initiation of conversion. The actual conversion will not start until the first rising edge of the clock after the start convert is again set high. At time t₀, B₁ is reset and B₂ – B₁₂ are set unconditionally. At t₁ the Bit 1 decision is made and Bit 2 is unconditionally reset. At t₂, the Bit 2 decision is made (keep) and Bit 3 is reset unconditionally. This sequence continues until the Bit 12 (LSB) decision (keep) is made at t₁₂. The STATUS flag is reset at time t₁₂ indicating that the conversion is complete and that the parallel output data is valid.

Corresponding serial and parallel data bits become valid on the same positive-going clock edge. Serial data does not change and is guaranteed valid on negative-going clock edges, however, serial data can be transferred quite simply by clocking it into a receiving shift register on these edges (see Figure 3). An external clock of 1MHz (AD5210) will yield 13μs conversion time. An external clock of 260kHz (AD5200) will yield 50μs conversion time.

The analog continuum is partitioned into $2^{12}$ discrete ranges for 12-bit conversion. All analog values within a given quantum are represented by the same digital code, usually assigned to the nominal midrange value. There is an inherent quantization uncertainty of ±1/2LSB, associated with the resolution, in addition to the actual conversion errors.

The actual conversion errors that are associated with A/D converters are combinations of analog errors due to the linear circuitry, matching and tracking properties of the ladder and scaling networks, reference error and power supply rejection. The matching and tracking errors in the converter have been minimized by the use of a monolithic DAC that includes the scaling network. The initial gain and offset errors have been internally trimmed to provide an absolute accuracy of ±0.05%.

Linearity error is defined as the deviation from a true straight line transfer characteristic from a zero analog input which calls for a zero digital output to a point which is defined as full scale. The linearity error is unadjustable and is the most meaningful indication of A/D converter accuracy. Differential nonlinearity is a measure of the deviation in the staircase step width between codes from the ideal least significant bit step size (Figure 4).

Monotonic behavior requires that the differential linearity error be less than 1LSB, however a monotonic converter can have missing codes; the AD52XX is specified as having no missing codes over the entire temperature range as specified on the data page.
There are three types of drift error over temperature: offset, gain and linearity. Offset drift causes a shift of the transfer characteristic left or right over the operating temperature range. Gain drift causes a rotation of the transfer characteristic about the zero or minus full scale point. The worst case accuracy drift is the summation of all three errors over temperature. Statistically, however, the drift error behaves as the root-sum-squared (RSS) and can be shown as:

$$\text{RSS} = \sqrt{\varepsilon_G^2 + \varepsilon_O^2 + \varepsilon_L^2}$$

$\varepsilon_G =$ Gain Drift Error (ppm/°C)

$\varepsilon_O =$ Offset Drift Error (ppm of FSR/°C)

$\varepsilon_L =$ Linearity Error (ppm of FSR/°C)

**Figure 4. Transfer Characteristics for an Ideal Bipolar A/D**

**GROUNDING**

Many data-acquisition components have two or more ground pins which are not connected together within the device. These "grounds" are usually referred to as the Digital Ground and Analog Ground (Analog Power Return). These grounds must be tied together at one point, usually at the system power-supply ground. Ideally, a single solid ground would be desirable. However, since current flows through the ground wires and etch stripes of the circuit cards, and since these paths have resistance and inductance, hundreds of millivolts can be generated between the system ground point and the ground pin of the AD52XX. Separate ground returns should be provided to minimize the current flow in the path from sensitive points to the system ground point. In this way supply currents and logic-gate return currents are not summed into the same return path as analog signals where they would cause measurement errors.

**Figure 5. Basic Grounding Practice**

Each of the AD52XX's supply terminals should be capacitively decoupled as close to the AD52XX as possible. A large value capacitor such as 1μF in parallel with 0.01μF capacitor is usually sufficient. Analog supplies are bypassed to the Analog Ground pin and the logic supply is bypassed to the Digital Ground pin.

**Figure 6. Power Supply Decoupling**

**SAMPLED DATA SYSTEMS**

The conversion speed of the AD52XX allows accurate digitization of high frequency signals and high throughput rates in multichannel data acquisition systems. To make the AD52XX capable of full benefit from this high speed, a fast sample-hold amplifier such as the AD346 or AD830-85 is required. Figures 7 and 8 show the use of an AD346 and AD830-85 as sample and holds in combination with the AD52XX.

**Figure 7. 66.6kHz–12 Bit, A/D Conversion System**

**Figure 8. 18.3kHz–12-Bit, A/D Conversion System**

In sampled data systems there are two limiting factors in digitizing high frequency signals. The maximum value of input signal frequency that can be acquired and digitized using a sample and hold amplifier and A/D converter combination is influenced by the bandwidth of the SHA, but it is also dictated by:

A. The aperture uncertainty (jitter) of the sample and hold amplifier.
B. The desired accuracy and corresponding resolution of the converter.

The resolution of an AD5210 is 1 part in 4096 to a tolerance of 0.012% of the full scale range, the maximum value of input signal frequency which can be digitized is determined by:

\[
F_{\text{MAX}} = \frac{2^{-N}}{(2\pi)(\text{Aperture Uncertainty})}
\]

\[
F_{\text{MAX/AD346}} = \frac{1}{(2\pi)(4096)(4 \times 10^{-10})} = 97.1\, \text{kHz}
\]

\[
F_{\text{MAX/ADSHC-85}} = \frac{1}{(2\pi)(4096)(5 \times 10^{-10})} = 77.7\, \text{kHz}
\]

The maximum throughput rate for each of these combinations is again different. The maximum throughput rate is the sum of the sample and hold acquisition time and A/D conversion time as shown in Figure 9.

Figure 9. START/E.O.C. Timing for Sampled Data System

When using an AD346 with an AD5212 the throughput rate is, 2.0μs acquisition time plus 13μs conversion time, 66.6kHz. To meet the requirements of the Nyquist sampling criteria, the AD346 and AD5210 combination can be used for input frequencies from dc through 33.3kHz; the ADSHC-85 and AD5210 combination for inputs from dc through 9.2kHz. Input frequencies higher than these (up to the maximum frequency) would result in "under-sampling" of the input signal. Signals up to the maximum frequency could be processed if their bandwidth is less than one-half the sample frequency.

A fast (32kHz) 12-bit DAS can be configured using the AD362 and the AD521X. The AD362 contains two 8-channel multiplexers, a differential amplifier, a sample-and-hold with high-speed output amplifier, a channel address latch and control logic. The multiplexers may be connected to the differential amplifier in either an 8-channel differential or 16-channel single-ended configuration. A feature of the AD362 is an internal user-controllable analog switch that connects the multiplexers in either a single-ended or differential mode. This allows a single device to perform in either mode without hardwire programming and permits a mixture of single-ended and differential sources to be interfaced by dynamically switching the input mode control.

CONVERT START USING A POSITIVE EDGE

In some systems it may be inconvenient to generate a negative going start convert pulse of the proper width. The circuit of Figure 11 can be used to start a conversion on the AD521X series of A/Ds with a positive going edge. To perform a conversion both the convert start signal and the E.O.C. must be low. The output of the inverter and nand gate will then be high in the high state. The converter will reset on the next rising clock edge. Resetting brings the E.O.C. to a high state; the inverter goes low; the convert start is still high so the output of the and gate goes high allowing the conversion to continue immediately. The convert start line has only to be brought back down before the conversion is complete.

**Table II.**

<table>
<thead>
<tr>
<th>Input Range</th>
<th>Speed</th>
<th>Internal Reference</th>
<th>External Reference</th>
</tr>
</thead>
<tbody>
<tr>
<td>-5V to +5V</td>
<td>13μs</td>
<td>AD5211</td>
<td>AD5214</td>
</tr>
<tr>
<td>-10V to +10V</td>
<td>13μs</td>
<td>AD5212</td>
<td>AD5215</td>
</tr>
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</table>

i.e., – the 13μs conversion time, ±10V input, external reference, extended temperature unit is the AD5215TD.
# Revision History

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<td>2/03—Data Sheet changed from REV. 0 to REV. A.</td>
<td>1</td>
</tr>
<tr>
<td>Added text to GENERAL DESCRIPTION</td>
<td>1</td>
</tr>
<tr>
<td>Updated OUTLINE DIMENSIONS</td>
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