1024-Position, Digital Potentiometer with Maximum ±1% R-Tolerance Error and 20-TP Memory

**Enhanced Product**

**AD5292-EP**

**FEATURES**
- Single-channel, 1024-position resolution
- 20 kΩ nominal resistance
- Maximum ±1% nominal resistor tolerance error (resistor performance mode)
- 20-times programmable wiper memory
- Rheostat mode temperature coefficient: 35 ppm/°C
- Voltage divider temperature coefficient: 5 ppm/°C
- +9 V to +33 V single-supply operation
- ±9 V to ±16.5 V dual-supply operation
- SPI-compatible serial interface
- Wiper setting readback
- Power-on refreshed from 20-TP memory

**ENHANCED PRODUCT FEATURES**
- Supports defense and aerospace applications (AQEC)
- Temperature range: −55°C to +125°C
- Controlled manufacturing baseline
- 1 assembly/test site
- 1 fabrication site
- Product change notification
- Qualification data available on request

**APPLICATIONS**
- Mechanical potentiometer replacement
- Instrumentation: gain and offset adjustment
- Programmable voltage-to-current conversion
- Programmable filters, delays, and time constants
- Programmable power supply
- Low resolution DAC replacement
- Sensor calibration

**GENERAL DESCRIPTION**

The AD5292-EP is a single-channel, 1024-position digital potentiometer that combines industry leading variable resistor performance with nonvolatile memory (NVM) in a compact package. This device is capable of operating across a wide voltage range, supporting both dual supply operation at ±10.5 V to ±16.5 V and single-supply operation at +21 V to +33 V, while ensuring less than 1% end-to-end resistor tolerance error and offering 20-time programmable (20-TP) memory.

The guaranteed industry leading low resistor tolerance error feature simplifies open-loop applications as well as precision calibration and tolerance matching applications.

The AD5292-EP device wiper settings are controllable through the SPI digital interface. Unlimited adjustments are allowed before programming the resistance value into the 20-TP memory. The AD5292-EP does not require any external voltage supply to facilitate fuse blow, and there are 20 opportunities for permanent programming. During 20-TP activation, a permanent blow fuse command freezes the wiper position (analogous to placing epoxy on a mechanical trimmer).

The AD5292-EP is available in a compact 14-lead TSSOP package. The part is guaranteed to operate over the extended industrial temperature range of −55°C to +125°C.

Additional application and technical information can be found in the AD5292 data sheet.

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1 The terms digital potentiometer and RDAC are used interchangeably.
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# REVISION HISTORY

4/2018—Rev. 0 to Rev. A
- Change to Enhanced Product Features Section .................................. 1
- Changes to Ordering Guide ............................................................. 15

9/2011—Revision 0: Initial Version
## SPECIFICATIONS

### ELECTRICAL CHARACTERISTICS—AD5292-EP

\( V_{\text{DD}} = 21 \text{ V to 33 V}, \ V_{\text{SS}} = 0 \text{ V}; \ V_{\text{DD}} = 10.5 \text{ V to 16.5 V}, \ V_{\text{SS}} = −10.5 \text{ V to } −16.5 \text{ V}; \ V_{\text{LOGIC}} = 2.7 \text{ V to 5.5 V}, \ V_A = V_{\text{DD}}, \ V_B = V_{\text{SS}}, −55°C < T_A < +125°C, \) unless otherwise noted.

### Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ1</th>
<th>Max</th>
<th>Unit</th>
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<tr>
<td><strong>DC CHARACTERISTICS—RHEOSTAT MODE</strong></td>
<td></td>
<td></td>
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<td></td>
</tr>
<tr>
<td>Resolution</td>
<td>N</td>
<td></td>
<td>10</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>Resistor Differential Nonlinearity</td>
<td>R-DNL</td>
<td>( R_{\text{RW}}, \ V_A = \text{NC} )</td>
<td>−1</td>
<td>+1</td>
<td></td>
<td>LSB</td>
</tr>
<tr>
<td>Resistor Integral Nonlinearity</td>
<td>R-INL</td>
<td>( R_{\text{RW}} = 20 \text{ k}\Omega, \</td>
<td>V_{\text{DD}} − V_{\text{SS}}</td>
<td>= 26 \text{ V to 33 V} )</td>
<td>−2</td>
<td>+2</td>
</tr>
<tr>
<td>Nominal Resistor Tolerance (R-Perf Mode)(^2)</td>
<td>( \Delta R_{\text{RW}}/R_{\text{AB}} )</td>
<td>See Table 2</td>
<td>−1</td>
<td>±0.5</td>
<td>+1</td>
<td>%</td>
</tr>
<tr>
<td>Nominal Resistor Tolerance (Normal Mode)(^3)</td>
<td>( \Delta R_{\text{RW}}/R_{\text{AB}} )</td>
<td></td>
<td>±7</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>Resistance Temperature Coefficient</td>
<td>( (\Delta R_{\text{RW}}/R_{\text{RW}}) \times 10^6 )</td>
<td>Code = full scale; see Figure 14</td>
<td>35</td>
<td></td>
<td></td>
<td>ppm/°C</td>
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<tr>
<td>Wiper Resistance</td>
<td>( R_w )</td>
<td>Code = zero scale</td>
<td>60</td>
<td>100</td>
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<td>Ω</td>
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<td><strong>DC CHARACTERISTICS—POTENTIOMETER DIVIDER MODE</strong></td>
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<td>Resolution</td>
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<td>10</td>
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<td></td>
<td>Bits</td>
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<td>Differential Nonlinearity</td>
<td>DNL</td>
<td></td>
<td>−1</td>
<td>+1</td>
<td></td>
<td>LSB</td>
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<tr>
<td>Integral Nonlinearity</td>
<td>INL</td>
<td></td>
<td>−2.5</td>
<td>+2.5</td>
<td></td>
<td>LSB</td>
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<tr>
<td>Voltage Divider Temperature Coefficient</td>
<td>( (\Delta V_{\text{DIV}}/V_{\text{DIV}}) \times 10^6 )</td>
<td>Code = half scale; see Figure 17</td>
<td>5</td>
<td></td>
<td></td>
<td>ppm/°C</td>
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<tr>
<td>Full-Scale Error</td>
<td>( V_{\text{WFSE}} )</td>
<td>Code = full scale</td>
<td>−8</td>
<td>+1</td>
<td></td>
<td>LSB</td>
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<tr>
<td>Zero-Scale Error</td>
<td>( V_{\text{WZSE}} )</td>
<td>Code = zero scale</td>
<td>0</td>
<td>10</td>
<td></td>
<td>LSB</td>
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<td>Terminal Voltage Range</td>
<td>( V_A, V_B, V_W )</td>
<td></td>
<td>( V_{\text{SS}} )</td>
<td>( V_{\text{DD}} )</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Capacitance A, Capacitance B</td>
<td>( C_A, C_B )</td>
<td>( f = 1 \text{ MHz}, ) measured to GND,</td>
<td>85</td>
<td></td>
<td></td>
<td>pF</td>
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<tr>
<td>Capacitance W(^4)</td>
<td>( C_W )</td>
<td>( f = 1 \text{ MHz}, ) measured to GND,</td>
<td>65</td>
<td></td>
<td></td>
<td>pF</td>
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<tr>
<td>Common-Mode Leakage Current(^4)</td>
<td>( I_{\text{CM}} )</td>
<td></td>
<td>−120</td>
<td>±1</td>
<td>120</td>
<td>nA</td>
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<td><strong>DIGITAL INPUTS</strong></td>
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<tr>
<td>Input Logic High(^4)</td>
<td>( V_{\text{IH}} )</td>
<td>JEDEC compliant</td>
<td>2.0</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>Input Logic Low(^4)</td>
<td>( V_{\text{IL}} )</td>
<td>( V_{\text{LOGIC}} = 2.7 \text{ V to 5.5 V} )</td>
<td>0.8</td>
<td></td>
<td></td>
<td>V</td>
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<tr>
<td>Input Current</td>
<td>( I_{\text{I}} )</td>
<td>( V_{\text{IN}} = 0 \text{ V or } V_{\text{LOGIC}} )</td>
<td>±1</td>
<td></td>
<td></td>
<td>µA</td>
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<tr>
<td>Input Capacitance(^4)</td>
<td>( C_{\text{IL}} )</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>pF</td>
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<td><strong>DIGITAL OUTPUTS (SDO and RDY)</strong></td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output High Voltage</td>
<td>( V_{\text{OH}} )</td>
<td>( R_{\text{PULL-UP}} = 2.2 \text{ k}\Omega to V_{\text{LOGIC}} )</td>
<td>( V_{\text{LOGIC}} − 0.4 )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Output Low Voltage</td>
<td>( V_{\text{OL}} )</td>
<td>( R_{\text{PULL-UP}} = 2.2 \text{ k}\Omega to V_{\text{LOGIC}} )</td>
<td>−1</td>
<td>+1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Three-State Leakage Current</td>
<td>( C_{\text{OL}} )</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>pF</td>
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<tr>
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<tr>
<td>Single-Supply Power Range</td>
<td>( V_{\text{DD}} )</td>
<td>( V_{\text{SS}} = 0 \text{ V} )</td>
<td>9</td>
<td>33</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Dual-Supply Power Range</td>
<td>( V_{\text{DD}}/V_{\text{SS}} )</td>
<td>( \pm 1 \text{ V} )</td>
<td>( \pm 16.5 \text{ V} )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Positive Supply Current</td>
<td>( I_{\text{D}} )</td>
<td>( V_{\text{DD}}/V_{\text{SS}} = \pm 16.5 \text{ V} )</td>
<td>0.1</td>
<td>2</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Negative Supply Current</td>
<td>( I_{\text{S}} )</td>
<td>( V_{\text{DD}}/V_{\text{SS}} = \pm 16.5 \text{ V} )</td>
<td>−2</td>
<td>−0.1</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>Logic Supply Range</td>
<td>( V_{\text{LOGIC}} )</td>
<td></td>
<td>2.7</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Logic Supply Current</td>
<td>( I_{\text{LOGIC}} )</td>
<td>( V_{\text{LOGIC}} = 5 \text{ V, } V_{\text{OH}} = 5 \text{ V or } V_{\text{IL}} = \text{GND} )</td>
<td>1</td>
<td>10</td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td>OTP Store Current(^4,7)</td>
<td>( I_{\text{LOGIC, PROG}} )</td>
<td>( V_{\text{IH}} = 5 \text{ V or } V_{\text{IL}} = \text{GND} )</td>
<td>25</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>OTP Read Current(^4,8)</td>
<td>( I_{\text{LOGIC, FUSE_READ}} )</td>
<td>( V_{\text{IH}} = 5 \text{ V or } V_{\text{IL}} = \text{GND} )</td>
<td>25</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td>Power Dissipation(^9)</td>
<td>( P_{\text{DSS}} )</td>
<td>( V_{\text{SS}} = 5 \text{ V or } V_{\text{IL}} = \text{GND} )</td>
<td>8</td>
<td>110</td>
<td></td>
<td>µW</td>
</tr>
<tr>
<td>Power Supply Rejection Ratio</td>
<td>( \text{PSRR} )</td>
<td>( \Delta V_{\text{DD}}/\Delta V_{\text{SS}} = \pm 15 \text{ V} ± 10% )</td>
<td>0.103</td>
<td></td>
<td></td>
<td>%/%</td>
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</table>

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### Dynamic Characteristics

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Bandwidth</td>
<td>BW</td>
<td>−3 dB</td>
<td>520</td>
<td></td>
<td></td>
<td>kHz</td>
</tr>
<tr>
<td>THD&lt;sub&gt;W&lt;/sub&gt;</td>
<td>THDW</td>
<td>V&lt;sub&gt;A&lt;/sub&gt; = 1 V rms, V&lt;sub&gt;B&lt;/sub&gt; = 0 V, f = 1 kHz</td>
<td>−93</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>VW Settling Time</td>
<td>t&lt;sub&gt;s&lt;/sub&gt;</td>
<td>V&lt;sub&gt;A&lt;/sub&gt; = 30 V, V&lt;sub&gt;B&lt;/sub&gt; = 0 V, ±0.5 LSB error, board capacitance = 170 pF</td>
<td>750</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Code = full-scale, normal mode</td>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Code = full-scale, R-Perf mode</td>
<td></td>
<td></td>
<td></td>
<td>2.5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Code = half-scale, normal mode</td>
<td></td>
<td></td>
<td></td>
<td>5</td>
<td></td>
<td>µs</td>
</tr>
<tr>
<td>Code = half-scale, R-Perf mode</td>
<td></td>
<td></td>
<td></td>
<td>10</td>
<td></td>
<td>nV/√Hz</td>
</tr>
</tbody>
</table>

1. Typical values represent average readings at 25°C, V<sub>DD</sub> = 15 V, V<sub>SS</sub> = −15 V, and V<sub>LOGIC</sub> = 5 V.
2. Resistor position nonlinearity error. R-InL is the deviation from an ideal value measured between R<sub>WB</sub> at Code 0x008 and Code 0x3FF or between R<sub>WA</sub> at Code 0x3F3 and Code 0x000. R-DNL measures the relative step change from ideal between successive tap positions. The specification is guaranteed in resistor performance mode, with a wiper current of 1 mA for V<sub>A</sub> < 12 V and 1.2 mA for V<sub>A</sub> ≥ 12 V.
3. Resistor performance mode. The terms resistor performance mode and R-Perf mode are used interchangeably.
4. Guaranteed by design and characterization, not subject to production test.
5. INL and DNL are measured at VW with the RDAC configured as a potentiometer divider similar to a voltage output DAC. V<sub>A</sub> = V<sub>DD</sub> and V<sub>B</sub> = 0 V. DNL specification limits of ±1 LSB maximum are guaranteed monotonic operating conditions.
6. Resistor Terminal A, Resistor Terminal B, and Resistor Terminal W have no limitations on polarity with respect to each other. Dual-supply operation enables ground-referenced bipolar signal adjustment.
7. Different from operating current; supply current for fuse program lasts approximately 550 µs.
8. Different from operating current; supply current for fuse read lasts approximately 550 µs.
9. P<sub>DIS</sub> is calculated from (I<sub>OD</sub> × V<sub>OD</sub>) + (I<sub>SS</sub> × V<sub>SS</sub>) + (I<sub>LOGIC</sub> × V<sub>LOGIC</sub>).
10. All dynamic characteristics use V<sub>DD</sub> = 15 V, V<sub>SS</sub> = −15 V, and V<sub>LOGIC</sub> = 5 V.

### Resistor Performance Mode Code Range

Table 2.

<table>
<thead>
<tr>
<th>Resistor Tolerance per Code</th>
<th></th>
<th></th>
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</thead>
<tbody>
<tr>
<td></td>
<td>R&lt;sub&gt;WB&lt;/sub&gt;</td>
<td>R&lt;sub&gt;WA&lt;/sub&gt;</td>
<td>R&lt;sub&gt;RB&lt;/sub&gt;</td>
<td>R&lt;sub&gt;R&lt;/sub&gt;</td>
<td>R&lt;sub&gt;WA&lt;/sub&gt;</td>
<td>R&lt;sub&gt;WB&lt;/sub&gt;</td>
<td>R&lt;sub&gt;WA&lt;/sub&gt;</td>
</tr>
<tr>
<td>1% R-Tolerance</td>
<td>From 0x1EF to 0x3FF</td>
<td>From 0x000 to 0x210</td>
<td>From 0x1F4 to 0x3FF</td>
<td>From 0x000 to 0x20B</td>
<td>From 0x1F4 to 0x3FF</td>
<td>From 0x000 to 0x20B</td>
<td>N/A</td>
</tr>
<tr>
<td>2% R-Tolerance</td>
<td>From 0x0C3 to 0x3FF</td>
<td>From 0x000 to 0x33C</td>
<td>From 0x0E6 to 0x3FF</td>
<td>From 0x000 to 0x319</td>
<td>From 0x131 to 0x3FF</td>
<td>From 0x000 to 0x2CE</td>
<td>From 0x000 to 0x33C</td>
</tr>
<tr>
<td>3% R-Tolerance</td>
<td>From 0x073 to 0x3FF</td>
<td>From 0x000 to 0x38C</td>
<td>From 0x087 to 0x3FF</td>
<td>From 0x000 to 0x378</td>
<td>From 0x0AF to 0x3FF</td>
<td>From 0x000 to 0x350</td>
<td>N/A</td>
</tr>
</tbody>
</table>

For −55°C < T<sub>A</sub> < +125°C
INTERFACE TIMING SPECIFICATIONS

\( V_{DD}/V_{SS} = \pm 15 \text{ V}, \ V_{LOGIC} = 2.7 \text{ V to 5.5 V}, -55^\circ C < T_A < +125^\circ C. \) All specifications \( T_{\text{MIN}} \) to \( T_{\text{MAX}} \), unless otherwise noted.

Table 3.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Limit(^1)</th>
<th>Unit</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_1 )</td>
<td>20 ns min</td>
<td>SCLK cycle time</td>
<td></td>
</tr>
<tr>
<td>( t_2 )</td>
<td>10 ns min</td>
<td>SCLK high time</td>
<td></td>
</tr>
<tr>
<td>( t_3 )</td>
<td>10 ns min</td>
<td>SCLK low time</td>
<td></td>
</tr>
<tr>
<td>( t_4 )</td>
<td>10 ns min</td>
<td>SYNC to SCLK falling edge setup time</td>
<td></td>
</tr>
<tr>
<td>( t_5 )</td>
<td>5 ns min</td>
<td>Data setup time</td>
<td></td>
</tr>
<tr>
<td>( t_6 )</td>
<td>5 ns min</td>
<td>Data hold time</td>
<td></td>
</tr>
<tr>
<td>( t_7 )</td>
<td>1 ns min</td>
<td>SCLK falling edge to SYNC rising edge</td>
<td></td>
</tr>
<tr>
<td>( t_8 )</td>
<td>400 ns (^3)</td>
<td>ns min</td>
<td>Minimum SYNC high time</td>
</tr>
<tr>
<td>( t_9 )</td>
<td>14 ns min</td>
<td>SYNC rising edge to next SCLK fall ignore</td>
<td></td>
</tr>
<tr>
<td>( t_{10} )</td>
<td>1 ns min</td>
<td>RDY rising edge to SYNC falling edge</td>
<td></td>
</tr>
<tr>
<td>( t_{11} )</td>
<td>40 ns max</td>
<td>SYNC rising edge to RDY fall time</td>
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<tr>
<td>( t_{12} )</td>
<td>2.4 ( \mu \text{S} ) max</td>
<td>RDY low time, RDAC register write command execute time (R-Perf mode)</td>
<td></td>
</tr>
<tr>
<td>( t_{12} )</td>
<td>410 ns max</td>
<td>RDY low time, RDAC register write command execute time (normal mode)</td>
<td></td>
</tr>
<tr>
<td>( t_{13} )</td>
<td>8 ms max</td>
<td>RDY low time, memory program execute time</td>
<td></td>
</tr>
<tr>
<td>( t_{14} )</td>
<td>1.5 ms min</td>
<td>Software/hardware reset</td>
<td></td>
</tr>
<tr>
<td>( t_{15} )</td>
<td>450 ns max</td>
<td>RDY low time, RDAC register readback execute time</td>
<td></td>
</tr>
<tr>
<td>( t_{16} )</td>
<td>1.3 ms max</td>
<td>RDY low time, memory readback execute time</td>
<td></td>
</tr>
<tr>
<td>( t_{17} )</td>
<td>450 ns max</td>
<td>SCLK rising edge to SDO valid</td>
<td></td>
</tr>
<tr>
<td>( \text{RESET} )</td>
<td>20 ns min</td>
<td>Minimum ( \text{RESET} ) pulse width (asynchronous)</td>
<td></td>
</tr>
<tr>
<td>( \text{POWER-UP} )(^5)</td>
<td>2 ms max</td>
<td>Power-on OTP restore time</td>
<td></td>
</tr>
</tbody>
</table>

\(^1\) All input signals are specified with \( t_R = t_F = 1 \text{ ns}/\sqrt{V}\) (10% to 90% of \( V_{DD} \)) and timed from a voltage level of \((V_{IL} + V_{IH})/2\).

\(^3\) Maximum SCLK frequency is 50 MHz.

\(^4\) Refer to \( t_5 \) and \( t_6 \) for RDAC register and memory commands operations.

\(^5\) Maximum time after \( V_{LOGIC} \) is equal to 2.5 V.
Timing Diagrams

Figure 3. Write Timing Diagram, CPOL = 0, CPHA = 1

Figure 4. Read Timing Diagram, CPOL = 0, CPHA = 1
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ C$, unless otherwise noted.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DD}$ to GND</td>
<td>$-0.3$ V to $+35$ V</td>
</tr>
<tr>
<td>$V_{SS}$ to GND</td>
<td>$+0.3$ V to $-25$ V</td>
</tr>
<tr>
<td>$V_{LOGIC}$ to GND</td>
<td>$-0.3$ V to $+7$ V</td>
</tr>
<tr>
<td>$V_{DD}$ to $V_{SS}$</td>
<td>$35$ V</td>
</tr>
<tr>
<td>$V_A$, $V_B$, $V_W$ to GND</td>
<td>$V_{SS} - 0.3$ V, $V_{DD} + 0.3$ V</td>
</tr>
<tr>
<td>Digital Input and Output Voltage to GND</td>
<td>$-0.3$ V to $V_{LOGIC} + 0.3$ V</td>
</tr>
<tr>
<td>$V_{EXT_CAP}$ Voltage to GND</td>
<td>$-0.3$ V to $+7$ V</td>
</tr>
<tr>
<td>$I_A$, $I_B$, $I_W$</td>
<td>$\pm 3$ mA</td>
</tr>
<tr>
<td>Continuous</td>
<td>$\pm 3/d_2$</td>
</tr>
<tr>
<td>Pulsed$^1$</td>
<td>$\pm 3/\sqrt{d_2}$</td>
</tr>
</tbody>
</table>

Operating Temperature Range$^3$

- $-55^\circ C$ to $+125^\circ C$
- $-65^\circ C$ to $+150^\circ C$

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

$\theta_J$ is defined by JEDEC specification JESD-51 and the value is dependent on the test board and test environment.

<table>
<thead>
<tr>
<th>Package Type</th>
<th>$\theta_J$</th>
<th>$\theta_J$</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>14-Lead TSSOP</td>
<td>93$^1$</td>
<td>20</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

$^1$ JEDEC 2S2P test board, still air (0 m/sec to 1 m/sec air flow).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

$^1$ Maximum terminal current is bounded by the maximum current handling of the switches, maximum power dissipation of the package, and maximum applied voltage across any two of the A, B, and W terminals at a given resistance.

$^2$ Pulse duty factor.

$^3$ Includes programming of OTP memory.
### Pin Configuration and Function Descriptions

![AD5292-EP Top View](top_view.png)

#### Table 6. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>RESET</td>
<td>Hardware Reset Pin. Refreshes the RDAC register with the contents of the 20-TP memory register. Factory default loads midscale until the first 20-TP wiper memory location is programmed. RESET is activated at the logic high transition. Tie RESET to VLOGIC if not used.</td>
</tr>
<tr>
<td>2</td>
<td>VSS</td>
<td>Negative Supply. Connect to 0 V for single-supply applications. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.</td>
</tr>
<tr>
<td>3</td>
<td>A</td>
<td>Terminal A of RDAC. VSS ≤ VA ≤ VDD.</td>
</tr>
<tr>
<td>4</td>
<td>W</td>
<td>Wiper Terminal of RDAC. VSS ≤ VW ≤ VDD.</td>
</tr>
<tr>
<td>5</td>
<td>B</td>
<td>Terminal B of RDAC. VSS ≤ VB ≤ VDD.</td>
</tr>
<tr>
<td>6</td>
<td>VDD</td>
<td>Positive Power Supply. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.</td>
</tr>
<tr>
<td>7</td>
<td>EXT_CAP</td>
<td>External Capacitor. Connect a 1 μF capacitor to EXT_CAP. This capacitor must have a voltage rating of ≥7 V.</td>
</tr>
<tr>
<td>8</td>
<td>VLOGIC</td>
<td>Logic Power Supply; 2.7 V to 5.5 V. This pin should be decoupled with 0.1 μF ceramic capacitors and 10 μF capacitors.</td>
</tr>
<tr>
<td>9</td>
<td>GND</td>
<td>Ground Pin, Logic Ground Reference.</td>
</tr>
<tr>
<td>10</td>
<td>DIN</td>
<td>Serial Data Input. The AD5292-EP has a 16-bit shift register. Data is clocked into the register on the falling edge of the serial clock input.</td>
</tr>
<tr>
<td>11</td>
<td>SCLK</td>
<td>Serial Clock Input. Data is clocked into the shift register on the falling edge of the serial clock input. Data can be transferred at rates up to 50 MHz.</td>
</tr>
<tr>
<td>12</td>
<td>SYNC</td>
<td>Falling Edge Synchronization Signal. This is the frame synchronization signal for the input data. When SYNC goes low, it enables the shift register and data is transferred in on the falling edges of the following clocks. The selected register is updated on the rising edge of SYNC following the 16th clock cycle. If SYNC is taken high before the 16th clock cycle, the rising edge of SYNC acts as an interrupt, and the write sequence is ignored by the DAC.</td>
</tr>
<tr>
<td>13</td>
<td>SDO</td>
<td>Serial Data Output. This open-drain output requires an external pull-up resistor. SDO can be used to clock data from the shift register in daisy-chain mode or in readback mode.</td>
</tr>
<tr>
<td>14</td>
<td>RDY</td>
<td>Ready Pin. This active-high open-drain output identifies the completion of a write or read operation to or from the RDAC register or memory.</td>
</tr>
</tbody>
</table>
**TYPICAL PERFORMANCE CHARACTERISTICS**

- **Figure 6. R-INL in R-Perf Mode vs. Code**
- **Figure 7. INL in R-Perf Mode vs. Code**
- **Figure 8. R-INL in Normal Mode vs. Code**
- **Figure 9. R-DNL in R-Perf Mode vs. Code**
- **Figure 10. DNL in R-Perf Mode vs. Code**
- **Figure 11. R-DNL in Normal Mode vs. Code**
Figure 18. 20 kΩ Gain vs. Frequency vs. Code

Figure 19. THD + Noise vs. Frequency

Figure 20. Bandwidth vs. Code vs. Net Capacitance

Figure 21. Power Supply Rejection Ratio vs. Frequency

Figure 22. THD + Noise vs. Amplitude

Figure 23. IDD Waveform While Blowing/Reading Fuse
Figure 24. Large-Signal Settling Time from Code Zero Scale

Figure 25. Theoretical Maximum Current vs. Code

Figure 26. Maximum Transition Glitch

Figure 27. Digital Feedthrough

Figure 28. VEXT_CAP Waveform While Reading Fuse Or Calibration

Figure 29. VEXT_CAP Waveform While Writing Fuse
Figure 30. Code Range > 1% R-Tolerance Error vs. Temperature

Figure 31. Code Range > 1% R-Tolerance Error vs. Voltage
TEST CIRCUITS

Figure 32 to Figure 37 define the test conditions used in the Specifications section.

Figure 32. Resistor Position Nonlinearity Error (Rheostat Operation; R-INL, R-DNL)

Figure 33. Potentiometer Divider Nonlinearity Error (INL, DNL)

Figure 34. Wiper Resistance

Figure 35. Power Supply Sensitivity (PSS, PSRR)

Figure 36. Gain vs. Frequency

Figure 37. Common-Mode Leakage Current
OUTLINE DIMENSIONS

Figure 38. 14-Lead Thin Shrink Small Outline Package [TSSOP] (RU-14)
Dimensions shown in millimeters

ORDERING GUIDE

<table>
<thead>
<tr>
<th>Model†</th>
<th>( R_{\text{ab}} ) (kΩ)</th>
<th>Resolution</th>
<th>Memory</th>
<th>Temperature Range</th>
<th>Package Description</th>
<th>Package Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>AD5292SRU-20-EP</td>
<td>20</td>
<td>1024</td>
<td>20-TP</td>
<td>−55°C to +125°C</td>
<td>14-Lead TSSOP</td>
<td>RU-14</td>
</tr>
<tr>
<td>AD5292SRUZ-20-EP</td>
<td>20</td>
<td>1024</td>
<td>20-TP</td>
<td>−55°C to +125°C</td>
<td>14-Lead TSSOP</td>
<td>RU-14</td>
</tr>
</tbody>
</table>

† Z = RoHS Compliant Part.