FEATURES
Throughput: 2 MSPS maximum
INL: ±0.4 LSB maximum
Guaranteed 16-bit no missing codes
Low power
9.5 mW at 2 MSPS (VDD only)
80 μW at 10 kSPS
16 mW at 2 MSPS (total)
SNR
96.2 dB typical at 1 kHz
95.5 dB typical at 100 kHz
THD
−123 dB typical at 1 kHz
−99 dB typical at 100 kHz
Ease of use features reduce system power and complexity
Input overvoltage clamp circuit
Reduced nonlinear input charge kickback
High-Z mode
Long acquisition phase
Input span compression
Fast conversion time allows low SPI clock rates
SPI-programmable modes, read/write capability, status word
Differential analog input range: ±VREF
0 V to VREF with VREF between 2.4 V to 5.1 V
Single 1.8 V supply operation with 1.71 V to 5.5 V logic interface
SAR architecture: no latency/pipeline delay
Guaranteed operation: −40°C to 125°C
Serial interface SPI-/QSPI-/MICROWIRE-/DSP-compatible
Ability to daisy-chain multiple ADCs and busy indicator
10-lead, 3 mm × 3 mm LFCSP and 10-lead, 3 mm × 4.90 mm MSOP
APPLICATIONS
Automatic test equipment
Machine automation
Medical equipment
Battery-powered equipment
Precision data acquisition systems

GENERAL DESCRIPTION
The AD4001 is a low noise, low power, high speed, 16-bit, 2 MSPS, precision successive approximation register (SAR) analog-to-digital converter (ADC). It incorporates ease of use features that lower the signal chain power, reduce signal chain complexity, and enable higher channel density. The high-Z mode, coupled with a long acquisition phase, eliminates the need for a dedicated high power, high speed ADC driver, thus broadening the range of low power precision amplifiers that can drive this ADC directly, while still achieving optimum performance. The input span compression feature enables the ADC driver amplifier and the ADC to operate off common supply rails without the need for a negative supply while preserving the full ADC code range. The low serial peripheral interface (SPI) clock rate requirement reduces the digital input/output power consumption, broadens processor options, and simplifies the task of sending data across digital isolation.

Operating from a 1.8 V supply, the AD4001 has a ±VREF fully differential input range with VREF ranging from 2.4 V to 5.1 V. The AD4001 consumes only 16 mW at 2 MSPS with a minimum SCK rate of 70 MHz in turbo mode and achieves ±0.4 LSB integral nonlinearity error (INL) maximum, guaranteed no missing codes at 16 bits with 96.2 dB typical signal-to-noise ratio (SNR). The reference voltage is applied externally and can be set independently of the supply voltage.

The SPI-compatible, versatile serial interface features seven different modes including the ability, using the SDI input, to daisy-chain several ADCs on a single 3-wire bus and provides an optional busy indicator. The AD4001 is compatible with 1.8 V, 2.5 V, 3 V, and 5 V logic, using the separate VIO supply.

The AD4001 is available in a 10-lead MSOP or a 10-lead LFCSP with operation specified from −40°C to +125°C. The device is pin compatible with the AD4003 18-bit, 2 MSPS, precision SAR differential ADC.
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## REVISION HISTORY

1/2017—Revision 0: Initial Version
SPECIFICATIONS

VDD = 1.71 V to 1.89 V, VIO = 1.71 V to 5.5 V, VREF = 5 V, all specifications T_MIN to T_MAX, high-Z mode disabled, span compression disabled, and turbo mode enabled (f_s = 2 MSPS), unless otherwise noted.

### Table 1.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RESOLUTION</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td>Bits</td>
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<tr>
<td>ANALOG INPUT</td>
<td></td>
<td>−V_REF</td>
<td>+V_REF</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Voltage Range</td>
<td>V_IN+ − V_IN−</td>
<td>−V_REF × 0.8</td>
<td>+V_REF × 0.8</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Operating Input Voltage</td>
<td>V_IN+, V_IN− to GND</td>
<td>0.1 × V_REF</td>
<td>0.9 × V_REF</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>Common-Mode Input Range</td>
<td>f_IN = 500 kHz</td>
<td>V_REF/2 − 0.125</td>
<td>V_REF/2</td>
<td>V_REF/2 + 0.125</td>
<td>V</td>
</tr>
<tr>
<td>Common-Mode Rejection Ratio (CMRR)</td>
<td>Acquisition phase, T = 25°C</td>
<td>68</td>
<td>0.3</td>
<td>nA</td>
<td></td>
</tr>
<tr>
<td>Analog Input Current</td>
<td>High-Z mode enabled, converting dc input at 2 MSPS</td>
<td>1</td>
<td>µA</td>
<td></td>
<td></td>
</tr>
<tr>
<td>THRU...</td>
<td></td>
<td>500</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>Throughput Rate</td>
<td>f_IN = 1 kHz</td>
<td>0</td>
<td>2</td>
<td>MSPS</td>
<td></td>
</tr>
<tr>
<td>DC ACCURACY</td>
<td></td>
<td>16</td>
<td></td>
<td></td>
<td>Bits</td>
</tr>
<tr>
<td>No Missing Codes</td>
<td></td>
<td>−0.4</td>
<td>±0.2</td>
<td>+0.4</td>
<td>LSB</td>
</tr>
<tr>
<td>Integral Nonlinearity Error (INL)</td>
<td></td>
<td>−0.5</td>
<td>±0.2</td>
<td>+0.5</td>
<td>LSB</td>
</tr>
<tr>
<td>Differential Nonlinearity Error (DNL)</td>
<td></td>
<td>0.35</td>
<td></td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>Transition Noise</td>
<td></td>
<td>−1.5</td>
<td>±0.1</td>
<td>+1.5</td>
<td>LSB</td>
</tr>
<tr>
<td>Total Harmonic Distortion (THD)</td>
<td></td>
<td>−0.28</td>
<td>+0.28</td>
<td>ppm/°C</td>
<td></td>
</tr>
<tr>
<td>Total Harmonic Distortion (THD)</td>
<td></td>
<td>−16.5</td>
<td>±0.4</td>
<td>+16.5</td>
<td>LSB</td>
</tr>
<tr>
<td>Power Supply Sensitivity</td>
<td>VDD = 1.8 V ± 5%</td>
<td>0.25</td>
<td></td>
<td>LSB</td>
<td></td>
</tr>
<tr>
<td>1/f Noise</td>
<td></td>
<td>6</td>
<td></td>
<td></td>
<td>µV p-p</td>
</tr>
<tr>
<td>AC ACCURACY</td>
<td></td>
<td>96.3</td>
<td></td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>Dynamic Range</td>
<td></td>
<td>54</td>
<td></td>
<td></td>
<td>µV rms</td>
</tr>
<tr>
<td>f_IN = 1 kHz, −0.5 dBFS, V_REF = 5 V</td>
<td></td>
<td>95.6</td>
<td>96.2</td>
<td>95.5</td>
<td>96</td>
</tr>
<tr>
<td>SNR</td>
<td></td>
<td>92.1</td>
<td>93.2</td>
<td></td>
<td>dB</td>
</tr>
<tr>
<td>SFDR</td>
<td></td>
<td>92</td>
<td>118</td>
<td>−117</td>
<td>dB</td>
</tr>
<tr>
<td>THD</td>
<td></td>
<td>92</td>
<td>93</td>
<td></td>
<td>dB</td>
</tr>
</tbody>
</table>

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### AD4001 Data Sheet

#### Parameter Test Conditions/Comments

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{\text{IN}} = 100$ kHz, $-0.5$ dBFS, $V_{\text{REF}} = 5$ V</td>
<td>SNR</td>
<td>95.5</td>
<td>dB</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>THD</td>
<td>$-99$</td>
<td>dB</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SINAD</td>
<td>93.8</td>
<td>dB</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$f_{\text{IN}} = 400$ kHz, $-0.5$ dBFS, $V_{\text{REF}} = 5$ V</td>
<td>SNR</td>
<td>91</td>
<td>dB</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>THD</td>
<td>$-92$</td>
<td>dB</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>SINAD</td>
<td>89</td>
<td>dB</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$-3$ dB Input Bandwidth</td>
<td>Aperture Delay</td>
<td>1</td>
<td>ns</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Aperture Jitter</td>
<td>1</td>
<td>ps rms</td>
<td>ps rms</td>
<td></td>
</tr>
</tbody>
</table>

#### Reference

- **Voltage Range ($V_{\text{REF}}$)**: 2.4 V to 5.1 V
- **Current**: 2 MSPS, $V_{\text{REF}} = 5$ V

#### Overvoltage Clamp

- $I_{\text{IN+}}/I_{\text{IN-}}$: $V_{\text{REF}} = 5$ V
- $V_{\text{IN+}}/V_{\text{IN-}}$ at Maximum $I_{\text{IN+}}/I_{\text{IN-}}$: $V_{\text{REF}} = 5$ V
- $V_{\text{IN+}}/V_{\text{IN-}}$ Clamp On/Off Threshold: $V_{\text{REF}} = 5$ V
- Deactivation Time: 360 ns
- REF Current at Maximum $I_{\text{IN+}}/I_{\text{IN-}}$: $V_{\text{IN+}}/V_{\text{IN-}} > V_{\text{REF}}$

#### Digital Inputs

- **Logic Levels**
  - Input Low Voltage, $V_{\text{IL}}$: $V_{\text{IO}} > 2.7$ V
  - Input High Voltage, $V_{\text{IH}}$: $V_{\text{IO}} > 2.7$ V
- **Input Low Current, $I_{\text{IL}}$**: $-1$ µA to $1$ µA
- **Input High Current, $I_{\text{IH}}$**: $-1$ µA to $1$ µA
- **Input Pin Capacitance**: 6 pF

#### Digital Outputs

- **Data Format**: Serial 16 bits, twos complement
- **Pipeline Delay**: Conversion results available immediately after completed conversion
- **Output Low Voltage, $V_{\text{OL}}$**: $I_{\text{sink}} = 500$ µA
- **Output High Voltage, $V_{\text{OH}}$**: $I_{\text{source}} = -500$ µA
- **Power Supplies**
  - **VDD**: 1.71 V to 1.89 V
  - **VIO**: 1.71 V to 5.5 V
- **Standby Current**: $V_{\text{DD}} = 1.8$ V, $V_{\text{IO}} = 1.8$ V, $T = 25^\circ$C
- **Power Dissipation**: 10 kSPS, high-Z mode disabled: 80 µW
  - 1 MSPS, high-Z mode disabled: 8 mW
  - 2 MSPS, high-Z mode disabled: 16 18.5 mW
  - 1 MSPS, high-Z mode enabled: 10 mW
  - 2 MSPS, high-Z mode enabled: 20 24.5 mW
- **Energy per Conversion**: 8 nJ/sample
Data Sheet AD4001

Parameter | Test Conditions/Comments | Min | Typ | Max | Unit
---|---|---|---|---|---
TEMPERATURE RANGE | Specified Performance | $T_{\text{MIN}}$ to $T_{\text{MAX}}$ | $-40$ | $+125$ | °C

1 The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS.

2 A throughput rate of 2 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 70 MHz. Refer to Table 4 for the maximum achievable throughput for different modes of operation.

3 Transient response is the time required for the ADC to acquire a full-scale input step to ±1 LSB accuracy.

4 The minimum and maximum values are guaranteed by characterization, not production tested.

5 See the 1/f noise plot in Figure 18.

TIMING SPECIFICATIONS

VDD = 1.71 V to 1.89 V, VIO = 1.71 V to 5.5 V, $V_{\text{REF}} = 5$ V, all specifications $T_{\text{MIN}}$ to $T_{\text{MAX}}$, high-Z mode disabled, span compression disabled, and turbo mode enabled ($f_{S} = 2$ MSPS), unless otherwise noted. See Figure 2 for the timing voltage levels.

Table 2. Digital Interface Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Conversion Time — CNV Rising Edge to Data Available</td>
<td>$t_{\text{CONV}}$</td>
<td>290</td>
<td>320</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Acquisition Phase</td>
<td>$t_{\text{ACQ}}$</td>
<td>290</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Time Between Conversions</td>
<td>$t_{\text{CYC}}$</td>
<td>500</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNV Pulse Width (CS Mode)</td>
<td>$t_{\text{CNW}}$</td>
<td>10</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Period (CS Mode)</td>
<td>$t_{\text{SCK}}$</td>
<td>9.8</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 2.7 V</td>
<td>12.3</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 1.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Period (Daisy-Chain Mode)</td>
<td>$t_{\text{SCK}}$</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 2.7 V</td>
<td>25</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 1.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Low Time</td>
<td>$t_{\text{SCKL}}$</td>
<td>3</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK High Time</td>
<td>$t_{\text{SCKH}}$</td>
<td>3</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Falling Edge to Data Remains Valid Delay</td>
<td>$t_{\text{HSDDO}}$</td>
<td>1.5</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Falling Edge to Data Valid Delay</td>
<td>$t_{\text{EN}}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 2.7 V</td>
<td>7.5</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 1.7 V</td>
<td>10.5</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNV or SDI Low to SDO D15 Most Significant Bit (MSB) Valid Delay (CS Mode)</td>
<td>$t_{\text{EDS}}$</td>
<td>20</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 2.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 1.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNV Rising Edge to First SCK Rising Edge Delay</td>
<td>$t_{\text{QUIET1}}$</td>
<td>190</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Last SCK Falling Edge to CNV Rising Edge Delay</td>
<td>$t_{\text{QUIET2}}$</td>
<td>60</td>
<td>ns</td>
<td></td>
<td></td>
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<tr>
<td>CNV or SDI High or Last SCK Falling Edge to SDO High Impedance (CS Mode)</td>
<td>$t_{\text{EHSDI}}$</td>
<td>2</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDI Valid Hold Time from CNV Rising Edge</td>
<td>$t_{\text{EHSDC}}$</td>
<td>2</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDI Valid Hold Time from CNV Rising Edge (Daisy-Chain Mode)</td>
<td>$t_{\text{EHSCNV}}$</td>
<td>12</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDI Valid Setup Time from SCK Rising Edge (Daisy-Chain Mode)</td>
<td>$t_{\text{EHSSC}}$</td>
<td>2</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDI Valid Hold Time from SCK Rising Edge (Daisy-Chain Mode)</td>
<td>$t_{\text{EHSSC}}$</td>
<td>2</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

1 The acquisition phase is the time available for the input sampling capacitors to acquire a new input with the ADC running at a throughput rate of 2 MSPS.

2 For turbo mode, $t_{\text{ACQ}}$ must match the $t_{\text{QUIET1}}$ minimum.

3 A throughput rate of 2 MSPS can only be achieved with turbo mode enabled and a minimum SCK rate of 70 MHz.

4 A 50% duty cycle is assumed for SCK.

5 See Figure 22 for SINAD vs. $t_{\text{QUIET2}}$.

Figure 2. Voltage Levels for Timing

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Table 3. Register Read/Write Timing

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
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<tbody>
<tr>
<td>READ/WRITE OPERATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNV Pulse Width(^1)</td>
<td>(t_{\text{CNVH}})</td>
<td>10</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SCK Period</td>
<td>(t_{\text{SCK}})</td>
<td>9.8</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>VIO &gt; 2.7 V</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 1.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Low Time</td>
<td>(t_{\text{SCKL}})</td>
<td>3</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SCK High Time</td>
<td>(t_{\text{SCKH}})</td>
<td>3</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>READ OPERATION</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNV Low to SDO D15 MSB Valid Delay</td>
<td>(t_{\text{EN}})</td>
<td></td>
<td>10</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>VIO &gt; 2.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 1.7 V</td>
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<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SCK Falling Edge to Data Remains Valid</td>
<td>(t_{\text{HSDO}})</td>
<td></td>
<td>1.5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>VIO &gt; 2.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 1.7 V</td>
<td></td>
<td></td>
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<td></td>
<td></td>
</tr>
<tr>
<td>SCK Falling Edge to Data Valid Delay</td>
<td>(t_{\text{VDDO}})</td>
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<td>7.5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>VIO &gt; 2.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIO &gt; 1.7 V</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CNV Rising Edge to SDO High Impedance</td>
<td>(t_{\text{DIS}})</td>
<td></td>
<td>10.5</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>WRITE OPERATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>SDI Valid Setup Time from SCK Rising Edge</td>
<td>(t_{\text{SSDISCK}})</td>
<td></td>
<td>2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>SDI Valid Hold Time from SCK Rising Edge</td>
<td>(t_{\text{HSDISCK}})</td>
<td></td>
<td>2</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CNV Rising Edge to SCK Edge Hold Time</td>
<td>(t_{\text{CNVSCK}})</td>
<td></td>
<td>0</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CNV Falling Edge to SCK Active Edge Setup Time</td>
<td>(t_{\text{CNVSCK}})</td>
<td></td>
<td>6</td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

\(^1\) For turbo mode, \(t_{\text{CNVH}}\) must match the \(t_{\text{QUIET1}}\) minimum.

Table 4. Achievable Throughput for Different Modes of Operation

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Test Conditions/Comments</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>THROUGHPUT, CS MODE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>3-Wire and 4-Wire Turbo Mode</td>
<td>(f_{\text{SCK}} = 100 \text{ MHz}, \text{VIO} \geq 2.7 \text{ V})</td>
<td>2</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
<tr>
<td>3-Wire and 4-Wire Turbo Mode</td>
<td>(f_{\text{SCK}} = 80 \text{ MHz}, \text{VIO} &lt; 2.7 \text{ V})</td>
<td>2</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
<tr>
<td>3-Wire and 4-Wire Turbo Mode and Six Status Bits</td>
<td>(f_{\text{SCK}} = 100 \text{ MHz}, \text{VIO} \geq 2.7 \text{ V})</td>
<td>2</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
<tr>
<td>3-Wire and 4-Wire Turbo Mode and Six Status Bits</td>
<td>(f_{\text{SCK}} = 80 \text{ MHz}, \text{VIO} &lt; 2.7 \text{ V})</td>
<td>1.86</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
<tr>
<td>3-Wire and 4-Wire Mode</td>
<td>(f_{\text{SCK}} = 100 \text{ MHz}, \text{VIO} \geq 2.7 \text{ V})</td>
<td>1.82</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
<tr>
<td>3-Wire and 4-Wire Mode</td>
<td>(f_{\text{SCK}} = 80 \text{ MHz}, \text{VIO} &lt; 2.7 \text{ V})</td>
<td>1.69</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
<tr>
<td>3-Wire and 4-Wire Mode and Six Status Bits</td>
<td>(f_{\text{SCK}} = 100 \text{ MHz}, \text{VIO} \geq 2.7 \text{ V})</td>
<td>1.64</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
<tr>
<td>3-Wire and 4-Wire Mode and Six Status Bits</td>
<td>(f_{\text{SCK}} = 80 \text{ MHz}, \text{VIO} &lt; 2.7 \text{ V})</td>
<td>1.5</td>
<td></td>
<td></td>
<td>MSPS</td>
</tr>
</tbody>
</table>
ABSOLUTE MAXIMUM RATINGS

Table 5.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Inputs</td>
<td></td>
</tr>
<tr>
<td>IN+, IN− to GND</td>
<td>−0.3 V to VREF + 0.4 V or ±50 mA</td>
</tr>
<tr>
<td>Supply Voltage</td>
<td></td>
</tr>
<tr>
<td>REF, VIO to GND</td>
<td>−0.3 V to +6.0 V</td>
</tr>
<tr>
<td>VDD to GND</td>
<td>−0.3 V to +2.1 V</td>
</tr>
<tr>
<td>VDD to VIO</td>
<td>−6 V to +2.4 V</td>
</tr>
<tr>
<td>Digital Inputs to GND</td>
<td>−0.3 V to VIO + 0.3 V</td>
</tr>
<tr>
<td>Digital Outputs to GND</td>
<td>−0.3 V to VIO + 0.3 V</td>
</tr>
<tr>
<td>Storage Temperature Range</td>
<td>−65°C to +150°C</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>150°C</td>
</tr>
<tr>
<td>Lead Temperature Soldering</td>
<td>260°C reflow as per JEDEC J-STD-020</td>
</tr>
<tr>
<td>ESD Ratings</td>
<td></td>
</tr>
<tr>
<td>Human Body Model</td>
<td>4 kV</td>
</tr>
<tr>
<td>Machine Model</td>
<td>200 V</td>
</tr>
<tr>
<td>Field-Induced Charged Device Model</td>
<td>1.25 kV</td>
</tr>
</tbody>
</table>

1 See the Analog Inputs section for an explanation of IN+ and IN−.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

Note that the clamp cannot sustain the overvoltage condition for an indefinite time.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

Table 6. Thermal Resistance

<table>
<thead>
<tr>
<th>Package Type</th>
<th>θJA</th>
<th>θJC</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>RM-101</td>
<td>147</td>
<td>38</td>
<td>°C/W</td>
</tr>
<tr>
<td>CP-10-91</td>
<td>114</td>
<td>33</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

1 Test Condition 1: thermal impedance simulated values are based upon use of 252P JEDEC PCB. See the Ordering Guide.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.
PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

Table 7. Pin Function Descriptions

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Mnemonic</th>
<th>Type</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>REF</td>
<td>AI</td>
<td>Reference Input Voltage. The $V_{REF}$ range is 2.4 V to 5.1 V. This pin is referred to the GND pin and must be decoupled closely to the GND pin with a 10 μF, X7R ceramic capacitor.</td>
</tr>
<tr>
<td>2</td>
<td>VDD</td>
<td>P</td>
<td>1.8 V Power Supply. The VDD range is 1.71 V to 1.89 V. Bypass VDD to GND with a 0.1 μF ceramic capacitor.</td>
</tr>
<tr>
<td>3</td>
<td>IN+</td>
<td>AI</td>
<td>Differential Positive Analog Input.</td>
</tr>
<tr>
<td>4</td>
<td>IN–</td>
<td>AI</td>
<td>Differential Negative Analog Input.</td>
</tr>
<tr>
<td>5</td>
<td>GND</td>
<td>P</td>
<td>Power Supply Ground.</td>
</tr>
<tr>
<td>6</td>
<td>CNV</td>
<td>DI</td>
<td>Convert Input. This input has multiple functions. On its leading edge, it initiates the conversions and selects the interface mode of the device: daisy-chain mode or CS mode. In CS mode, the SDO pin is enabled when CNV is low. In daisy-chain mode, the data is read when CNV is high.</td>
</tr>
<tr>
<td>7</td>
<td>SDO</td>
<td>DO</td>
<td>Serial Data Output. The conversion result is output on this pin. It is synchronized to SCK.</td>
</tr>
<tr>
<td>8</td>
<td>SCK</td>
<td>DI</td>
<td>Serial Data Clock Input. When the device is selected, the conversion result is shifted out by this clock.</td>
</tr>
<tr>
<td>9</td>
<td>SDI</td>
<td>DI</td>
<td>Serial Data Input. This input provides multiple features. It selects the interface mode of the ADC as follows: Daisy-Chain mode is selected if SDI is low during the CNV rising edge. In this mode, SDI is used as a data input to daisy-chain the conversion results of two or more ADCs onto a single SDO line. The digital data level on SDI is output on SDO with a delay of 16 SCK cycles. CS mode is selected if SDI is high during the CNV rising edge. In this mode, either SDI or CNV can enable the serial output signals when low. If SDI or CNV is low when the conversion is complete, the busy indicator feature is enabled. With CNV low, the device can be programmed by clocking in a 16-bit word on SDI on the rising edge of SCK.</td>
</tr>
<tr>
<td>10</td>
<td>VIO</td>
<td>P</td>
<td>Input/Output Interface Digital Power. Nominally, this pin is at the same supply as the host interface (1.8 V, 2.5 V, 3 V, or 5 V). Bypass VIO to GND with a 0.1 μF ceramic capacitor.</td>
</tr>
<tr>
<td>N/A 2</td>
<td>EPAD</td>
<td>P</td>
<td>Exposed Pad (LFCSP Only). Connect the exposed pad to GND. This connection is not required to meet the specified performance.</td>
</tr>
</tbody>
</table>

1 AI is analog input, P is power, DI is digital input, and DO is digital output.
2 N/A means not applicable.
TYPICAL PERFORMANCE CHARACTERISTICS

VDD = 1.8 V, VIO = 3.3 V, VREF = 5 V, T = 25°C, high-Z mode disabled, span compression disabled, and turbo mode enabled (fS = 2 MSPS), unless otherwise noted.

Figure 5. INL vs. Code for Various Temperatures, VREF = 5 V

Figure 6. INL vs. Code for Various Temperatures, VREF = 2.5 V

Figure 7. INL vs. Code, High-Z and Span Compression Modes Enabled, VREF = 5 V

Figure 8. DNL vs. Code for Various Temperatures, VREF = 5 V

Figure 9. DNL vs. Code for Various Temperatures, VREF = 2.5 V

Figure 10. DNL vs. Code, High-Z and Span Compression Modes Enabled, VREF = 5 V
Figure 11. Histogram of a DC Input at Code Center, $V_{\text{REF}} = 2.5$ V and $V_{\text{REF}} = 5$ V

Figure 14. Histogram of a DC Input at Code Transition, $V_{\text{REF}} = 2.5$ V and $V_{\text{REF}} = 5$ V

Figure 12. 1 kHz, −0.5 dBFS Input Tone FFT, Wide View, $V_{\text{REF}} = 5$ V

Figure 15. 1 kHz, −0.5 dBFS Input Tone FFT, Wide View, $V_{\text{REF}} = 2.5$ V

Figure 13. 100 kHz, −0.5 dBFS Input Tone FFT, Wide View

Figure 16. 400 kHz, −0.5 dBFS Input Tone FFT, Wide View

VREF = 5V
SNR = 95.48dB
THD = −98.63dB
SINAD = 93.84dB

VREF = 5V
SNR = 96.25dB
THD = −124.30dB
SINAD = 96.23dB

VREF = 5V
SNR = 93.12dB
THD = −118.26dB
SINAD = 93.11dB

VREF = 2.5V
SNR = 95.48dB
THD = −98.63dB
SINAD = 93.84dB

VREF = 2.5V
SNR = 93.12dB
THD = −118.26dB
SINAD = 93.11dB
Figure 17. SNR, SINAD, and ENOB vs. Reference Voltage

Figure 18. 1/f Noise for 0.1 Hz to 10 Hz Bandwidth, 50 kSPS, 2500 Samples Averaged per Reading

Figure 19. SNR vs. Decimation Rate for Various Input Frequencies

Figure 20. THD and SFDR vs. Reference Voltage

Figure 21. Reference Current vs. Reference Voltage

Figure 22. SINAD vs. tQUIET2
Figure 23. SNR, SINAD, and ENOB vs. Temperature, \( f_{\text{IN}} = 1 \text{ kHz} \)

Figure 24. Operating Currents vs. Temperature

Figure 25. Zero Error and Gain Error vs. Temperature, Positive Full Scale (PFS) and Negative Full Scale (NFS)

Figure 26. THD and SFDR vs. Temperature, \( f_{\text{IN}} = 1 \text{ kHz} \)

Figure 27. Standby Current vs. Temperature

Figure 28. \( t_{\text{SDO}} \) vs. Load Capacitance
**TERMINOLOGY**

**Integral Nonlinearity Error (INL)**
INL refers to the deviation of each individual code from a line drawn from negative full scale through positive full scale. The point used as negative full scale occurs ½ LSB before the first code transition. Positive full scale is defined as a level 1½ LSB beyond the last code transition. The deviation is measured from the middle of each code to the true straight line (see Figure 30).

**Differential Nonlinearity Error (DNL)**
In an ideal ADC, code transitions are 1 LSB apart. DNL is the maximum deviation from this ideal value. It is often specified in terms of resolution for which no missing codes are guaranteed.

**Zero Error**
Zero error is the difference between the ideal midscale voltage, that is, 0 V, from the actual voltage producing the midscale output code, that is, 0 LSB.

**Gain Error**
The first transition (from 100 ... 00 to 100 ... 01) occurs at a level ½ LSB above nominal negative full scale (−4.999981 V for the ±5 V range). The last transition (from 011 ... 10 to 011 ... 11) occurs for an analog voltage 1½ LSB below the nominal full scale (+4.999943 V for the ±5 V range). The gain error is the deviation of the difference between the actual level of the last transition and the actual level of the first transition from the difference between the ideal levels.

**Spurious-Free Dynamic Range (SFDR)**
SFDR is the difference, in decibels (dB), between the rms amplitude of the input signal and the peak spurious signal.

**Effective Number of Bits (ENOB)**
ENOB is a measurement of the resolution with a sine wave input. It is related to SINAD as follows:

\[
ENOB = \frac{(SINAD_{dB} - 1.76)}{6.02}
\]

ENOB is expressed in bits.

**Noise Free Code Resolution**
Noise free code resolution is the number of bits beyond which it is impossible to distinctly resolve individual codes. It is calculated as

\[
\text{Noise Free Code Resolution} = \log_2\left(\frac{2^n}{\text{Peak-to-Peak Noise}}\right)
\]

Noise free code resolution is expressed in bits.

**Effective Resolution**
Effective resolution is calculated as

\[
\text{Effective Resolution} = \log_2\left(\frac{2^n}{\text{RMS Input Noise}}\right)
\]

Effective resolution is expressed in bits.

**Total Harmonic Distortion (THD)**
THD is the ratio of the rms sum of the first five harmonic components to the rms value of a full-scale input signal and is expressed in decibels.

**Dynamic Range**
Dynamic range is the ratio of the rms value of the full scale to the total rms noise measured. The value for dynamic range is expressed in decibels. It is measured with a signal at −60 dBFS so that it includes all noise sources and DNL artifacts.

**Signal-to-Noise Ratio (SNR)**
SNR is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics and dc. The value for SNR is expressed in decibels.

**Signal-to-Noise-and-Distortion Ratio (SINAD)**
SINAD is the ratio of the rms value of the actual input signal to the rms sum of all other spectral components that are less than the Nyquist frequency, including harmonics but excluding dc. The value of SINAD is expressed in decibels.

**Aperture Delay**
Aperture delay is the measure of the acquisition performance and is the time between the rising edge of the CNV input and when the input signal is held for a conversion.

**Transient Response**
Transient response is the time required for the ADC to acquire a full-scale input step to ±1 LSB accuracy.

**Common-Mode Rejection Ratio (CMRR)**
CMRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the common-mode voltage of IN+ and IN− at the frequency, f.

\[
\text{CMRR (dB)} = 10\log\left(\frac{P_{ADC\_IN}}{P_{ADC\_OUT}}\right)
\]

where:

\[
P_{ADC\_IN} \text{ is the common-mode power at the frequency, } f, \text{ applied to the IN+ and IN− inputs.}
\]

\[
P_{ADC\_OUT} \text{ is the power at the frequency, } f, \text{ in the ADC output.}
\]

**Power Supply Rejection Ratio (PSRR)**
PSRR is the ratio of the power in the ADC output at the frequency, f, to the power of a 200 mV p-p sine wave applied to the ADC VDD supply at the frequency, f.

\[
\text{PSRR (dB)} = 10\log\left(\frac{P_{VDD\_IN}}{P_{ADC\_OUT}}\right)
\]

where:

\[
P_{VDD\_IN} \text{ is the power at the frequency, } f, \text{ at the VDD pin.}
\]

\[
P_{ADC\_OUT} \text{ is the power at the frequency, } f, \text{ in the ADC output.}
\]
CIRCUIT INFORMATION

The AD4001 is a high speed, low power, single-supply, precise, 16-bit ADC based on a SAR architecture.

The AD4001 is capable of converting 2,000,000 samples per second (2 MSPS) and powers down between conversions. When operating at 10 kSPS, for example, it typically consumes 80 μW, making it ideal for battery-powered applications because its power scales linearly with throughput. The AD4001 has a valid first conversion after being powered down for long periods.

The AD4001 provides the user with an on-chip track-and-hold feature and does not exhibit any pipeline delay or latency, making it ideal for multiplexed applications.

The AD4001 incorporates a multitude of unique ease of use features that result in a lower system power and footprint.

The AD4001 has an internal voltage clamp that protects the device from overvoltage damage on the analog inputs.

The analog input incorporates circuitry that reduces the nonlinear charge kickback seen from a typical switched capacitor SAR input. This reduction in kickback, combined with a longer acquisition phase, means reduced settling requirements on the driving amplifier. This combination allows the use of lower bandwidth and lower power amplifiers as drivers. It has the additional benefit of allowing a larger resistor value in the input RC filter and a corresponding smaller capacitor, which results in a smaller RC load for the amplifier, improving stability and power dissipation.

High-Z mode can be enabled via the SPI interface by programming a register bit (see Table 14). When high-Z mode is enabled, the ADC input has a low input charging current at low input signal frequencies, as well as improved distortion over a wide frequency range up to 100 kHz. For frequencies above 100 kHz and multiplexing, disable high-Z mode.

For single-supply applications, a span compression feature creates additional headroom and footroom for the driving amplifier to access the full range of the ADC.

The fast conversion time of the AD4001, along with turbo mode, allows low clock rates to read back conversions even when running at the full 2 MSPS throughput rate. Note that a throughput rate of 2 MSPS can be achieved only with turbo mode enabled and a minimum 70 MHz SCK rate.

The AD4001 can interface to any 1.8 V to 5 V digital logic family. It is available in a 10-lead MSOP or a tiny 10-lead LFCSP that allows space savings and flexible configurations.

The AD4001 is pin for pin compatible with some of the 14-/16-/18-bit precision SAR ADCs listed in Table 8.

<table>
<thead>
<tr>
<th>Bits</th>
<th>100 kSPS</th>
<th>250 kSPS</th>
<th>400 kSPS to 500 kSPS</th>
<th>≥1000 kSPS</th>
</tr>
</thead>
<tbody>
<tr>
<td>18</td>
<td>AD7989-1</td>
<td>AD7691</td>
<td>AD7690, AD7989-5</td>
<td>AD4003,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>AD7982,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>AD7984</td>
</tr>
<tr>
<td>16</td>
<td>AD7684</td>
<td>AD7687</td>
<td>AD7688, AD7693</td>
<td>AD4001,</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>AD7915</td>
</tr>
<tr>
<td>16†</td>
<td>AD7680,</td>
<td>AD7685,</td>
<td>AD7686, AD7988-5</td>
<td>AD4000,</td>
</tr>
<tr>
<td></td>
<td>AD7683,</td>
<td>AD7694</td>
<td></td>
<td>AD7980,</td>
</tr>
<tr>
<td></td>
<td>AD7988-1</td>
<td></td>
<td></td>
<td>AD7983</td>
</tr>
<tr>
<td>14†</td>
<td>AD7940</td>
<td>AD7942</td>
<td>AD7946</td>
<td>Not applicable</td>
</tr>
</tbody>
</table>

† True differential.
‡ Pin for pin compatible.
§ Pseudo differential.

CONVERTER OPERATION

The AD4001 is a SAR-based ADC using a charge redistribution sampling digital-to-analog converter (DAC). Figure 29 shows the simplified schematic of the ADC. The capacitive DAC consists of two identical arrays of 16 binary weighted capacitors that are connected to the comparator inputs.

During the acquisition phase, terminals of the array tied to the input of the comparator are connected to GND via the SW+ and SW− switches. All independent switches connect the other terminal of each capacitor to the analog inputs. Therefore, the capacitor arrays are used as sampling capacitors and acquire the analog signal on the IN+ and IN− inputs.
When the acquisition phase is complete and the CNV input goes high, a conversion phase initiates. When the conversion phase begins, SW+ and SW− are opened first. The two capacitor arrays are then disconnected from the inputs and connected to the GND input. The differential voltage between the IN+ and IN− inputs captured at the end of the acquisition phase is applied to the comparator inputs, causing the comparator to become unbalanced. By switching each element of the capacitor array between GND and VREF, the comparator input varies by binary weighted voltage steps (VREF/2, VREF/4, ..., VREF/65,536). The control logic toggles these switches, starting with the MSB, to bring the comparator back into a balanced condition. After the completion of this process, the control logic generates the ADC output code and a busy signal indicator.

Because the AD4001 has an on-board conversion clock, the serial clock, SCK, is not required for the conversion process.

### Table 9. Output Codes and Ideal Input Voltages

<table>
<thead>
<tr>
<th>Description</th>
<th>Analog Input, VREF = 5 V</th>
<th>VREF = 5 V with Span Compression Enabled</th>
<th>Digital Output Code (Hex)</th>
</tr>
</thead>
<tbody>
<tr>
<td>+FSR – 1 LSB</td>
<td>+4.999847 V</td>
<td>+3.999878 V</td>
<td>0x7FFF1</td>
</tr>
<tr>
<td>Midscale + 1 LSB</td>
<td>+152.6 μV</td>
<td>+122.1 μV</td>
<td>0x0001</td>
</tr>
<tr>
<td>Midscale</td>
<td>0 V</td>
<td>0 V</td>
<td>0x0000</td>
</tr>
<tr>
<td>Midscale – 1 LSB</td>
<td>−152.6 μV</td>
<td>−122.1 μV</td>
<td>0xFFFF</td>
</tr>
<tr>
<td>−FSR + 1 LSB</td>
<td>−4.999847 V</td>
<td>−3.999878 V</td>
<td>0x8001</td>
</tr>
<tr>
<td>−FSR</td>
<td>−5 V</td>
<td>−4 V</td>
<td>0x80002</td>
</tr>
</tbody>
</table>

1 This output code is also the code for an overranged analog input (VIN+ − VIN− above VREF).
2 This output code is also the code for an underranged analog input (VIN+ − VIN− below −VREF).

### Transfer Functions

The ideal transfer characteristics for the AD4001 are shown in Figure 30 and Table 9.

![ADC Ideal Transfer Function (FSR Is Full-Scale Range)](image-url)
APPLICATIONS INFORMATION

TYPICAL APPLICATION DIAGRAMS

Figure 31 shows an example of the recommended connection diagram for the AD4001 when multiple supplies are available. This configuration is used for best performance because the amplifier supplies can be selected to allow the maximum signal range.

Figure 32 shows a recommended connection diagram when using a single-supply system. This setup is preferable when only a limited number of rails are available in the system and power dissipation is of critical importance.

Figure 33 shows a recommended connection diagram when using a fully differential amplifier.

1SEE THE VOLTAGE REFERENCE INPUT SECTION FOR REFERENCE SELECTION. CREF IS USUALLY A 10µF CERAMIC CAPACITOR (X7R).

2SPAN COMPRESSION MODE ENABLED.

3SEE TABLE 10 FOR RC FILTER AND AMPLIFIER SELECTION.
ANALOG INPUTS

Figure 35 shows an equivalent circuit of the analog input structure, including the overvoltage clamp of the AD4001.

Input Overvoltage Clamp Circuit

Most ADC analog inputs, IN+ and IN−, have no overvoltage protection circuitry apart from ESD protection diodes. During an overvoltage event, an ESD protection diode from an analog input pin (IN+ or IN−) to REF forward biases and shorts the input pin to REF, potentially overloading the reference or causing damage to the device. The AD4001 internal overvoltage clamp circuit with a larger external resistor (REXT = 200 Ω) eliminates the need for external protection diodes and protects the ADC inputs against dc overvoltages.

In applications where the amplifier rails are greater than VREF and less than ground, it is possible for the output to exceed the input voltage range of the device. In this case, the AD4001 internal voltage clamp circuit ensures that the voltage on the input pin does not exceed VREF + 0.4 V and prevents damage to the device by clamping the input voltage in a safe operating range and by avoiding disturbance of the reference, which is particularly important for systems that share the reference among multiple ADCs.
If the analog input exceeds the reference voltage by 0.4 V, the internal clamp circuit turns on and the current flows through the clamp into ground, preventing the input from rising further and potentially causing damage to the device. The clamp turns on before D1 (see Figure 35) and can sink up to 50 mA of current.

When the clamp is active, it sets the OV clamp flag bit in the register that can be read back (see Table 14), which is a sticky bit that must be read to be cleared. The status of the clamp can also be checked in the status bits using an overvoltage clamp flag (see Table 15). The clamp circuit does not dissipate static power in the off state. Note that the clamp cannot sustain the overvoltage condition for an indefinite time.

The external RC filter is usually present at the ADC input to band limit the input signal. During an overvoltage event, excessive voltage is dropped across R\textsubscript{EXT}, and R\textsubscript{EXT} becomes part of the protection circuit. The R\textsubscript{EXT} value can vary from 200 Ω to 20 kΩ for 15 V protection. The C\textsubscript{EXT} value can be as low as 100 pF for correct operation of the clamp. See Table 1 for the input overvoltage clamp specifications.

**Figure 35. Equivalent Analog Input Circuit**

### Differential Input Considerations

The analog input structure allows the sampling of the true differential signal between IN+ and IN−. By using these differential inputs, signals common to both inputs are rejected. Figure 36 shows the common-mode rejection capability of the AD4001 over frequency. It is important to note that the differential input signals must be truly antiphase in nature, 180° out of phase, which is required to keep the common-mode voltage of the input signal within the specified range around V\textsubscript{REF}/2 shown in Table 1.

**Figure 36. Common-Mode Rejection Ratio vs. Frequency, VIO = 3.3 V, V\textsubscript{REF} = 5 V, 25°C**

### Switched Capacitor Input

During the acquisition phase, the impedance of the analog inputs (IN+ or IN−) can be modeled as a parallel combination of Capacitor C\textsubscript{PIN} and the network formed by the series connection of R\textsubscript{IN} and C\textsubscript{IN}. C\textsubscript{PIN} is primarily the pin capacitance. R\textsubscript{IN} is typically 400 Ω and is a lumped component composed of serial resistors and the on resistance of the switches. C\textsubscript{IN} is typically 40 pF and is mainly the ADC sampling capacitor.

During the conversion phase, where the switches are open, the input impedance is limited to C\textsubscript{PIN}. R\textsubscript{IN} and C\textsubscript{IN} make a single-pole, low-pass filter that reduces undesirable aliasing effects and limits noise.

### RC Filter Values

The RC filter value and driving amplifier can be selected depending on the input signal bandwidth of interest at the full 2 MSPS throughput. Lower input signal bandwidth means that the RC cutoff can be lower, thereby reducing noise into the converter. For optimum performance at various throughputs, use the recommended RC values (200 Ω, 180 pF) and the ADA4807-1.

The RC values in Table 10 are chosen for ease of drive considerations and also greater ADC input protection. The combination of a large R value (200 Ω) and small C value result in a reduced dynamic load for the amplifier to drive. The smaller value of C means few stability and phase margin concerns with the amplifier. The large value of R limits the current into the ADC input when the amplifier output exceeds the ADC input range.

**Table 10. RC Filter and Amplifier Selection for Various Input Bandwidths**

<table>
<thead>
<tr>
<th>Input Signal Bandwidth (kHz)</th>
<th>R (Ω)</th>
<th>C (pF)</th>
<th>Recommended Amplifier</th>
<th>Recommended Fully Differential Amplifier</th>
</tr>
</thead>
<tbody>
<tr>
<td>&lt;10</td>
<td>200</td>
<td>180</td>
<td>See the High-Z Mode section</td>
<td>ADA4940-1</td>
</tr>
<tr>
<td>&lt;200</td>
<td>200</td>
<td>180</td>
<td>ADA4807-1</td>
<td>ADA4940-1</td>
</tr>
<tr>
<td>&gt;200</td>
<td>200</td>
<td>120</td>
<td>ADA4897-1</td>
<td>ADA4932-1</td>
</tr>
<tr>
<td>Multiplexed</td>
<td>200</td>
<td>120</td>
<td>ADA4897-1</td>
<td>ADA4932-1</td>
</tr>
</tbody>
</table>
DRIVER AMPLIFIER CHOICE

Although the AD4001 is easy to drive, the driver amplifier must meet the following requirements:

- The noise generated by the driver amplifier must be kept low enough to preserve the SNR and transition noise performance of the AD4001. The noise from the driver is filtered by the single-pole, low-pass filter of the AD4001 analog input circuit made by \( R_{IN} \) and \( C_{IN} \), or by the external filter, if one is used. Because the typical noise of the AD4001 is 54 \( \mu V \) rms, the SNR degradation due to the amplifier is

\[
SNR_{LOSS} = 20 \log \left( \frac{54}{\sqrt{54^2 + \frac{\pi}{2} f_{-3dB} (Ne_N)^2}} \right)
\]

where:
- \( f_{-3dB} \) is the input bandwidth, in megahertz, of the AD4001 (10 MHz) or the cutoff frequency of the input filter, if one is used.
- \( N \) is the noise gain of the amplifier (for example, 1 in buffer configuration).
- \( e_N \) is the equivalent input noise voltage of the op amp in nV/\( \sqrt{Hz} \).

- For ac applications, the driver must have a THD performance commensurate with the AD4001.
- For multichannel multiplexed applications, the driver amplifier and the AD4001 analog input circuit must settle for a full-scale step onto the capacitor array at a 16-bit level (0.0001525%, 15.25 ppm). In the data sheet of the amplifier, settling at 0.1% to 0.01% is more commonly specified. This settling may differ significantly from the settling time at a 16-bit level and must be verified prior to driver selection.

Single to Differential Driver

For applications using a single-ended analog signal, either bipolar or unipolar, the ADA4940-1 single-ended to differential driver allows a differential input to the device. The schematic is shown in Figure 34.

High Frequency Input Signals

The AD4001 ac performance over a wide input frequency range is shown in Figure 37. Unlike other traditional SAR ADCs, the AD4001 ac performance holds up to the Nyquist frequency.

EASE OF DRIVE FEATURES

Input Span Compression

In single-supply applications, it is desirable to use the full range of the ADC; however, the amplifier can have some headroom and footroom requirements, which can be a problem, even if it is a rail-to-rail input and output amplifier. The use of span compression increases the headroom and footroom available to the amplifier by reducing the input range by 10% from the top and bottom of the range while still accessing all available ADC codes (see Figure 39). The SNR decreases by approximately 1.9 dB (20 \( \times \) log(8/10)) for the reduced input range when span compression is enabled. Span compression is disabled by default but can be enabled by writing to the relevant register bit (see the Digital Interface section).
High-Z Mode

The AD4001 incorporates high-Z mode, which reduces the nonlinear charge kickback when the capacitor DAC switches back to the input at the start of acquisition. Figure 40 shows the input current of the AD4001 with high-Z mode enabled and disabled. The low input current makes the ADC easier to drive than the traditional SAR ADCs available in the market, even with high-Z mode disabled. The input current reduces further to sub microampere range when high-Z mode is enabled. The high-Z mode is disabled by default but can be enabled by writing to the register (see Table 14). Disable high-Z mode for input frequencies above 100 kHz or multiplexing.

System designers looking to achieve the optimum data sheet performance from high resolution precision SAR ADCs are often forced to use a dedicated high power, high speed amplifier to drive the traditional switched capacitor SAR ADC inputs for their precision applications, which is one of the common pain points encountered in designing a precision data acquisition signal chain. The benefits of high-Z mode are low input current for slow (<10 kHz) or dc type signals and improved distortion (THD) performance over a frequency range of up to 100 kHz. High-Z mode allows a choice of lower power and bandwidth precision amplifiers with a lower RC filter cutoff to drive the ADC, removing the need for dedicated high speed ADC drivers, which saves system power, size, and cost in precision, low bandwidth applications. High-Z mode allows the amplifier and RC filter in front of the ADC to be chosen based on the signal bandwidth of interest and not based on the settling requirements of the switched capacitor SAR ADC inputs.

Additionally, the AD4001 can be driven with a much higher source impedance than traditional SARs, which means the resistor in the RC filter can have a value 10 times larger than previous SAR designs and, with high-Z mode enabled, can tolerate even larger impedance. Figure 41 shows the THD performance for various source impedances with high-Z mode disabled and enabled.

When high-Z mode is enabled, the ADC consumes approximately 2 mW/MSPS extra power; however, this power is still significantly lower than using dedicated ADC drivers like the ADA4807-1. For any system, the front end usually limits the overall ac/dc performance of the signal chain. It is evident from the data sheets of the selected precision amplifiers, shown in Figure 42 and Figure 43, that their own noise and distortion performance dominates the SNR and THD specification at a certain input frequency.
Long Acquisition Phase

The AD4001 also features a very fast conversion time of 290 ns, which results in a long acquisition phase. The acquisition is further extended by a key feature of the AD4001; the ADC returns back to the acquisition phase typically 100 ns before the end of the conversion. This feature provides an even longer time for the ADC to acquire the new input voltage. A longer acquisition phase reduces the settling requirement on the driving amplifier, and a lower power/bandwidth amplifier can be chosen. The longer acquisition phase means that a lower RC filter cutoff can be used, which means a noisier amplifier can also be tolerated. A larger value of R can be used in the RC filter with a corresponding smaller value of C, reducing amplifier stability concerns without affecting distortion performance significantly. A larger value of R also results in reduced dynamic power dissipation in the amplifier.

See Table 10 for details on setting the RC filter bandwidth and choosing a suitable amplifier.

VOLTAGE REFERENCE INPUT

A 10 μF (X7R, 0805 size) ceramic chip capacitor is appropriate for the optimum performance of the reference input.

For higher performance and lower drift, use a reference such as the ADR4550. Use a low power reference such as the ADR3450 at the expense of a slight decrease in the noise performance. It is recommended to use a reference buffer, such as the ADA4807-1, between the reference and the ADC reference input. It is important to consider the optimum capacitance size necessary to keep the reference buffer stable as well as to meet the minimum ADC requirement previously stated in this section (that is, a 10 μF ceramic chip capacitor).

POWER SUPPLY

The AD4001 uses two power supply pins: a core supply (VDD) and a digital input/output interface supply (VIO). VIO allows direct interface with any logic between 1.8 V and 5.5 V. To reduce the number of supplies needed, VIO and VDD can be tied together for 1.8 V operation. The ADP7118 low noise, CMOS, low dropout (LDO) linear regulator is recommended to power the VDD and VIO pins. The AD4001 is independent of power supply sequencing between VIO and VDD. Additionally, the AD4001 is insensitive to power supply variations over a wide frequency range, as shown in Figure 44.

The AD4001 powers down automatically at the end of each conversion phase; therefore, the power scales linearly with the sampling rate. This feature makes the device ideal for low sampling rates (even of a few hertz) and battery-powered applications. Figure 45 shows the AD4001 total power dissipation and individual power dissipation for each rail.

DIGITAL INTERFACE

Although the AD4001 has a reduced number of pins, it offers flexibility in its serial interface modes. The AD4001 can also be programmed via 16-bit SPI writes to the configuration registers. When in CS mode, the AD4001 is compatible with SPI, QSPI™, digital hosts, and DSPs. In this mode, the AD4001 can use either a 3-wire or 4-wire interface. A 3-wire interface using the CNV, SCK, and SDO signals minimizes wiring connections, which is useful, for instance, in isolated applications. A 4-wire interface using the SDI, CNV, SCK, and SDO signals allows CNV, which initiates the conversions, to be independent of the readback.
timing (SDI). This interface is useful in low jitter sampling or
simultaneous sampling applications.

The AD4001 provides a daisy-chain feature using the SDI input
for cascading multiple ADCs on a single data line similar to a
shift register.

The mode in which the device operates depends on the SDI
level when the CNV rising edge occurs. CS mode is selected if
SDI is high, and daisy-chain mode is selected if SDI is low. The
SDI hold time is such that when SDI and CNV are connected
together, daisy-chain mode is always selected.

In either 3-wire or 4-wire mode, the AD4001 offers the option
of forcing a start bit in front of the data bits. This start bit can be
used as a busy signal indicator to interrupt the digital host and
trigger the data reading. Otherwise, without a busy indicator, the
user must time out the maximum conversion time prior to
readback.

The busy indicator feature is enabled in CS mode if CNV or SDI
is low when the ADC conversion ends.

The state of SDO on power-up is either low or high-Z
depending on the states of CNV and SDI, as shown in in Table 11.

<table>
<thead>
<tr>
<th>CNV</th>
<th>SDI</th>
<th>SDO</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Low</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>High-Z</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Low</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>High-Z</td>
</tr>
</tbody>
</table>

The AD4001 has turbo mode capability in both 3-wire and 4-wire
mode. Turbo mode is enabled by writing to the configuration
register and replaces the busy indicator feature when enabled.
Turbo mode allows a slower SPI clock rate, making interfacing
cleaner. A throughput rate of 2 MSPS can be achieved only with
turbo mode enabled and a minimum SCK rate of 70 MHz.

Status bits can also be clocked out at the end of the conversion
data if the status bits are enabled in the configuration register.
There are six status bits in total, as described in Table 12.

The AD4001 is configured by 16-bit SPI writes to the desired
configuration register. The 16-bit word can be written via the
SDI line while CNV is held low. The 16-bit word consists of an
8-bit header and 8-bit register data. For isolated systems, the
ADuM141D is recommended, which has a maximum clock rate
of 70 MHz and allows the AD4001 to run at 2 MSPS.

REGISTER READ/WRITE FUNCTIONALITY

The AD4001 register bits are programmable, and their default
statuses are shown in Table 12. The register map is shown in

<table>
<thead>
<tr>
<th>ADDR[1:0]</th>
<th>Bit 7</th>
<th>Bit 6</th>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
<th>Reset</th>
</tr>
</thead>
<tbody>
<tr>
<td>0x0</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Reserved</td>
<td>Enable six status bits</td>
<td>Span compression</td>
<td>High-Z mode</td>
<td>Turbo mode</td>
<td>Overvoltage (OV) clamp flag (read only sticky bit)</td>
<td>0xE1</td>
</tr>
</tbody>
</table>
THE USER MUST WAIT $t_{\text{CONV}}$ WHEN READING BACK THE CONVERSION RESULT AND PERFORMING A REGISTER WRITE AT THE SAME TIME.

Figure 46. Register Read Timing Diagram (X Means Don’t Care)

Figure 47. Register Write Timing Diagram

Figure 48. Register Write Timing Diagram, Daisy-Chain Mode
STATUS WORD

The 6-bit status word can be appended to the end of a conversion result, and the default conditions of these bits are defined in Table 15. The status bits must be enabled in the register setting. When the overvoltage clamp flag is a 0, it indicates an overvoltage condition. The overvoltage clamp flag status bit updates on a per conversion basis.

Table 15. Status Bits (Default Conditions)

<table>
<thead>
<tr>
<th>Bit 5</th>
<th>Bit 4</th>
<th>Bit 3</th>
<th>Bit 2</th>
<th>Bit 1</th>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>Overvoltage (OV) clamp flag</td>
<td>Span compression</td>
<td>High-Z mode</td>
<td>Turbo mode</td>
<td>Reserved</td>
<td>Reserved</td>
</tr>
</tbody>
</table>

The SDO line goes to high-Z after the sixth status bit is clocked out (except in daisy-chain mode). The user is not required to clock out all status bits to start the next conversion. The serial interface timing for CS mode, 3-wire without busy indicator, including status bits, is shown in Figure 49.
**CS MODE, 3-WIRE TURBO MODE**

This mode is typically used when a single AD4001 is connected to an SPI-compatible digital host. It provides additional time during the end of the ADC conversion process to clock out the previous conversion result, providing a lower SCK rate. The AD4001 can achieve a throughput rate of 2 MSPS only when turbo mode is enabled and using a minimum SCK rate of 70 MHz. The connection diagram is shown in Figure 50, and the corresponding timing diagram is shown in Figure 51.

This mode replaces the 3-wire with busy indicator mode by programming the turbo mode bit, Bit 1 (see Table 14).

When SDI is forced high, a rising edge on CNV initiates a conversion. The previous conversion data is available to read after the CNV rising edge. The user must wait $t_{QUIET1}$ time after CNV is brought high before bringing CNV low to clock out the previous conversion result. The user must also wait $t_{QUIET2}$ time after the last falling edge of SCK to when CNV is brought high.

When the conversion is complete, the AD4001 enters the acquisition phase and powers down. When CNV goes low, the MSB is output to SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.
**CS MODE, 3-WIRE WITHOUT BUSY INDICATOR**

This mode is typically used when a single AD4001 is connected to an SPI-compatible digital host. The connection diagram is shown in Figure 52, and the corresponding timing diagram is shown in Figure 53.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects CS mode, and forces SDO to high impedance. After a conversion is initiated, it continues until completion irrespective of the state of CNV. This feature can be useful, for instance, to bring CNV low to select other SPI devices, such as analog multiplexers; however, CNV must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the AD4001 enters the acquisition phase and powers down. When CNV goes low, the MSB is output onto SDO. The remaining data bits are clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

There must not be any digital activity on SCK during the conversion.
CS MODE, 3-WIRE WITH BUSY INDICATOR

This mode is typically used when a single AD4001 is connected to an SPI-compatible digital host with an interrupt input (IRQ). The connection diagram is shown in Figure 54, and the corresponding timing diagram is shown in Figure 55.

With SDI tied to VIO, a rising edge on CNV initiates a conversion, selects CS mode, and forces SDO to high impedance. SDO is maintained in high impedance until the completion of the conversion irrespective of the state of CNV. Prior to the minimum conversion time, CNV can select other SPI devices, such as analog multiplexers; however, CNV must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up resistor on the SDO line, this transition can be used as an interrupt signal to initiate the data reading controlled by the digital host. The AD4001 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th SCK falling edge or when CNV goes high (whichever occurs first), SDO returns to high impedance.

If multiple AD4001 devices are selected at the same time, the SDO output pin handles this contention without damage or induced latch-up. Meanwhile, it is recommended to keep this contention as short as possible to limit extra power dissipation. There must not be any digital activity on the SCK during the conversion.
CS MODE, 4-WIRE TURBO MODE

This mode is typically used when a single AD4001 is connected to an SPI-compatible digital host. It provides additional time during the end of the ADC conversion process to clock out the previous conversion result, giving a lower SCK rate. The AD4001 can achieve a throughput rate of 2 MSPS only when turbo mode is enabled and using a minimum SCK rate of 70 MHz. The connection diagram is shown in Figure 56, and the corresponding timing diagram is shown in Figure 57.

This mode replaces the 4-wire with busy indicator mode by programming the turbo mode bit, Bit 1 (see Table 14).

The previous conversion data is available to read after the CNV rising edge. The user must wait \( t_{QUIET1} \) time after CNV is brought high before bringing SDI low to clock out the previous conversion result. The user must also wait \( t_{QUIET2} \) time after the last falling edge of SCK to when CNV is brought high.

When the conversion is complete, the AD4001 enters the acquisition phase and powers down. The ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance.

Figure 56. CS Mode, 4-Wire Turbo Mode Connection Diagram

Figure 57. CS Mode, 4-Wire Turbo Mode Timing Diagram
**CS MODE, 4-WIRE WITHOUT BUSY INDICATOR**

This mode is typically used when multiple AD4001 devices are connected to an SPI-compatible digital host.

A connection diagram example using two AD4001 devices is shown in Figure 58, and the corresponding timing is shown in Figure 59.

With SDI high, a rising edge on CNV initiates a conversion, selects CS mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI and CNV are low, SDO is driven low. Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers; however, SDI must be returned high before the minimum conversion time elapses and then held high for the maximum possible conversion time to avoid the generation of the busy signal indicator.

When the conversion is complete, the AD4001 enters the acquisition phase and powers down. Each ADC result can be read by bringing its SDI input low, which consequently outputs the MSB onto SDO. The remaining data bits are then clocked by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the 16th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance and another AD4001 can be read.

![Figure 58. CS Mode, 4-Wire Without Busy Indicator Connection Diagram](image1)

![Figure 59. CS Mode, 4-Wire Without Busy Indicator Serial Interface Timing Diagram](image2)
**CS MODE, 4-WIRE WITH BUSY INDICATOR**

This mode is typically used when a single AD4001 is connected to an SPI-compatible digital host with an interrupt input, and when it is desired to keep CNV, which samples the analog input, independent of the signal used to select the data reading. This independence is particularly important in applications where low jitter on CNV is desired.

The connection diagram is shown in Figure 60, and the corresponding timing is shown in Figure 61.

With SDI high, a rising edge on CNV initiates a conversion, selects CS mode, and forces SDO to high impedance. In this mode, CNV must be held high during the conversion phase and the subsequent data readback. If SDI and CNV are low, SDO is driven low. Prior to the minimum conversion time, SDI can select other SPI devices, such as analog multiplexers; however, SDI must be returned low before the minimum conversion time elapses and then held low for the maximum possible conversion time to guarantee the generation of the busy signal indicator.

When the conversion is complete, SDO goes from high impedance to low impedance. With a pull-up resistor on the SDO line, this transition can be used as an interrupt signal to initiate the data readback controlled by the digital host. The AD4001 then enters the acquisition phase and powers down. The data bits are then clocked out, MSB first, by subsequent SCK falling edges. The data is valid on both SCK edges. Although the rising edge can be used to capture the data, a digital host using the SCK falling edge allows a faster reading rate, provided it has an acceptable hold time. After the optional 17th SCK falling edge or when SDI goes high (whichever occurs first), SDO returns to high impedance.
DAISY-CHAIN MODE

Use this mode to daisy-chain multiple AD4001 devices on a 3-wire or 4-wire serial interface. This feature is useful for reducing component count and wiring connections, for example, in isolated multiconverter applications or for systems with a limited interfacing capacity. Data readback is analogous to clocking a shift register.

A connection diagram example using two AD4001 devices is shown in Figure 62, and the corresponding timing is shown in Figure 63.

When SDI and CNV are low, SDO is driven low. With SCK low, a rising edge on CNV initiates a conversion, selects daisy-chain mode, and disables the busy indicator. In this mode, CNV is held high during the conversion phase and the subsequent data readback. When the conversion is complete, the MSB is output onto SDO, and the AD4001 enters the acquisition phase and powers down. The remaining data bits stored in the internal shift register are clocked out of SDO by subsequent SCK falling edges. For each ADC, SDI feeds the input of the internal shift register and is clocked by the SCK rising edges. Each ADC in the daisy-chain outputs its data MSB first, and 16 × N clocks are required to read back the N ADCs. The data is valid on both SCK edges. The maximum conversion rate is reduced because of the total readback time.

It is possible to write to each ADC register in daisy-chain mode. The timing diagram is shown in Figure 48. This mode requires 4-wire operation because data is clocked in on the SDI line with CNV held low. The same command byte and register data can be shifted through the entire chain to program all ADCs in the chain with the same register contents, which requires 8 × (N + 1) clocks for N ADCs. It is possible to write different register contents to each ADC in the chain by writing to the furthest ADC in the chain, first using 8 × (N + 1) clocks, and then the second furthest ADC with 8 × N clocks, and so forth until reaching the nearest ADC in the chain, which requires 16 clocks for the command and register data. It is not possible to read register contents in daisy-chain mode; however, the 6 status bits can be enabled if the user wants to know the ADC configuration. Note that enabling the status bits requires 6 extra clocks to clock out the ADC result and the status bits per ADC in the chain. Turbo mode cannot be used in daisy-chain mode.

Figure 62. Daisy-Chain Mode Connection Diagram

Figure 63. Daisy-Chain Mode Serial Interface Timing Diagram
LAYOUT GUIDELINES

The PCB that houses the AD4001 must be designed so that the analog and digital sections are separated and confined to certain areas of the board. The pinout of the AD4001, with its analog signals on the left side and its digital signals on the right side, eases this task.

Avoid running digital lines under the device because they couple noise onto the die, unless a ground plane under the AD4001 is used as a shield. Fast switching signals, such as CNV or clocks, must not run near analog signal paths. Avoid crossover of digital and analog signals.

At least one ground plane must be used. It can be common or split between the digital and analog sections. In the latter case, join the planes underneath the AD4001 devices.

The AD4001 voltage reference input (REF) has a dynamic input impedance. Decouple the REF pin with minimal parasitic inductances by placing the reference decoupling ceramic capacitor close to (ideally right up against) the REF and GND pins and connect them with wide, low impedance traces.

Finally, decouple the VDD and VIO power supplies of the AD4001 with ceramic capacitors, typically 100 nF, placed close to the AD4001 and connected using short, wide traces to provide low impedance paths and to reduce the effect of glitches on the power supply lines.

An example of a layout following these rules is shown in Figure 64 and Figure 65.

EVALUATING THE AD4001 PERFORMANCE

Other recommended layouts for the AD4001 are outlined in the documentation of the evaluation board for the AD4001 (EVAL-AD4001FMCZ). The evaluation board package includes a fully assembled and tested evaluation board, documentation, and software for controlling the board from a PC via the EVAL-SDP-CH1Z.
OUTLINE DIMENSIONS

Figure 66. 10-Lead Mini Small Outline Package [MSOP] (RM-10)
Dimensions shown in millimeters

Figure 67. 10-Lead Lead Frame Chip Scale Package [LFCSP]
3 mm × 3 mm Body and 0.75 mm Package Height (CP-10-9)
Dimensions shown in millimeters

ORDERING GUIDE

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<th>Temperature Range</th>
<th>Package Description</th>
<th>Ordering Quantity</th>
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<td>±0.4 LSB</td>
<td>−40°C to +125°C</td>
<td>10-Lead MSOP</td>
<td>Tube, 50</td>
<td>RM-10</td>
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</tr>
<tr>
<td>AD4001BRMZ-RL7</td>
<td>±0.4 LSB</td>
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<tr>
<td>EVAL-AD4001FMCZ</td>
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1 Z = RoHS Compliant Part.