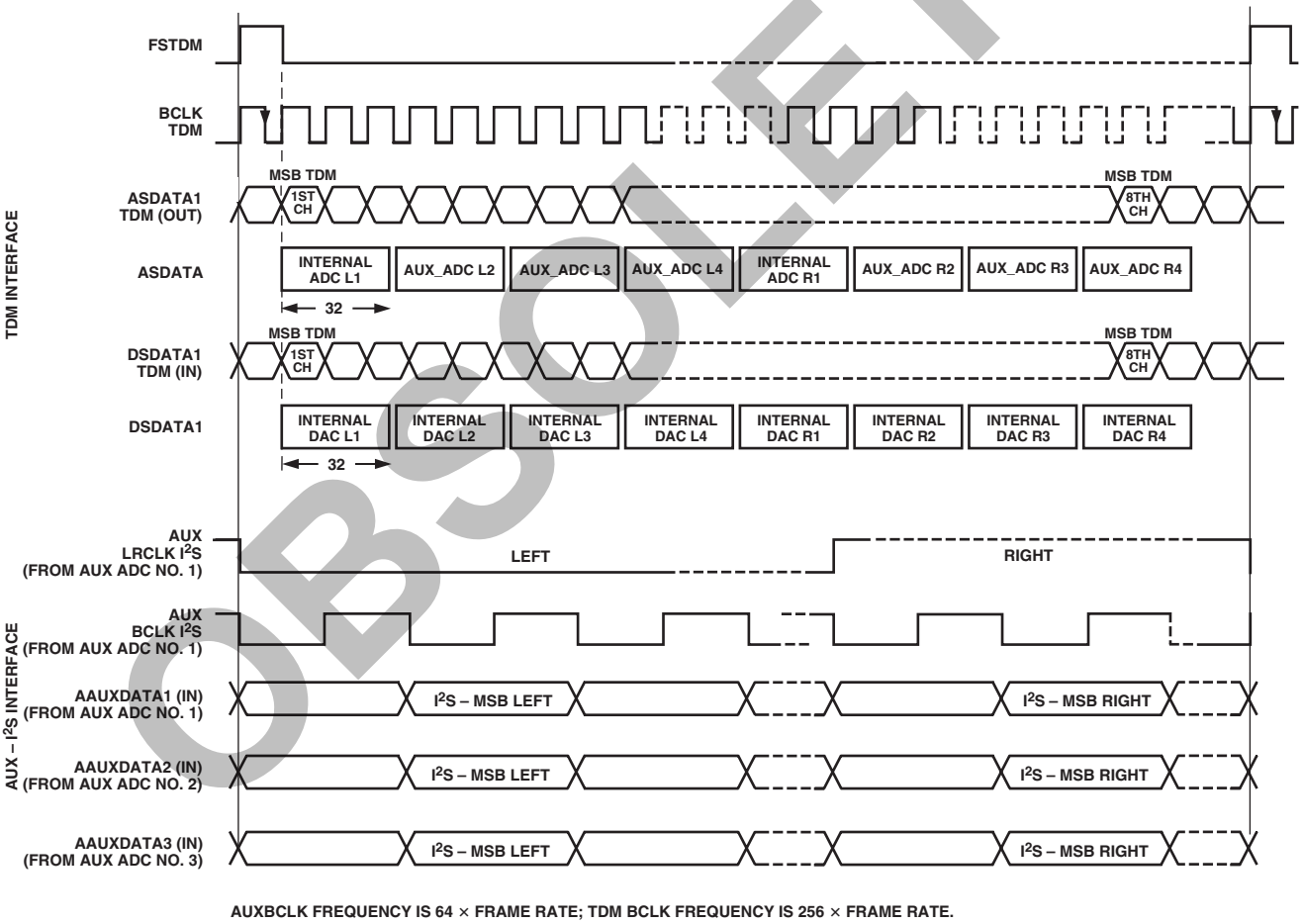
Table IV. Pin Function Changes in Auxiliary Mode

Pin Name	I²S Mode	Auxiliary Mode
ASDATA (O)	I²S Data Out, Internal ADC	TDM Data Out to SHARC.
DSDATA1 (I)	I²S Data In, Internal DAC1	TDM Data In from SHARC.
DSDATA2 (I)/AAUXDATA1 (I)	I²S Data In, Internal DAC2	AUX-I²S Data In 1 (from External ADC).
DSDATA3 (I)/AAUXDATA2 (I)	I²S Data In, Internal DAC3	AUX-I²S Data In 2 (from External ADC).
AAUXDATA3 (I)	Not Connected	AUX-I²S Data In 3 (from External ADC).
ALRCLK (O)	LRCLK for ADC	TDM Frame Sync Out to SHARC (FSTDM).
ABCLK (O)	BCLK for ADC	TDM BCLK Out to SHARC.
DLRCLK (I)/AUXLRCLK (I/O)	LRCLK In/Out Internal DACs	AUX LRCLK In/Out. Driven by external LRCLK from ADC in slave mode. In master mode, driven by MCLK/512.
DBCLK (I)/AUXBCLK (I/O)	BCLK In/Out Internal DACs	AUX BCLK In/Out. Driven by external BCLK from ADC in slave mode. In master mode, driven by MCLK/8.
DAUXDATA (O)	Not Connected	AUX-I²S Data Out (to External DAC).



AUXBCLK FREQUENCY IS 64 × FRAME RATE; TDM BCLK FREQUENCY IS 256 × FRAME RATE.

Figure 11. Auxiliary Mode Timing

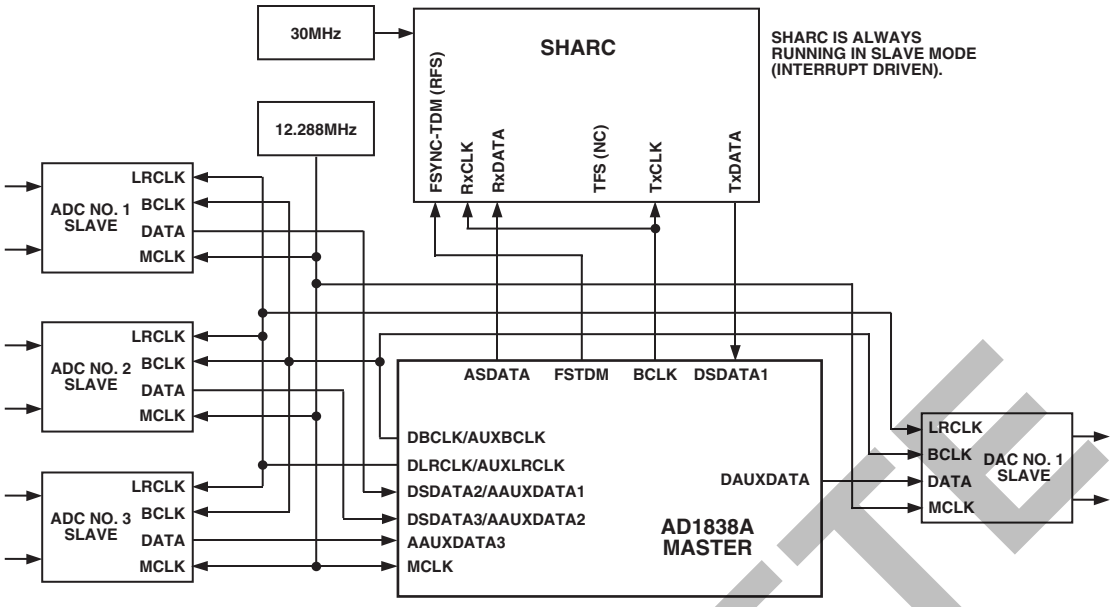


Figure 12. Auxiliary Mode Connection (Master Mode) to SHARC

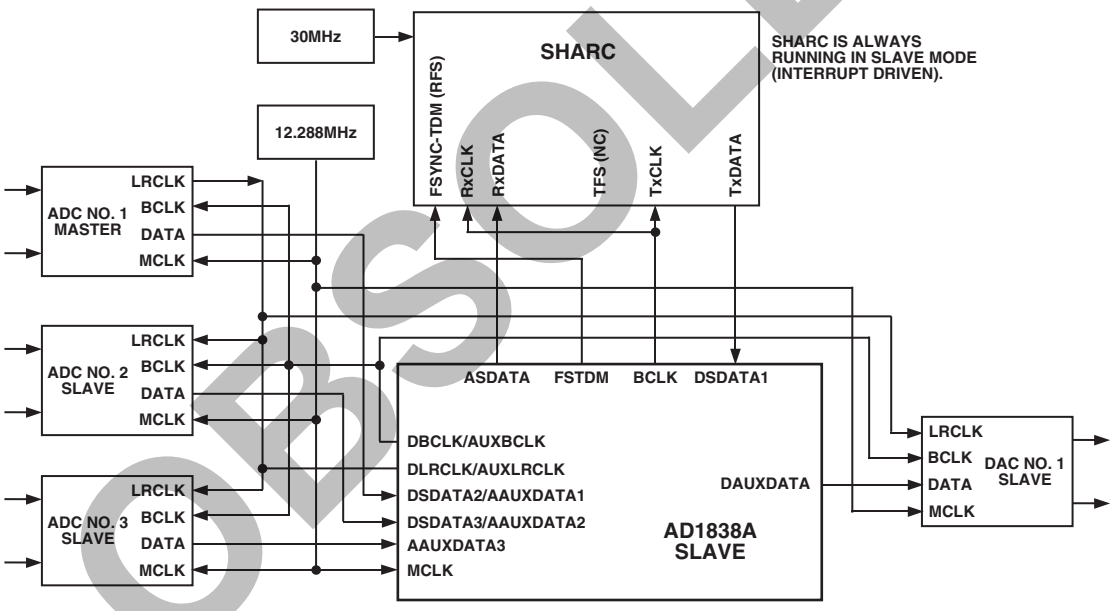


Figure 13. Auxiliary Mode Connection (Slave Mode) to SHARC

CONTROL/STATUS REGISTERS

The AD1838A has 13 control registers, 11 of which are used to set the operating mode of the part. The other two registers, ADC Peak 0 and ADC Peak 1, are read-only and should not be programmed. Each of the registers is 10 bits wide with the exception of the ADC peak reading registers, which are 6 bits wide. Writing to a control register requires a 16-bit data frame to be transmitted. Bits 15 to 12 are the address bits of the required register. Bit 11 is a read/write bit. Bit 10 is reserved and should always be programmed to 0. Bits 9 to 0 contain the 10-bit value that is to be written to the register or, in the case of a read operation, the 10-bit register contents. Figure 3 shows the format of the SPI read and write operation.

DAC Control Registers

The AD1838A register map has eight registers that are used to control the functionality of the DAC section of the part. The function of the bits in these registers is discussed below.

Sample Rate
These bits control the sample rate of the DACs. Based on a 24.576 MHz IMCLK, sample rates of 48 kHz, 96 kHz, and 192 kHz are available. The MCLK scaling bits in ADC Control Register 3 should be programmed appropriately, based on the master clock frequency.

Power-Down/Reset
This bit controls the power-down status of the DAC section. By default, normal mode is selected. But by setting this bit, the digital section of the DAC stage can be put into a low power mode, thus reducing the digital current. The analog output section of the DAC stage is not powered down.

DAC Data-Word Width
These two bits set the word width of the DAC data. Compact disk (CD) compatibility may require 16 bits, but many modern digital audio formats require 24-bit sample resolution.

DAC Data Format
The AD1838A serial data interface can be configured to be compatible with a choice of popular interface formats, including I^2S, LJ, RJ, or DSP modes. Details of these interface modes are given in the Serial Data Port section.

De-emphasis
The AD1838A provides built-in de-emphasis filtering for the three standard sample rates of 32.0 kHz, 44.1 kHz, and 48 kHz.

Mute DAC
Each of the six DACs in the AD1838A has its own independent mute control. Setting the appropriate bit mutes the DAC output. The AD1838A uses a clickless mute function that attenuates the output to approximately –100 dB over a number of cycles.

Stereo Replicate
Setting this bit copies the digital data sent to the stereo pair DAC1 to the three other stereo DACs in the system. This allows all three stereo DACs to be driven by one digital data stream. Note that in this mode, DAC data sent to the other DACs is ignored.

DAC Volume Control
Each DAC in the AD1838A has its own independent volume control. The volume of each DAC can be adjusted in 1024 linear steps by programming the appropriate register. The default value for this register is 1023, which provides no attenuation, i.e., full volume.

ADC Control Registers

The AD1838A register map has five registers that are used to control the functionality and to read the status of the ADCs. The function of the bits in each of these registers is discussed below.

ADC Peak Level
These two registers store the peak ADC result from each channel when the ADC peak readback function is enabled. The peak result is stored as a 6-bit number from 0 dB to –63 dB in 1 dB steps. The value contained in the register is reset once it has been read, allowing for continuous level adjustment as required. Note that the ADC peak level registers use the 6 MSB in the register to store the results.

Sample Rate
This bit controls the sample rate of the ADCs. Based on a 24.576 MHz IMCLK, sample rates of 48 kHz and 96 kHz are available. The MCLK scaling bits in ADC Control Register 3 should be programmed appropriately based on the master clock frequency.

ADC Power-Down
This bit controls the power-down status of the ADC section and operates in a similar manner to the DAC power-down.

High-Pass Filter
The ADC signal path has a digital high-pass filter. Enabling this filter removes the effect of any dc offset in the analog input signal from the digital output codes.

ADC Data-Word Width
These two bits set the word width of the ADC data.

ADC Data Format
The AD1838A serial data interface can be configured to be compatible with a choice of popular interface formats, including I^2S, LJ, RJ, or DSP modes.

Master/Slave Auxiliary Mode
When the AD1838A is operating in the auxiliary mode, the auxiliary ADC control pins, AUXBCLK and AUXLRCLK, which connect to the external ADCs, can be set to operate as a master or slave. If the pins are set in slave mode, one of the external ADCs should provide the LRCLK and BCLK signals.

ADC Peak Readback
Setting this bit enables ADC peak reading. See the ADCs section for more information.

Table V. Control Register Map

Register Address	Register Name	Description	Type	Width	Reset Setting (Hex)
0000	DACCTRL1	DAC Control 1	R/$\overline{W}$	10	000
0001	DACCTRL2	DAC Control 2	R/$\overline{W}$	10	000
0010	DACVOL1	DAC Volume—Left 1	R/$\overline{W}$	10	3FF
0011	DACVOL2	DAC Volume—Right 1	R/$\overline{W}$	10	3FF
0100	DACVOL3	DAC Volume—Left 2	R/$\overline{W}$	10	3FF
0101	DACVOL4	DAC Volume—Right 2	R/$\overline{W}$	10	3FF
0110	DACVOL5	DAC Volume—Left 3	R/$\overline{W}$	10	3FF
0111	DACVOL6	DAC Volume—Right 3	R/$\overline{W}$	10	3FF
1000	Reserved	Reserved	R/$\overline{W}$	10	Reserved
1001	Reserved	Reserved	R/$\overline{W}$	10	Reserved
1010	ADCPeak0	ADC Left Peak	R	6	000
1011	ADCPeak1	ADC Right Peak	R	6	000
1100	ADCCTRL1	ADC Control 1	R/$\overline{W}$	10	000
1101	ADCCTRL2	ADC Control 2	R/$\overline{W}$	10	000
1110	ADCCTRL3	ADC Control 3	R/$\overline{W}$	10	000
1111	Reserved	Reserved	R/$\overline{W}$	10	Reserved

Table VI. DAC Control 1

				Function			
Address	R/$\overline{W}$	RES	De-emphasis	DAC Data Format	DAC Data-Word Width	Power-Down Reset	Sample Rate
15, 14, 13, 12	11	10	9, 8	7, 6, 5	4, 3	2	1, 0
0000	0	0	00 = None 01 = 44.1 kHz 10 = 32.0 kHz 11 = 48.0 kHz	000 = I^2S 001 = RJ 010 = DSP 011 = LJ 100 = Packed 256 101 = Packed 128 110 = Reserved 111 = Reserved	00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = Reserved	0 = Normal 1 = Power-Down	00 = 48 kHz 01 = 96 kHz 10 = 192 kHz 11 = 48 kHz

Table VII. DAC Control 2

					Function							
					MUTE DAC							
Address	R/$\overline{W}$	RES	Reserved	Stereo Replicate	Reserved	Reserved	OUTR3	OUTL3	OUTR2	OUTL2	OUTR1	OUTL1
15, 14, 13, 12	11	10	9	8	7	6	5	4	3	2	1	0
0001	0	0	0	0 = Off 1 = Replicate	0	0	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute	0 = On 1 = Mute

Table VIII. DAC Volume Control

Address	R/$\overline{W}$	RES	Function: DAC Volume
15, 14, 13, 12	11	10	9, 8, 7, 6, 5, 4, 3, 2, 1, 0
0010 = DACL1 0011 = DACR1 0100 = DACL2 0101 = DACR2 0110 = DACL3 0111 = DACR3	0	0	0000000000 = Mute 0000000001 = 1/1023 0000000010 = 2/1023 1111111110 = 1022/1023 1111111111 = 1023/1023

Table IX. ADC Peak

Address	R/$\overline{W}$	RES	Function: Six Data Bits	Function: Four Fixed Bits
15, 14, 13, 12	11	10	9, 8, 7, 6, 5, 4	3, 2, 1, 0
1010 = Left ADC 1011 = Right ADC	1	0	000000 = 0 dBFS 000001 = –1 dBFS 000010 = –2 dBFS 111111 = –63 dBFS	0000 These four bits are always zero.

Table X. ADC Control 1

Address	R/$\overline{W}$	RES	Function: Reserved	Filter	ADC Power-Down	Sample Rate	Reserved
15, 14, 13, 12	11	10	9	8	7	6	5, 4, 3, 2, 1, 0
1100	0	0	0	0 = All Pass 1 = High-Pass	0 = Normal 1 = Power-Down	0 = 48 kHz 1 = 96 kHz	0, 0, 0, 0, 0, 0 0, 0, 0, 0, 0, 0

Table XI. ADC Control 2

Address	R/$\overline{W}$	RES	Function: Master/Slave Aux Mode	ADC Data Format	ADC Data-Word Width	AUXDATA	RES	ADC MUTE: Right	ADC MUTE: Left
15, 14, 13, 12	11	10	9	8, 7, 6	5, 4	3	2	1	0
1101	0	0	0 = Slave 1 = Master	000 = I^{2}S 001 = RJ 010 = DSP 011 = LJ 100 = Packed 256 101 = Packed 128 110 = Auxiliary 256 111 = Auxiliary 512 101 = Packed 128 110 = Auxiliary 256 111 = Auxiliary 512	00 = 24 Bits 01 = 20 Bits 10 = 16 Bits 11 = Reserved	0 = Off 1 = On	0	0 = On 1 = Mute	0 = On 1 = Mute

Table XII. ADC Control 3

Address	R/$\overline{W}$ RES	RES	Reserved	Function: IMCLK Clocking Scaling	ADC Peak Readback	DAC Test Mode	ADC Test Mode
15, 14, 13, 12	11	10	9, 8	7, 6	5	4, 3, 2	1, 0
1110	0	0	0, 0	00 = MCLK × 2 01 = MCLK 10 = MCLK × 2/3 11 = MCLK × 2	0 = Disabled Peak Readback 1 = Enabled Peak Readback	000 = Normal Mode All Others Reserved	00 = Normal Mode All Others Reserved

CASCADE MODE

Dual AD1838A Cascade

The AD1838A can be cascaded to an additional AD1838A, which, in addition to six external stereo ADCs and one external stereo DAC, can be used to create a 32-channel audio system with 16 inputs and 16 outputs. The cascade is designed to connect to a SHARC DSP and operates in a time division multiplexing (TDM) format. Figure 14 shows the connection diagram for cascade operation. The digital interface for both parts must be set to operate in Auxiliary 512 mode by programming ADC Control Register 2. AD1838A No. 1 is set as a master device by connecting the $\overline{M}$/S pin to DGND and AD1838A No. 2 is set as a slave device by connecting the $\overline{M}$/S to ODVDD. Both devices should be run from the same MCLK and $\overline{PD}$/$\overline{RST}$ signals to ensure that they are synchronized.

With Device 1 set as a master, it will generate the frame-sync and bit clock signals. These signals are sent to the SHARC and Device 2 ensuring that both know when to send and receive data.

The cascade can be thought of as two 256-bit shift registers, one for each device. At the beginning of a sample interval, the shift registers contain the ADC results from the previous sample interval. The first shift register (Device 1) clocks data into the SHARC and also clocks in data from the second shift register (Device 2). While this is happening, the SHARC is sending DAC data to the second shift register. By the end of the sample interval, all 512 bits of ADC data in the shift registers will have been clocked into the SHARC and been replaced by DAC data, which is subsequently written to the DACs. Figure 15 shows the timing diagram for the cascade operation.

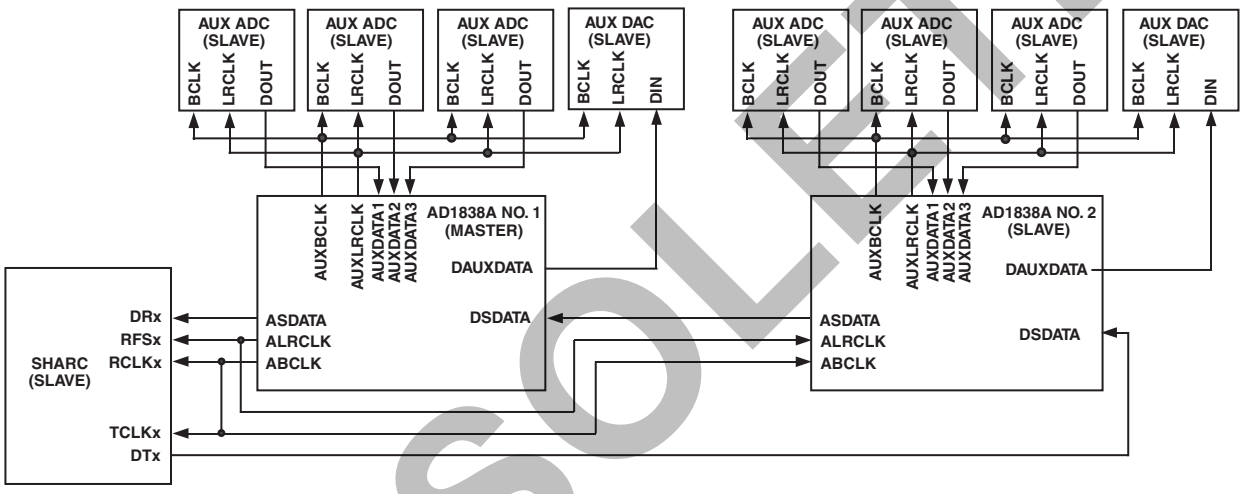


Figure 14. Dual AD1838A Cascade

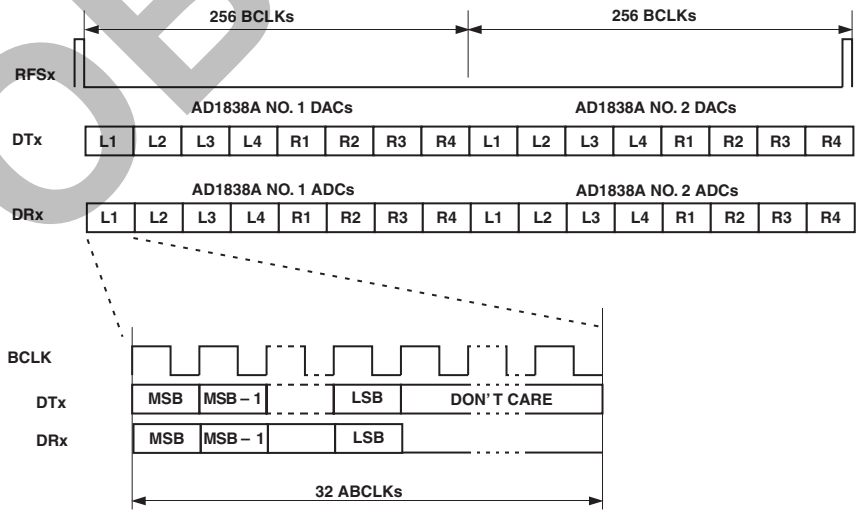


Figure 15. Dual AD1838A Cascade Timing

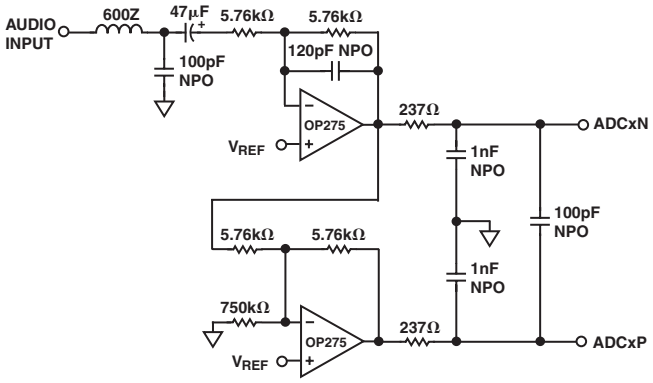


Figure 16. Typical ADC Input Filter Circuit

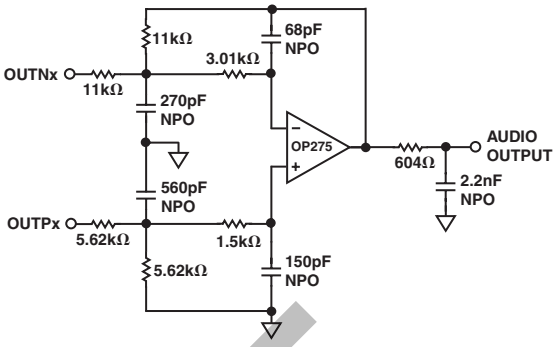
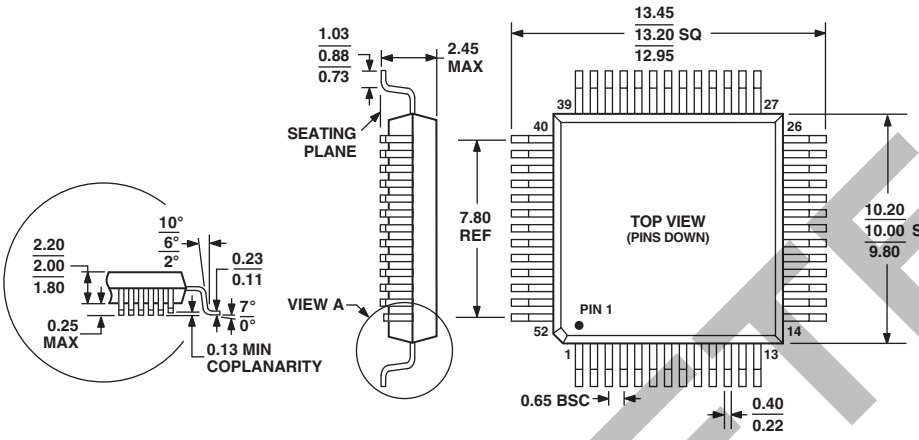


Figure 17. Typical DAC Output Filter Circuit

OUTLINE DIMENSIONS

52-Lead Metric Quad Flat Package [MQFP]
(S-52-1)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MS-022-AC.

C03626–0–2/04(A)

Revision History

Location	Page
2/04—Data Sheet changed from REV. 0 to REV. A.	
Changes to ORDERING GUIDE	6
Deleted Clock Signals section	11
Added AD1835A CLOCKING SCHEME section	11
Added Table II and Table III and renumbered following tables	11
Changes to Auxiliary (TDM Mode) section	13
Changes to Figure 5	14
Changes to Figure 6	14
Added Figures 7a and 8a	15
Renamed Figure 7 and Figure 8 to Figure 7b and Figure 8b	15
Changes to Figure 9	15
Changes to Table VIII	21
Updated OUTLINE DIMENSIONS	24