**LT8582**

**Dual 3A Boost/Inverting/SEPIC DC/DC Converter with Fault Protection**

**FEATURES**
- Dual 42V, 3A Combined Power Switch
- Master/Slave (1.7A/1.3A) Switch Design
- Wide Input Range: 2.5V to 22V Operating, 40V Maximum Transient
- Power Good Pin for Event Based Sequencing
- Switching Frequency Up to 2.5MHz
- Each Channel Easily Configurable as a Boost, SEPIC, Inverting or Flyback Converter
- Low VCESAT Switch: 270mV at 2.75A (Typical)
- Can be Synchronized to an External Clock
- Output Short-Circuit Protection
- High Gain SHDN Pin Accepts Slowly Varying Input Signals
- 24-Pin 7mm × 4mm DFN Package

**APPLICATIONS**
- Local Power Supply
- Vacuum Fluorescent Display (VFD) Bias Supplies
- TFT-LCD Bias Supplies
- Automotive Engine Control Unit (ECU) Power

**DESCRIPTION**

The LT®8582 is a dual independent channel PWM DC/DC converter with a power good pin and built-in fault protection to help guard against input overvoltage and overtemperature conditions. Each channel consists of a 42V master switch and a 42V slave switch that can be tied together for a total current limit of 3A.

The LT8582 is ideal for many local power supply designs. Each channel can be easily configured in boost, SEPIC, inverting, or flyback configurations. Together, the two channels can produce a 12V and a –12V output with 14.4W of combined output power from a 5V input. In addition, the LT8582’s slave switch allows the part to be configured in high voltage, high power charge pump topologies that are more efficient and require fewer components than traditional circuits.

The LT8582 also features innovative SHDN pin circuitry that allows for slowly varying input signals and an adjustable undervoltage lockout function. Additional features such as output short protection, frequency foldback and soft-start are integrated. The LT8582 is available in a 24-pin 7mm × 4mm DFN package.

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**TYPICAL APPLICATION**

1.5MHz, 5V to ±12V

**Efficiency and Power Loss**

( Load Between 12V and –12V Outputs )
LT8582

**ABSOLUTE MAXIMUM RATINGS**

(Note 1)

- $V_{IN1}$ Voltage: $-0.3V$ to $40V$
- SWA1/SWB1 Voltage: $-0.4V$ to $42V$
- RT1 Voltage: $-0.3V$ to $5V$
- SS1 Voltage: $-0.3V$ to $2.5V$
- FBX1 Voltage: $-0.3V$ to $5V$
- $V_{C1}$ Voltage: $-0.3V$ to $2V$
- SHDN1 Voltage: $-0.3V$ to $40V$
- SHDN1 Current: $-1mA$
- SYNC1 Voltage: $-0.3V$ to $5.5V$
- GATE1 Voltage: $-0.3V$ to $60V$
- PG1 Voltage: $-0.3V$ to $40V$
- PG1 Current: $\pm 0.5mA$
- CLKOUT1: (Note 5)

**Operating Junction Temperature Range**

- LT8582E: $-40°C$ to $125°C$
- LT8582I: $-40°C$ to $125°C$

**Storage Temperature Range**

- $-65°C$ to $150°C$

**Note:** Absolute maximum ratings are shown for channel 1 only. Channel 2 ratings are identical.

**PIN CONFIGURATION**

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**ORDER INFORMATION**

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT8582EDKD#PBF</td>
<td>LT8582EDKD#TRPBF</td>
<td>8582</td>
<td>24-Pin (7mm × 4mm) Plastic DFN</td>
<td>$-40°C$ to $125°C$</td>
</tr>
<tr>
<td>LT8582IDKD#PBF</td>
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</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). \( V_IN = 5V, V_{SHDN} = V_IN \), unless otherwise noted (Note 2). Specifications are identical for both channels unless noted otherwise.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Minimum Input Voltage ( V_{IN} )</td>
<td>●</td>
<td>2.3</td>
<td>2.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>( V_{IN} ) Overvoltage Lockout</td>
<td></td>
<td>22.2</td>
<td>24.5</td>
<td>27</td>
<td>V</td>
</tr>
<tr>
<td>Positive Feedback Voltage</td>
<td>●</td>
<td>1.185</td>
<td>1.204</td>
<td>1.220</td>
<td>V</td>
</tr>
<tr>
<td>Negative Feedback Voltage</td>
<td>●</td>
<td>2</td>
<td>7</td>
<td>16</td>
<td>mV</td>
</tr>
<tr>
<td>Positive FBX Pin Bias Current ( V_{FBX} ) = Positive Feedback Voltage, Current into Pin</td>
<td>●</td>
<td>81</td>
<td>83.3</td>
<td>85</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Negative FBX Pin Bias Current ( V_{FBX} ) = Negative Feedback Voltage, Current out of Pin</td>
<td>●</td>
<td>81</td>
<td>83.3</td>
<td>85.5</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>Error Amp Transconductance ( \Delta I = 10\mu A )</td>
<td></td>
<td>280</td>
<td>( \mu mhos )</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error Amp Voltage Gain</td>
<td></td>
<td>80</td>
<td>V/V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Quiescent Current ( V_{SHDN} = 2.5V ), Not Switching</td>
<td></td>
<td>2.1</td>
<td>2.5</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Quiescent Current in Shutdown ( V_{SHDN} = 0 )</td>
<td></td>
<td>0</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>Reference Line Regulation ( 2.5V \leq V_{IN} \leq 20V )</td>
<td></td>
<td>0.01</td>
<td>0.05</td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td>Switching Frequency, ( f_{OSC} ) ( R_f = 31.6k\Omega ) ( R_f = 407k\Omega )</td>
<td></td>
<td>2.125</td>
<td>2.5</td>
<td>2.875</td>
<td>MHz</td>
</tr>
<tr>
<td>Switching Frequency in Foldback Compared to Normal ( f_{OSC} )</td>
<td></td>
<td>1/6</td>
<td>ratio</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Switching Frequency Range Free-Running or Synchronizing</td>
<td></td>
<td>200</td>
<td>2500</td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>SYNC High Level for Sync</td>
<td></td>
<td>1.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNC Low Level for Sync</td>
<td></td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SYNC Clock Pulse Duty Cycle ( V_{SYNC} = 0V ) to 2V</td>
<td></td>
<td>20</td>
<td>80</td>
<td>%</td>
<td></td>
</tr>
<tr>
<td>Recommended Min SYNC Ratio ( I_{SYNC}/I_{OSC} )</td>
<td></td>
<td>3/4</td>
<td>ratio</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum Off-Time</td>
<td></td>
<td>45</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Minimum On-Time</td>
<td></td>
<td>55</td>
<td>ns</td>
<td></td>
<td></td>
</tr>
<tr>
<td>SWA Current Limit Minimum Duty Cycle</td>
<td></td>
<td>1.8</td>
<td>2.4</td>
<td>3</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td></td>
<td>1.3</td>
<td>1.8</td>
<td>2.5</td>
<td>A</td>
</tr>
<tr>
<td>SWA FAULT Current Limit Minimum Duty Cycle</td>
<td></td>
<td>2.2</td>
<td>2.8</td>
<td>3.5</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Duty Cycle</td>
<td></td>
<td>1.6</td>
<td>2.3</td>
<td>3.0</td>
<td>A</td>
</tr>
<tr>
<td>SW Current Sharing, ( ISWB/ISWA ) SWA and SWB Tied Together</td>
<td></td>
<td>0.79</td>
<td>A/A</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( SWA + SWB ) Current Limit Minimum Duty Cycle, ( ISWB/ISWA = 0.79 )</td>
<td></td>
<td>3.3</td>
<td>4.3</td>
<td>5.4</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Duty Cycle, ( ISWB/ISWA = 0.79 )</td>
<td></td>
<td>2.3</td>
<td>4.1</td>
<td>4.5</td>
<td>A</td>
</tr>
<tr>
<td>( SWA + SWB ) FAULT Current Limit Minimum Duty Cycle, ( ISWB/ISWA = 0.79 )</td>
<td></td>
<td>4</td>
<td>5</td>
<td>6.3</td>
<td>A</td>
</tr>
<tr>
<td>Maximum Duty Cycle, ( ISWB/ISWA = 0.79 )</td>
<td></td>
<td>2.8</td>
<td>4</td>
<td>5.4</td>
<td>A</td>
</tr>
<tr>
<td>Switch ( V_{CESAT} )</td>
<td>( I_{SWA} + I_{SWB} = 2.75A )</td>
<td></td>
<td>270</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>SWA Leakage Current ( V_{SWA} = 5V, V_{SHDN} = 0 )</td>
<td></td>
<td>0.01</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>SWB Leakage Current ( V_{SWB} = 5V, V_{SHDN} = 0 )</td>
<td></td>
<td>0.01</td>
<td>1</td>
<td>( \mu A )</td>
<td></td>
</tr>
<tr>
<td>SS Charge Current ( V_{SS} = 30mV ), Current Flows out of SS Pin</td>
<td></td>
<td>5.7</td>
<td>8.8</td>
<td>11.7</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>SS Discharge Current Part in FAULT, ( V_{SS} = 2.1V ), Current Flows into SS Pin</td>
<td></td>
<td>5.7</td>
<td>8.8</td>
<td>11.7</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>SS High Detection Voltage Part in FAULT</td>
<td></td>
<td>1.65</td>
<td>1.84</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>SS Low Detection Voltage Part Exiting FAULT</td>
<td></td>
<td>15</td>
<td>55</td>
<td>100</td>
<td>mV</td>
</tr>
<tr>
<td>SHDN Minimum Input Voltage High Active Mode, ( SHDN ) Rising</td>
<td></td>
<td>1.26</td>
<td>1.31</td>
<td>1.4</td>
<td>V</td>
</tr>
<tr>
<td>Active Mode, ( SHDN ) Falling</td>
<td></td>
<td>1.21</td>
<td>1.27</td>
<td>1.35</td>
<td>V</td>
</tr>
<tr>
<td>SHDN Input Voltage Low Shutdown Mode</td>
<td></td>
<td>0.3</td>
<td>V</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

The \( \bullet \) denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). \( V_{IN} = 5V \), \( V_{SHDN} = V_{IN} \), unless otherwise noted (Note 2). Specifications are identical for both channels unless noted otherwise.

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<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>SHDN Pin Bias Current</td>
<td>( V_{SHDN} = 3V )</td>
<td>10.1</td>
<td>12.1</td>
<td>14.1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>( V_{SHDN} = 1.3V )</td>
<td>0</td>
<td>0.1</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>( V_{SHDN} = 0V )</td>
<td>12.1</td>
<td>14.1</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>CLKOUT Output Voltage High</td>
<td>1mA out of CLKOUT Pin</td>
<td>1.9</td>
<td>2.1</td>
<td>2.3</td>
<td>V</td>
</tr>
<tr>
<td>CLKOUT Output Voltage Low</td>
<td>1mA into CLKOUT Pin</td>
<td>30</td>
<td>200</td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>CLKOUT1 Duty Cycle</td>
<td>All ( T_J )</td>
<td>50</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>CLKOUT2 Duty Cycle</td>
<td>( T_J = -40^\circ C )</td>
<td>22.5</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>( T_J = 25^\circ C )</td>
<td>42</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td>( T_J = 125^\circ C )</td>
<td>72</td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td>CLKOUT Rise Time</td>
<td>( C_{CLKOUT} = 120pF )</td>
<td>25</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>CLKOUT Fall Time</td>
<td>( C_{CLKOUT} = 120pF )</td>
<td>15</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>GATE Pull-Down Current</td>
<td>( V_{GATE} = 3V )</td>
<td>( \bullet )</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>( V_{GATE} = 20V )</td>
<td></td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
</tr>
<tr>
<td>GATE Leakage Current</td>
<td>( V_{GATE} = 50V ), GATE Off</td>
<td>0.01</td>
<td></td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>PG Threshold for Positive Feedback Voltage</td>
<td>( V_{FBX} ) Rising</td>
<td>1.09</td>
<td>1.15</td>
<td>1.20</td>
<td>V</td>
</tr>
<tr>
<td>PG Threshold for Negative Feedback Voltage</td>
<td>( V_{FBX} ) Falling</td>
<td>20</td>
<td>65</td>
<td>120</td>
<td>mV</td>
</tr>
<tr>
<td>PG Hysteresis for Feedback Voltage</td>
<td></td>
<td>4</td>
<td></td>
<td></td>
<td>mV</td>
</tr>
<tr>
<td>PG Output Voltage Low</td>
<td>100( \mu A ) into PG Pin, ( V_{FBX} = 1V )</td>
<td>( \bullet )</td>
<td>70</td>
<td>150</td>
<td>mV</td>
</tr>
<tr>
<td>PG Leakage Current</td>
<td>( V_{PG} = 40V ), ( V_{FBX} = 1.204V )</td>
<td>0.01</td>
<td></td>
<td>1</td>
<td>( \mu A )</td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT8582E is guaranteed to meet performance specifications from \( 0^\circ C \) to \( 125^\circ C \) junction temperature. Specifications over the \( -40^\circ C \) to \( 125^\circ C \) operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT8582I is guaranteed over the full \( -40^\circ C \) to \( 125^\circ C \) operating junction temperature range.

**Note 3:** Current limit guaranteed by design and/or correlation to static test.

**Note 4:** This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed \( 125^\circ C \) when overtemperature protection is active. Continuous operation over the specified maximum operating junction temperature may impair device reliability.

**Note 5:** Do not apply a positive or negative voltage or current source to CLKOUT, otherwise permanent damage may occur.
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C \), unless otherwise noted.

- **Switch Current Limit vs Duty Cycle**
- **Switch Saturation Voltage**
- **Switch Current Sharing**

- **Switch Current Limit at Minimum Duty Cycle**
- **Commanded Current Limit vs SS Voltage**
- **CLKOUT Duty Cycle**

- **Oscillator Frequency**
- **Switching Frequency During Soft-Start**
- **Gate Pin Current \( (V_{SS} = 2.1V) \)**
TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = 25^\circ C$, unless otherwise noted.

**Gate Pin Current ($V_{GATE} = 5V$)**

**Positive Feedback Voltage**

**Active/Lockout Threshold**

**SHDN Pin Current**

**SHDN Pin Current**

**Internal UVLO**

**CLKOUT Rise and Fall Times at 1MHz**

**$V_{IN}$ Overvoltage Lockout**

**PG Threshold**
PIN FUNCTIONS (CH1/CH2)

FBX1, FBX2 (Pin 6/Pin 7): Positive and Negative Feedback Pins. For an inverting or noninverting output converter, tie a resistor from the FBX pin to VOUT according to the following equations:

\[ R_{FBX} = \left( \frac{V_{OUT} - 1.204V}{83.3 \mu A} \right); \text{Noninverting Converter} \]

\[ R_{FBX} = \left( \frac{|V_{OUT}| + 7mV}{83.3 \mu A} \right); \text{Inverting Converter} \]

VC1, VC2 (Pin 5/Pin 8): Error Amplifier Output Pins. Tie external compensation network to these pins.

GATE1, GATE2 (Pin 4/Pin 9): PMOS Gate Drive Pins. The GATE pin is a pull-down current source and can be used to drive the gate of an external PMOS transistor for output short-circuit protection or output disconnect. The GATE pin current increases linearly with the SS pin voltage, with a maximum pull-down current of 1mA at SS voltages exceeding 550mV. Note that if the SS voltage is greater than 550mV and the GATE pin voltage is less than 2V, the GATE pin looks like a 2kΩ impedance to ground. See the Appendix for more information.

PG1, PG2 (Pin 3/Pin 10): Power Good Indication Pins. This active high pin indicates that the FBX pin voltage for the corresponding channel is within 4% of its regulation voltage (VFBX > 1.15V for noninverting outputs or VFBX < 65mV for inverting outputs). For most applications, a 4% change in VFBX corresponds to an 8% change in VOUT. This open drain output requires a pull-up resistor to indicate power good. Also, the status is valid only when SHDN > 1.31V and VIN > 2.3V.

VIN1, VIN2 (Pin 2/Pin 11): Input Supply Pins. Must be locally bypassed.

SWA1, SWA2 (Pin 1/Pin 12): Master Switch Pins. This is the collector of the internal master NPN power switch for each channel. SWA is designed to handle a peak collector current of 1.7A (minimum). Minimize the metal trace area connected to this pin to minimize EMI.

SWB1, SWB2 (Pin 24/Pin 13): Slave Switch Pins. This is the collector of the internal slave NPN power switch for each channel. SWB is designed to handle a peak collector current of 1.3A (minimum). Minimize the metal trace area connected to this pin to minimize EMI.

CLKOUT1, CLKOUT2 (Pin 23/Pin 14): Clock Output Pins. Use these pins to synchronize one or more other ICs to either channel of the LT8582. Can also be used to synchronize channel 1 or channel 2 of the LT8582 with the other channel of the LT8582. This pin oscillates at the same frequency as the internal oscillator of the part or, if active, the SYNC pin. The CLKOUT pin signal on CH1 is 180° out of phase with the internal oscillator or SYNC pin and the duty cycle is fixed at ~50%. The CLKOUT pin signal on CH2 is in phase with the internal oscillator or SYNC pin and the duty cycle varies linearly with the part’s junction temperature. Note that CLKOUT of either channel is only meant to drive capacitive loads up to 120pF.

SHDN1, SHDN2 (Pin 22/Pin 15): Shutdown Pins. In conjunction with the UVLO (undervoltage lockout) circuit, these pins are used to enable/disable the channel and restart the soft-start sequence. Drive below 0.3V to disable the channel with very low quiescent current. Drive above 1.31V (typical) to activate the channel and restart the soft-start sequence. Do not float these pins.

RT1, RT2 (Pin 21/Pin 16): Timing Resistor Pins. Adjusts the switching frequency of the corresponding channel. Place a resistor from these pins to ground to set the frequency to a fixed free running level. Do not float these pins.

SS1, SS2 (Pin 20/Pin 17): Soft-Start Pins. Place a soft-start capacitor here. Upon start-up, the SS pins will be charged by a (nominally) 250k resistor to ~2.1V. During a fault, the SS pin for the corresponding channel will be slowly charged up and discharged as part of a timeout sequence (see the State Diagram for more information).

SYNC1, SYNC2 (Pin 19/Pin 18): Use to synchronize the switching frequency of a channel to an outside clock. The high voltage level of the clock must exceed 1.3V and the low level must be less than 0.4V. Drive these pins to less than 0.4V to revert to the internal free running clock for the corresponding channel. See the Applications Information section for more information.

GND (Exposed Pad Pin 25): Ground. Exposed pad must be soldered directly to local ground plane.
**Figure 1. Block Diagram**

**LT8582**

**BLOCK DIAGRAM**

**Note:** BLOCK DIAGRAM FOR CH1 IS SHOWN. BLOCK DIAGRAM FOR CH2 IS IDENTICAL, EXCEPT CLKOUT SIGNAL FOR CH1 IS 180° OUT OF PHASE WITH THE INTERNAL OSCILLATOR AND HAS A FIXED 50% DUTY CYCLE AND CLKOUT SIGNAL FOR CH2 IS IN PHASE WITH THE INTERNAL OSCILLATOR AND ITS DURY CYCLE VARIES LINEARLY WITH THE PART'S JUNCTION TEMPERATURE.
Figure 2. State Diagram
**OPERATION**

**OPERATION – OVERVIEW**

The LT8582 uses a constant frequency, current mode control scheme to provide excellent line and load regulation. Each channel’s undervoltage lockout (UVLO) function, together with soft-start and frequency foldback, offer a controlled means of starting up. Fault features are incorporated into each channel of the LT8582 to facilitate the detection of output shorts, overvoltage and overtemperature conditions. Please refer to the Block Diagram (Figure 1) and the State Diagram (Figure 2) for the following description of the part’s operation.

**OPERATION – START-UP**

Several functions are provided to enable a very clean start-up of both channels of the LT8582.

**Precise Turn-On Voltage**

The SHDN pin on each channel is compared to an internal voltage reference to give a precise turn on voltage level. Taking each SHDN pin above 1.31V enables the corresponding channel. Taking each SHDN pin below 300mV shuts down the channel, resulting in extremely low quiescent current for that channel. The SHDN pin has 35mV of hysteresis to protect against glitches and slow ramping.

**Configurable Undervoltage Lockout (UVLO)**

The SHDN pin can also be used to create a configurable UVLO for each channel. This function sets the turn on/off of each of LT8582’s channels at a desired voltage (VINUVLO). Figure 3 shows how a resistor divider (or a single resistor) from VIN to the SHDN pin can be used to program VINUVLO. RUVLO2 is optional. If left out, set it to infinite in the equation below. For increased accuracy, set RUVLO2 ≤ 10k. Pick RUVLO1 as follows:

\[
R_{UVLO1} = \frac{VIN_{UVLO} - 1.31V}{\left(\frac{1.31V}{R_{UVLO2}}\right) + 12.3\mu A}
\]

**Internal Undervoltage Lockout (UVLO)**

Regardless of where external circuitry sets VINUVLO, the LT8582 also has internal UVLO circuitry that disables the chip when VIN < 2.3V (typical).

**Soft-Start of Switch Current**

The soft-start circuitry provides for a gradual ramp-up of the switch current in each channel (refer to Commanded Current Limit vs SS Voltage in Typical Performance Characteristics). When the channel is taken out of shutdown, the external SS capacitor is first discharged. This resets the state of the logic circuits in the channel. Then an integrated 250k resistor pulls the channel’s SS pin to ~1.84V. The ramp rate of the SS pin voltage is set by this 250k resistor and the external capacitor connected to this pin. Once SS gets to ~1.84V, the CLKOUT pin is enabled and an internal regulator pulls the pin up quickly to ~2.1V. Typical values for the external soft-start capacitor range from 100nF to 1μF.

**Soft-Start of External PMOS (if used)**

The soft-start circuitry also gradually ramps up the GATE pin pull-down current for the corresponding channel. This allows an external PMOS to slowly turn on (M1 in Block Diagram). The GATE pin current increases linearly with SS voltage, with a maximum current of 1mA when the SS voltage gets above 550mV. Note that if the GATE pin voltage is less than 2V for SS voltages exceeding 550mV, then the GATE pin impedance to ground is 2kΩ. The soft turn on of the external PMOS helps limit inrush current at start up, making hot plugs of LT8582s feasible.
OPERATION

Sample Mode
Sample mode is the mechanism used by the LT8582 to aid in the detection of output shorts. It refers to a state of the LT8582 where the master and slave power switches (Q1 and Q2) are turned on for a minimum period of time every clock cycle (or every few clock cycles in frequency foldback) in order to sample the inductor current. If the sampled current through Q1 exceeds the master switch fault current limit of 2A (minimum), the LT8582 triggers an overcurrent fault internally for that channel (see Operation – Fault section for details). Sample mode exists when FBX for that channel is out of regulation by more than 4% (65mV < FBX < 1.15V). During this mode, PG will be pulled low.

Frequency Foldback
The frequency foldback circuit reduces the switching frequency for that channel when 144mV < FBX < 1.03V (typical). This feature lowers the minimum duty cycle that the channel can achieve, thus allowing better control of the inductor current during start-up. When the FBX voltage is pulled outside of the above mentioned range, the switching frequency for that channel returns to normal.

Note that the peak inductor current at start-up is a function of many variables including load profile, output capacitance, target V_OUT, V_IN, switching frequency, etc.

OPERATION – REGULATION
The following description of the LT8582’s operation assumes that the FBX voltage is close enough to its regulation target so that the part is not in sample mode. Also, this description applies equally to both channels independently of each other. Use the Block Diagram as a reference when stepping through the following description of the LT8582 operating in regulation.

At the start of each oscillator cycle, the SR latch (SR1) is set, which turns on the power switches Q1 and Q2. The collector current through the master switch, Q1, is ~1.3 times the collector current through the slave switch, Q2, when the collectors of the two switches are tied together. Q1’s emitter current flows through a current sense resistor (R_S) generating a voltage proportional to the switch current. This voltage (amplified by A4) is added to a stabilizing ramp and the resulting sum is fed into the positive terminal of the PWM comparator A3. When the voltage on the positive input of A3 exceeds the voltage on the negative input, the SR latch is reset, turning off the master and slave power switches. The voltage on the negative input of A3 (V_C pin) is set by A1 (or A2), which is simply an amplified difference between the FBX pin voltage and the reference voltage (1.204V if the LT8582 is configured as a noninverting converter, or 7mV if configured as an inverting converter). In this manner, the error amplifier sets the correct peak current level to maintain output regulation.

As long as the channel is not in fault and the SS pin exceeds 1.84V, the LT8582 drives the CLKOUT pin for that channel at the frequency set by the RT pin or the SYNC pin. The CLKOUT pin can synchronize other ICs, including additional LT8582s or the other channel of an LT8582, up to 120pF load on CLKOUT. For channel 1, CLKOUT1 has a fixed duty cycle and is 180° out of phase with the internal clock. For channel 2, CLKOUT2’s duty cycle varies linearly with channel 2’s junction temperature and may be used as a temperature monitor.

OPERATION – FAULT
Each of the following events can trigger a fault in the LT8582:

1. SW Overcurrent:
   a. I_{SWA} > 2A (minimum)
   b. (I_{SWA} + I_{SWB}) > 3.5A (minimum)
2. V_IN Voltage > 22.2V (minimum)
3. Die Temperature > 165°C
OPERATION

Refer to the State Diagram (Figure 2) for the following description of the LT8582’s operation during a fault event. When a fault is detected on a channel, the LT8582 disables the CLKOUT pin for that channel, turns off the power switches for that channel and the GATE pin for that channel becomes high impedance. The external PMOS, M1, is turned off by the external RGATE resistor (see Block Diagram). With the external PMOS turned off, the power path from VIN to VOUT is opened, protecting power path components. Also, as soon as the feedback voltage falls inside the range 65mV < FBX < 1.15V, PG pulls low. Refer to Figure 4 for the case of an output short.

At the beginning of a fault event, a timeout sequence commences where the SS pin for that channel is charged up to 1.84V (the SS pin will continue charging up to ~2.1V and be held there in the case of a FAULT event that still exists) and then discharged to 55mV. This timeout period relieves the chip, the PMOS and other power path components from electrical and thermal stress for a minimum amount of time set by the voltage ramp rate on the SS pin.

OPERATION – CURRENT LIMIT

The current limit operates independently of the FAULT current limit. The current limit sets a maximum switch current. This switch current limit is duty cycle dependent, but for most applications will be around 3A minimum (see the Electrical Characteristics). Once this limit is reached, the switch duty cycle decreases, reducing the magnitude of the output voltage. If, despite the reduced duty cycle the switch current reaches the FAULT current limit, the part will behave as described in the Operation – Fault section.

Figure 4. Output Short-Circuit Protection of the LT8582
APPLICATIONS INFORMATION

Boost Converter Component Selection

Table 1. Boost Converter Design Equations

<table>
<thead>
<tr>
<th>Step</th>
<th>Equations</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 1: Inputs</td>
<td>Choose $V_{IN}$, $V_{OUT}$ and $f_{OSC}$ to calculate equations below.</td>
</tr>
<tr>
<td>Step 2: DC</td>
<td>$DC \equiv \frac{V_{OUT} - V_{IN} + 0.5V}{V_{OUT} + 0.5V - 0.3V}$</td>
</tr>
<tr>
<td>Step 3: L1</td>
<td>$L_{TYP} = \frac{(V_{IN} - 0.3) \cdot DC}{f_{OSC} \cdot 1A}$ (1)</td>
</tr>
<tr>
<td></td>
<td>$L_{MIN} = \frac{(V_{IN} - 0.3V) \cdot (2 \cdot DC - 1)}{1.7A \cdot f_{OSC} \cdot (1 - DC)}$ (2)</td>
</tr>
<tr>
<td></td>
<td>$L_{MAX} = \frac{(V_{IN} - 0.3V) \cdot DC}{f_{OSC} \cdot 0.18A}$ (3)</td>
</tr>
<tr>
<td>Step 4: $I_{RIPPLE}$</td>
<td>$I_{RIPPLE} = \frac{(V_{IN} - 0.3V) \cdot DC}{f_{OSC} \cdot L_{1}}$</td>
</tr>
<tr>
<td>Step 5: $I_{OUT}$</td>
<td>$I_{OUT} = \left( \frac{3A - I_{RIPPLE}}{2} \right) \cdot (1 - DC)$</td>
</tr>
<tr>
<td>Step 6: $D1$</td>
<td>$V_R \geq V_{OUT}; I_{AVG} \geq I_{OUT}$</td>
</tr>
<tr>
<td>Step 7: $C_{OUT}$</td>
<td>$C_{OUT1} = C_{OUT2}$</td>
</tr>
<tr>
<td></td>
<td>$I_{OUT \cdot DC} \geq f_{OSC} (0.01 \cdot V_{OUT} - 0.5 \cdot I_{OUT \cdot R_{DSON_PMOS}})$</td>
</tr>
<tr>
<td></td>
<td>- If PMOS is not used, then use just one capacitor where $C_{OUT} = C_{OUT1} + C_{OUT2}$</td>
</tr>
<tr>
<td>Step 8: $C_{IN}$</td>
<td>$C_{IN} \geq C_{VIN} + C_{PWR} \geq \frac{3A \cdot DC}{50 \cdot f_{OSC} \cdot 0.005 \cdot V_{IN} + \frac{I_{RIPPLE}}{8 \cdot f_{OSC} \cdot 0.005 \cdot V_{IN}}}$</td>
</tr>
<tr>
<td>Step 9: $R_{FBX}$</td>
<td>$R_{FBX} = \left( \frac{V_{OUT} - 1.204V}{83.3 \mu A} \right)$</td>
</tr>
<tr>
<td>Step 10: $R_T$</td>
<td>$R_T = \frac{81.6}{f_{OSC}}$</td>
</tr>
<tr>
<td>Step 11: PMOS</td>
<td>Only needed for input or output disconnect. See PMOS Selection in the Appendix for information on sizing the PMOS and the biasing resistor, $R_{GATE}$ and picking appropriate UVLO components.</td>
</tr>
</tbody>
</table>

Note 1: Above equations use numbers good for many applications but for more exact results use the equations from the appendix with numbers from the Electrical Characteristics.

Note 2: The final values for $C_{OUT1}, C_{OUT2}$ and $C_{IN}$ may deviate from the above equations in order to obtain desired load transient performance.

Figure 5. Boost Converter – The Component Values Given Are Typical Values for a 1.5MHz, 5V to 12V Boost

Each channel of the LT8582 can be configured as a boost converter as in Figure 5. This topology allows for positive output voltages that are higher than the input voltage. An external PMOS (optional) driven by the GATE pin of the LT8582 can achieve input or output disconnect during a FAULT event, SHDN < 1.31V, or $V_{IN}$ < 2.3V. Figure 5 shows the configuration for output disconnect. A single feedback resistor sets the output voltage. For output voltages higher than 40V, see the Charge Pump Topology in the Charge Pump Aided Regulators section.

Table 1 is a step-by-step set of equations to calculate component values for the LT8582 when operating as a boost converter. Input parameters are input and output voltage and switching frequency ($V_{IN}$, $V_{OUT}$ and $f_{OSC}$ respectively). Refer to the Appendix for further information on the design equations presented in Table 1.

Variable Definitions:

- $V_{IN}$ = Input Voltage
- $V_{OUT}$ = Output Voltage
- DC = Power Switch Duty Cycle
- $f_{OSC}$ = Switching Frequency
- $I_{OUT}$ = Maximum Output Current
- $I_{RIPPLE}$ = Inductor Ripple Current
- $R_{DSON\_PMOS}$ = $R_{DSON}$ of External Output PMOS (set to 0 if not using PMOS)
SEPIC Converter Component Selection – Coupled or Uncoupled Inductors

Each channel of the LT8582 can also be configured as a SEPIC as shown in Figure 6. This topology allows for positive output voltages that are lower, equal, or higher than the input voltage. Output disconnect is inherently built into the SEPIC topology, meaning no DC path exists between the input and output due to capacitor C1. Therefore the external PMOS is not required.

Table 2 is a step-by-step set of equations to calculate component values for the LT8582 when operating as a SEPIC converter. Input parameters are input and output voltage and switching frequency (VIN, VOUT and fOSC respectively). Refer to the Appendix for further information on the design equations presented in Table 2.

Variable Definitions:
VIN = Input Voltage
VOUT = Output Voltage
DC = Power Switch Duty Cycle
fOSC = Switching Frequency
IOUT = Maximum Output Current
IRIPPLE = Inductor Ripple Current

Table 2. SEPIC Design Equations

<table>
<thead>
<tr>
<th>PARAMETERS/EQUATIONS</th>
<th>Step 1: Inputs</th>
<th>Choose VIN, VOUT and fOSC to calculate equations below.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 2: DC</td>
<td>DC = ( \frac{V_{OUT} + 0.5V}{V_{IN} + V_{OUT} + 0.5V - 0.3V} )</td>
<td></td>
</tr>
<tr>
<td>Step 3: L</td>
<td>( L_{\text{TYP}} = \frac{(V_{IN} - 0.3V) \cdot DC}{fOSC \cdot 1A} ) (1)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( L_{\text{MIN}} = \frac{(V_{IN} - 0.3V) \cdot (2 \cdot DC - 1)}{1.7A \cdot fOSC \cdot (1 - DC)} ) (2)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>( L_{\text{MAX}} = \frac{(V_{IN} - 0.3V) \cdot DC}{fOSC \cdot 0.18A} ) (3)</td>
<td></td>
</tr>
</tbody>
</table>

- Solve equations 1, 2 and 3 for a range of L values
- The minimum of the L value range is the higher of \( L_{\text{TYP}} \) and \( L_{\text{MIN}} \)
- The maximum of the L value range is \( L_{\text{MAX}} \)
- \( L = L_1 = L_2 \) for coupled inductors.
- \( L = L_1 || L_2 \) for uncoupled inductors.

| Step 4: IRIPPLE       | \( I_{RIPPLE} = \frac{(V_{IN} - 0.3V) \cdot DC}{fOSC \cdot L} \) |
| Step 5: IOUT          | \( I_{OUT} = \left( 3A - \frac{I_{RIPPLE}}{2} \right) \cdot (1 - DC) \) |
| Step 6: D1            | \( V_R \geq V_{IN} + V_{OUT}; I_{AVG} \geq I_{OUT} \) |
| Step 7: C1            | \( C_1 \geq 1\mu F; V_{RATING} \geq V_{IN} \) |
| Step 8: COUT          | \( C_{OUT} \geq \frac{I_{OUT} \cdot DC}{fOSC \cdot 0.005 \cdot V_{OUT}} \) |
| Step 9: CIN           | \( C_{IN} \geq C_{VIN} + C_{PWR} \geq \frac{3A \cdot DC}{50 \cdot fOSC \cdot 0.005 \cdot V_{IN} + 8 \cdot fOSC \cdot 0.005 \cdot V_{IN}} \cdot I_{RIPPLE} \) |
| Step 10: RFBX         | \( R_{FBX} = \left( \frac{V_{OUT} - 1.204V}{83.39A} \right) \) |
| Step 11: RT           | \( R_T = \frac{81.6}{fOSC} - 1\cdot fOSC \text{ in MHz, } R_T \text{ in k}\Omega \) |

Note 1: Above equations use numbers good for many applications but for more exact results use the equations from the appendix with numbers from the Electrical Characteristics.

Note 2: The final values for \( C_{OUT} \) and \( C_{IN} \) may deviate from the above equations in order to obtain desired load transient performance.
APPLICATIONS INFORMATION

Dual Inductor Inverting Converter Component Selection – Coupled or Uncoupled Inductors

Figure 7. Dual Inductor Inverting Converter – The Component Values Given Are Typical Values for a 1.5MHz, 5V to –12V Inverting Topology Using Coupled Inductors

Table 3. Dual Inductor Inverting Design Equations

<table>
<thead>
<tr>
<th>Step 1: Inputs</th>
<th>Choose ( V_{IN} ), ( V_{OUT} ) and ( f_{OSC} ) to calculate equations below.</th>
</tr>
</thead>
<tbody>
<tr>
<td>Step 2: DC</td>
<td>( DC = \frac{</td>
</tr>
<tr>
<td>Step 3: L</td>
<td>( L_{\text{TYP}} = \frac{(V_{IN} - 0.3V) \cdot DC}{f_{OSC} \cdot 1A} ) (1)</td>
</tr>
<tr>
<td></td>
<td>( L_{\text{MIN}} = \frac{(V_{IN} - 0.3V) \cdot (2 \cdot DC - 1)}{1.7A \cdot f_{OSC} \cdot (1 - DC)} ) (2)</td>
</tr>
<tr>
<td></td>
<td>( L_{\text{MAX}} = \frac{(V_{IN} - 0.3V) \cdot DC}{f_{OSC} \cdot 0.18A} ) (3)</td>
</tr>
<tr>
<td></td>
<td>• Solve equations 1, 2 and 3 for a range of L values</td>
</tr>
<tr>
<td></td>
<td>• The minimum of the L value range is the higher of ( L_{\text{TYP}} ) and ( L_{\text{MIN}} )</td>
</tr>
<tr>
<td></td>
<td>• The maximum of the L value range is ( L_{\text{MAX}} )</td>
</tr>
<tr>
<td></td>
<td>• ( L = L_1 = L_2 ) for coupled inductors.</td>
</tr>
<tr>
<td></td>
<td>• ( L = L_1 \parallel L_2 ) for uncoupled inductors.</td>
</tr>
<tr>
<td>Step 4: ( I_{\text{RIPPLE}} )</td>
<td>( I_{\text{RIPPLE}} = \frac{(V_{IN} - 0.3V) \cdot DC}{f_{OSC} \cdot L} )</td>
</tr>
<tr>
<td>Step 5: ( I_{\text{OUT}} )</td>
<td>( I_{\text{OUT}} = \left(3A \cdot \frac{I_{\text{RIPPLE}}}{2}\right) \cdot (1 - DC) )</td>
</tr>
<tr>
<td>Step 6: ( D_1 )</td>
<td>( V_R &gt; V_{IN} +</td>
</tr>
<tr>
<td>Step 7: ( C_1 )</td>
<td>( C_1 \geq 1\mu\text{F}; V_{\text{RATING}} \geq V_{IN} +</td>
</tr>
<tr>
<td>Step 8: ( C_{\text{OUT}} )</td>
<td>( C_{\text{OUT}} \geq \frac{I_{\text{RIPPLE}}}{8 \cdot f_{OSC} \cdot 0.005 \cdot</td>
</tr>
<tr>
<td>Step 9: ( C_{\text{IN}} )</td>
<td>( C_{\text{IN}} \geq C_{\text{VIN}} + CPWR \geq 3A \cdot DC )</td>
</tr>
<tr>
<td></td>
<td>( \frac{50 \cdot f_{OSC} \cdot 0.005 \cdot V_{IN} + 8 \cdot f_{OSC} \cdot 0.005 \cdot V_{IN}}{8 \cdot f_{OSC} \cdot 0.005 \cdot V_{IN}} )</td>
</tr>
<tr>
<td>Step 10: ( R_{\text{FBX}} )</td>
<td>( R_{\text{FBX}} = \left</td>
</tr>
<tr>
<td>Step 11: ( R_T )</td>
<td>( R_T = \frac{81.6}{f_{OSC}} \cdot 1; f_{OSC} ) in MHz, ( R_T ) in ( k\Omega )</td>
</tr>
</tbody>
</table>

Table 3 is a step-by-step set of equations to calculate component values for the LT8582 when operating as a dual inductor inverting converter. Input parameters are input and output voltage and switching frequency (\( V_{IN} \), \( V_{OUT} \) and \( f_{OSC} \) respectively). Refer to the Appendix for further information on the design equations presented in Table 3.

Variable Definitions:

\( V_{IN} \) = Input Voltage
\( V_{OUT} \) = Output Voltage
\( DC \) = Power Switch Duty Cycle
\( f_{OSC} \) = Switching Frequency
\( I_{\text{OUT}} \) = Maximum Output Current
\( I_{\text{RIPPLE}} \) = Inductor Ripple Current

Due to its unique FBX pin, each channel of the LT8582 can work in a dual inductor inverting configuration as shown in Figure 7. Changing the connections of \( L_2 \) and the Schottky diode in the SEPIC topology results in generating negative output voltages. This configuration results in very low output voltage ripple due to inductor \( L_2 \) in series with the output. Output disconnect is inherently built into this topology because of capacitor \( C_1 \).

Note 1: Above equations use numbers good for many applications but for more exact results use the equations from the appendix with numbers from the Electrical Characteristics.

Note 2: The final values for \( C_{\text{OUT}} \), and \( C_{\text{IN}} \) may deviate from the above equations in order to obtain desired load transient performance.
APPLICATIONS INFORMATION

LAYOUT GUIDELINES FOR LT8582

General Layout Guidelines

- To improve thermal performance, solder the exposed ground pad of the LT8582 to the ground plane, with multiple vias in and around the pad connecting to additional ground planes.

- A ground plane should be used under the switcher circuitry to prevent interplane coupling and reduce overall noise.

- High speed switching paths (see specific topology below for more information) must be kept as short as possible.

- The $V_C$, $FBX$ and $R_T$ components should be placed as close to the LT8582 as possible, while being as far away as practically possible from the switch node. The ground for these components should be separated from the switch current path.

- Place the bypass capacitors for the $V_{IN}$ pins ($C_{VIN}$) as close as possible to the LT8582.

- Place the bypass capacitors for the inductors ($C_{PWR}$) as close as possible to the inductors.

- Bypass capacitors $C_{PWR}$ and $C_{VIN}$ may be combined into a single bypass capacitor, $C_{IN}$, if the input side of the inductor can be close to the $V_{IN}$ pin of the LT8582.

Boost Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing switch, diode $D_1$, output capacitor $C_{OUT_1}$ and ground return as short as possible to minimize parasitic inductive spikes during switching.

SEPIC Topology Specific Layout Guidelines

- Keep length of loop (high speed switching path) governing switch, flying capacitor $C_1$, diode $D_1$, output capacitor $C_{OUT_1}$ and ground return as short as possible to minimize parasitic inductive spikes during switching.

Inverting Topology Specific Layout Guidelines

- Keep ground return path from the cathode of $D_2$ (to chip) separated from output capacitor $C_{OUT_3}$’s ground return path (to chip) in order to minimize switching noise coupling into the output. Notice the separate ground return for $D_2$’s cathode in Figure 8.

- Keep length of loop (high speed switching path) governing switch, flying capacitor $C_1$ (in Figure 8), diode $D_2$ and ground return as short as possible to minimize parasitic inductive spikes during switching.
APPLICATIONS INFORMATION

THERMAL CONSIDERATIONS

Overview

For the LT8582 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. This can be accomplished by taking advantage of the thermal pad on the underside of the chip. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the chip and into copper planes with as much area as possible.

Power and Thermal Calculations

Power dissipation in the LT8582 chip comes from four primary sources: switch $I^2R$ loss, NPN base drive loss (AC + DC) and chip bias current. The following formulas assume continuous mode operation, so they should not be used for calculating thermal losses or efficiency in discontinuous mode or at light load currents.

Figure 8. Suggested Component Placement for Boost and Dual Inductor Inverting Topologies. Note the Separate Ground Return for the $R_T$, SS, and $V_C$ Components as Well as D2’s Cathode
Figure 9. Suggested Component Placement for SEPIC and Dual Inductor Inverting Topologies. Note the Separate Ground Return for the RT, SS, and VC Components as Well as D2’s Cathode.
APPLICATIONS INFORMATION

Table 4 calculates the power dissipation of one channel of the LT8582 for a particular boost application (V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0.8A, f_{OSC}=1.5MHz, V_{D}=0.5V, V_{CESAT}=0.270V).

From P_{TOTAL} in Table 4, die junction temperature can be calculated using the appropriate thermal resistance number and worst-case ambient temperature:

\[ T_J = T_A + \theta_{JA} \times P_{TOTAL} \]

where \( T_J \) = die junction temperature, \( T_A \) = ambient temperature and \( \theta_{JA} \) is the thermal resistance from the silicon junction to the ambient air.

The published \( \theta_{JA} \) value is 34°C/W for the 7mm × 4mm 24-pin DFN package package. In practice, lower \( \theta_{JA} \) values are realizable if board layout is performed with appropriate grounding (accounting for heat sinking properties of the board) and other considerations listed in the Board Layout Guidelines section. For instance, a \( \theta_{JA} \) value of ~16°C/W was consistently achieved for DFN packages of the LT8582 (at V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0.8A, f_{OSC}=1.5MHz) when board layout was optimized as per the suggestions in the Board Layout Guidelines section.

Junction Temperature Measurement

The duty cycle of CLKOUT2 is linearly proportional to die junction temperature (\( T_J \)) near the CLKOUT2 pin. To get an accurate reading, measure the duty cycle of the CLKOUT signal and use the following equation to approximate the junction temperature:

\[ T_J = \frac{D_{CLKOUT} - 34.5\%}{0.3\%} \]

where \( D_{CLKOUT} \) is the CLKOUT duty cycle in % and \( T_J \) is the die junction temperature in °C. Although the absolute die temperature can deviate from the above equation by ±10°C, the relationship between the CLKOUT duty cycle and change in die temperature is well defined. A 3% increase in CLKOUT duty cycle corresponds to ~10°C increase in die temperature.

Note that the CLKOUT pin is only meant to drive capacitive loads up to 120pF.

Thermal Lockout

When the die temperature exceeds 165°C (see Operation Section), a fault condition occurs and the part goes into thermal lockout. The fault condition ceases when the die temperature drops to ~160°C (nominal).

Table 4. Calculations Example with V_{IN}=5V, V_{OUT}=12V, I_{OUT}=0.8A, f_{OSC}=1.5MHz, V_{D}=0.5V, V_{CESAT}=0.27V

<table>
<thead>
<tr>
<th>DEFINITION OF VARIABLES</th>
<th>EQUATION</th>
<th>DESIGN EXAMPLE</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC = Switch Duty Cycle</td>
<td>DC = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}.</td>
<td>DC = \frac{12V - 5V + 0.5V}{12V + 0.5V - 0.270V}.</td>
<td>DC = 61.3%</td>
</tr>
<tr>
<td>I_{IN} = Average Input Current</td>
<td>I_{IN} = \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta}.</td>
<td>I_{IN} = \frac{12V \cdot 0.8A}{5V \cdot 0.88}.</td>
<td>I_{IN} = 2.18A</td>
</tr>
<tr>
<td>η = Power Conversion Efficiency (typically 88% at high currents)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_{SW} = Switch I^2R Loss</td>
<td>P_{SW} = DC \cdot I_{IN}^2 \cdot R_{SW}.</td>
<td>P_{SW} = 0.613 \cdot (2.18A)^2 \cdot 95\Omega.</td>
<td>P_{SW} = 277mW</td>
</tr>
<tr>
<td>R_{SW} = Switch Resistance (typically 95\Omega combined SWA and SWB)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P_{BAC} = Base Drive Loss (AC)</td>
<td>P_{BAC} = 13ns \cdot I_{IN} \cdot V_{OUT} \cdot f_{OSC}.</td>
<td>P_{BAC} = 13ns \cdot 2.18A \cdot 12V \cdot 1.5MHz.</td>
<td>P_{BAC} = 511mW</td>
</tr>
<tr>
<td>P_{BDC} = Base Drive Loss (DC)</td>
<td>P_{BDC} = \frac{V_{IN} \cdot I_{IN} \cdot DC}{\beta_{SW _at _IN}.}.</td>
<td>P_{BDC} = \frac{5V \cdot 2.18A \cdot 0.613}{50}.</td>
<td>P_{BDC} = 134mW</td>
</tr>
<tr>
<td>P_{PINP} = Chip Bias Loss</td>
<td>P_{PINP} = 11mA \cdot V_{IN}.</td>
<td>P_{PINP} = 11mA \cdot 5V.</td>
<td>P_{PINP} = 55mW</td>
</tr>
</tbody>
</table>

Note: These power calculations are for one channel of the LT8582. The power consumption of both channels should be taken into account when calculating die temperature.
SWITCHING FREQUENCY

There are several considerations in selecting the operating frequency of the converter. The first is staying clear of sensitive frequency bands, which cannot tolerate any spectral noise. For example, in RF communication products with a 455kHz IF, switching above 600kHz is desired. Communication products with sensitivity to 1.1MHz would require to set the switching frequency to 1.5MHz or higher. Also, like any other switching regulator, harmonics of much higher frequency than the switching frequency are also produced. The second consideration is the physical size of the converter. As the operating frequency goes up, the inductor and filter capacitors go down in value and size. The trade-off is efficiency, since the switching losses due to inductor AC loss, NPN base drive (see Thermal Calculations), Schottky diode charge and other capacitive loss terms increase proportionally with frequency.

Oscillator Timing Resistor (RT)

The operating frequency of the LT8582 can be set by the internal free running oscillator. When the SYNC pin for a channel is driven low (< 0.4V), the oscillator frequency for that channel is set by a resistor from the RT pin to ground. The oscillator frequency is calculated using the following formula:

\[
 f_{\text{osc}} = \frac{81.6}{R_T + 1}
\]

where \( f_{\text{osc}} \) is in MHz and \( R_T \) is in kΩ. Conversely, \( R_T \) (in kΩ) can be calculated from the desired frequency (in MHz) using:

\[
 R_T = \frac{81.6}{f_{\text{osc}}} - 1
\]

Clock Synchronization

The operating frequency of each channel of the LT8582 can be set by an external source by simply providing a clock into the SYNC pin for that channel (\( R_T \) resistor still required). The LT8582 will revert to its internal free running oscillator clock (set by the \( R_T \) resistor) when the SYNC pin is driven below 400mV for several free running clock periods.

Driving the SYNC pin of a channel high for an extended period of time effectively stops the oscillator for that channel. As a result, the switching operation for that channel of the LT8582 will stop and the CLKOUT pin of that channel will be pulled low.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 200kHz to 2.5MHz.
2. The SYNC frequency can be higher than the free running oscillator frequency (as set by the \( R_T \) resistor), \( f_{\text{osc}} \), but should not be less than 25% below \( f_{\text{osc}} \).

Clock Synchronization of Additional Regulators

The CLKOUT pins of the LT8582 can be used to synchronize additional switching regulators or other channels of LT8582s, as shown in the Typical Application figure on the front page.

The frequency of channel 1 of the LT8582 is set by the external \( R_T \) resistor. The SYNC pin of channel 2 of the LT8582 is driven by the CLKOUT pin of channel 1 of the LT8582. Channel 1’s CLKOUT pin has a 50% duty cycle intended for driving SYNC2 and is 180° out of phase for reduced input ripple or multiphase topologies.

Note that the RT pin of channel 2 of the LT8582 must have a resistor tied to ground. It takes a few clock cycles for the CLKOUT signal to begin oscillating and it is preferable for all LT8582 channels to have the same internal free running frequency. Therefore, in general, use the same value \( R_T \) resistor for all of the synchronized LT8582s.

EVENT BASED SEQUENCING

The PG pin may be used to sequence other ICs since it is pulled low as long as the LT8582 is enabled and the magnitude of the output voltage is below regulation (refer to the Block Diagram). Since the PG pin is an open drain output, it can be used to pull the SHDN pin of another IC low until the output of one of the channels of the LT8582
APPLICATIONS INFORMATION

is close to its regulation voltage. This method allows the PG pin to disable multiple ICs. Refer to Figure 10 for the necessary connections. Alternatively, the PG pin may be used to pull the SS pin of another switching regulator low, preventing the other regulator from switching.

The master switch, immune from the flying capacitor current spike (seen only by the slave switch), can therefore sense the inductor current more accurately.

Since the slave switch can sustain large current spikes, the diodes that feed current into the flying capacitors do not need current limiting resistors, leading to efficiency and thermal improvements, as well as a smaller solution size.

High \( V_{\text{OUT}} \) Charge Pump Topology

The LT8582 can be used in a charge pump topology as shown in Figure 11, multiplying the output of a boost converter. The master switch (SWA) can be used to drive the boost converter, while the slave switch (SWB) can be used to drive one or more charge pump stages. This topology is useful for high voltage applications including VFD bias supplies.

CHARGE PUMP AIDED REGULATORS

Designing charge pumps with the LT8582 can offer efficient solutions with fewer components than traditional circuits because of the master/slave switch configuration on the IC. Although the slave switch, SWB, operates in phase with the master switch, SWA, only the current through the master switch (SWA) is sensed by the current comparator (A4 in the Block Diagram). This method of operation by the master/slave switches can offer the following benefits to charge pump designs:

- The slave switch, by not performing a current sense operation like the master switch, can sustain fairly large current spikes without falsely tripping the current comparator. In a charge pump, these spikes occur when the flying capacitors charge up. Since this current spike flows through SWB, it does not affect the operation of the current comparator (A4 in the Block Diagram).

Figure 10. Using the Two LT8582 Channels, with Power Supply Sequencing

Figure 11. High \( V_{\text{OUT}} \) Charge Pump Topology
**APPLICATIONS INFORMATION**

**Single Inductor Inverting Topology**

If there is a need to use just one inductor to generate a negative output voltage whose magnitude is greater than \( V_{IN} \), the single inductor inverting topology (shown in Figure 12) can be used. Since the master and slave switches are isolated by a Schottky diode, the current spike through \( C_1 \) will flow only through the slave switch, preventing the current comparator, \( (A_4 \) in the Block Diagram) from false tripping. Output disconnect is inherently built into the single inductor topology.

![Figure 12. Single Inductor Inverting Topology](image)

**HOT-PLUG**

High inrush currents associated with hot-plugging \( V_{IN} \) can largely be rejected with the use of an external PMOS. A simple hot-plug controller can be designed by connecting an external PMOS in series with \( V_{IN} \), with the gate of the PMOS being driven by the GATE pin of the LT8582. The GATE pin pull-down current is linearly proportional to the SS voltage. Since the SS charge up time is relatively slow, the GATE pin pull-down current will increase gradually, thereby turning on the external PMOS slowly. Controlled in this manner, the PMOS acts as an input current limiter when \( V_{IN} \) hot-plugs or ramps up sharply.

Likewise, when the PMOS is connected in series with the output, inrush current into the output capacitor can be limited during a hot-plug event. To illustrate this, the circuit in Figure 5 was reconfigured by adding a large 1500\( \mu \)F capacitor to the output. An 18\( \Omega \) resistive load was used and \( C_SS \) was increased to 10\( \mu \)F. Figure 13 shows the results of hot-plugging this reconfigured circuit. Notice how the inductor current is well behaved.

![Figure 13. \( V_{IN} \) Hot-Plug Control. Inrush Current Is Well Controlled](image)
APPENDIX

INDEPENDENT CHANNELS

Either channel may be used independently of the other channel. To disable one channel, drive SHDN of that channel low. Activating or deactivating one channel will not alter the functionality of the other channel.

SETTING THE OUTPUT VOLTAGE

The output voltage is set by connecting a resistor ($R_{FBX}$) from $V_{OUT}$ to the FBX pin. $R_{FBX}$ is determined by using the following equation:

$$R_{FBX} = \frac{|V_{OUT} - V_{FBX}|}{83.3\mu A}$$

where $V_{FBX}$ is 1.204V (typical) for noninverting topologies (i.e. boost and SEPIC regulators) and 7mV (typical) for inverting topologies (see the Electrical Characteristics).

POWER SWITCH DUTY CYCLE

In order to maintain loop stability and deliver adequate current to the load, the power NPNs (Q1 and Q2 in the Block Diagram) cannot remain on for 100% of each clock cycle. The maximum allowable duty cycle is given by:

$$DC_{MAX} = \frac{(T_P - \text{MinOffTime})}{T_P} \cdot 100\%$$

where $T_P$ is the clock period and MinOffTime (found in the Electrical Characteristics) is typically 45ns.

Conversely, the power NPNs (Q1 and Q2 in the Block Diagram) cannot remain off for 100% of each clock cycle and will turn on for a minimum on time (MinOnTime) when in regulation. This MinOnTime governs the minimum allowable duty cycle given by:

$$DC_{MIN} = \frac{\text{MinOnTime}}{T_P} \cdot 100\%$$

Where $T_P$ is the clock period and MinOnTime (found in the Electrical Characteristics) is typically 55ns.

The application should be designed such that the operating duty cycle is between $DC_{MIN}$ and $DC_{MAX}$.

Duty cycle equations for several common topologies are given below where $V_D$ is the diode forward voltage drop and $V_{CESAT}$ is the collector to emitter saturation voltage of the switch. $V_{CESAT}$, with SWA and SWB tied together, is typically 270mV when the combined switch current ($I_{SWA} + I_{SWB}$) is 2.75A.

For the boost topology (see Figure 5):

$$DC_{BOOST} = \frac{V_{OUT} - V_{IN} + V_D}{V_{OUT} + V_D - V_{CESAT}}$$

For the SEPIC or dual inductor inverting topology (see Figure 6 and Figure 7):

$$DC_{SEPIC \_& \_INVERT} = \frac{|V_{OUT}| + V_D}{V_{IN} + |V_{OUT}| + V_D - V_{CESAT}}$$

For the single inductor inverting topology (see Figure 12):

$$DC_{SI\_INVERT} = \frac{|V_{OUT}| - V_{IN} + V_{CESAT} + 3 \cdot V_D}{|V_{OUT}| + 3 \cdot V_D}$$

The LT8582 can be used in configurations where the duty cycle is higher than $DC_{MAX}$, but it must be operated in the discontinuous conduction mode so that the effective duty cycle is reduced.

INDUCTOR SELECTION

General Guidelines

The high frequency operation of the LT8582 allows for the use of small surface mount inductors. For high efficiency, choose inductors with high frequency core material, such as ferrite, to reduce core losses. Also to improve efficiency, choose inductors with more volume for a given inductance. The inductor should have low DCR (copper-wire resistance) to reduce $I^2R$ losses and must be able to handle the peak inductor current without saturating. Note that in some applications, the current handling requirements of the inductor can be lower, such as in the SEPIC topology where each inductor only carries one half of the total switch current. Multilayer chip inductors usually do not have enough core volume to support peak inductor currents in the 2A to 6A range. To minimize radiated noise,
APPENDIX

use a toroidal or shielded inductor. See Table 5 for a list of inductor manufacturers.

Table 5. Inductor Manufacturers

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Model/Serial Numbers</th>
<th>Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coilcraft</td>
<td>MSD7342 XAL6060 Series</td>
<td><a href="http://www.coilcraft.com">www.coilcraft.com</a></td>
</tr>
<tr>
<td>Vishay</td>
<td>IHLP-2020BZ-01 IHLP-2525CZ-01 Series</td>
<td><a href="http://www.vishay.com">www.vishay.com</a></td>
</tr>
<tr>
<td>WÜRTH</td>
<td>WE-PD WE-DD WE-TDC Series</td>
<td><a href="http://www.we-online.com">www.we-online.com</a></td>
</tr>
<tr>
<td>Cooper Bussman</td>
<td>Octa-Pac Plus DRQ-125 DRQ-74 Series</td>
<td><a href="http://www.cooperbussmann.com">www.cooperbussmann.com</a></td>
</tr>
<tr>
<td>Sumida</td>
<td>CDR6D28MN CDR7D28MN Series</td>
<td><a href="http://www.sumida.com">www.sumida.com</a></td>
</tr>
<tr>
<td>Taiyo Yuden</td>
<td>NR Series</td>
<td><a href="http://www.t-yuden.com">www.t-yuden.com</a></td>
</tr>
<tr>
<td>TDK</td>
<td>VLE SLF RLF Series</td>
<td><a href="http://www.tdk.com">www.tdk.com</a></td>
</tr>
</tbody>
</table>

Minimum Inductance

Although there can be a trade-off with efficiency, it is often desirable to minimize board space by choosing smaller inductors. When choosing an inductor, there are three conditions that limit the minimum inductance: (1) providing adequate load current, (2) avoiding subharmonic oscillation and (3) supplying a minimum ripple current to avoid false tripping of the current comparator.

Adequate Load Current

Small value inductors result in increased ripple currents and thus, due to the limited peak switch current, decrease the average current that can be provided to the load. In order to provide adequate load current, $L$ should be at least:

$$L_{\text{BOOST}} > \frac{DC \cdot (V_{IN} - V_{CESAT})}{2 \cdot f_{\text{OSC}} \cdot \left(I_{PK} - \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta}\right)}$$

Boost Topology

or

$$L_{\text{DUAL}} > \frac{DC \cdot (V_{IN} - V_{CESAT})}{2 \cdot f_{\text{OSC}} \cdot \left(I_{PK} - \frac{V_{OUT} \cdot I_{OUT}}{V_{IN} \cdot \eta} - I_{OUT}\right)}$$

SEPIC or Inverting Topologies

where

$L_{\text{BOOST}} = L_1$ for boost topologies (see Figure 5)

$L_{\text{DUAL}} = L_1 = L_2$ for coupled dual inductor topologies (see Figures 6 and 7)

$L_{\text{DUAL}} = L_1 || L_2$ for uncoupled dual inductor topologies (see Figures 6 and 7)

$DC$ = Switch duty cycle (see Power Switch Duty Cycle section in Appendix)

$I_{PK}$ = Maximum Peak Switch Current; should not exceed 3A for a combined SWA + SWB current, or 1.7A if only SWA is being used.

$\eta$ = Power conversion efficiency (typically 88% for boost and 82% for dual inductor topologies at high currents)

$f_{\text{OSC}}$ = Switching frequency

$I_{OUT}$ = Maximum load current

Negative values of $L_{\text{BOOST}}$ or $L_{\text{DUAL}}$ indicate that the output load current $I_{OUT}$ exceeds the switch current limit capability of the LT8582.

Avoiding Subharmonic Oscillations

Subharmonic oscillations can occur when the duty cycle is greater than 50%. The LT8582’s internal slope compensation circuit will avoid this, provided that the inductance exceeds a certain minimum value. In applications that operate with duty cycles greater than 50%, the inductance must be at least:

$$L_{\text{MIN}} > \frac{(V_{IN} - V_{CESAT}) \cdot (2 \cdot DC - 1)}{1.7A \cdot f_{\text{OSC}} \cdot (1 - DC)}$$

where

$L_{\text{MIN}} = L_1$ for boost topologies (see Figure 5)

$L_{\text{MIN}} = L_1 = L_2$ for coupled dual inductor topologies (see Figures 6 and 7)

$L_{\text{MIN}} = L_1 || L_2$ for uncoupled dual inductor topologies (see Figures 6 and 7)
APPENDIX

Maximum Inductance

Excessive inductance can reduce current ripple to levels that are difficult for the current comparator (A4 in the Block Diagram) to easily distinguish the peak current. This causes duty cycle jitter and/or poor regulation. The maximum inductance can be calculated by:

\[ L_{\text{MAX}} = \frac{V_{\text{IN}} - V_{\text{CESAT}}}{180\text{mA}} \cdot \frac{DC}{f_{\text{OSC}}} \]

where

\( L_{\text{MAX}} = L_1 \) for boost topologies (see Figure 5)
\( L_{\text{MAX}} = L_1 = L_2 \) for coupled dual inductor topologies (see Figures 6 and 7)
\( L_{\text{MAX}} = L_1 \parallel L_2 \) for uncoupled dual inductor topologies (see Figures 6 and 7)

Inductor Current Rating

Inductors must have a rating greater than their peak operating current to prevent saturation, which results in efficiency losses. The maximum inductor current (considering start-up, transient, and steady-state conditions) is given by:

\[ I_{\text{L, PEAK}} = I_{\text{LIM}} + \frac{V_{\text{IN}} \cdot T_{\text{MIN_PROP}}}{L} \]

where

\( I_{\text{L, PEAK}} = \) Peak of Inductor Current in \( L_1 \) for boost topology, or peak of the sum of inductor currents in \( L_1 \) and \( L_2 \) for dual inductor topologies.
\( I_{\text{LIM}} = \) For hard saturation inductors, 5.4A when SWA and SWB are tied together, or 3A when only SWA is being used. For soft saturation inductors, 3.3A when SWA and SWB are tied together, or 1.8A when only SWA is being used.
\( T_{\text{MIN_PROP}} = 55\text{ns} \) (propagation delay through the current feedback loop)

Note that these equations offer conservative results for the required inductor current ratings. The current ratings could be lower for applications with light loads and small transients if the SS capacitor is sized appropriately to limit inductor currents at start-up.

DIODE SELECTION

Schottky diodes, with their low forward voltage drops and fast switching speeds, are recommended for use with the LT8582. Choose a Schottky diode with low parasitic capacitance to reduce reverse current spikes through the power switch of the LT8582. The Diodes Inc. PD3S230H diode is a very good choice with a 30V reverse voltage rating and an average forward current of 2A.

OUTPUT CAPACITOR SELECTION

Low ESR (equivalent series resistance) capacitors should be used at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X5R or X7R types are preferred, as these retain their capacitance over wide voltage and temperature ranges. A 10μF to 22μF output capacitor is sufficient for most applications, but systems with very low output currents may need only 2.2μF to 10μF. Always use a capacitor with a sufficient voltage rating. Many ceramic capacitors, particularly 0805 or 0603 case sizes, have greatly reduced capacitance at the desired output voltage. Tantalum polymer or OS-CON capacitors can be used, but it is likely that these capacitors will occupy more board area than ceramics and will have a higher ESR with greater output ripple.

INPUT CAPACITOR SELECTION

Ceramic capacitors make a good choice for the input bypass capacitor and should be placed as close as possible to the \( V_{\text{IN}} \) pin of the chip as well as to the inductor connected to the input of the power path. If it is not possible to optimally place a single input capacitor, then use two separate capacitors—use one at the \( V_{\text{IN}} \) pin of the chip (see the equation for \( C_{\text{VIN}} \) in Table 1, Table 2 and Table 3).
APPENDIX

and one at the input to the power path (see the equation for CPWR in Table 1, Table 2 and Table 3). A 4.7μF to 20μF input capacitor is sufficient for most applications.

Table 6 shows a list of several ceramic capacitor manufacturers. Consult the manufacturers for detailed information on their entire selection of ceramic parts.

Table 6. Ceramic Capacitor Manufacturers

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>TDK</td>
<td><a href="http://www.tdk.com">www.tdk.com</a></td>
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<tr>
<td>Murata</td>
<td><a href="http://www.murata.com">www.murata.com</a></td>
</tr>
<tr>
<td>Taiyo Yuden</td>
<td><a href="http://www.t-yuden.com">www.t-yuden.com</a></td>
</tr>
<tr>
<td>Kemet</td>
<td><a href="http://www.kemet.com">www.kemet.com</a></td>
</tr>
</tbody>
</table>

PMOS SELECTION

An external PMOS, controlled by the LT8582's GATE pin, can be used to facilitate input or output disconnect. The GATE pin turns on the PMOS gradually during start-up (see soft-start of external PMOS in the Operation section) and turns the PMOS off when the LT8582 is in shutdown or in fault.

The use of the external PMOS, controlled by the GATE pin, is particularly beneficial when dealing with unintended output shorts in a boost regulator. In a conventional boost regulator, the inductor, Schottky diode and power switches are susceptible to damage in the event of an output short. Using an external PMOS in the boost regulator's power path (path from VIN to VOUT) controlled by the GATE pin, will serve to disconnect the input from the output when the output has a short. This helps to save the chip and the other components in the power path from damage. Ensure that both the diode and the inductor can survive low duty cycle current pulses of 5 to 6 times their steady state levels.

The PMOS chosen must be capable of handling the maximum input or output current depending on whether it is used at the input or the output (see Figure 5).

Ensure that the PMOS is biased with enough source to gate voltage (VSG) to enhance the device into the triode mode of operation. The higher the VSG voltage that biases the PMOS into triode, the lower the RDSON of the PMOS, thereby lowering power dissipation in the device during normal operation, as well as improving the efficiency of the application. The following equations show the relationship between RGATE (see Block Diagram) and the desired VSG that the PMOS is biased with, where VS is the PMOS source voltage:

\[
V_{SG} = \begin{cases} 
V_S \frac{R_{GATE}}{R_{GATE} + 2k\Omega} & \text{if } V_{GATE} < 2V \\
1mA \times R_{GATE} & \text{if } V_{GATE} \geq 2V 
\end{cases}
\]

When using a PMOS, it is advisable to configure the specific application for undervoltage lockout (see the Operations section). The goal is to have VIN get to a certain minimum voltage where the PMOS has sufficient VSG.

Figure 5 shows the PMOS connected in series with the output to act as an output disconnect during a fault condition. Using a PMOS with a high VT (~2V) can help to reduce extraneous current spikes during hot-plug. The resistor divider from VIN to the SHDN pin sets UVLO at 4V for this application.

Connecting the PMOS in series with the output offers certain advantages over connecting it in series with the input:

- Since the load current is always less than the input current for a boost converter, the current rating of the PMOS will be reduced.
- A PMOS in series with the output can be biased with a higher overdrive voltage than a PMOS used in series with the input, since VOUT > VIN. This higher overdrive results in a lower RDSON rating for the PMOS, thereby improving the efficiency of the regulator.

In contrast, an input connected PMOS works as a simple hot-plug controller (covered in more detail in the Hot-Plug section). The input connected PMOS also functions as an inexpensive means of protecting against multiple output shorts in boost applications that synchronize the LT8582 with other compatible chips.
APPENDIX

Table 7 shows a list of several discrete PMOS manufacturers. Consult the manufacturers for detailed information on their entire selection of PMOSs.

Table 7. Discrete PMOS Manufacturers

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Website</th>
</tr>
</thead>
<tbody>
<tr>
<td>Vishay</td>
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</tr>
<tr>
<td>ON Semiconductor</td>
<td><a href="http://www.onsemi.com">www.onsemi.com</a></td>
</tr>
<tr>
<td>Fairchild Semiconductor</td>
<td><a href="http://www.fairchildsemi.com">www.fairchildsemi.com</a></td>
</tr>
<tr>
<td>Diodes Incorporated</td>
<td><a href="http://www.diodes.com">www.diodes.com</a></td>
</tr>
</tbody>
</table>

COMPENSATION – ADJUSTMENT

To compensate the feedback loop of the LT8582, a series resistor capacitor network in parallel with an optional single capacitor should be connected from the V_C pin to GND. For most applications, choose a series capacitor in the range of 1nF to 10nF with 2.2nF being a good starting value. The optional parallel capacitor should range in value from 22pF to 220pF with 47pF being a good starting value. The compensation resistor, R_C, is usually in the range of 5k to 50k with 10k being a good starting value. A good technique to compensate a new application is to use a 100k potentiometer in place of the series resistor R_C. With the series and parallel capacitors at 4.7nF and 47pF respectively, adjust the potentiometer while observing the transient response and the optimum value for R_C can be found. Figures 14a to Figure 14c illustrate this process for the circuit of Figure 17 with a load current stepped between 300mA and 800mA. Figure 14a shows the transient response with R_C equal to 1k. The phase margin is poor as evidenced by the excessive ringing in the output voltage and inductor current. In Figure 14b, the value of R_C is increased to 3.15k, which results in a more damped response. Figure 14c shows the results when R_C is increased further to 6.49k. The transient response is nicely damped and the compensation procedure is complete.

Compensation – Theory

Like all other current mode switching regulators, the LT8582 needs to be compensated for stable and efficient operation. Two feedback loops are used in the LT8582: a fast current loop which does not require compensation and a slower voltage loop which does. Standard bode plot analysis can be used to understand and adjust the voltage feedback loop.

As with any feedback loop, identifying the gain and phase contribution of the various elements in the loop is critical. Figure 15 shows the key equivalent elements of a boost converter. Because of the fast current control loop, the power stage of the chip, inductor and diode have been replaced by a combination of the equivalent transconductance amplifier g_mp and the current controlled current source (which converts I_VIN to (ηV_IN/V_OUT) • I_VIN). g_mp acts as a current source where the peak input current, I_VIN, is proportional to the V_C voltage. η is the efficiency of the switching regulator and is typically about 88% at higher currents.
Note that the maximum output currents of $g_{mp}$ and $g_{ma}$ are finite. The output current of the $g_{mp}$ stage is limited by the minimum switch current limit (see the Electrical Specifications) and the output of the $g_{ma}$ stage is nominally limited to about ±12μA.

From Figure 15, the DC gain, poles and zeros can be calculated as follows:

**DC GAIN:**

$$A_{DC} = (g_{ma} \cdot R_0) \cdot g_{mp} \cdot \left( \eta \cdot \frac{V_{IN}}{V_{OUT}} \cdot \frac{R_L}{2} \right) \cdot \frac{0.5R_2}{R_1 + 0.5R_2}$$

**Output Pole:**

$$P_1 = \frac{2}{2 \cdot \pi \cdot R_L + C_{OUT}}$$

**Error Amp Pole:**

$$P_2 = \frac{1}{2 \cdot \pi \cdot (R_0 + R_C) C_C}$$

**Error Amp Zero:**

$$Z_1 = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C}$$

**ESR Zero:**

$$Z_2 = \frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{OUT}}$$

**RHP Zero:**

$$Z_3 = \frac{V_{IN}^2 \cdot R_L}{2 \cdot \pi \cdot V_{OUT}^2 \cdot L}$$

**High Frequency Pole:**

$$P_3 > \frac{f_s}{3}$$

**Phase Lead Zero:**

$$Z_4 = \frac{1}{2 \cdot \pi \cdot R_1 \cdot C_{PL}}$$

**Phase Lead Pole:**

$$P_4 = \frac{1}{2 \cdot \pi \cdot \frac{0.5 \cdot R_1 \cdot R_2}{R_1 + 0.5R_2} \cdot C_{PL}}$$

**Error Amp Filter Pole:**

$$P_5 = \frac{1}{2 \cdot \pi \cdot \frac{R_C \cdot R_0 \cdot C_F}{R_C + R_0} \cdot C_F < C_C \cdot 10}$$
APPENDIX

The current mode zero (Z3) is a right half plane zero which can be an issue in feedback control design, but is manageable with proper external component selection.

Using the circuit in Figure 17 as an example, Table 8 shows the parameters used to generate the bode plot shown in Figure 16.

Table 8. Bode Plot Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
<th>UNITS</th>
<th>COMMENT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_L )</td>
<td>20</td>
<td>( \Omega )</td>
<td>Application Specific</td>
</tr>
<tr>
<td>( C_{\text{OUT}} )</td>
<td>22</td>
<td>( \mu F )</td>
<td>Application Specific</td>
</tr>
<tr>
<td>( R_{\text{ESR}} )</td>
<td>1</td>
<td>m( \Omega )</td>
<td>Application Specific</td>
</tr>
<tr>
<td>( R_D )</td>
<td>305</td>
<td>k( \Omega )</td>
<td>Not Adjustable</td>
</tr>
<tr>
<td>( C_C )</td>
<td>4700</td>
<td>pF</td>
<td>Adjustable</td>
</tr>
<tr>
<td>( C_F )</td>
<td>47</td>
<td>pF</td>
<td>Optional/Adjustable</td>
</tr>
<tr>
<td>( C_{\text{PL}} )</td>
<td>0</td>
<td>pF</td>
<td>Optional/Adjustable</td>
</tr>
<tr>
<td>( R_C )</td>
<td>6.49</td>
<td>k( \Omega )</td>
<td>Adjustable</td>
</tr>
<tr>
<td>( R_1 )</td>
<td>130</td>
<td>k( \Omega )</td>
<td>Adjustable</td>
</tr>
<tr>
<td>( R_2 )</td>
<td>14.5</td>
<td>k( \Omega )</td>
<td>Not Adjustable</td>
</tr>
<tr>
<td>( V_{\text{REF}} )</td>
<td>1.204</td>
<td>V</td>
<td>Not Adjustable</td>
</tr>
<tr>
<td>( V_{\text{OUT}} )</td>
<td>12</td>
<td>V</td>
<td>Application Specific</td>
</tr>
<tr>
<td>( V_{\text{IN}} )</td>
<td>5</td>
<td>V</td>
<td>Application Specific</td>
</tr>
<tr>
<td>( g_m )</td>
<td>270</td>
<td>( \mu \text{mho} )</td>
<td>Not Adjustable</td>
</tr>
<tr>
<td>( g_m' )</td>
<td>15.1</td>
<td>mho</td>
<td>Not Adjustable</td>
</tr>
<tr>
<td>( L )</td>
<td>4.7</td>
<td>( \mu H )</td>
<td>Application Specific</td>
</tr>
<tr>
<td>( f_{\text{OSC}} )</td>
<td>1.5</td>
<td>MHz</td>
<td>Adjustable</td>
</tr>
</tbody>
</table>

From Figure 16, the phase is \(-130^\circ\) when the gain reaches 0dB, giving a phase margin of 50\(^\circ\). The crossover frequency is 5kHz, which is many times lower than the frequency of the RHP zero Z3, thus providing for adequate phase margin.
1.5MHz, 5V to ±12V Boost and Inverting Converter Can Survive Output Shorts

**Efficiency and Power Loss (Load Between 12V and –12V Outputs)**

**Output Short from 12V Output to Ground**

**Transient Response with 0.15A to 0.45A to 0.15A Output Load Step Between Rails**
TYPICAL APPLICATIONS

VFD (Vacuum Fluorescent Display) and Filament Power Supply Switches at 1MHz

Efficiency and Power Loss

Efficiency and Power Loss

*CHANNEL 1 MAX OUTPUT POWER 8W
**OPTIONAL FOR OUTPUT SHORT PROTECTION
TYPICAL APPLICATIONS

Tracking ±15V Supplies from a 2.7V to 5.5V Input

Efficiency and Power Loss
(VIN = 3.6V with Load Between 15V and –15V Outputs)

15V and –15V Outputs vs Load Current
(VIN = 3.6V, Load on 15V Output)

15V and –15V Outputs vs Load Current
(VIN = 3.6V, Load on –15V Output)

15V and –15V Outputs vs Load Current
(VIN = 3.6V, Load Between 15V and –15V Outputs)
TYPICAL APPLICATIONS

SuperCap Backup Power

System Level Diagram

Charging SuperCaps

Input Removed, Holdup for ~110 s with 500 mA Load
**TYPICAL APPLICATIONS**

**12V and 5V Sequenced Outputs from a 3V to 19V Input**

**Efficiency and Power Loss** *(VIN = 12V with Load on 12V Output)*

**Cycle-to-Cycle (5V Output)**

**Efficiency and Power Loss** *(VIN = 12V with Load on 5V Output)*
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DKD Package
24-Lead Plastic DFN (7mm × 4mm)
(Reference LTC DWG # 05-08-1864 Rev 0)

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WXXX) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS

4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RECOMMENDED SOLDER PAD LAYOUT
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED

PACKAGE OUTLINE

BOTTOM VIEW—EXPOSED PAD

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
**TYPICAL APPLICATION**

700kHz SEPIC and Inverting Converter Generates ±5V Outputs from a 3V to 19V Input

**Efficiency and Power Loss**  
(VIN = 12V with Load Between 5V and –5V Outputs)

**RELATED PARTS**

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>LT3581</td>
<td>3.3A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter</td>
<td>V_{IN} = 2.5V to 22V, V_{OUT(MAX)} = 42V, I_{Q} = 1.9mA, I_{SD} = &lt; 1μA, 4mm × 3mm DFN-14, MSOP-16E</td>
</tr>
<tr>
<td>LT3579</td>
<td>6A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter</td>
<td>V_{IN} = 2.5V to 16V, V_{OUT(MAX)} = 42V, I_{Q} = 1.9mA, I_{SD} = &lt; 1μA, 4mm × 5mm QFN-20, TSSOP-20</td>
</tr>
<tr>
<td>LT3580</td>
<td>2A (I_{SW}), 42V, 2.5MHz, High Efficiency Step-Up DC/DC Converter</td>
<td>V_{IN} = 2.5V to 32V, V_{OUT(MAX)} = 42V, I_{Q} = 1mA, I_{SD} = &lt; 1μA, 3mm × 3mm DFN-8, MSOP-8E</td>
</tr>
<tr>
<td>LT3471</td>
<td>Dual Output 1.3A (I_{SW}), 1.2MHz, High Efficiency Step-Up DC/DC Converter</td>
<td>V_{IN} = 2.4V to 16V, V_{OUT(MAX)} = ±40V, I_{Q} = 2.5mA, I_{SD} &lt; 1μA, 3mm × 3mm DFN-10 Package</td>
</tr>
<tr>
<td>LT3479</td>
<td>3A (I_{SW}), 40V, 3.5MHz, High Efficiency Step-Up DC/DC Converter</td>
<td>V_{IN} = 2.5V to 24V, V_{OUT(MAX)} = 40V, I_{Q} = 5mA, I_{SD} = &lt; 1μA, 4mm × 3mm DFN-14, TSSOP-16E</td>
</tr>
<tr>
<td>LT3477</td>
<td>40V, 3A, Full Featured DC/DC Converter</td>
<td>V_{IN} = 2.5V to 25V, V_{OUT(MAX)} = 40V, I_{Q} = 5mA, I_{SD} &lt; 1μA, QFN, TSSOP-20E Packages</td>
</tr>
<tr>
<td>LT1946/LT1946A</td>
<td>1.5A (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converter</td>
<td>V_{IN} = 2.6V to 16V, V_{OUT(MAX)} = 34V, I_{Q} = 3.2mA, I_{SD} &lt; 1μA, MSPE Package</td>
</tr>
<tr>
<td>LT1935</td>
<td>2A (I_{SW}), 40V, 1.2MHz, High Efficiency Step-Up DC/DC Converter</td>
<td>V_{IN} = 2.3V to 16V, V_{OUT(MAX)} = 40V, I_{Q} = 3mA, I_{SD} &lt; 1μA, ThinSOT™ Package</td>
</tr>
<tr>
<td>LT1310</td>
<td>2A (I_{SW}), 40V, 1.2MHz, High Efficiency Step-Up DC/DC Converter</td>
<td>V_{IN} = 2.3V to 16V, V_{OUT(MAX)} = 40V, I_{Q} = 3mA, I_{SD} &lt; 1μA, ThinSOT™ Package</td>
</tr>
<tr>
<td>LT3436</td>
<td>3A (I_{SW}), 800kHz, 34V Step-Up DC/DC Converter</td>
<td>V_{IN} = 3V to 25V, V_{OUT(MAX)} = 34V, I_{Q} = 0.9mA, I_{SD} &lt; 6μA, TSSOP-16E Package</td>
</tr>
</tbody>
</table>