

Revision A6 may be identified by the date/revision brand yywwA6, where yy and ww are the year and work-week of manufacture, respectively. This errata sheet is valid only when used in conjunction with the most current version of the data sheet available from Dallas Semiconductor on our website at www.maxim-ic.com.

ERRATA

1. An interrupt priority, whether natural or register driven, does not affect its ability to cause an exit from Stop mode. As a result, if Stop mode is entered from an interrupt service routine, a lower priority interrupt that would normally not be serviced causes an exit from Stop mode.

Work Around: Do not enter Stop mode from an interrupt service routine.

2. The instruction XCH A, direct can produce unreliable results when the source register is associated with the interrupts (i.e., IE, IP, EIE, EIP) and there is a simultaneous interrupt.

Work Around: Use a MOV direct, A or similar instructions to modify one of the above registers.

3. Setting Timer 0 to mode 3 (two 8-bit timers) disrupts the normal operation of Timer 1's output. All other modes and combinations of modes of Timers 0 and 1 are fully functional. One consequence of this erratum is that combinations of modes of Timers 0 and 1 are fully functional. One consequence of this erratum is that while Timer 0 is in mode 3, Timer 1 should not be used as a baud rate generator for the serial port. Also, Timer 0 in mode 3 will only clock at the divide-by-12 rate.

Work Around: Do not put Timer 0 in mode 3 while Timer 1 is being used as a baud rate generator (or any other function that requires an interrupt.) This erratum will be corrected in a future revision of the device.

4. When Timer 2 is used in auto-reload mode with up/down count enabled (DCEN = 1), the EXF2 bit does not toggle as specified. Up/down counting, interrupt generation, and all other aspects of this mode function correctly.

Work Around: Do not use EXF2 in this mode.

5. At voltages below 4.25V, serial ports 0 and 1 operating in modes 1, 2, or 3 may not properly detect a false start bit, causing the device to erroneously detect the start of a serial reception.

Work Around: Operate the device V_{CC} as close as possible to 5.0 V.

6. Either serial port operating in mode 0 may violate the t_{QVXL} spec when the external crystal speed is above 25MHz.

Work Around: Use the rising edge only of the clock to latch output data if the external crystal speed is above 25MHz.
7. The broadcast address portion of either serial port's address recognition mode does not function. All other aspects of this mode work properly.

Work Around: Use the "Given Address" (SADDR masked by SADEN) to create a group that may be addressed separately or as a unit
8. Modifying the Clock Control Register (CKCON; 8Eh) while the watchdog timer is enabled can advance the watchdog timer count by an indeterminate amount. This can result in an inaccurate watchdog timer period. This will not occur if the current watchdog timeout period is already set to its maximum count ($WD1 = WD0 = 1$), and a 11 is written to the Watchdog Timer Mode Select Bits (CKCON.7–6).

Work Around: If the watchdog timer is enabled, reset the watchdog timer via the RWT bit (WDCON.0) before accessing the CKCON register. This will prevent an unexpected early time-out of the watchdog timer.
9. Timers 0, 1, and 2 can exhibit improper operation in counter mode if the transitions on their respective input pin are within 1 clock cycle of the rising edge of ALE. This can result in missed or extra timer counts. This caveat also applies to Timers 0 and 1 in timer mode if the $\overline{INT0}$ and $\overline{INT1}$ inputs are used in the Gate function to control the timers. This situation does not occur with signals that are synchronized to processor operation and do not transition coincident with the rising edge of ALE.

Work Around: Qualify the input on the above mentioned signals so that they do not transition with the rising edge of ALE. This can be easily done by gating the input signal with a D-type flip-flop using the falling edge of ALE as a clocking signal.
10. The bits associated with the Status Register (STATUS; C5h) are disabled.

Work Around: NONE. This register will be enabled in the next revision of the device
11. A typographical error in some versions of the data sheet erroneously lists Ports 0 and 2 as being tested to the V_{OH1} specification. These ports have not been and will not be tested to this specification.

Work Around: NONE. This specification will not alter the functional characteristics of the devices.

12. When any reset occurs during the execution of an extended MOVX data memory access, most instructions located at 0000h can fail to execute correctly. The exception is the LCALL instruction, mentioned below. In each case the failure causes the program to incorrectly execute the first several machine cycles of the affected instruction(s).

Work Around: Use the instruction LCALL at location 0000h (the reset vector) to jump to the starting point of the main user code. This will use two bytes of the stack, which can be easily restored if necessary by resetting the stack pointer.

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15. When a short reset stimulus occurs during the execution of an extended MOVX data memory access, the ALE signal may not be driven with the strong transition drivers (V_{OH2} test levels) on the first instruction fetch following reset. This reduced drive current may not allow the ALE signal to rise to a logic high level before the first instruction fetch at location 0000h, possibly latching an incorrect address. This situation will only occur during a watchdog timer reset (the timer generates a momentary pulse to the internal reset circuitry) or when an external reset pulse of less than $2\mu\text{s}$ is asserted. This errata does not affect a power-on reset as the internal crystal warmup period counter provides a reset pulse of greater than $2\mu\text{s}$.

Work Around: If the watchdog timer reset function is employed, use the watchdog timer interrupt to ensure that the device will not be executing MOVX instructions when the watchdog timer reset occurs. If an external reset stimulus is used, be sure that it is at least $2\mu\text{s}$ in duration.