The LTC®6994 is a programmable delay block with a range of 1µs to 33.6 seconds. The LTC6994 is part of the TimerBlox® family of versatile silicon timing devices.

A single resistor, \( R_{\text{SET}} \), programs an internal master oscillator frequency, setting the LTC6994’s time base. The input-to-output delay is determined by this master oscillator and an internal clock divider, \( N_{\text{DIV}} \), programmable to eight settings from 1 to \( 2^{21} \):

\[
\text{t}_{\text{DELAY}} = \frac{N_{\text{DIV}} \cdot R_{\text{SET}}}{50\, \text{k}Ω} \cdot 1\, \mu\text{s}, \quad N_{\text{DIV}} = 1, 8, 64, ..., 2^{21}
\]

The output (OUT) follows the input (IN) after delaying the rising and/or falling transitions. The LTC6994-1 will delay the rising or falling edge. The LTC6994-2 will delay both transitions, and adds the option to invert the output.

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>DELAY FUNCTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC6994-1</td>
<td>or</td>
</tr>
<tr>
<td>LTC6994-2</td>
<td>or</td>
</tr>
</tbody>
</table>

The LTC6994 also offers the ability to dynamically adjust the delay time via a separate control voltage.

For easy configuration of the LTC6994, download the TimerBlox Designer tool at www.linear.com/timerblox.
LTC6994-1/LTC6994-2

**ABSOLUTE MAXIMUM RATINGS (Note 1)**

Supply Voltage (V+) to GND ................................................. 6V
Maximum Voltage on Any Pin
.................................................. (GND – 0.3V) ≤ V_PIN ≤ (V+ + 0.3V)
Operating Temperature Range (Note 2)
LTC6994C ............................................. –40°C to 85°C
LTC6994I ............................................. –40°C to 85°C
LTC6994H .......................................... –40°C to 125°C
LTC6994MP ....................................... –55°C to 125°C

**Specified Temperature Range (Note 3)**
LTC6994C ............................................. 0°C to 70°C
LTC6994I ............................................. –40°C to 85°C
LTC6994H .......................................... –40°C to 125°C
LTC6994MP ....................................... –55°C to 125°C

**Junction Temperature**
.................................................. 150°C

**Storage Temperature Range**
.................................................. 150°C

**Lead Temperature (Soldering, 10 sec)**
S6 Package .................................................. 300°C

**PIN CONFIGURATION**

**ORDER INFORMATION**

Lead Free Finish

<table>
<thead>
<tr>
<th>TAPE AND REEL (MIN)</th>
<th>TAPE AND REEL</th>
<th>PART MARKING</th>
<th>PACKAGE DESCRIPTION</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC6994CDCB-1#TRMPBF</td>
<td>LTC6994CDCB-1#TRMPBF</td>
<td>LFCT</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC6994IDCB-1#TRMPBF</td>
<td>LTC6994IDCB-1#TRMPBF</td>
<td>LFCT</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6994HDCB-1#TRMPBF</td>
<td>LTC6994HDCB-1#TRMPBF</td>
<td>LFCT</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC6994CDCB-2#TRMPBF</td>
<td>LTC6994CDCB-2#TRMPBF</td>
<td>LFCW</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC6994IDCB-2#TRMPBF</td>
<td>LTC6994IDCB-2#TRMPBF</td>
<td>LFCW</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6994HDCB-2#TRMPBF</td>
<td>LTC6994HDCB-2#TRMPBF</td>
<td>LFCW</td>
<td>6-Lead (2mm × 3mm) Plastic DFN</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC6994CS6-1#TRMPBF</td>
<td>LTC6994CS6-1#TRMPBF</td>
<td>LTFC</td>
<td>6-Lead Plastic TSOT-23</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC6994IS6-1#TRMPBF</td>
<td>LTC6994IS6-1#TRMPBF</td>
<td>LTFC</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6994HS6-1#TRMPBF</td>
<td>LTC6994HS6-1#TRMPBF</td>
<td>LTFC</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC6994MPS6-1#TRMPBF</td>
<td>LTC6994MPS6-1#TRMPBF</td>
<td>LTFC</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–55°C to 125°C</td>
</tr>
<tr>
<td>LTC6994CS6-2#TRMPBF</td>
<td>LTC6994CS6-2#TRMPBF</td>
<td>LTFCX</td>
<td>6-Lead Plastic TSOT-23</td>
<td>0°C to 70°C</td>
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<tr>
<td>LTC6994IS6-2#TRMPBF</td>
<td>LTC6994IS6-2#TRMPBF</td>
<td>LTFCX</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6994HS6-2#TRMPBF</td>
<td>LTC6994HS6-2#TRMPBF</td>
<td>LTFCX</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC6994MPS6-2#TRMPBF</td>
<td>LTC6994MPS6-2#TRMPBF</td>
<td>LTFCX</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–55°C to 125°C</td>
</tr>
</tbody>
</table>

TRM = 500 pieces. *Temperature grades are identified by a label on the shipping container.
Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on lead based finish parts.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/
**ELECTRICAL CHARACTERISTICS**

The * denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. Test conditions are $V^+ = 2.25V$ to $5.5V$, $IN = 0V$, $DIVCODE = 0$ to $15$ ($N_{DIV} = 1$ to $2^{15}$), $R_{SET} = 50k$ to $800k$, $R_{LOAD} = 5k$, $C_{LOAD} = 5pF$ unless otherwise noted.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{DELAY}$</td>
<td>Delay Time</td>
<td></td>
<td>$1\mu$s</td>
<td>$33.55$ sec</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$\Delta t_{DELAY}$</td>
<td>Delay Accuracy (Note 4)</td>
<td>$N_{DIV} \geq 512$</td>
<td>$\pm 1.7$</td>
<td>$\pm 3.0$</td>
<td>$%$</td>
<td>$%$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$8 \leq N_{DIV} \leq 64$</td>
<td>$\pm 2.4$</td>
<td>$\pm 3.4$</td>
<td>$%$</td>
<td>$%$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$N_{DIV} = 1$</td>
<td>$\pm 3.8$</td>
<td>$\pm 5.1$</td>
<td>$%$</td>
<td>$%$</td>
</tr>
<tr>
<td>$\Delta t_{DELAY}/\Delta T$</td>
<td>Delay Drift Over Temperature</td>
<td>$N_{DIV} \geq 512$</td>
<td>$\pm 0.006$</td>
<td>$%/°C$</td>
<td></td>
<td>$%/°C$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$N_{DIV} \leq 64$</td>
<td>$\pm 0.008$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Delay Change With Supply</td>
<td>$N_{DIV} \geq 512$</td>
<td>$V^+ = 4.5V$ to $5.5V$</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.25V$ to $4.5V$</td>
<td>$\pm 0.6$</td>
<td>$\pm 0.2$</td>
<td>$%$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$8 \leq N_{DIV} \leq 64$</td>
<td>$V^+ = 4.5V$ to $5.5V$</td>
<td>$\pm 0.9$</td>
<td>$\pm 0.2$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.7V$ to $4.5V$</td>
<td>$\pm 0.7$</td>
<td>$\pm 0.2$</td>
<td>$0.4$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.25V$ to $2.7V$</td>
<td>$\pm 1.1$</td>
<td>$\pm 0.1$</td>
<td>$0.9$</td>
</tr>
<tr>
<td>$\Delta t_{DELAY}/\Delta T$</td>
<td></td>
<td></td>
<td>$N_{DIV} = 1$</td>
<td>$V^+ = 5.5V$</td>
<td>$1.0$</td>
<td>$%P-P$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.25V$</td>
<td>$0.5$</td>
<td>$%P-P$</td>
</tr>
<tr>
<td>$\Delta t_{DELAY}/\Delta T$</td>
<td></td>
<td></td>
<td>$N_{DIV} = 8$</td>
<td></td>
<td>$0.20$</td>
<td>$%P-P$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$N_{DIV} = 64$</td>
<td></td>
<td>$0.05$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$N_{DIV} = 512$</td>
<td></td>
<td>$0.20$</td>
<td>$%P-P$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$N_{DIV} = 4096$</td>
<td></td>
<td>$0.03$</td>
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<tr>
<td>$t_S$</td>
<td>Delay Change Settling Time (Note 9)</td>
<td>$t_{MASTER} = t_{DELAY}/N_{DIV}$</td>
<td>$6 \times t_{MASTER}$</td>
<td></td>
<td></td>
<td>$\mu$s</td>
</tr>
<tr>
<td>Power Supply</td>
<td>Operating Supply Voltage Range</td>
<td></td>
<td>$2.25$</td>
<td>$5.5$</td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Power-On Reset Voltage</td>
<td></td>
<td>$1.95$</td>
<td></td>
<td>$V$</td>
<td></td>
</tr>
<tr>
<td>$I_{S,IDLE}$</td>
<td>Supply Current (Idle)</td>
<td>$R_L = \infty$, $R_{SET} = 50k$, $N_{DIV} \leq 64$</td>
<td>$V^+ = 5.5V$</td>
<td></td>
<td>$165$</td>
<td>$200$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.25V$</td>
<td></td>
<td>$125$</td>
<td>$160$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = \infty$, $R_{SET} = 50k$, $N_{DIV} \geq 512$</td>
<td></td>
<td>$135$</td>
<td>$175$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 5.5V$</td>
<td></td>
<td>$105$</td>
<td>$140$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.25V$</td>
<td></td>
<td>$70$</td>
<td>$110$</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_L = \infty$, $R_{SET} = 800k$, $N_{DIV} \leq 64$</td>
<td></td>
<td>$60$</td>
<td>$95$</td>
<td>$\mu A$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 5.5V$</td>
<td></td>
<td>$65$</td>
<td>$100$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$V^+ = 2.25V$</td>
<td></td>
<td>$55$</td>
</tr>
<tr>
<td>Analog Inputs</td>
<td>Voltage at SET Pin</td>
<td></td>
<td>$0.97$</td>
<td>$1.00$</td>
<td>$1.03$</td>
<td>$V$</td>
</tr>
<tr>
<td>$\Delta V_{SET}/\Delta T$</td>
<td>VSET Drift Over Temperature</td>
<td></td>
<td>$\pm 75$</td>
<td></td>
<td>$\mu V/°C$</td>
<td></td>
</tr>
<tr>
<td>$R_{SET}$</td>
<td>Frequency-Setting Resistor</td>
<td></td>
<td>$50$</td>
<td>$800$</td>
<td>$\Omega$</td>
<td></td>
</tr>
<tr>
<td>$V_{DIV}$</td>
<td>DIV Pin Voltage</td>
<td></td>
<td>$0$</td>
<td>$V^+$</td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>$\Delta V_{DIV}/\Delta V^*$</td>
<td>DIV Pin Valid Code Range (Note 5)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>$%$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Deviation from Ideal $V_{DIV}/V^* = (DIVCODE + 0.5)/16$</td>
<td></td>
<td></td>
<td>$\pm 1.5$</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>DIV Pin Input Current</td>
<td></td>
<td></td>
<td>$\pm 10$</td>
</tr>
</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

The \* denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25°C \). Test conditions are \( V^+ = 2.25V \) to \( 5.5V \), \( IN = 0V \), \( DIVCODE = 0 \) to \( 15 \) \((NDIV = 1 \) to \( 2^{21}\)), \( R_{SET} = 50k \) to \( 800k \), \( R_{LOAD} = \infty \), \( C_{LOAD} = 5pF \) unless otherwise noted.

#### SYMBOL | PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
---|---|---|---|---|---|---
Digital I/O

| IN Pin Input Capacitance | | | 2.5 | | | pF
| IN Pin Input Current | \( IN = 0V \) to \( V^+ \) | | | \( \pm 10 \) | | nA
| \( V_{IH} \) | High Level IN Pin Input Voltage \((Note 6)\) | | | \( 0.7 \) • \( V^+ \) | | V
| \( V_{IL} \) | Low Level IN Pin Input Voltage \((Note 6)\) | | | \( 0.3 \) • \( V^+ \) | | V
| \( I_{OUT(MAX)} \) | Output Current \( V^+ = 2.7V \) to \( 5.5V \) | | | \( \pm 20 \) | | mA
| \( V_{OH} \) | High Level Output Voltage \((Note 7)\) \( V^+ = 5.5V \) | \( I_{OUT} = -1mA \) | 5.45 | 5.48 | | V
| | | \( I_{OUT} = -16mA \) | 4.84 | 5.15 | | V
| | | \( V^+ = 3.3V \) \( I_{OUT} = -1mA \) | 3.24 | 3.27 | | V
| | | \( I_{OUT} = -10mA \) | 2.75 | 2.99 | | V
| | | \( V^+ = 2.25V \) \( I_{OUT} = -1mA \) | 2.17 | 2.21 | | V
| | | \( I_{OUT} = -8mA \) | 1.58 | 1.88 | | V
| \( V_{OL} \) | Low Level Output Voltage \((Note 7)\) \( V^+ = 5.5V \) | \( I_{OUT} = 1mA \) | 0.22 | 0.26 | | V
| | | \( I_{OUT} = 16mA \) | 0.26 | 0.54 | | V
| | | \( V^+ = 3.3V \) \( I_{OUT} = 1mA \) | 0.03 | 0.05 | | V
| | | \( I_{OUT} = 10mA \) | 0.22 | 0.46 | | V
| | | \( V^+ = 2.25V \) \( I_{OUT} = 1mA \) | 0.03 | 0.07 | | V
| | | \( I_{OUT} = 8mA \) | 0.26 | 0.54 | | V
| \( t_{PD} \) | Propagation Delay \( V^+ = 5.5V \) | | | 10 | | ns
| | | \( V^+ = 3.3V \) | 14 | | ns
| | | \( V^+ = 2.25V \) | 24 | | ns
| \( t_{WIDTH} \) | Minimum Recognized Input Pulse Width \( V^+ = 3.3V \) | | | 5 | | ns
| \( t_r \) | Output Rise Time \((Note 8)\) \( V^+ = 5.5V \) | | | 1.1 | | ns
| | | \( V^+ = 3.3V \) | 1.7 | | ns
| | | \( V^+ = 2.25V \) | 2.7 | | ns
| \( t_f \) | Output Fall Time \((Note 8)\) \( V^+ = 5.5V \) | | | 1.0 | | ns
| | | \( V^+ = 3.3V \) | 1.6 | | ns
| | | \( V^+ = 2.25V \) | 2.4 | | ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LTC6994C is guaranteed functional over the operating temperature range of \(-40°C\) to \( 85°C\).

**Note 3:** The LTC6994C is guaranteed to meet specified performance from \( 0°C \) to \( 70°C \). The LTC6994C is designed, characterized and expected to meet specified performance from \(-40°C \) to \( 85°C \) but it is not tested or QA sampled at these temperatures. The LTC6994I is guaranteed to meet specified performance from \(-40°C \) to \( 85°C \). The LTC6994H is guaranteed to meet specified performance from \(-40°C \) to \( 125°C \). The LTC6994MP is guaranteed to meet specified performance from \(-55°C \) to \( 125°C \).

**Note 4:** Delay accuracy is defined as the deviation from the \( t_{DELAY} \) equation, assuming \( R_{SET} \) is used to program the delay.

**Note 5:** See Operation section, Table 1 and Figure 2 for a full explanation of how the DIV pin voltage selects the value of DIVCODE.

**Note 6:** The IN pin has hysteresis to accommodate slow rising or falling signals. The threshold voltages are proportional to \( V^+ \). Typical values can be estimated at any supply voltage using:

\[
V_{IN(RISING)} \approx 0.55 \cdot V^+ + 185mV \quad \text{and} \quad V_{IN(FALLING)} \approx 0.48 \cdot V^+ - 155mV
\]

**Note 7:** To conform to the Logic IC Standard, current out of a pin is arbitrarily given a negative value.

**Note 8:** Output rise and fall times are measured between the 10% and the 90% power supply levels with 5pF output load. These specifications are based on characterization.

**Note 9:** Settling time is the amount of time required for the output to settle within ±1% of the final delay after a 0.5x or 2x change in \( I_{SET} \).

**Note 10:** Jitter is the ratio of the deviation of the programmed delay to the mean of the delay. This specification is based on characterization and is not 100% tested.
**TYPICAL PERFORMANCE CHARACTERISTICS**

V\(^+\) = 3.3V, R\(_{SET}\) = 200k and T\(_A\) = 25°C unless otherwise noted.

**Delay Drift vs Temperature**
- **(N\(_{DIV}\) ≤ 64)**
- **(N\(_{DIV}\) ≥ 512)**

**Delay Drift vs Supply Voltage**
- **(N\(_{DIV}\) = 1)**
- **(N\(_{DIV}\) > 1)**

---

**Table:**

<table>
<thead>
<tr>
<th>Temperature (°C)</th>
<th>DRIFT (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>-50</td>
<td>0</td>
</tr>
<tr>
<td>-25</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>25</td>
<td>0</td>
</tr>
<tr>
<td>75</td>
<td>0</td>
</tr>
<tr>
<td>100</td>
<td>0</td>
</tr>
<tr>
<td>125</td>
<td>0</td>
</tr>
</tbody>
</table>

**Graphs:**

- **RSET = 50k**
- **RSET = 200k**
- **RSET = 800k**

**RISING EDGE DELAY** REFERENCED TO V\(^+\) = 4V

**FALLING EDGE DELAY** REFERENCED TO V\(^+\) = 4V

---

**Notes:**

- SUPPLY (V)
- RISING EDGE DELAY
- FALLING EDGE DELAY
- REFERENCED TO V\(^+\) = 4V
TYPICAL PERFORMANCE CHARACTERISTICS

$V^+ = 3.3\text{V}$, $R_{\text{SET}} = 200\text{k\Omega}$ and $T_A = 25^\circ\text{C}$ unless otherwise noted.

Delay Error vs $R_{\text{SET}}$ ($N_{\text{DIV}} = 1$)

Delay Error vs $R_{\text{SET}}$ ($8 \leq N_{\text{DIV}} \leq 64$)

Delay Error vs $R_{\text{SET}}$ ($N_{\text{DIV}} \geq 512$)

Delay Error vs $N_{\text{DIV}}$ (NDIV = 1)

Delay Error vs $N_{\text{DIV}}$ (8 ≤ NDIV ≤ 64)

Delay Error vs $N_{\text{DIV}}$ (NDIV ≥ 512)

$V_{\text{SET}}$ Drift vs $I_{\text{SET}}$

$V_{\text{SET}}$ Drift vs Supply Voltage

$V_{\text{SET}}$ vs Temperature

$V_{\text{SET}}$ = 10µA

$V^+ = 4\text{V}$

$T_A$ = 25°C

$R_{\text{SET}}$ = 50k

$R_{\text{SET}}$ = 800k

3 PARTS
**TYPICAL PERFORMANCE CHARACTERISTICS**

\(V^+ = 3.3V, R_{SET} = 200k\) and \(T_A = 25^\circ\)C unless otherwise noted.

---

**Typical \(V_{SET}\) Distribution**

- 2 LOTS
- DFN AND SOT-23
- 1274 UNITS

**Supply Current vs Supply Voltage**

- \(I_{\text{ACTIV}}(V+) = 50k, +1, \text{ACTIVE}\)
- \(I_{\text{ACTIV}}(V+) = 50k, +1, \text{IDLE}\)
- \(I_{\text{ACTIV}}(V+) = 100k, +8, \text{ACTIVE}\)
- \(I_{\text{ACTIV}}(V+) = 100k, +8, \text{IDLE}\)

**Supply Current vs Temperature**

- \(I_{\text{ACTIV}}(V+) = 50k, +1, \text{ACTIVE}\)
- \(I_{\text{ACTIV}}(V+) = 50k, +1, \text{IDLE}\)
- \(I_{\text{ACTIV}}(V+) = 100k, +3, \text{ACTIVE}\)
- \(I_{\text{ACTIV}}(V+) = 800k, +512\)

**Supply Current vs \(t_{\text{DELAY}}\) (5V)**

- \(I_{\text{ACTIV}}(5V) = 50k, +1, \text{ACTIVE}\)
- \(I_{\text{ACTIV}}(5V) = 50k, +1, \text{IDLE}\)
- \(I_{\text{ACTIV}}(2.5V) = 100k, +8, \text{ACTIVE}\)
- \(I_{\text{ACTIV}}(2.5V) = 100k, +8, \text{IDLE}\)

**IN Threshold Voltage vs Supply Voltage**

- POSITIVE GOING
- NEGATIVE GOING

**Peak-to-Peak Jitter vs \(t_{\text{DELAY}}\)**

- \(\text{PEAK-TO-Peak Jitter} = 1.5, 5.5V\)
- \(\text{PEAK-TO-Peak Jitter} = 1.2, 2.25V\)
- \(\text{PEAK-TO-Peak Jitter} = 0.6, 5.5V\)
- \(\text{PEAK-TO-Peak Jitter} = 0.6, 5.5V\)

**Typical \(I_{\text{SET}}\) Current Limit vs \(V^+\)**

- SET PIN SHORTED TO GND
TYPICAL PERFORMANCE CHARACTERISTICS

V+ = 3.3V, RSET = 200k and TA = 25°C unless otherwise noted.

Input Propagation Delay (tPD)
vs Supply Voltage

![Input Propagation Delay Graph]

Rise and Fall Time
vs Supply Voltage

![Rise and Fall Time Graph]

Output Resistance
vs Supply Voltage

![Output Resistance Graph]

Start-Up, RSET = 800k
(LTC6994-1)

![Start-Up Graph 1]

Start-Up, RSET = 50k
(LTC6994-2, POL = 1)

![Start-Up Graph 2]
**PIN FUNCTIONS (DCB/S6)**

**V+ (Pin 1/Pin 5):** Supply Voltage (2.25V to 5.5V). This supply should be kept free from noise and ripple. It should be bypassed directly to the GND pin with a 0.1µF capacitor.

**DIV (Pin 2/Pin 4):** Programmable Divider and Polarity Input. The DIV pin voltage ($V_{DIV}$) is internally converted into a 4-bit result (DIVCODE). $V_{DIV}$ may be generated by a resistor divider between $V^+$ and GND. Use 1% resistors to ensure an accurate result. The DIV pin and resistors should be shielded from the OUT pin or any other traces that have fast edges. Limit the capacitance on the DIV pin to less than 100pF so that $V_{DIV}$ settles quickly. The MSB of DIVCODE (POL) selects the delay functionality. For the LTC6994-1, POL = 0 will delay the rising transition and POL = 1 will delay the falling transition. For the LTC6994-2, both transitions are delayed so POL = 1 can be used to invert the output.

**SET (Pin 3/Pin 3):** Delay Setting Input. The voltage on the SET pin ($V_{SET}$) is regulated to 1V above GND. The amount of current sourced from the SET pin ($I_{SET}$) programs the master oscillator frequency. The $I_{SET}$ current range is 1.25µA to 20µA. The delayed output transition will be not occur if $I_{SET}$ drops below approximately 500nA. Once $I_{SET}$ increases above 500nA the delayed edge will transition. A resistor connected between SET and GND is the most accurate way to set the delay. For best performance, use a precision metal or thin film resistor of 0.5% or better tolerance and 50ppm/°C or better temperature coefficient. For lower accuracy applications an inexpensive 1% thick film resistor may be used.

Limit the capacitance on the SET pin to less than 10pF to minimize jitter and ensure stability. Capacitance less than 100pF maintains the stability of the feedback circuit regulating the $V_{SET}$ voltage.

**IN (Pin 4/Pin 1):** Logic Input. Depending on the version and POL bit setting, rising or falling edges on IN will propagate to OUT after a programmable delay. The LTC6994-1 will delay only the rising or falling edge. The LTC6994-2 will delay both edges.

**GND (Pin 5/Pin 2):** Ground. Tie to a low inductance ground plane for best performance.

**OUT (Pin 6/Pin 6):** Output. The OUT pin swings from GND to $V^+$ with an output resistance of approximately 30Ω. When driving an LED or other low impedance load a series output resistor should be used to limit source/sink current to 20mA.
LTC6994-1/LTC6994-2

BLOCK DIAGRAM (S6 package pin numbers shown)

- **4-BIT A/D CONVERTER**
- **DIGITAL FILTER**
- **INPUT BUFFER**
- **MASTER OSCILLATOR**
  - \( I_{\text{MASTER}} = \frac{V_{\text{SET}}}{100k\Omega} \times I_{\text{SET}} \)
- **PROGRAMMABLE DIVIDER**
  - Divide by \(1, 8, 64, 512, 4096, 2^{15}, 2^{18}, 2^{21} \)
- **HALT OSCILLATOR**
  - If \( I_{\text{SET}} < 500 \text{nA} \)
- **MCLK**
- **EDGE-CONTROLLED DELAY LOGIC**
- **OUTPUT POLARITY (LTC6994-2)**

**Pins**
- **1**: INPUT
- **2**: GND
- **3**: VSET = 1V
- **4**: VSET = -1V
- **5**: V^*
- **6**: OUT

**Components**
- \( R_1, R_2 \)
- \( I_{\text{SET}} \)
- \( V_{\text{SET}} \)
- \( V^* \)
- MCLK

**Specifications**
- \( t_{\text{MASTER}} = 1\mu\text{s} \)
- \( 50k/\Omega \)

**Polarity (LTC6994-2)**
- **POLE**

**Additional Features**
- **4-BIT A/D CONVERTER**
- **50k/\Omega**
- **ISET**
- **VSET = 1V**
- **GNDSET**

**Diode**
- \( \text{D} \)
**OPERATION**

The LTC6994 is built around a master oscillator with a 1µs minimum period. The oscillator is controlled by the SET pin current (I_SET) and voltage (V_SET), with a 1µs/50kΩ conversion factor that is accurate to ±1.7% under typical conditions.

\[ t_{MASTER} = \frac{1\mu s}{50k\Omega} \cdot \frac{V_{SET}}{I_{SET}} \]

A feedback loop maintains V_SET at 1V ±30mV, leaving I_SET as the primary means of controlling the input-to-output delay. The simplest way to generate I_SET is to connect a resistor (R_SET) between SET and GND, such that \( I_{SET} = \frac{V_{SET}}{R_{SET}} \). The master oscillator equation reduces to:

\[ t_{MASTER} = 1\mu s \cdot \frac{R_{SET}}{50k\Omega} \]

From this equation, it is clear that V_SET drift will not affect the input-to-output delay when using a single program resistor (R_SET). Error sources are limited to R_SET tolerance and the inherent accuracy \( \Delta t_{DELAY} \) of the LTC6994.

R_SET may range from 50k to 800k (equivalent to I_SET between 1.25µA and 20µA).

When the input makes a transition that will be delayed (as determined by the part version and POL bit setting), the master oscillator is enabled to time the delay. When the desired duration is reached, the output is allowed to transition.

The LTC6994 also includes a programmable frequency divider which can further divide the frequency by 1, 8, 64, 512, 4096, 2^{15}, 2^{18} or 2^{21}. This extends the delay duration by those same factors. The divider ratio N_DIV is set by a resistor divider attached to the DIV pin.

\[ t_{DELAY} = \frac{N_{DIV}}{50k\Omega} \cdot \frac{V_{SET}}{I_{SET}} \cdot 1\mu s \]

With R_SET in place of V_SET/I_SET the equation reduces to:

\[ t_{DELAY} = \frac{N_{DIV} \cdot R_{SET}}{50k\Omega} \cdot 1\mu s \]

**DIVCODE**

The DIV pin connects to an internal, V+ referenced 4-bit A/D converter that determines the DIVCODE value. DIVCODE programs two settings on the LTC6994:

1. **DIVCODE** determines the frequency divider setting, N_DIV.
2. The DIVCODE MSB is the POL bit, and configures a different polarity setting on the two versions.
   a. LTC6994-1: POL selects rising or falling-edge delays. POL = 0 will delay rising-edge transitions. POL = 1 will delay falling-edge transitions.
   b. LTC6994-2: POL selects the output inversion. POL = 1 inverts the output signal.

V_DIV may be generated by a resistor divider between V+ and GND as shown in Figure 1.

Table 1 offers recommended 1% resistor values that accurately produce the correct voltage division as well as the corresponding N_DIV and POL values for the recommended resistor pairs. Other values may be used as long as:

1. The V_DIV/V+ ratio is accurate to ±1.5% (including resistor tolerances and temperature effects)
2. The driving impedance (R1||R2) does not exceed 500kΩ.
**OPERATION**

If the voltage is generated by other means (i.e., the output of a DAC) it must track the \( V^+ \) supply voltage. The last column in Table 1 shows the ideal ratio of \( V_{DIV} \) to the supply voltage, which can also be calculated as:

\[
\frac{V_{DIV}}{V^+} = \frac{DIVCODE + 0.5}{16} \pm 1.5\%
\]

For example, if the supply is 3.3V and the desired DIVCODE is 4, \( V_{DIV} = 0.281 \times 3.3 = 928\text{mV} \pm 50\text{mV} \).

Figure 2 illustrates the information in Table 1, showing that \( N_{DIV} \) is symmetric around the DIVCODE midpoint.

<table>
<thead>
<tr>
<th>DIVCODE</th>
<th>POL</th>
<th>( N_{DIV} )</th>
<th>Recommended ( t_{DELAY} )</th>
<th>R1 (k)</th>
<th>R2 (k)</th>
<th>( V_{DIV}/V^+ )</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>1( \mu \text{s} ) to 16( \mu \text{s} )</td>
<td>Open</td>
<td>Short</td>
<td>( \leq 0.03125 \pm 0.015 )</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>8</td>
<td>8( \mu \text{s} ) to 128( \mu \text{s} )</td>
<td>976</td>
<td>102</td>
<td>0.09375 \pm 0.015</td>
</tr>
<tr>
<td>2</td>
<td>0</td>
<td>64</td>
<td>64( \mu \text{s} ) to 1.024( \text{ms} )</td>
<td>976</td>
<td>182</td>
<td>0.15625 \pm 0.015</td>
</tr>
<tr>
<td>3</td>
<td>0</td>
<td>512</td>
<td>512( \mu \text{s} ) to 8.192( \text{ms} )</td>
<td>1000</td>
<td>280</td>
<td>0.21875 \pm 0.015</td>
</tr>
<tr>
<td>4</td>
<td>0</td>
<td>4,096</td>
<td>4.096( \text{ms} ) to 65.54( \text{ms} )</td>
<td>1000</td>
<td>392</td>
<td>0.28125 \pm 0.015</td>
</tr>
<tr>
<td>5</td>
<td>0</td>
<td>32,768</td>
<td>32.77( \text{ms} ) to 524.3( \text{ms} )</td>
<td>1000</td>
<td>523</td>
<td>0.34375 \pm 0.015</td>
</tr>
<tr>
<td>6</td>
<td>0</td>
<td>262,144</td>
<td>262.1( \text{ms} ) to 4.194( \text{sec} )</td>
<td>1000</td>
<td>681</td>
<td>0.40625 \pm 0.015</td>
</tr>
<tr>
<td>7</td>
<td>0</td>
<td>2,097,152</td>
<td>2.097( \text{sec} ) to 33.55( \text{sec} )</td>
<td>1000</td>
<td>887</td>
<td>0.46875 \pm 0.015</td>
</tr>
<tr>
<td>8</td>
<td>1</td>
<td>2,097,152</td>
<td>2.097( \text{sec} ) to 33.55( \text{sec} )</td>
<td>887</td>
<td>1000</td>
<td>0.53125 \pm 0.015</td>
</tr>
<tr>
<td>9</td>
<td>1</td>
<td>262,144</td>
<td>262.1( \text{ms} ) to 4.194( \text{sec} )</td>
<td>681</td>
<td>1000</td>
<td>0.59375 \pm 0.015</td>
</tr>
<tr>
<td>10</td>
<td>1</td>
<td>32,768</td>
<td>32.77( \text{ms} ) to 524.3( \text{ms} )</td>
<td>523</td>
<td>1000</td>
<td>0.65625 \pm 0.015</td>
</tr>
<tr>
<td>11</td>
<td>1</td>
<td>4,096</td>
<td>4.096( \text{ms} ) to 65.54( \text{ms} )</td>
<td>392</td>
<td>1000</td>
<td>0.71875 \pm 0.015</td>
</tr>
<tr>
<td>12</td>
<td>1</td>
<td>512</td>
<td>512( \mu \text{s} ) to 8.192( \text{ms} )</td>
<td>280</td>
<td>1000</td>
<td>0.78125 \pm 0.015</td>
</tr>
<tr>
<td>13</td>
<td>1</td>
<td>64</td>
<td>64( \mu \text{s} ) to 1.024( \text{ms} )</td>
<td>182</td>
<td>976</td>
<td>0.84375 \pm 0.015</td>
</tr>
<tr>
<td>14</td>
<td>1</td>
<td>8</td>
<td>8( \mu \text{s} ) to 128( \mu \text{s} )</td>
<td>102</td>
<td>976</td>
<td>0.90625 \pm 0.015</td>
</tr>
<tr>
<td>15</td>
<td>1</td>
<td>1</td>
<td>1( \mu \text{s} ) to 16( \mu \text{s} )</td>
<td>Short</td>
<td>Open</td>
<td>( \geq 0.96875 \pm 0.015 )</td>
</tr>
</tbody>
</table>
**OPERATION**

**Edge-Controlled Delay**

The LTC6994 is a programmable delay or pulse qualifier. It can perform noise filtering, which distinguishes it from a delay line (which simply delays all input transitions).

When the voltage on the LTC6994 input pin (IN) transitions low or high, the LTC6994 can delay the corresponding output transition by any time from 1µs to 33.6 seconds.

**LTC6994-1 Functionality**

Figures 3 details the basic operation of the LTC6994-1 when configured to delay rising edge transitions (POL = 0). A rising edge on the IN pin initiates the timing. OUT remains low for the duration of $t_{\text{DELAY}}$. If IN stays high then OUT will transition high after this time. If the input doesn’t remain high long enough for OUT to transition high then the timing will restart on each successive rising edge. In this way, the LTC6994-1 can serve as a pulse qualifier, filtering out noisy or short signals.

On a falling edge at the input, the output will follow immediately (after a short propagation delay $t_{\text{PD}}$). Note that the output pulse width may be extremely short if IN falls immediately after OUT rises.

Figure 4 details the operation of the LTC6994-1 when configured to delay falling edges (POL = 1).

![Figure 3. Rising-Edge Delayed Timing Diagram (LTC6994-1, POL = 0)](image3)

![Figure 4. Falling-Edge Delayed Timing Diagram (LTC6994-1, POL = 1)](image4)
LTC6994-1/LTC6994-2

OPERATION

LTC6994-2 Functionality

Figures 5 details the basic operation of the LTC6994-2 when configured for noninverting operation (POL = 0). As before, a rising edge on the IN pin initiates the timing and, if IN remains high, OUT will transition high after $t_{DELAY}$. Unlike the LTC6994-1, falling edges are delayed in the same way. When IN transitions low, OUT will follow after $t_{DELAY}$.

If the input doesn’t remain high or low long enough for OUT to follow, the timing will restart on the next transition.

Also unlike the LTC6994-1, the output pulse width can never be less than $t_{DELAY}$. Therefore, the LTC6994-2 can generate pulses with a defined minimum width.

Figure 6 details the operation of the LTC6994-2 when the output is inverted (POL = 1).

![Both Edges Delayed Timing Diagram](image)

**Figure 5. Both Edges Delayed Timing Diagram (LTC6994-2, POL = 0)**

![Both Edges Delayed (Inverting) Timing Diagram](image)

**Figure 6. Both Edges Delayed (Inverting) Timing Diagram (LTC6994-2, POL = 1)**
OPERATION

Changing DIVCODE After Start-Up

Following start-up, the A/D converter will continue monitoring $V_{DIV}$ for changes. Changes to DIVCODE will be recognized slowly, as the LTC6994 places a priority on eliminating any “wandering” in the DIVCODE. The typical delay depends on the difference between the old and new DIVCODE settings and is proportional to the master oscillator period.

$$t_{DIVCODE} = 16 \times (\Delta DIVCODE + 6) \times t_{MASTER}$$

A change in DIVCODE will not be recognized until it is stable, and will not pass through intermediate codes. A digital filter is used to guarantee the DIVCODE has settled to a new value before making changes to the output. However, if the delay timing is active during the transition, the actual delay can take on a value between the two settings.

![Figure 7a. DIVCODE Change from 0 to 2](image)

![Figure 7b. DIVCODE Change from 2 to 0](image)

Start-Up Time

When power is first applied, the power-on reset (POR) circuit will initiate the start-up time, $t_{START}$. The OUT pin is held low during this time and the IN pin has no control over the output. The typical value for $t_{START}$ ranges from 0.5ms to 8ms depending on the master oscillator frequency (independent of $N_{DIV}$):

$$t_{START(TYP)} = 500 \times t_{MASTER}$$

During start-up, the DIV pin A/D converter must determine the correct DIVCODE before the LTC6994 can respond to an input. The start-up time may increase if the supply or DIV pin voltages are not stable. For this reason, it is recommended to minimize the capacitance on the DIV pin so it will properly track $V^*$. Less than 100pF will not extend the start-up time.

At the end of $t_{START}$ the DIVCODE and IN pin settings are recognized, and the state of the IN pin is transferred to the output (without additional delay). If IN is high at the end of $t_{START}$, OUT will go high. Otherwise OUT will remain low. The LTC6994-2 with POL = 1 is the exception because it inverts the signal. At this point, the LTC6994 is ready to respond to rising/falling edges on the input.

![Figure 8. Start-Up Timing Diagram](image)
APPLICATIONS INFORMATION

Basic Operation

The simplest and most accurate method to program the LTC6994 is to use a single resistor, R_SET, between the SET and GND pins. The design procedure is a 3-step process. Alternatively, Linear Technology offers the easy-to-use TimerBlox Designer tool to quickly design any LTC6994 based circuit. Download the free TimerBlox Designer software at www.linear.com/timerblox.

Step 1: Select the LTC6994 Version and POL Bit Setting.

Choose LTC6994-1 to delay one (rising or falling) input transition. The POL bit then defines which edge is to be delayed. POL = 0 delays rising edges. POL = 1 delays falling edges.

Choose LTC6994-2 to delay rising and falling edges. Set POL = 0 for normal operation, or POL = 1 to invert the output.

Step 2: Select the N_DIV Frequency Divider Value.

As explained earlier, the voltage on the DIV pin sets the DIVCODE which determines both the POL bit and the N_DIV value. For a given delay time (t_DELAY), N_DIV should be selected to be within the following range:

\[ \frac{t_{\text{DELAY}}}{16\mu s} \leq N_{\text{DIV}} \leq \frac{t_{\text{DELAY}}}{1\mu s} \]  

(1)

To minimize supply current, choose the lowest N_DIV value. However, in some cases a higher value for N_DIV will provide better accuracy (see Electrical Characteristics).

Table 1 can also be used to select the appropriate N_DIV values for the desired t_DELAY.

With POL already chosen, this completes the selection of DIVCODE. Use Table 1 to select the proper resistor divider or V_DIV/V+ ratio to apply to the DIV pin.

Step 3: Calculate and Select R_SET.

The final step is to calculate the correct value for R_SET using the following equation:

\[ R_{\text{SET}} = \frac{50k}{1\mu s} \cdot \frac{t_{\text{DELAY}}}{N_{\text{DIV}}} \]  

(2)

Select the standard resistor value closest to the calculated value.

Example: Design a circuit to delay falling edges by t_DELAY = 100µs with minimum power consumption.

Step 1: Select the LTC6994 Version and POL Bit Setting.

To delay negative transitions, choose the LTC6994-1 with POL = 1.

Step 2: Select the N_DIV Frequency Divider Value.

Choose an N_DIV value that meets the requirements of Equation (1), using t_DELAY = 100µs:

\[ 6.25 \leq N_{\text{DIV}} \leq 100 \]

Potential settings for N_DIV include 8 and 64. N_DIV = 8 is the best choice, as it minimizes supply current by using a large R_SET resistor. POL = 1 and N_DIV = 8 requires DIVCODE = 14. Using Table 1, choose R1 = 102k and R2 = 976k values to program DIVCODE = 14.

Step 3: Select R_SET.

Calculate the correct value for R_SET using Equation (2).

\[ R_{\text{SET}} = \frac{50k}{1\mu s} \cdot \frac{100\mu s}{8} = 625k \]

Since 625k is not available as a standard 1% resistor, substitute 619k if a −0.97% shift in t_DELAY is acceptable. Otherwise, select a parallel or series pair of resistors such as 309k and 316k to attain a more precise resistance.

The completed design is shown in Figure 9.

![Figure 9. 100µs Negative-Edge Delay](Image)
Voltage-Controlled Delay

With one additional resistor, the LTC6994 output delay can be manipulated by an external voltage. As shown in Figure 10, voltage $V_{\text{CTRL}}$ sources/sinks a current through $R_{\text{MOD}}$ to vary the $I_{\text{SET}}$ current, which in turn modulates the delay as described in Equation (3):

$$t_{\text{DELAY}} = \frac{N_{\text{DIV}} \cdot R_{\text{MOD}}}{50k\Omega} \cdot \frac{1\mu s}{1 + \frac{R_{\text{MOD}}}{R_{\text{SET}}} \cdot \frac{V_{\text{CTRL}}}{V_{\text{SET}}}}$$

(3)

Digital Delay Control

The control voltage can be generated by a DAC (digital-to-analog converter), resulting in a digitally-controlled delay. Many DACs allow for the use of an external reference. If such a DAC is used to provide the $V_{\text{CTRL}}$ voltage, the $V_{\text{SET}}$ dependency can be eliminated by buffering $V_{\text{SET}}$ and using it as the DAC’s reference voltage, as shown in Figure 11. The DAC’s output voltage now tracks any $V_{\text{SET}}$ variation and eliminates it as an error source. The SET pin cannot be tied directly to the reference input of the DAC because the current drawn by the DAC’s REF input would affect the delay.

$I_{\text{SET}}$ Extremes (Master Oscillator Frequency Extremes)

When operating with $I_{\text{SET}}$ outside of the recommended 1.25µA to 20µA range, the master oscillator operates outside of the 62.5kHz to 1MHz range in which it is most accurate.

The oscillator will still function with reduced accuracy for $I_{\text{SET}} < 1.25µA$. At approximately 500nA, the oscillator will stop. Under this condition, the delay timing can still be initiated, but will not terminate until $I_{\text{SET}}$ increases and the master oscillator starts again.

At the other extreme, it is not recommended to operate the master oscillator beyond 2MHz because the accuracy of the DIV pin ADC will suffer.

Figure 10. Voltage-Controlled Delay

Figure 11. Digitally Controlled Delay
**APPLICATIONS INFORMATION**

**Settling Time**

Following a $2 \times$ or $0.5 \times$ step change in $I_{SET}$, the output delay takes approximately six master clock cycles ($6 \times t_{\text{MASTER}}$) to settle to within 1% of the final value. An example is shown in Figure 12, using the circuit in Figure 10.

![Figure 12. Typical Settling Time](image12)

**Coupling Error**

The current sourced by the SET pin is used to bias the internal master oscillator. The LTC6994 responds to changes in $I_{SET}$ almost immediately, which provides excellent settling time. However, this fast response also makes the SET pin sensitive to coupling from digital signals, such as the IN input.

Even an excellent layout will allow *some* coupling between IN and SET. Additional error is included in the specified accuracy for $N_{DIV} = 1$ to account for this. Figure 13 shows that ±1 supply variation is dependent on coupling from rising or falling inputs.

A very poor layout can actually degrade performance further. The PCB layout should avoid routing SET next to IN (or any other fast-edge, wide-swing signal).

![Figure 13. Delay Drift vs Supply Voltage](image13)
Power Supply Current

The Electrical Characteristics table specifies the supply current while the part is idle (waiting for an input transition). \( I_{S(IDLE)} \) varies with the programmed \( t_{DELAY} \) and the supply voltage, as described by the equations in Table 2, valid for both the LTC6994-1 and LTC6994-2.

Table 2. Approximate Idle Supply Current Equations

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>TYPICAL ( I_{S(IDLE)} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N_{DIV} \leq 64 )</td>
<td>( V^+ \cdot \left( \frac{N_{DIV} \cdot 7pF + 4pF}{t_{DELAY}} \right) + \frac{V^+}{500k\Omega} + 2.2 \cdot I_{SET} + 50\mu A )</td>
</tr>
<tr>
<td>( N_{DIV} \geq 512 )</td>
<td>( V^+ \cdot \left( \frac{N_{DIV} \cdot 7pF}{t_{DELAY}} \right) + \frac{V^+}{500k\Omega} + 1.8 \cdot I_{SET} + 50\mu A )</td>
</tr>
</tbody>
</table>

When an input transition starts the delay timing circuitry, the instantaneous supply current increases to \( I_{S(ACTIVE)} \):

\[
I_{S(ACTIVE)} = I_{S(IDLE)} + \Delta I_{S(ACTIVE)}
\]

\( \Delta I_{S(ACTIVE)} \) can be estimated using the equations in Table 3, assuming a periodic input with frequency \( f_{IN} \). The equations assume the input pulse width is greater than \( t_{DELAY} \); otherwise, the output will not transition (and the increase in supply current will be less).

Table 3. Active Increase in Supply Current

<table>
<thead>
<tr>
<th>CONDITION</th>
<th>DEVICE</th>
<th>TYPICAL ( \Delta I_{S(ACTIVE)} )^*</th>
</tr>
</thead>
<tbody>
<tr>
<td>( N_{DIV} \leq 64 )</td>
<td>LTC6994-1</td>
<td>( f_{IN} \cdot V^+ \cdot \left( \frac{N_{DIV} \cdot 5pF + 18pF + C_{LOAD}}{t_{DELAY}} \right) )</td>
</tr>
<tr>
<td>LTC6994-2</td>
<td>( f_{IN} \cdot V^+ \cdot \left( \frac{N_{DIV} \cdot 10pF + 22pF + C_{LOAD}}{t_{DELAY}} \right) )</td>
<td></td>
</tr>
<tr>
<td>( N_{DIV} \geq 512 )</td>
<td>Either Version</td>
<td>( f_{IN} \cdot V^+ \cdot C_{LOAD} )</td>
</tr>
</tbody>
</table>

^*Ignoring resistive loads (assumes \( R_{LOAD} = \infty \))

Figures 14 and 15 show how the supply current increases from \( I_{S(IDLE)} \) as the input frequency increases. At higher \( N_{DIV} \) settings, the increase in active current is smaller.
Supply Bypassing and PCB Layout Guidelines

The LTC6994 is an accurate monostable multivibrator when used in the appropriate manner. The part is simple to use and by following a few rules, the expected performance is easily achieved. Adequate supply bypassing and proper PCB layout are important to ensure this.

Figure 16 shows example PCB layouts for both the SOT-23 and DCB packages using 0603 sized passive components. The layouts assume a two layer board with a ground plane layer beneath and around the LTC6994. These layouts are a guide and need not be followed exactly.

1. Connect the bypass capacitor, C1, directly to the V+ and GND pins using a low inductance path. The connection from C1 to the V+ pin is easily done directly on the top layer. For the DCB package, C1’s connection to GND is also simply done on the top layer. For the SOT-23, OUT can be routed through the C1 pads to allow a good C1 GND connection. If the PCB design rules do not allow that, C1’s GND connection can be accomplished through multiple vias to the ground plane. Multiple vias for both the GND pin connection to the ground plane and the C1 connection to the ground plane are recommended to minimize the inductance. Capacitor C1 should be a 0.1µF ceramic capacitor.

2. Place all passive components on the top side of the board. This minimizes trace inductance.

3. Place RSET as close as possible to the SET pin and make a direct, short connection. The SET pin is a current summing node and currents injected into this pin directly modulate the output delay. Having a short connection minimizes the exposure to signal pickup.

4. Connect RSET directly to the GND pin. Using a long path or vias to the ground plane will not have a significant affect on accuracy, but a direct, short connection is recommended and easy to apply.

5. Use a ground trace to shield the SET pin. This provides another layer of protection from radiated signals.

6. Place R1 and R2 close to the DIV pin. A direct, short connection to the DIV pin minimizes the external signal coupling.
TYPICAL APPLICATIONS

Delayed One-Shot

Pulse Stretcher

Switch/Relay Debouncer
TYPICAL APPLICATIONS

Edge Chatter Filter

INPUT MUST BE STABLE FOR AT LEAST 10µs

Crossover Gate—Break-Before-Make Interval Timer

1ms OFF INTERVAL AT EACH TRANSITION
PACKAGE DESCRIPTION


**DCB Package**

6-Lead Plastic DFN (2mm × 3mm)

(Reference LTC DWG # 05-08-1715 Rev A)

**PACKAGE OUTLINE**

- 3.55 ±0.05 (2 SIDES)
- 1.65 ±0.05 (2 SIDES)
- 2.15 ±0.05
- 0.25 ± 0.05
- 1.35 ±0.05 (2 SIDES)
- 0.50 BSC

**RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS**

- 0.200 REF
- 0.75 ±0.05
- 0.00 – 0.05

**BOTTOM VIEW—EXPOSED PAD**

- R = 0.115 TYP
- R = 0.05 TYP
- 4
- 6
- 3
- 1

**NOTE:**

1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (TBD)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE
PACKAGE DESCRIPTION
Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOULD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.
# REVISION HISTORY

<table>
<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
<th>PAGE NUMBER</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>7/11</td>
<td>Revised the Description section. Added text to Basic Operation paragraph in the Applications Information section.</td>
<td>1, 16</td>
</tr>
<tr>
<td>B</td>
<td>1/12</td>
<td>Added MP-Grade. Corrected sizing of the Typical Performance Characteristics curves G31 and G32.</td>
<td>1, 2, 4, 8</td>
</tr>
</tbody>
</table>
Press-and-Hold (0.3s to 4s) Delay Timer

![Diagrams of LTC6994-1 and LTC6994-2](Diagram)

### Typical Application

**Related Parts**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1799</td>
<td>1MHz to 33MHz ThinSOT Silicon Oscillator</td>
<td>Wide Frequency Range</td>
</tr>
<tr>
<td>LTC6900</td>
<td>1MHz to 20MHz ThinSOT Silicon Oscillator</td>
<td>Low Power, Wide Frequency Range</td>
</tr>
<tr>
<td>LTC6906/LTC6907</td>
<td>10kHz to 1MHz or 40kHz ThinSOT Silicon Oscillator</td>
<td>Micropower, I$_{SUPPLY}$ = 35µA at 400kHz</td>
</tr>
<tr>
<td>LTC6930</td>
<td>Fixed Frequency Oscillator, 32.768kHz to 8.192MHz</td>
<td>0.09% Accuracy, 110µs Start-Up Time, 105µA at 32kHz</td>
</tr>
<tr>
<td>LTC6990</td>
<td>TimerBlox: Voltage-Controlled Silicon Oscillator</td>
<td>Fixed-Frequency or Voltage-Controlled Operation</td>
</tr>
<tr>
<td>LTC6991</td>
<td>TimerBlox: Resettable Low Frequency Oscillator</td>
<td>Clock Periods up to 9.5 hours</td>
</tr>
<tr>
<td>LTC6992</td>
<td>TimerBlox: Voltage-Controlled Pulse Width Modulator (PWM)</td>
<td>Simple PWM with Wide Frequency Range</td>
</tr>
<tr>
<td>LTC6993</td>
<td>TimerBlox: Monostable Pulse Generator (One-Shot)</td>
<td>Resistor-Programmable Pulse Width of 1µs to 34s</td>
</tr>
</tbody>
</table>