LTC6909

1 to 8 Output, Multiphase Silicon Oscillator with Spread Spectrum Modulation

FEATURES

- 1-, 2-, 3-, 4-, 5-, 6-, 7- or 8-Phase Outputs
- One External Resistor Sets the Output Frequency from 12.5kHz to 6.67MHz
- Optional Spread Spectrum Frequency for Improved EMI Performance
- ±10% Frequency Spreading
- Outputs Can Be Held Low or Floated (Hi-Z)
- Three Spread Spectrum Modulation Rates $f_{\text{OUT}}/16$, $f_{\text{OUT}}/32$ and $f_{\text{OUT}}/64$
- 400μA Supply Current
- Operates from a Single 2.7V to 5.5V Supply
- Fast Start-Up Time
- First Cycle Accurate
- Outputs Are High Impedance Until Frequency Settles
- MS16 Package

APPLICATIONS

- Synchronizing Multiple Switching Power Supplies

DESCRIPTION

The LTC®6909 is an easy to use precision oscillator that can provide 1-, 2-, 3-, 4-, 5-, 6-, 7- or 8-phase synchronized outputs. The LTC6909 also offers spread spectrum frequency modulation (SSFM), which can be enabled to improve electromagnetic compatibility (EMC) performance.

Eight separate outputs provide up to eight rail-to-rail, 50% duty cycle clock signals. Using three logic inputs, the outputs are configured for phase separation, ranging from 45° to 120° (three to eight phases). The clock outputs can also be held low or configured for Hi-Z. A single resistor, combined with the phase configuration, sets the output frequency, based on the following formula:

$$f_{\text{OUT}} = 20\text{MHz} \cdot \frac{10k}{R_{\text{SET}} \cdot \text{PH}}$$

where PH = 3, 4, 5, 6, 7 or 8

The LTC6909 can be used in applications requiring only one or two output phases. Alternatively, the LTC6908 family of parts provides the same two output signals but in a smaller SOT-23 or 2mm × 3mm DFN package. The LTC6908-1 provides complimentary (180°) outputs while the LTC6908-2 provides quadrature (90°) outputs.
**LTC6909**

### ABSOLUTE MAXIMUM RATINGS

(Not 1)

Supply Voltage (V+A) to GND: 6V
Supply Voltage (V+D) to GND: 6V
Maximum Voltage on Any Pin: (GND – 0.3V) ≤ VPIN ≤ (V+ + 0.3V)

Operating Temperature Range (Note 2)
  - LTC6909C: –40°C to 85°C
  - LTC6909I: –40°C to 85°C
  - LTC6909H: –40°C to 125°C

Specified Temperature Range (Note 3)
  - LTC6909C: 0°C to 70°C
  - LTC6909I: –40°C to 85°C
  - LTC6909H: –40°C to 125°C

Junction Temperature: 150°C

Storage Temperature Range: –65°C to 150°C

Lead Temperature (Soldering, 10 sec): 300°C

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### ORDER INFORMATION

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC6909CMS#PBF</td>
<td>LTC6909CMS#TRPBF</td>
<td>6909</td>
<td>16-Lead Plastic MSOP</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC6909IMS#PBF</td>
<td>LTC6909IMS#TRPBF</td>
<td>6909</td>
<td>16-Lead Plastic MSOP</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6909HMS#PBF</td>
<td>LTC6909HMS#TRPBF</td>
<td>6909</td>
<td>16-Lead Plastic MSOP</td>
<td>–40°C to 125°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)

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### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at TA = 25°C or as noted. Test conditions are V+ = V*A = V*D = 2.7V to 5.5V, RL = 5k, CL = 5pF unless otherwise noted. The modulation is turned off (MOD is connected to OUT1) and PH = 8 unless otherwise specified. RSET is defined as the resistor connected from the SET pin to the V*A pin.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>ΔfMASTER</td>
<td>Frequency Accuracy (Notes 4, 5)</td>
<td>V+ = 5V, PH = 3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>500kHz ≤ fMASTER ≤ 10MHz</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500kHz ≤ fMASTER ≤ 10MHz</td>
<td>●</td>
<td>±1</td>
<td>±2.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500kHz ≤ fMASTER ≤ 10MHz</td>
<td>●</td>
<td>±3</td>
<td>±4.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100kHz ≤ fMASTER ≤ 500kHz</td>
<td>●</td>
<td>±3</td>
<td>±4.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100kHz ≤ fMASTER ≤ 20MHz</td>
<td>●</td>
<td>±3</td>
<td>±4.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V+ = 2.7V, PH = 3</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500kHz ≤ fMASTER ≤ 10MHz</td>
<td></td>
<td></td>
<td></td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500kHz ≤ fMASTER ≤ 10MHz</td>
<td>●</td>
<td>±0.5</td>
<td>±2.5</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500kHz ≤ fMASTER ≤ 10MHz</td>
<td>●</td>
<td>±2</td>
<td>±3</td>
<td>%</td>
</tr>
<tr>
<td></td>
<td></td>
<td>500kHz ≤ fMASTER ≤ 10MHz</td>
<td>●</td>
<td>±2.5</td>
<td>±4.5</td>
<td>%</td>
</tr>
<tr>
<td>ΔfOUT/ΔT</td>
<td>Frequency Drift Over Temperature</td>
<td>RSET = 100k</td>
<td>●</td>
<td>±0.004</td>
<td></td>
<td>%/°C</td>
</tr>
<tr>
<td>ΔfOUT/V+</td>
<td>Frequency Drift Over Supply</td>
<td>V+ = 4.5V to 5.5V, RSET = 100k</td>
<td>●</td>
<td>0.4</td>
<td>0.9</td>
<td>%/V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V+ = 2.7V to 3.6V, RSET = 100k</td>
<td>●</td>
<td>0.04</td>
<td>0.35</td>
<td>%/V</td>
</tr>
</tbody>
</table>

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4909a
### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$ or as noted. Test conditions are $V^* = V^D = 2.7$V to 5.5V, $R_L = 5k$, $C_L = 5pF$ unless otherwise noted. The modulation is turned off (MOD is connected to OUT1) and PH = 8 unless otherwise specified. $R_{\text{SET}}$ is defined as the resistor connected from the SET pin to the V*A pin.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\text{SET}}$</td>
<td>Range of the $R_{\text{SET}}$ Resistor Connected Between the V*A Pin and the SET Pin</td>
<td>$4.5V \leq V^* \leq 5.5V$</td>
<td>10</td>
<td>2000</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$2.7V \leq V^* \leq 4.5V$</td>
<td>20</td>
<td>2000</td>
<td>kΩ</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Frequency Spread with SSFM Enabled</td>
<td>$R_{\text{SET}} = 100k$, MOD Pin = V*, GND or Open</td>
<td>●</td>
<td>±7</td>
<td>±10</td>
<td>±13</td>
</tr>
<tr>
<td></td>
<td>Long-Term Stability of the Output Frequency (Note 9)</td>
<td></td>
<td>300</td>
<td>ppm/√kHz</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Duty Cycle (Note 6) SSFM Disabled</td>
<td></td>
<td>●</td>
<td>45</td>
<td>50</td>
<td>55</td>
</tr>
<tr>
<td>$V^A$, $V^D$</td>
<td>Operating Supply Voltage Range</td>
<td>●</td>
<td>2.7</td>
<td>5.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>$V^*$ Combined Supply Current</td>
<td>$R_{\text{SET}} = 2M$, $R_L = \infty$, PH = 8, MOD = V*, ((f_{\text{OUT}} = 12.5kHz)), SSFM = f_{\text{OUT}}/64$</td>
<td>●</td>
<td>0.6</td>
<td>0.85</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^* = 5V$, $V^* = 2.7V$</td>
<td></td>
<td>0.55</td>
<td>0.8</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_{\text{SET}} = 20k$, $R_L = \infty$, PH = 3, MOD = GND, ((f_{\text{OUT}} = 3.33MHz)), SSFM = f_{\text{OUT}}/16$</td>
<td>●</td>
<td>2.4</td>
<td>2.7</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^* = 5V$, $V^* = 2.7V$</td>
<td></td>
<td>1.55</td>
<td>1.8</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_{\text{SET}} = 2M$, $R_L = \infty$, PH = 8, MOD = OUT1, ((f_{\text{OUT}} = 12.5kHz)), SSFM Off$</td>
<td>●</td>
<td>0.4</td>
<td>0.65</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^* = 5V$, $V^* = 2.7V$</td>
<td></td>
<td>0.37</td>
<td>0.6</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{\text{IH, MOD}}$</td>
<td>High Level MOD Input Voltage</td>
<td>●</td>
<td>$V^* - 0.4$</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IL, MOD}}$</td>
<td>Low Level MOD Input Voltage</td>
<td>●</td>
<td>0.4</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{\text{MOD}}$</td>
<td>MOD Input Current (Note 7)</td>
<td>MOD Pin = V*, $V^* = 5V$, MOD Pin = GND, $V^* = 5V$</td>
<td>●</td>
<td>–4</td>
<td>2</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>MOD Pin = GND, $V^* = 5V$</td>
<td></td>
<td>–2</td>
<td>4</td>
<td>μA</td>
</tr>
<tr>
<td>$V_{\text{RH, PH}}$</td>
<td>High Level PHx Input Voltage</td>
<td>PHx Refers to PH0, PH1 and PH2</td>
<td>●</td>
<td>$V^* - 0.4$</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IL, PH}}$</td>
<td>Low Level PHx Input Voltage</td>
<td>PHx Refers to PH0, PH1 and PH2</td>
<td>●</td>
<td>0.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{IN, PHX}}$</td>
<td>Digital Input Current, PH0, PH1, PH2</td>
<td>$0V &lt; V_{\text{IN}} &lt; V^*$</td>
<td>●</td>
<td>±1</td>
<td>μA</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OH}}$</td>
<td>High Level Output Voltage (OUT1 Through OUT8)(Note 7)</td>
<td>$V^* = 5V$, No Load</td>
<td>4.92</td>
<td>4.65</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>5mA Load to GND</td>
<td>4.35</td>
<td>4.65</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^* = 2.7V$, No Load</td>
<td>2.63</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3mA Load to GND</td>
<td>2.1</td>
<td>2.4</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OL}}$</td>
<td>Low Level Output Voltage (OUT1 Through OUT8)(Note 7)</td>
<td>$V^* = 5V$, No Load</td>
<td>0.25</td>
<td>0.55</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>5mA Load to V*</td>
<td>0.07</td>
<td>0.55</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^* = 2.7V$, No Load</td>
<td>0.25</td>
<td>0.55</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>3mA Load to V*</td>
<td>0.07</td>
<td>0.55</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$t_r$</td>
<td>Output Rise Time (Note 8)</td>
<td>$V^* = 5V$, 1.6</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^* = 2.7V$, 2.5</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>Output Fall Time (Note 8)</td>
<td>$V^* = 5V$, 1.6</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V^* = 2.7V$, 2</td>
<td>ns</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** LTC6909C and the LTC6909I are guaranteed functional over the operating temperature range of −40°C to 85°C.

**Note 3:** The LTC6909C is guaranteed to meet specified performance from 0°C to 70°C. The LTC6909C is designed, characterized and expected to meet specified performance from −40°C to 85°C but is not tested or QA sampled at these temperatures. The LTC6909I is guaranteed to meet specified performance from −40°C to 85°C. The LTC6909H is guaranteed to meet specified performance from −40°C to 125°C.
### Electrical Characteristics

**Note 4:** $f_{\text{MASTER}}$ is the internal master oscillator frequency. The output frequency is $f_{\text{MASTER}}/\text{PH}$. The PH value is determined by the connections of the PH0, PH1 and PH2 pins as described in the Applications Information section.

**Note 5:** Frequency accuracy is defined as the deviation from the $f_{\text{OUT}}$ equation. $f_{\text{MASTER}} = 20\text{MHz} \times 10k/R_{\text{SET}}$, $f_{\text{OUT}} = 20\text{MHz} \times 10k/(R_{\text{SET}} \times \text{PH})$, PH = 3, 4, 5, 6, 7 or 8.

**Note 6:** Guaranteed by 5V test.

**Note 7:** To conform to the Logic IC Standard, current out of a pin is defined as a negative value.

**Note 8:** Output rise and fall times are measured between the 10% and the 90% power supply levels with no output loading. These specifications are based on characterization.

### Typical Performance Characteristics

#### Frequency Error vs $R_{\text{SET}}$, $V^+ = 2.7\text{V}$

- **Guaranteed Min/Max**
- **Typical**
- **$T_A = 25^\circ\text{C}$**

#### Frequency Error vs $R_{\text{SET}}$, $V^+ = 5\text{V}$

- **Guaranteed Min/Max**
- **Typical**
- **$T_A = 25^\circ\text{C}$**

#### Frequency Error vs Temperature

- **Typical**
- **$T_A = 25^\circ\text{C}$**

#### Supply Current vs Supply Voltage

- **$P_{\text{H}} = 3$, SSFM Enabled**
- **$C_{\text{LOAD}} = 5\text{pF}$**
- **$R_{\text{LOAD}} = 5\text{k}$**
- **$R_{\text{SET}} = 20\text{k}$**
- **$R_{\text{SET}} = 100\text{k}$**
- **$R_{\text{SET}} = 400\text{k}$**
- **$R_{\text{SET}} = 2\text{M}$**

#### Supply Current vs $R_{\text{SET}}$ (SSFM Enabled)

- **$V^+ = 5\text{V}$**, PH = 3
- **$V^+ = 2.7\text{V}$**, PH = 3
- **$V^+ = 2.7\text{V}$**, PH = 5

#### Supply Current vs $R_{\text{SET}}$ (SSFM Disabled)

- **$V^+ = 5\text{V}$**, PH = 2
- **$V^+ = 2.7\text{V}$**, PH = 8

**Note 9:** Long term drift on silicon oscillators is primarily due to the movement of ions and impurities within the silicon and is tested at 30°C under otherwise nominal operating conditions. Long term drift is specified as ppm/$\sqrt{\text{kHz}}$ due to the typically nonlinear nature of the drift. To calculate drift for a set time period, translate that time into thousands of hours, take the square root and multiply by the typical drift number. For instance, a year is 8.77kHz and would yield a drift of 888ppm at 300ppm/$\sqrt{\text{kHz}}$. Drift without power applied to the device (aging) may be approximated as $1/10\text{th}$ of the drain with power, or 30ppm/$\sqrt{\text{kHz}}$ for a 300ppm/$\sqrt{\text{kHz}}$ device.
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Temperature

Typical Output Resistance vs Supply Voltage

Output Rise/Fall Time vs Supply Voltage

Jitter vs RSET

Output Operating at 3.33MHz

Output Operating at 6.66MHz

Output Frequency Spectrum SSFM Enable and Disabled
PIN FUNCTIONS

**V+A (Pin 1):** Analog Voltage Supply (2.7V ≤ V+A ≤ 5.5V). This supply should be kept free of noise and ripple. It should be bypassed directly to GND with a 0.1μF or greater low ESR capacitor. V+A and V+D must be connected to the same supply voltage.

**GND (Pin 2):** Ground Connections. Should be tied to a ground plane for best performance.

**PH0, PH1, PH2 (Pins 3, 4, 15):** Output Phasing Selection Pins. These are standard CMOS logic input pins and they do not have an internal pull-up or pull-down. These pins must be connected to a valid logic input 0 or 1 voltage. Connect the pins to GND for a logic 0 and to the V+D pin for a logic 1. These pins configure the output phase relationships as follows:

<table>
<thead>
<tr>
<th>PH2</th>
<th>PH1</th>
<th>PH0</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>All Outputs Are Floating (Hi-Z)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>All Outputs Are Held Low</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>3-Phase Mode (PH = 3)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>4-Phase Mode (PH = 4)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5-Phase Mode (PH = 5)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>6-Phase Mode (PH = 6)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>7-Phase Mode (PH = 7)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8-Phase Mode (PH = 8)</td>
</tr>
</tbody>
</table>

The PH0, PH1, PH2 pin connections not only determine the phase relationship of the output signals but also divide the master oscillator frequency by the value PH.

**OUT1 Through OUT8 (Pins 5 Through 12):** Oscillator Outputs. These are CMOS rail-to-rail logic outputs with a series resistance of approximately 40Ω, capable of driving 1k and/or 50pF loads. Larger loads may cause minor frequency inaccuracies due to supply bounce at high frequencies. When any output pin is not in use, it is in a floating, high impedance state. The outputs are also held in a high impedance state during start-up. After the part’s internal frequency setting loop has settled, the outputs are active, clean and operating at the set frequency (first cycle accurate).

**V+D (Pin 13):** Digital Voltage Supply (2.7V ≤ V+D ≤ 5.5V). This pin should be bypassed directly to GND with a 0.1μF or greater low ESR capacitor. V+D and V+A must be connected to the same supply voltage.

**MOD (Pin 14):** Spread Spectrum Frequency Modulation Setting Input. This input selects among four modulation rate settings. The MOD pin should be tied to ground for an $f_{\text{OUT}}/16$ modulation rate. Floating the MOD pin selects an $f_{\text{OUT}}/32$ modulation rate. The MOD pin should be tied to V+D for the $f_{\text{OUT}}/64$ modulation rate. Tying one of the active outputs to the MOD pin turns the modulation off. To detect a floating MOD pin, the LTC6909 attempts to pull the pin to the midsupply point. This is realized with two internal current sources, one tied to V+D and MOD and the other one tied to GND and MOD. Therefore, driving the MOD pin high requires sourcing approximately 2μA. Likewise, driving the MOD pin low requires sinking approximately 2μA. When the MOD pin is floated for the $f_{\text{OUT}}/32$ modulation rate, it must be bypassed using a 1nF or larger, capacitor to GND. Any AC signal coupling to the MOD pin could potentially be detected and stop the frequency modulation.

**SET (Pin 16):** Frequency Setting Resistor Input. The value of the resistor connected between this pin and V+A determines the frequency of the master oscillator. The output frequency, $f_{\text{OUT}}$, is the master oscillator frequency divided by PH as set by the PH0, PH1 and PH2 pin connections. The voltage on this pin is held approximately 1.1V below V+A. For best performance, use a precision metal film resistor with a value between 20k and 400k, and limit the capacitance on the pin to less than 10pF. Resistor values outside of this range will have some loss of accuracy as noted in the Electrical Characteristics table.
When a clock signal is present at the Mod pin input, the modulation is disabled.
As shown in the Block Diagram, the LTC6909’s master oscillator is controlled by the ratio of the voltage between the V* and SET pins and the current entering the SET pin (I_MASTER). When the spread spectrum frequency modulation (SSFM) is disabled, I_MASTER is strictly determined by the (V*A – V_SET) voltage and the R_SET resistor. When SSFM is enabled, I_MASTER is modulated by a filtered pseudorandom noise (PRN) signal. Here the I_MASTER current is a random value uniformly distributed between (I_SET – 10%) and (I_SET + 10%). In this way, the frequency is modulated to produce an approximately flat frequency spectrum, centered about the set frequency with a bandwidth equal to approximately 20% of the center frequency.

The voltage on the SET pin is forced to approximately 1.1V below V*A by the PMOS transistor and its gate bias voltage. This voltage is accurate to ±5% at a particular input current and supply voltage (see Figure 1). The LTC6909 is optimized for use with resistors between 20k and 400k corresponding to master oscillator frequencies between 500kHz and 10MHz. Accurate master oscillator frequencies up to 20MHz (R_SET = 10k) are attainable if the supply voltage is greater than 4V. The R_SET resistor, connected between the V*A and SET pins, locks together the (V*A – V_SET) voltage and the current I_SET. This allows the parts to attain excellent frequency accuracy regardless of the precision of the SET pin. The master oscillation frequency is:

\[ f_{\text{MASTER}} = 20MHz \cdot \frac{10k}{R_{\text{SET}}} \]

When the spread spectrum frequency modulation (SSFM) is disabled, the master oscillator frequency is stationary. When SSFM is enabled, the master oscillator frequency varies from 0.9 \cdot f_{\text{MASTER}} to 1.1 \cdot f_{\text{MASTER}}.

Output Frequency and Configurations

The output frequency of the LTC6909 is set by the R_SET resistor value and the connections of the PH0, PH1 and PH2 logic input pins. The following formula defines the relationship:

\[ f_{\text{OUT}} = 20MHz \cdot \frac{10k}{R_{\text{SET}} \cdot \text{PH}} \]

where PH = 3, 4, 5, 6, 7 or 8 and is defined as follows:

<table>
<thead>
<tr>
<th>PH2</th>
<th>PH1</th>
<th>PH0</th>
<th>MODE</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>All Outputs Are Floating (Hi-Z)</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>All Outputs Are Held Low</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>3-Phase Mode (PH = 3)</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
<td>4-Phase Mode (PH = 4)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>5-Phase Mode (PH = 5)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
<td>6-Phase Mode (PH = 6)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
<td>7-Phase Mode (PH = 7)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>1</td>
<td>8-Phase Mode (PH = 8)</td>
</tr>
</tbody>
</table>

The PH0, PH1 and PH2 pins are standard logic input pins. These pins do not have any active pull-up or pull-down circuitry. As such, they cannot be left floating and must be connected to a valid logic high or low voltage. The PH0, PH1 and PH2 pin connections not only divide the master oscillator frequency by the value PH but also determine the phase relationship between the output signals. Figure 2 shows the output waveforms for each of the eight possible output configurations.

Note that 2-phase, complementary (180° phase shifted) outputs are available in the 4-, 6- and 8-phase modes by choosing the correct pair of signals. For example, in 4-phase mode, OUT1 and OUT3 (or OUT2 and OUT4) are complementary.
**Figure 2a. Output Waveforms for Different PH Settings**

- **PH2 - PH1 - PH0 = 000**
  - All outputs are Hi-Z

- **PH2 - PH1 - PH0 = 001**
  - All outputs are LOW

- **PH2 - PH1 - PH0 = 010**
  - PH = 3, fOUTPUT = fMASTER/3
  - Adjacent outputs are phase shifted by 120°

- **PH2 - PH1 - PH0 = 011**
  - PH = 4, fOUTPUT = fMASTER/4
  - Adjacent outputs are phase shifted by 90°

- **PH2 - PH1 - PH0 = 100**
  - PH = 5, fOUTPUT = fMASTER/5
  - Adjacent outputs are phase shifted by 72°

- **PH2 - PH1 - PH0 = 101**
  - PH = 6, fOUTPUT = fMASTER/6
  - Adjacent outputs are phase shifted by 60°
Figure 2b. Output Waveforms for Different PH Settings

PH2 - PH1 - PH0 = 110  PH = 7, f\text{OUTPUT} = \frac{f\text{MASTER}}{7}  ADJACENT OUTPUTS ARE PHASE SHIFTED BY 51.43°

PH2 - PH1 - PH0 = 111  PH = 8, f\text{OUTPUT} = \frac{f\text{MASTER}}{8}  ADJACENT OUTPUTS ARE PHASE SHIFTED BY 45°
**OPERATION**

**Spread Spectrum Frequency Modulation**

The LTC6909 can operate with spread spectrum frequency modulation (SSFM). In this mode, the oscillator's frequency is modulated by a pseudorandom noise (PRN) signal to spread the oscillator's energy over a wide frequency band. This spreading decreases the peak electromagnetic radiation levels and improves electromagnetic compatibility (EMC) performance.

The amount of frequency spreading is fixed at 20% (±10%), where frequency spreading is defined as:

Frequency Spreading (in %) = 100 • (f_{MAX} – f_{MIN})/f_{OUT}

The I_{MASTER} current is a dynamic signal generated by a multiplying digital-to-analog converter (MDAC) referenced to I_SET and lowpass filtered. I_{MASTER} varies in a pseudorandom noise-like manner between 0.9 • I_SET and 1.1 • I_SET. This causes the output frequency to vary in a pseudorandom noise-like manner between 0.9 • f_{OUT} and 1.1 f_{OUT}.

To disable the SSFM, connect one of the active outputs to the MOD pin. An AC detector circuit shuts down the modulation circuitry if a frequency in the vicinity of the output frequency is detected at the MOD pin.

As stated previously, the modulating waveform is a pseudorandom noise-like waveform. The pseudorandom signal is generated by a linear feedback shift register that is 15 bits long. The pseudorandom sequence will repeat every \((2^{15} − 1) • N\) clock cycles. This guarantees a repetition rate below 13Hz for output frequencies up to 6.67MHz. Seven bits of the shift register are sent in parallel to the MDAC which produces the modulating current waveform. Being a digitally generated signal, the output of the MDAC is not a perfectly smooth waveform, but consists of \((2^{7})\) discrete steps that change every shift register clock cycle. Note that the shift register clock is the output frequency, f_{OUT}, divided by N, where N is the modulation rate divider setting, which is determined by the state of the MOD pin. The MOD pin should be tied to ground for the N = 16 setting. Floating the MOD pin selects N = 32. The MOD pin should be tied to V+ for the N = 64 setting.

The output of the MDAC is then filtered by a lowpass filter with a corner frequency set to the modulation rate \((f_{OUT}/N)\). This limits the rate of frequency change and softens the corners of the frequency control signal, but allows the waveform to fully settle at each frequency step. The rise and fall times of this single pole filter are approximately 0.35/f_{CORNER}. This is beneficial for clocking switching regulators, as discussed in the Applications Information section. Figure 3 illustrates how the output frequency varies over time.

---

**Figure 3**

**Diagram**

- f_{OUT} ± 10%
- 128 STEPS
- f_{STEP} = N/f_{OUT}
- t_{REPEAT} = \((2^{15} − 1) • Nf_{OUT}\)
- t_{STEP}
- t_{REPEAT}
APPLICATIONS INFORMATION

SELECTING THE FREQUENCY-SETTING RESISTOR

The LTC6909 has a master oscillator frequency range spanning 100kHz to 20MHz depending on the $R_{SET}$ resistor value. However, accuracy may suffer if the oscillator is operated at a master oscillator frequency greater than 10MHz with a supply voltage lower than 4V. With a linear correspondence between the master oscillator period and the $R_{SET}$ resistance, a simple equation relates resistance with frequency.

$$R_{SET} = 10k \cdot \frac{20MHz}{f_{MASTER}}$$

$$R_{SET_{MIN}} = 10k (5V \text{ supply}), 20k (2.7V \text{ supply}),$$

$$R_{SET_{MAX}} = 2M$$

Any $R_{SET}$ resistor tolerance will shift the output frequency by the same amount.

ALTERNATIVE METHODS OF SETTING THE OUTPUT FREQUENCY OF THE LTC6909

The oscillator may be programmed by any method that sources a current into the SET pin. The circuit in Figure 4 sets the oscillator frequency using a programmable current source and in the expression for $f_{OUT}$, the resistor $R_{SET}$ is replaced by the ratio of $1.1V/I_{CONTROL}$. As already explained in the Operation section, the voltage difference between $V^+$ and SET is approximately $1.1V \pm 5\%$, therefore, the Figure 4 circuit is less accurate than if a resistor controls the output frequency.

$$f_{MASTER} = 10k \cdot \frac{20MHz}{1.13V} \cdot I_{CONTROL}$$

Figure 4. Current Controlled Oscillator

Figure 5 shows the LTC6909 configured as a VCO. A voltage source is connected in series with an external 10k resistor. The master oscillator frequency, $f_{MASTER}$, will vary with $V_{CONTROL}$, that is the voltage source connected between $V^+$ and the SET pin. Again, this circuit decouples the relationship between the input current and the voltage between $V^+$ and SET, the frequency accuracy will be degraded. The oscillator frequency, however, will increase monotonically with decreasing $V_{CONTROL}$.

SETTING THE MODULATION RATE OF THE LTC6909

The modulation rate of the LTC6909 is equal to $f_{OUT}/N$, where $N$ is the modulation rate divider setting, which is determined by the state of the MOD pin. The MOD pin should be tied to ground for the $N = 16$ setting. Floating the MOD pin selects $N = 32$. The MOD pin should be tied to $V^+$ for the $N = 64$ setting. To disable the SSFM, connect one of the active outputs to the MOD pin. An AC detector circuit shuts down the modulation circuitry if a frequency that is close to the output frequency is detected at the MOD pin.

When the MOD pin is floated, for the $f_{OUT}$/32 modulation rate, it must be bypassed by at least a 1nF capacitor to GND. Any AC signal coupling to the MOD pin could potentially be detected and stop the frequency modulation.

DRIVING LOGIC CIRCUITS

The outputs of the LTC6909 are suitable for driving general digital logic circuits. However, the form of frequency spreading used in the LTC6909 may not be suitable for many logic designs. Many logic designs have fairly tight timing and cycle-to-cycle jitter requirements. These systems often benefit from a spread spectrum clocking system where the frequency is slowly and linearly modulated by a triangular waveform, not a pseudorandom waveform. This type of frequency spreading maintains a minimal difference in the timing from one clock edge to the next adjacent clock edge (cycle-to-cycle jitter). The LTC6909 uses a pseudorandom modulating signal where the frequency
transitions have been slowed and the corners rounded by a first order lowpass filter with a corner frequency set to the modulation rate (f_{\text{OUT}}/N), where N is the modulation rate divider setting, which is determined by the state of the MOD pin. This filtered modulating signal may be acceptable for many logic systems but the cycle-to-cycle jitter issues must be considered carefully.

**DRIVING SWITCHING REGULATORS**

The LTC6909 is designed primarily to provide an accurate and stable clock for switching regulator systems. The CMOS logic outputs are suitable for directly driving most switching regulators and switching controllers. Linear Technology has a broad line of fully integrated switching regulators and switching regulator controllers designed for synchronization to an external clock. All of these parts have one pin assigned for external clock input. The nomenclature varies depending on the part's family history. SYNC, PLLIN, SYNC/MODE, EXTCLK, FCB and S/S (shorthand for SYNC/SHDN) are examples of clock input pin names used with Linear Technology ICs.

For the best EMC performance, the LTC6909 should be run with the MOD pin tied to ground (SSFM enabled, modulation rate set to f_{\text{OUT}}/16). Regulatory testing is done with strictly specified bandwidths and conditions. Modulating faster than, or as close to, the test bandwidth as possible gives the lowest readings. The optimal modulating rate is not as straightforward when the goal is to lower radiated signal levels interfering with other circuitry in the system. The modulation rate will have to be evaluated with the specific system conditions to determine the optimal rate. Depending on the specific frequency synchronization method a switching regulator employs, the modulation rate must be within the synchronization capability of the regulator. Many regulators use a phase-locked loop (PLL) for synchronization. For these parts, the PLL loop filter should be designed to have sufficient capture range and bandwidth.

The frequency hopping transitions of the LTC6909 are slowed by a lowpass filter. The corner frequency of this filter is set to the modulation rate (f_{\text{OUT}}/N), where N is the modulation rate divider setting, which is determined by the state of the MOD pin. The MOD pin should be tied to ground for the N = 16 setting. Floating the MOD pin selects N = 32. The MOD pin should be tied to V^+ for the N = 64 setting. This is an important feature when driving a switching regulator. The switching regulator is itself a servo loop with a bandwidth typically on the order of 1/10 to 1/20 of the operating frequency. When the clock frequency's transition is within the bandwidth of the switching regulator, the regulator's output stays in regulation. If the transition is too sharp, beyond the bandwidth of the switching regulator, the regulator's output will experience a sharp jump and then settle back into regulation. If the bandwidth of the regulator is sufficiently high, beyond f_{\text{OUT}}/N, then there will not be any regulation issues.

One aspect of the output voltage that will change is the output ripple voltage. Every switching regulator has some output ripple at the clock frequency. For most switching regulator designs with fixed MOSFET's, fixed inductor, fixed capacitors, the amount of ripple will vary with the regulator's operating frequency (the main exception being hysteretic architecture regulators). An increase in frequency results in lower ripple and a frequency decrease gives more ripple. This is true for static frequencies or dynamic frequency modulated systems. If the modulating signal was a triangle wave, the regulator's output would have a ripple that is amplitude modulated by the triangle wave. This repetitive signal on the power supply could cause system problems by mixing with other desired signals creating distortion. Depending on the switching regulator's inductor design and triangle wave frequency, it may even result in an audible noise. The LTC6909 uses a pseudorandom noise-like signal. On an oscilloscope, it looks essentially noise-like of even amplitude. The signal is broadband and any mixing issues are eliminated. Additionally, the pseudorandom signal repeats at such a low rate that it is well below the audible range.

The LTC6909 with the spread spectrum frequency modulation enabled results in improved EMC performance. If the bandwidth of the switching regulator is sufficient, not a difficult requirement in most cases, the regulator's regulation, efficiency and load response are maintained while...
峰电磁辐射（或传导）是减少。输出纹波可能会略有增加，但其行为非常类似于噪声，且其系统影响是无害的。

**SUPPLY BYPASSING, SIGNAL CONNECTIONS AND PCB LAYOUT**

使用LTC6909在扩展频谱模式下自然地消除了任何对输出频率精度和稳定性的担忧，因为它会不断跳跃到新的设置。在固定频率应用中，一些对V+供电电压纹波的关注是必要的，以最小化额外的输出频率误差。在固定频率的LTC6909输出时钟用于同步提供V+供电的相同开关调节器的应用中，如果纹波超过30mVP-P，则可能会在时钟中出现显著的抖动，因为从C1到GND的连接是直接在顶层完成的。

LTC6909的精度受上述所述的电源纹波影响。V+D引脚在电源电压中是不敏感的，V+A引脚提供模拟部分的电源，并且电流主要依赖于输出电容的加载和电源电压。

图6展示了如何连接V+A和V+D电源引脚到电源以及建议的PCB布局。PCB布局假设双层板在板下有一层地平面，并且有0805尺寸的无源组件。PCB布局在图6中是一个指南，但不一定要完全遵循。然而，有以下几项需要注意的项。

1. 应当在板下和板周围设置一个地平面。将GND引脚连接到此平面通过多个（至少三个）焊盘来尽量减少电感。
2. 将电容器C1和C2尽可能地靠近V+A和V+D引脚，以减少电容器引脚和部分引脚之间的电感。
3. V+A和V+D引脚到主要供电的连接应通过低阻抗路径。如果板有一个V+电源平面，则使用它而不是图6中所示的顶层连接。在每个点连接V+A和V+D引脚到V+平面以尽量减少电感。
4. 将电容器C1和C2直接连接到GND引脚，使用低电感路径。从C1到GND的连接很容易直接在顶层完成。C2路径更为困难，但可以通过多个焊盘来完成。
5. 将RSET电阻直接连接到SET引脚和V+A引脚。将电阻通过任何方式连接到V+供应，而不是直接到V+A引脚，将导致更大的频率误差。
6. 在使用LTC6909时禁用扩展频谱，一个主动输出连接到MOD引脚。最好是通过将OUT1信号在板下绕过部分来完成此操作。需要在MOD引脚之间和RSET电阻之间创建一个地屏蔽以尽量减少OUT1信号的耦合。
9. The connections for PH0, PH1 and PH2 are not shown in Figure 6. These pins are connected to either GND or V+D depending on the output phasing required for the application. Connection to ground is done underneath the part. Connecting PH2 to V+D is also straightforward. Connecting PH0 or PH1 to V+D may require one or both traces to go down a layer. If you are dynamically changing one or all of the PH pins, place a 10k resistor in series with the signal line. Locate the resistor fairly close to the PH pin. This signal typically comes from a microcontroller or the power good signal from a switching regulator and is usually quite noisy. The series resistor provides some isolation between the noisy signal and the LTC6909.

**START-UP ISSUES AND CONSIDERATIONS**

The start-up time and settling time to within 1\% of the final value is estimated by the following equation:

$$t_{START} \approx RSET \times \left( \frac{25 \mu s}{1k} \right) + 10 \mu s$$

For instance, with $R_{SET} = 100k$, the LTC6909 will settle to within 1\% of its 1MHz final value in approximately 260\µs. Figure 7 shows the start-up time for various $R_{SET}$ resistors.

To assist in an orderly start-up sequence, the LTC6909’s outputs are in a high impedance state for the first 128 master clock cycles after power-up. This ensures that the first clock cycle is very close to the desired operating frequency.

Powering up and down complex multiphase switching regulator circuits is always chaotic and can have serious system consequences if it is not done carefully. In addition to the LTC6909’s muting of the outputs to ensure first cycle accuracy, the PH0-PH1-PH2 codes 000 (all outputs are

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**Figure 6. Supply Bypassing and PCB Layout**

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**Figure 7. Start-Up Time**
high impedance) and 001 (all outputs are low) are useful for controlling the clocking of switching regulators during start-up. At start-up, most switching regulators ignore the clock input until a power good state is achieved. Nearly all of Linear Technology's switching regulators operate in this manner. However, some switching regulators from other vendors do not ignore the clock input on start-up and yet are not synchronizable until the power good state is reached. Attempting to synchronize these switching regulators before they reach the power good state can lead to problems. For these switching regulators it is best to have the LTC6909 held in the PH0-PH1-PH2 codes 000 or 001 until the switching regulator issues a power good signal. In most cases, simply connecting a switching regulator's power good signal to the PH0, PH1 and/or PH2 pins accomplishes this. At most, an additional single logic inverter is required to switch from either the 000 or 001 states to any of the other six states through a power good signal.

Another way to use the PH0, PH1 and PH2 inputs to assist with power-up/down issues is to use an external part to provide a supply monitor or an undervoltage lockout (UVLO). There are several parts available that combine a comparator with a reference to fulfill this function. The LTC6909 does not have its own internal UVLO. If the supply is below 2.7V, frequency accuracy may suffer. At a supply voltage around 2V or lower, the LTC6909 will operate erratically or will stop. It may stop randomly in a logic high or low state.

Figure 8 shows a circuit using an LTC1998 to monitor the supply voltage and control the logic state of the PH0 and PH1 pins. The LTC1998's threshold is set at 2.5V with 50mV of hysteresis. On power-up, as the supply ramps up, the LTC1998 holds PH0 and PH1 low, keeping the LTC6909's outputs in a high impedance state. Once the supply is above 2.55V, the LTC1998 pulls the PH0 and PH1 pins high, setting the LTC6909 into the 4-phase operating mode. On power-down, the supply ramps down and the LTC1998's output goes low once the supply is below 2.45V. This puts the LTC6909's outputs in the high impedance state. All switch overs are synchronized to the LTC6909's internal oscillator to avoid glitches and runt pulses.

To adjust the on/off supply voltage threshold, change the configuration of the LTC1998. As with the power good signal, at most an additional single logic inverter is required to switch from either the 000 or 001 states to any of the other six states.

Figure 8. Adding a UVLO Feature to the LTC6909. In This Example, the LTC6909 Is in 4-Phase Mode for a $V^+ > \approx 2.5V$ (PHx = 011) and the Outputs Are All High Impedance for $V^+ < \approx 2.5V$ (PHx = 000)
Simply Parallel Multiple DC/DC µModule® Regulator Systems to Achieve Higher Output Current. Board Layout Is as Easy as Copying and Pasting Each µModule Regulator’s Layout With Very Few External Components Required.
TYPICAL APPLICATIONS

Using Additional Standard Logic Inverters to Achieve 10- and 14-Phase Outputs
(Inverters Are 74HC04 or Equivalent)

10 OUTPUT PHASES (OUTPUTS SHIFTED BY 36 DEGREES)

14 OUTPUT PHASES (OUTPUTS SHIFTED BY 25.71 DEGREES)

0° (360°)
180°
72°
252°
144°
324°
216°
36°
288°
108°
51.43°
231.43°
102.86°
282.86°
154.29°
334.29°
205.71°
25.71°
257.14°
77.14°
308.57°
128.57°
TYPICAL APPLICATIONS

Combining Eight Outputs With a Lowpass Filter to Create a Sine Wave

[Diagram of the LTC6909 with eight outputs and a lowpass filter, showing connections and values such as 2.7V to 5.5V, 0.1µF, 100kHz SINE WAVE OUTPUT, V+ = 5V, THD = 0.2%, and 500mV/DIV, 2µs/DIV.]
**PACKAGE DESCRIPTION**

**MS Package**
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)

**Gauge Plane**

**DETAIL “A”**

**SEATING PLANE**

**NOTE:**
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
# Revision History

<table>
<thead>
<tr>
<th>REV</th>
<th>DATE</th>
<th>DESCRIPTION</th>
<th>PAGE NUMBER</th>
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<tr>
<td>A</td>
<td>1/11</td>
<td>Revised typical value for $\Delta f_{\text{MASTER}}, ; 10\text{MHz} \leq f_{\text{MASTER}} \leq 20\text{MHz}$ to ±2.7. Revised Typical Applications drawings for 10 and 14 output phases.</td>
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Providing an 8-Phase Synchronizing Clock to LTM Modules

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<tr>
<th>PART NUMBER</th>
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<th>COMMENTS</th>
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<tbody>
<tr>
<td>LTC1799</td>
<td>1kHz to 33MHz ThinSOT™ Oscillator, Resistor Set</td>
<td>Wide Frequency Range</td>
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<td>LTC6900</td>
<td>1kHz to 20MHz ThinSOT Oscillator, Resistor Set</td>
<td>Low Power, Wide Frequency Range</td>
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<td>LTC6902</td>
<td>Multiphase Oscillator with Spread Spectrum Modulation</td>
<td>2-, 3- or 4-Phase Outputs</td>
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<td>LTC6903/LTC6904</td>
<td>1kHz to 68MHz Serial Port Programmable Oscillator</td>
<td>0.1% Frequency Resolution, I2C or SPI Interface</td>
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<td>LTC6905</td>
<td>17MHz to 170MHz ThinSOT Oscillator, Resistor Set</td>
<td>High Frequency, 100µs Start-Up, 7ps RMS Jitter</td>
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<td>LTC6905-XXX</td>
<td>Fixed Frequency ThinSOT Oscillators, Up to 133MHz</td>
<td>No Trim Components Required</td>
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<td>Micropower ThinSOT Oscillator, Resistor Set</td>
<td>10kHz to 1MHz, 12mA at 100kHz</td>
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<td>LTC6907</td>
<td>Micropower ThinSOT Oscillator, Resistor Set</td>
<td>40kHz to 4MHz, 36µA at 400kHz</td>
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<tr>
<td>LTC6908-1</td>
<td>50kHz to 10MHz Dual Output ThinSOT Oscillator, Resistor Set</td>
<td>Complementary Outputs (0°/180°)</td>
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<tr>
<td>LTC6908-2</td>
<td>50kHz to 10MHz Dual Output ThinSOT Oscillator, Resistor Set</td>
<td>Quadrature Outputs (0°/90°)</td>
</tr>
<tr>
<td>LTC6930-XXX</td>
<td>Fixed Frequency Oscillator, 32.768kHz to 8.192MHz</td>
<td>0.09% Accuracy, 110µs Startup Time, 105µA at 32kHz</td>
</tr>
</tbody>
</table>