LTC6268/LTC6269 500MHz Ultra-Low Bias Current FET Input Op Amp

FEATURES
- Gain Bandwidth Product: 500MHz
- Low Input Bias Current:
  ±3fA Typ. Room Temperature
  4pA Max at 125°C
- Current Noise (100kHz): 5.5fA/√Hz
- Voltage Noise (1MHz): 4.3nV/√Hz
- Extremely Low CIN 450fF
- Rail-to-Rail Output
- Slew Rate: 400V/µs
- Supply Range: 3.1V to 5.25V
- Quiescent Current: 16.5mA
- Harmonic Distortion (2VP-P):
  –100dB at 1MHz
  –80dB at 10MHz
- Operating Temp Range: –40°C to 125°C
- Single in 8-Lead SO-8, 6-Lead TSOT-23 Packages
- Dual in 8-Lead MS8, 3mm × 3mm 10-Lead DFN 10 Packages

APPLICATIONS
- Trans-Impedance Amplifiers
- ADC Drivers
- CCD Output Buffer
- Photomultiplier Tube Post-Amplifier
- Low IBIAS Circuits

DESCRIPTION
The LTC6268/LTC6269 is a single/dual 500MHz FET-input operational amplifier with extremely low input bias current and low input capacitance. It also features low input-referred current noise and voltage noise making it an ideal choice for high speed transimpedance amplifiers, CCD output buffers, and high-impedance sensor amplifiers. Its low distortion makes the LTC6268/LTC6269 an ideal amplifier for driving SAR ADCs.

It operates on 3.1V to 5.25V supply and consumes 16.5mA per amplifier. A shutdown feature can be used to lower power consumption when the amplifier is not in use.

The LTC6268 single op amp is available in 8-lead SOIC and 6-lead SOT-23 packages. The SOIC package includes two unconnected pins which can be used to create an input pin guard ring to protect against board leakage currents. The LTC6269 dual op amp is available in 8-lead MSOP with exposed pad and 3mm × 3mm 10-lead DFN packages. They are fully specified over the –40°C to 85°C and the –40°C to 125°C temperature ranges.

LTC, LT, LTC, LT®M, Linear Technology and the Linear logo are registered trademarks of Linear Technology Corporation. All other trademarks are the property of their respective owners.

TYPICAL APPLICATION
20kΩ Gain 65MHz Trans-Impedance Amplifier

20kΩ TIA Frequency Response

For more information www.linear.com/LTC6268
ABSOLUTE MAXIMUM RATINGS

(Note 1)
Supply Voltage $V^+$ to $V^-$ ........................................... 5.5V
Input Voltage ........................................... $V^– - 0.2V$ to $V^+ + 0.2V$
Input Current ($+IN$, $-IN$)(Note 2) ........................................... ±1mA
Input Current (SHDN) ........................................... ±1mA
Output Current ($I_{OUT}$) (Note 8, 9) ......................... 135mA
Output Short-Circuit Duration (Note 3) ... Thermally Limited
Operating Temperature Range
LTC6268I/LTC6269I ........................................... –40°C to 85°C
LTC6268H/LTC6269H ........................................... –40°C to 125°C

Specified Temperature Range (Note 4)
LTC6268I/LTC6269I ........................................... –40°C to 85°C
LTC6268H/LTC6269H ........................................... –40°C to 125°C

Maximum Junction Temperature ................................ 150°C
Storage Temperature Range ................................ –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ......................... 300°C

PIN CONFIGURATION

TOP VIEW
NC 1 8 SHDN
$-IN$ 2 7 $V^+$
$+IN$ 3 6 OUT
NC 4 5 $V^–$

S8 PACKAGE
8-LEAD PLASTIC SO
$T_{JMAX} = 150°C, \theta_{JA} = 120°C/W$ (NOTE 5)

TOP VIEW
OUT 1 6 $V^+$
$V^–$ 2 5 SHDN
$+IN$ 3 4 $-IN$

S6 PACKAGE
6-LEAD PLASTIC TSOT-23
$T_{JMAX} = 150°C, \theta_{JA} = 192°C/W$ (NOTE 5)

TOP VIEW
OUTA 1 8 $V^+$
$-INA$ 2 9 7 OUTB
$+INA$ 3 6 $-INB$
$V^–$ 4 5 $+INB$

MS8 PACKAGE
8-LEAD PLASTIC MSOP
$T_{JMAX} = 150°C, \theta_{JA} = 40°C/W$ (NOTE 5)
EXPOSED PAD (PIN 9) IS $V^–$, IT IS RECOMMENDED TO SOLDER TO PCB

TOP VIEW
OUTA 10 $V^+$
$-INA$ 9 11 OUTB
$+INA$ 8 3 $-INB$
$V^–$ 7 2 $+INB$
SDA 6 1 SDB

DD PACKAGE
10-LEAD (3mm $\times$ 3mm) PLASTIC DFN
$T_{JMAX} = 150°C, \theta_{JA} = 43°C/W$ (NOTE 5)
EXPOSED PAD (PIN 11) IS $V^+$, IT IS RECOMMENDED TO SOLDER TO PCB
### ORDER INFORMATION

<table>
<thead>
<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>SPECIFIED TEMPERATURE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC6268IS6#TRMPBF</td>
<td>LTC6268IS6#TRPBF</td>
<td>LTGFS</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6268HS6#TRMPBF</td>
<td>LTC6268HS6#TRPBF</td>
<td>LTGFS</td>
<td>6-Lead Plastic TSOT-23</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC6268IS8#PBF</td>
<td>LTC6268IS8#TRPBF</td>
<td>6268</td>
<td>8-Lead Plastic SOIC</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6268HS8#PBF</td>
<td>LTC6268HS8#TRPBF</td>
<td>6268</td>
<td>8-Lead Plastic SOIC</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC6269IMS8E#PBF</td>
<td>LTC6269IMS8E#TRPBF</td>
<td>LTGFP</td>
<td>8-Lead Plastic MSOP</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6269HMS8E#PBF</td>
<td>LTC6269HMS8E#TRPBF</td>
<td>LTGFP</td>
<td>8-Lead Plastic MSOP</td>
<td>–40°C to 125°C</td>
</tr>
<tr>
<td>LTC6269IDD#PBF</td>
<td>LTC6269IDD#TRPBF</td>
<td>LGFN</td>
<td>10-Lead Plastic DD</td>
<td>–40°C to 85°C</td>
</tr>
<tr>
<td>LTC6269HDD#PBF</td>
<td>LTC6269HDD#TRPBF</td>
<td>LGFN</td>
<td>10-Lead Plastic DD</td>
<td>–40°C to 125°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)
For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)

### 5.0V ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$, $V_{SUPPLY} = 5.0V$ ($V^+ = 5V$, $V^- = 0V$, $V_{CM} = mid-supply$), $R_L = 1kΩ$, $C_L = 10pF$, $V_{SHDN}$ is unconnected.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DS}$</td>
<td>Input Offset Voltage $V_{CM} = 2.75V$</td>
<td>●</td>
<td>–0.7</td>
<td>0.2</td>
<td>0.7</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>$V_{CM} = 4.0V$</td>
<td>●</td>
<td>–1.0</td>
<td>0.2</td>
<td>1.0</td>
<td>mV</td>
</tr>
<tr>
<td>$TC_{VDS}$</td>
<td>Input Offset Voltage Drift $V_{CM} = 2.75V$</td>
<td>4</td>
<td>μV/°C</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_B$</td>
<td>Input Bias Current (Notes 6, 8) $V_{CM} = 2.75V$</td>
<td>●</td>
<td>–900</td>
<td>±3</td>
<td>20</td>
<td>fA</td>
</tr>
<tr>
<td></td>
<td>$V_{CM} = 4.0V$</td>
<td>●</td>
<td>–900</td>
<td>±4</td>
<td>20</td>
<td>fA</td>
</tr>
<tr>
<td>$I_{OS}$</td>
<td>Input Offset Current (Notes 6, 8) $V_{CM} = 2.75V$</td>
<td>●</td>
<td>–450</td>
<td>±4</td>
<td>20</td>
<td>fA</td>
</tr>
<tr>
<td></td>
<td>$V_{CM} = 4.0V$</td>
<td>●</td>
<td>–450</td>
<td>±4</td>
<td>20</td>
<td>fA</td>
</tr>
<tr>
<td>$e_n$</td>
<td>Input Voltage Noise Density, $V_{CM} = 2.75V$ $f = 1MHz$</td>
<td>4.3</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Voltage Noise Density, $V_{CM} = 4.0V$ $f = 1MHz$</td>
<td>4.9</td>
<td>nV/√Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$i_n$</td>
<td>Input Referred Noise Voltage $f = 0.1Hz to 10Hz$</td>
<td>13</td>
<td>μVp-p</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Current Noise Density, $V_{CM} = 2.75V$ $f = 100kHz$</td>
<td>5.5</td>
<td>fA/√Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Input Current Noise Density, $V_{CM} = 4.0V$ $f = 100kHz$</td>
<td>5.3</td>
<td>fA/√Hz</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{IN}$</td>
<td>Input Resistance</td>
<td>Differential</td>
<td>&gt;1000</td>
<td>kΩ</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Common Mode</td>
<td>&gt;1000</td>
<td>kΩ</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{IN}$</td>
<td>Input Capacitance</td>
<td>Differential (DC to 200MHz)</td>
<td>100</td>
<td>fF</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Common Mode (DC to 100MHz)</td>
<td>450</td>
<td>fF</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$CMRR$</td>
<td>Common Mode Rejection Ratio $V_{CM} = 0.5V$ to 3.2V (PNP Side)</td>
<td>●</td>
<td>72</td>
<td>64</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$V_{CM} = 0$ to 4.5V</td>
<td>●</td>
<td>70</td>
<td>52</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>$IVR$</td>
<td>Input Voltage Range</td>
<td>Guaranteed by CMRR</td>
<td>0</td>
<td>4.5</td>
<td>V</td>
<td></td>
</tr>
</tbody>
</table>
### 5.0V Electrical Characteristics

The * denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ$C, $V_{\text{SUPPLY}} = 5.0V$ ($V^+ = 5V$, $V^- = 0V$, $V_{\text{CM}}$ = mid-supply), $R_L = 1k\Omega$, $C_L = 10pF$, $V_{\text{SHDN}}$ is unconnected.

![Image](image.png)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>$V_{\text{CM}} = 1.0V$, $V_{\text{SUPPLY}}$ Ranges from 3.1V to 5.25V</td>
<td>78 75</td>
<td>95 95</td>
<td>dB  dB</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.1</td>
<td>5.25</td>
<td>dB  dB</td>
<td></td>
</tr>
<tr>
<td>$A_V$</td>
<td>Open Loop Voltage Gain</td>
<td>$V_{\text{OUT}} = 0.5V$ to 4.5V, $R_{\text{LOAD}} = 10k$</td>
<td>125 40</td>
<td>250 250</td>
<td>V/mV  V/mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_{\text{LOAD}} = 100$</td>
<td>10 10</td>
<td>21 21</td>
<td>V/mV  V/mV</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OL}}$</td>
<td>Output Swing Low (Input Overdrive 30mV) Measured from $V^-$</td>
<td>$I_{\text{SINK}} = 10mA$</td>
<td>80 80</td>
<td>140 140</td>
<td>mV  mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{\text{SINK}} = 25mA$</td>
<td>130 130</td>
<td>200 200</td>
<td>mV  mV</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{OH}}$</td>
<td>Output Swing High (Input Overdrive 30mV) Measured from $V^+$</td>
<td>$I_{\text{SOURCE}} = 10mA$</td>
<td>70 70</td>
<td>140 140</td>
<td>mV  mV</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$I_{\text{SOURCE}} = 25mA$</td>
<td>160 160</td>
<td>270 270</td>
<td>mV  mV</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{SC}}$</td>
<td>Output Short Circuit Current</td>
<td>(Note 9)</td>
<td>60 60</td>
<td>90 90</td>
<td>mA  mA</td>
<td></td>
</tr>
<tr>
<td>$I_S$</td>
<td>Supply Current Per Amplifier</td>
<td></td>
<td>15 15</td>
<td>16.5 16.5</td>
<td>mA  mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>9 9</td>
<td>18 18</td>
<td>mA  mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Supply Current in Shutdown (Per Amplifier)</td>
<td></td>
<td>0.39 0.39</td>
<td>0.85 0.85</td>
<td>mA  mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>1.2 1.2</td>
<td>mA  mA</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{SHDN}}$</td>
<td>Shutdown Pin Current</td>
<td>$V_{\text{SHDN}} = 0.75V$</td>
<td>$-12 -12$</td>
<td>2 2</td>
<td>µA  µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{SHDN}} = 1.50V$</td>
<td>$-12 -12$</td>
<td>2 2</td>
<td>µA  µA</td>
<td></td>
</tr>
<tr>
<td>$V_{\text{IL}}$</td>
<td>SHDN Input Low Voltage</td>
<td>Disable</td>
<td></td>
<td></td>
<td>0.75 0.75</td>
<td>V  V</td>
</tr>
<tr>
<td>$V_{\text{IH}}$</td>
<td>SHDN Input High Voltage</td>
<td>Enable. If SHDN is Unconnected, Amp is Enabled</td>
<td></td>
<td>1.5 1.5</td>
<td>V  V</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{ON}}$</td>
<td>Turn On Time, Delay from SHDN Toggle to Output Reaching 90% of Target</td>
<td>$V_{\text{SHDN}}$ Toggle from 0V to 2V, $A_V = 1$</td>
<td></td>
<td>580 580</td>
<td>ns  ns</td>
<td></td>
</tr>
<tr>
<td>$t_{\text{OFF}}$</td>
<td>Turn Off Time, Delay from SHDN Toggle to Output High Z</td>
<td>$V_{\text{SHDN}}$ Toggle from 2V to 0V, $A_V = 1$</td>
<td></td>
<td>480 480</td>
<td>ns  ns</td>
<td></td>
</tr>
<tr>
<td>BW</td>
<td>–3dB Closed Loop Bandwidth</td>
<td>$A_V = 1$</td>
<td></td>
<td>350 350</td>
<td>MHz  MHz</td>
<td></td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td>$f = 10MHz$</td>
<td></td>
<td>400 400</td>
<td>MHz  MHz</td>
<td></td>
</tr>
<tr>
<td>$t_S$</td>
<td>Settling Time, 1V to 4V, Unity Gain</td>
<td></td>
<td></td>
<td>17 17</td>
<td>ns  ns</td>
<td></td>
</tr>
<tr>
<td>SR+</td>
<td>Slew Rate+</td>
<td>$A_V = 6 (R_C = 499, R_G = 100)$, $V_{\text{OUT}} = 0.5V$ to 4.5V, Measured 20% to 80%, $C_{\text{LOAD}} = 10pF$</td>
<td>300 300</td>
<td>400 400</td>
<td>V/µs  V/µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{OUT}} = 4.5V$ to 0.5V, Measured 80% to 20%, $C_{\text{LOAD}} = 10pF$</td>
<td>200 200</td>
<td>200 200</td>
<td>V/µs  V/µs</td>
<td></td>
</tr>
<tr>
<td>SR−</td>
<td>Slew Rate−</td>
<td>$A_V = 6 (R_C = 499, R_G = 100)$, $V_{\text{OUT}} = 0.5V$ to 4.5V, Measured 20% to 80%, $C_{\text{LOAD}} = 10pF$</td>
<td>180 180</td>
<td>260 260</td>
<td>V/µs  V/µs</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{OUT}} = 4.5V$ to 0.5V, Measured 80% to 20%, $C_{\text{LOAD}} = 10pF$</td>
<td>130 130</td>
<td>130 130</td>
<td>V/µs  V/µs</td>
<td></td>
</tr>
<tr>
<td>FPBW</td>
<td>Full Power Bandwidth (Note 7)</td>
<td>$4V_{\text{P-P}}$</td>
<td>21</td>
<td>21</td>
<td>MHz  MHz</td>
<td></td>
</tr>
<tr>
<td>HD</td>
<td>Harmonic Distortion(HD2/HD3)</td>
<td>$A_i = 1$, 10MHz, $2V_{\text{P-P}}$, $V_{\text{CM}} = 1.75V$, $R_L = 1k$</td>
<td></td>
<td>$-81/-90$</td>
<td>dB  dB</td>
<td></td>
</tr>
<tr>
<td>THD+N</td>
<td>Total Harmonic Distortion and Noise</td>
<td>$A_i = 1$, 10MHz, $2V_{\text{P-P}}$, $V_{\text{CM}} = 1.75V$, $R_L = 1k$</td>
<td>0.01</td>
<td>$-79.6$</td>
<td>%  dB</td>
<td></td>
</tr>
<tr>
<td>$I_{\text{LEAK}}$</td>
<td>Output Leakage Current in Shutdown</td>
<td>$V_{\text{SHDN}} = 0V$, $V_{\text{OUT}} = 0V$</td>
<td></td>
<td>400 400</td>
<td>nA  nA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{\text{SHDN}} = 0V$, $V_{\text{OUT}} = 5V$</td>
<td>400 400</td>
<td>400 400</td>
<td>nA  nA</td>
<td></td>
</tr>
</tbody>
</table>
### 3.3V ELECTRICAL CHARACTERISTICS

The • denotes specifications that apply over the full operating temperature range, otherwise specifications are at \( T_A = 25°C \), \( V_{\text{SUPPLY}} = 3.3V \) (\( V^+ = 3.3V \), \( V^- = 0V \), \( V_{\text{CM}} = \text{mid-supply} \), \( R_L = 1k\Omega \), \( C_L = 10pF \), \( V_{\text{SHDN}} \text{ is unconnected} \).

#### SYMBOL PARAMETER | CONDITIONS | MIN | TYP | MAX | UNITS
---|---|---|---|---|---
\( V_{\text{OS}} \) | Input Offset Voltage \( V_{\text{CM}} = 1.0V \) | • | –0.7 | 0.2 | 0.7 | mV
 | \( V_{\text{CM}} = 2.3V \) | • | –2.5 | 2.5 | mV
\( TCV_{\text{OS}} \) | Input Offset Voltage Drift \( V_{\text{CM}} = 1.0V \) | | 4 | | \( \mu V/C \)
\( I_B \) | Input Bias Current (Notes 6, 8) \( V_{\text{CM}} = 1.0V \) \( \text{LTC6268I/LTC6269I} \) | • | –20 | ±3 | 20 | fA
 | \( \text{LTC6268H/LTC6269H} \) | • | –900 | 900 | fA
 | \( V_{\text{CM}} = 2.3V \) \( \text{LTC6268I/LTC6269I} \) | • | –20 | ±3 | 20 | fA
 | \( \text{LTC6268H/LTC6269H} \) | • | –900 | 900 | fA
\( I_{\text{OS}} \) | Input Offset Current (Notes 6, 8) \( V_{\text{CM}} = 1.0V \) \( \text{LTC6268I/LTC6269I} \) | • | –40 | ±6 | 40 | fA
 | \( \text{LTC6268H/LTC6269H} \) | • | –450 | 450 | fA
 | \( V_{\text{CM}} = 2.3V \) \( \text{LTC6268I/LTC6269I} \) | • | –2 | | 2 | pA
\( \varepsilon_n \) | Input Voltage Noise Density, \( V_{\text{CM}} = 1.0V \) \( f = 1\text{MHz} \) | | 4.3 | | nV/\sqrt{Hz}
 | Input Voltage Noise Density, \( V_{\text{CM}} = 2.3V \) \( f = 1\text{MHz} \) | | 4.9 | | nV/\sqrt{Hz}
\( \varepsilon_n \) | Input Referred Noise Voltage \( f = 0.1\text{Hz to 10Hz} \) | | 13 | | \( \mu V_{P-P} \)
\( I_n \) | Input Current Noise Density, \( V_{\text{CM}} = 1.0V \) \( f = 100\text{kHz} \) | | 5.6 | | fA/\sqrt{Hz}
 | Input Current Noise Density, \( V_{\text{CM}} = 2.3V \) \( f = 100\text{kHz} \) | | 5.3 | | fA/\sqrt{Hz}
\( R_{\text{IN}} \) | Input Resistance Differential \( V_{\text{CM}} = 0.5V \text{ to } 1.2V \) (PNP Side) | | 63 | 60 | 100 | dB
 | Common Mode \( V_{\text{CM}} = 0V \text{ to } 2.8V \) (Full Range) | | 60 | 50 | 77 | dB
\( C_{\text{IN}} \) | Input Capacitance Differential (DC to 200MHz) | | 100 | | fF
 | Common Mode (DC to 100MHz) | | 450 | | fF
\( \text{CMRR} \) | Common Mode Rejection Ratio \( V_{\text{CM}} = 0.5V \text{ to } 1.2V \) (PNP Side) | • | 63 | 60 | 100 | dB
 | \( V_{\text{CM}} = 0V \text{ to } 2.8V \) (Full Range) | • | 60 | 50 | 77 | dB
\( \text{IVR} \) | Input Voltage Range Guaranteed by \text{CMRR} | • | 0 | 2.8 | V
\( A_V \) | Open Loop Voltage Gain \( V_{\text{OUT}} = 0.5V \text{ to } 2.8V \) \( R_{\text{LOAD}} = 10k \) | • | 80 | 40 | 200 | V/mV
 | \( R_{\text{LOAD}} = 100 \) | • | 10 | 2 | 18 | V/mV
\( V_{\text{DL}} \) | Output Swing Low \( \text{Input Overdrive 30mV). Measured from } V^- \) \( I_{\text{SINK}} = 10mA \) | • | 80 | 140 | 200 | mV
 | \( I_{\text{SINK}} = 25mA \) | • | 140 | 200 | 260 | mV
\( V_{\text{DH}} \) | Output Swing High \( \text{Input Overdrive 30mV). Measured from } V^+ \) \( I_{\text{SOURCE}} = 10mA \) | • | 80 | 140 | 200 | mV
 | \( I_{\text{SOURCE}} = 25mA \) | • | 170 | 270 | 370 | mV
\( I_{\text{SC}} \) | Output Short Circuit Current \( \text{(Note 9)} \) | • | 50 | 80 | 35 | mA
\( I_S \) | Supply Current per Amplifier | • | 14.5 | 16 | 17.5 | 9 | mA

For more information visit [www.linear.com/LTC6268](http://www.linear.com/LTC6268)
### 3.3V Electrical Characteristics

The * denotes specifications that apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ C$, $V_{\text{supply}} = 3.3V$ ($V^+ = 3.3V$, $V^- = 0V$, $V_{\text{CM}} = \text{mid-supply}$) $R_L = 1k\Omega$, $C_L = 10\, \text{pF}$, $V_{\text{SHDN}}$ is unconnected.

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$I_{\text{SHDN}}$</td>
<td>Shutdown Pin Current</td>
<td>$V_{\text{SHDN}} = 0.75V$ $V_{\text{SHDN}} = 1.5V$</td>
<td>–12</td>
<td>2</td>
<td>12</td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$V_{\text{IL}}$</td>
<td>SHDN Input Low Voltage</td>
<td>Disable</td>
<td></td>
<td></td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>$V_{\text{IH}}$</td>
<td>SHDN Input High Voltage</td>
<td>Enable. If SHDN is Unconnected, Amp Is Enabled</td>
<td>1.5</td>
<td></td>
<td></td>
<td>$V$</td>
</tr>
<tr>
<td>$t_{\text{ON}}$</td>
<td>Turn On Time, Delay from SHDN Toggle to Output Reaching 90% of Target</td>
<td>SHDN Toggle from 0V to 2V</td>
<td>710</td>
<td></td>
<td></td>
<td>$\text{ns}$</td>
</tr>
<tr>
<td>$t_{\text{OFF}}$</td>
<td>Turn Off Time, Delay from SHDN Toggle to Output High Z</td>
<td>SHDN Toggle from 2V to 0V</td>
<td>620</td>
<td></td>
<td></td>
<td>$\text{ns}$</td>
</tr>
<tr>
<td>BW</td>
<td>–3dB Closed Loop Bandwidth</td>
<td>$A_V = 1$</td>
<td>350</td>
<td></td>
<td></td>
<td>$\text{MHz}$</td>
</tr>
<tr>
<td>GBW</td>
<td>Gain-Bandwidth Product</td>
<td>$f = 10, \text{MHz}$</td>
<td>370</td>
<td>420</td>
<td></td>
<td>$\text{MHz}$</td>
</tr>
<tr>
<td>$SR^+$</td>
<td>Slew Rate+</td>
<td>$A_V = 6 , (R_F = 499, \quad R_G = 100)$, $V_{\text{OUT}} = 0.5V , \text{to} , 2.8V , \text{Measured} , 20% , \text{to} , 80%$, $C_{\text{LOAD}} = 10, \text{pF}$</td>
<td>300</td>
<td>400</td>
<td></td>
<td>$\text{V}/\mu \text{s}$</td>
</tr>
<tr>
<td>$SR^-$</td>
<td>Slew Rate–</td>
<td>$A_V = 6 , (R_F = 499, \quad R_G = 100)$, $V_{\text{OUT}} = 2.8V , \text{to} , 0.5V , \text{Measured} , 80% , \text{to} , 20%$, $C_{\text{LOAD}} = 10, \text{pF}$</td>
<td>180</td>
<td>260</td>
<td></td>
<td>$\text{V}/\mu \text{s}$</td>
</tr>
<tr>
<td>FPBW</td>
<td>Full Power Bandwidth (Note 7)</td>
<td>$2V_{\text{P-P}}$</td>
<td>40</td>
<td></td>
<td></td>
<td>$\text{MHz}$</td>
</tr>
<tr>
<td>HD</td>
<td>Harmonic Distortion(HD2/HD3)</td>
<td>$A = 1, \quad 10, \text{MHz}\quad 1, \text{V}<em>{\text{p-p}}, \quad V</em>{\text{CM}} = 1.65V, \quad R_L = 1k$</td>
<td>–81/–90</td>
<td></td>
<td></td>
<td>$\text{dB}$</td>
</tr>
<tr>
<td>THD+N</td>
<td>Total Harmonic Distortion and Noise</td>
<td>$A = 1, \quad 10, \text{MHz}\quad 1, \text{V}<em>{\text{p-p}}, \quad V</em>{\text{CM}} = 1.65V, \quad R_L = 1k$</td>
<td>0.01</td>
<td></td>
<td></td>
<td>$%$</td>
</tr>
</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The inputs are protected by two series connected ESD protection diodes to each power supply. The input current should be limited to less than 1mA. The input voltage should not exceed 200mV beyond the power supply.

**Note 3:** A heat sink may be required to keep the junction temperature below the absolute maximum rating when the output is shorted indefinitely.

**Note 4:** The LTC6268/LTC6269 is guaranteed to meet specified performance from –40°C to 85°C. The LTC6268H/LTC6269H is guaranteed to meet specified performance from –40°C to 125°C.

**Note 5:** Thermal resistance varies with the amount of PC board metal connected to the package. The specified values are for short traces connected to the leads.

**Note 6:** The input bias current is the average of the currents into the positive and negative input pins. Typical measurement is for S8 package.

**Note 7:** Full Power Bandwidth is calculated from slew rate using the following equation: $\text{FPBW} = \frac{\text{SR}}{(2\pi \times V_{\text{PEAK}})}$

**Note 8:** This parameter is specified by design and/or characterization and is not tested in production.

**Note 9:** The LTC6268/LTC6269 is capable of producing peak output currents in excess of 135mA. Current density limitations within the IC require the continuous current supplied by the output (sourcing or sinking) over the operating lifetime of the part be limited to under 135mA (Absolute Maximum).
TYPICAL PERFORMANCE CHARACTERISTICS  \(T_A = 25^\circ C\), unless otherwise noted.

- **Input Offset Voltage Distribution**
  - \(V_S = \pm 2.5V\)
  - \(V_{CM} = 0.25V\)

- **Input Offset Drift Distribution**
  - \(V_S = \pm 2.5V\)
  - \(V_{CM} = 0.25V\)
  - \(V_{CM} = 1.5V\)

- **Input Offset Voltage vs Common Mode Voltage**
  - \(V_S = \pm 2.5V\)

- **Input Offset Voltage vs Supply Voltage**
  - \(V_S = 0V, V_S^+ = 3.1V\) to 5.25V
  - \(V_{CM} = 1V\)

- **Input Offset Voltage vs Output Current**
  - \(V_S = \pm 2.5V\)
  - \(V_{CM} = 1.5V\)
  - \(V_{CM} = 0.25V\)

- **PSRR vs Frequency**
  - \(V_S = \pm 2.5V\)
  - \(V_{CM} = 0.25V\)

- **CMRR vs Frequency**
  - \(V_S = \pm 2.5V\)
  - \(V_{CM} = 0.25V\)

For more information [www.linear.com/LTC6268](http://www.linear.com/LTC6268)
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ\text{C}, \) unless otherwise noted.

**Input Bias Current vs Common Mode Voltage**

**Input Bias Current vs Supply Voltage**

**Input Bias Current vs Temperature**

**Output Saturation Voltage vs Load Current (Output Low)**

**Output Saturation Voltage vs Load Current (Output High)**

**Output Short Circuit Current vs Supply Voltage**

**Input Referred Voltage Noise**

**Wide Band Input Referred Voltage Noise**

**0.1Hz to 10Hz Output Voltage Noise**

For more information [www.linear.com/LTC6268](http://www.linear.com/LTC6268)
For more information www.linear.com/LTC6268
TYPICAL PERFORMANCE CHARACTERISTICS  \( T_A = 25^\circ C, \) unless otherwise noted.

**Large Signal Response**

\( V_S = \pm 2.5V, A_V = 1, R_{LOAD} = 1k\)

**Supply Current vs Supply Voltage**

\( V_S = 0V\)

\( V_{CM} = 1V\)

\( A_V = 1\)

**Supply Current vs Shutdown Voltage**

\( V_S = 0V, 5V\)

\( V_{CM} = 2.75V\)

\( A_V = 1\)

\( C_{LOAD} = 0pF, 10pF\)

\( TA = –55^\circ C, 25^\circ C, 125^\circ C\)

**Supply Current vs Shutdown Voltage**

\( V_S = 0V, 3.1V\)

\( V_{CM} = 1V\)

\( A_V = 1\)

\( C_{LOAD} = 0pF, 10pF\)

\( TA = –55^\circ C, 25^\circ C, 125^\circ C\)
PIN FUNCTIONS

–IN: Inverting Input of the Amplifier. The voltage range of this pin is from \( V^- \) to \( V^+ - 0.5V \).

+IN: Non-Inverting Input. The voltage range of this pin is from \( V^- \) to \( V^+ - 0.5V \).

\( V^+ \): Positive Power Supply. Total supply (\( V^+ - V^- \)) voltage is from 3.1V to 5.25V. Split supplies are possible as long as the total voltage between \( V^+ \) and \( V^- \) is between 3.1V and 5.25V. A bypass capacitor of 0.1µF should be used between \( V^+ \) to ground as close to the pin as possible.

\( V^- \): Negative Power Supply. Normally tied to ground, it can also be tied to a voltage other than ground as long as the voltage difference between \( V^+ \) and \( V^- \) is between 3.1V and 5.25V. If it is not connected to ground, bypass it to ground with a capacitor of 0.1µF as close to the pin as possible.

\( \text{SHDN, SDA, SDB} \): Active Low op amp shutdown, threshold is 0.75V above the negative supply, \( V^- \). If left unconnected, the amplifier is enabled.

OUT: Amplifier Output.

NC: Not connected. May be used to create a guard ring around the input to guard against board leakage currents. See Applications Information section for more details.

SIMPLIFIED SCHEMATIC

[Diagram showing the pin functions and internal structure of the LTC6268 amplifier]

LTC6268 Simplified Schematic Diagram
**OPERATION**

The LTC6268 input signal range is specified from the negative supply to 0.5V below the positive power supply, while the output can swing from rail-to-rail. The schematic above depicts a simplified schematic of the amplifier.

The input pins drive a CMOS buffer stage. The CMOS buffer stage creates replicas of the input voltages to boot strap the protection diodes. In turn, the buffer stage drives a complementary input stage consisting of two differential amplifiers, active over different ranges of input common mode voltage. The main differential amplifier is active with input common mode voltages from the negative power supply to approximately 1.55V below the positive supply, with the second amplifier active over the remaining range to 0.5V below the positive supply rail. The buffer and output bias stage uses a special compensation technique ensuring stability of the op amp. The common emitter topology of output transistors Q1/Q2 enables the output to swing from rail-to-rail.

**APPLICATIONS INFORMATION**

**Noise**

To minimize the LTC6268's noise over a broad range of applications, careful consideration has been placed on input referred voltage noise (e_N), input referred current noise (i_N) and input capacitance C_IN.

For a trans-impedance amplifier (TIA) application such as shown in Figure 1, all three of these op amp parameters, plus the value of feedback resistance R_F, contribute to noise behavior in different ways, and external components and traces will add to C_IN. It is important to understand the impact of each parameter independently. Input referred voltage noise (e_N) consists of flicker noise (or 1/f noise), which dominates at lower frequencies, and thermal noise which dominates at higher frequencies. For LTC6268, the 1/f corner, or transition between 1/f and thermal noise, is at 80kHz. The i_N and R_F contributions to input referred noise current at the minus input are relatively straight forward, while the e_N contribution is amplified by the noise gain. Because there is no gain resistor, the noise gain is calculated using feedback resistor(R_F) in conjunction with impedance of C_IN as (1 + 2π R_F * C_IN * Freq), which increases with frequency. All of the contributions will be limited by the closed loop bandwidth. The equivalent input current noise is shown in Figures 2-5, where e_N represents contribution from input referred voltage noise (e_N), i_N represents contribution from input referred current noise (i_N), and R_F represents contribution from feedback resistor (R_F). TIA gain (R_F) and capacitance at input (C_IN) are also shown on each figure. Comparing Figures 2 & 3, and 4 & 5 for higher frequencies, e_N dominates when C_IN is high (5pF) due to the amplification mentioned above while i_N dominates when C_IN is low (1pF). At lower frequencies, the

---

For more information [www.linear.com/LTC6268](http://www.linear.com/LTC6268)
RF contribution dominates for 10k and 100k. Since wide band $\theta_N$ is 4.3nV/√Hz (see typical performance characteristics), RF contribution will become a lesser factor at lower frequencies if $R_F$ is less than 1.16kΩ as indicated by the following equation:

$$\frac{\theta_N}{R_F} \leq 1$$

**Optimizing the Bandwidth for TIA Application**

The capacitance at the inverting input node can cause amplifier stability problems if left unchecked. When the feedback around the op amp is resistive ($R_F$), a pole will be created with $R_F \| C_N$. This pole can create excessive phase shift and possibly oscillation. Referring to Figure 1, the response at the output is:

$$\frac{R_F}{1 + \frac{2\zeta s}{\omega} + \frac{s^2}{\omega^2}}$$
Where $R_F$ is the DC gain of the TIA, $\omega$ is the natural frequency of the closed loop, which can be expressed as:

$$\omega = \frac{2\pi GBW}{\sqrt{R_F(C_{IN} + C_F)}}$$

$\zeta$ is the damping factor of the loop, which can be expressed as

$$\zeta = \frac{1}{2} \left( \frac{1}{\sqrt{2\pi GBW \cdot R_F(C_{IN} + C_F)}} + \frac{2\pi GBW}{R_F(C_{IN} + C_F)} \right)$$

Where $C_{IN}$ is the total capacitance at the inverting input node of the op amp, and $GBW$ is the gain bandwidth of the op amp. There are two regions that the system will be stable regardless of $C_F$. The first region is when $R_F$ is less than $1/(4\pi \cdot C_{IN} \cdot GBW)$. In this region, the pole produced by the feedback resistor and $C_{IN}$ is at a high frequency which does not cause stability problems. The second region is where:

$$R_F > \frac{A_o^2}{\pi GBW \cdot C_{IN}}$$

Where $A_o$ is the DC open loop gain of the op amp, and the pole formed by $R_F \cdot C_{IN}$ is the dominant pole.

For $R_F$ between these two regions, the small capacitor $C_F$ in parallel with $R_F$ can introduce enough damping to stabilize the loop. By assuming $C_{IN} >> C_F$, the following condition needs to be met for $C_F$:

$$C_F > \sqrt{\frac{C_{IN}}{\pi \cdot GBW \cdot R_F}}$$

The above condition implies that higher $GBW$ will require lower feedback capacitance $C_F$, which will have higher loop bandwidth. Table 1 shows the optimal $C_F$ for $R_F$ of 10kΩ and 100kΩ and $C_{IN}$ of 1pF and 5pF.

<table>
<thead>
<tr>
<th>$R_F$</th>
<th>$C_{IN} = 1pF$</th>
<th>$C_{IN} = 5pF$</th>
</tr>
</thead>
<tbody>
<tr>
<td>10kΩ</td>
<td>0.25pF</td>
<td>0.56pF</td>
</tr>
<tr>
<td>100kΩ</td>
<td>0.08pF</td>
<td>0.18pF</td>
</tr>
</tbody>
</table>

**Achieving Higher Bandwidth with Higher Gain TIAs**

Good layout practices are essential to achieving best results from a TIA circuit. The following two examples show drastically different results from an LTC6268 in a 499kΩ TIA. (See Figure 6.) The first example is with an 0603 resistor in a basic circuit layout. In a simple layout, without expending a lot of effort to reduce feedback capacitance, the bandwidth achieved is about 2.5MHz. In this case, the bandwidth of the TIA is limited not by the $GBW$ of the LTC6268, but rather by the fact that the feedback capacitance is reducing the actual feedback impedance (the TIA gain itself) of the TIA. Basically, it's a resistor bandwidth limitation. The impedance of the 499kΩ is being reduced by its own parasitic capacitance at high frequency. From the 2.5MHz bandwidth and the 499kΩ low frequency gain, we can estimate the total feedback capacitance as $C = 1/(2\pi \cdot 2.5MHz \cdot 499k\Omega) = 0.13pF$. That’s fairly low, but it can be reduced further.
With some extra layout techniques to reduce feedback capacitance, the bandwidth can be increased. Note that we are increasing the effective “bandwidth” of the 499kΩ resistance. One of the main ways to reduce capacitance is to increase the distance between the plates, in this case the plates being the two endcaps of the component resistor. For that reason, it will serve our purposes to go to a longer resistor. An 0805 is longer than an 0603, but its endcaps are also larger in area, increasing capacitance again. However, increasing distance between the endcaps is not the only way to decrease capacitance, and the extra distance between the resistor endcaps also allows the easy application of another technique to reduce feedback capacitance. A very powerful method to reduce plate to plate capacitance is to shield the E field paths that give rise to the capacitance. In this particular case, the method is to place a short ground trace between the resistor pads, near the TIA output end.

Such a ground trace shields the output field from getting to the summing node end of the resistor and effectively shunts the field to ground instead. Keeping the trace close to the output end increases the output load capacitance very slightly. See Figure 8 for a pictorial representation.

Figure 9 shows the dramatic increase in bandwidth simply by careful attention to low capacitance methods around the feedback resistance. Bandwidth was raised from 2.5MHz to 11.2MHz, a factor greater than 4. Methods implemented were two:

1) Minimal pad sizing. Check with your board assembler for minimum acceptable pad sizing, or assemble this resistor using other means, and

2) Shield the feedback capacitance using a ground trace under the feedback resistor near the output side.

Figure 8. A Normal Layout at Left and a Field-Shunting Layout at Right. Simply Adding a Ground Trace Under the Feedback Resistor Does Much to Shunt Field Away from the Feedback Side and Dumps It to Ground. Note That the Dielectric Constant of Fr4 and Ceramic Is Typically 4, so Most of the Capacitance Is in the Solids and Not Through the Air. (Reduced Pad Size On Right Is Not Shown.)

Figure 9. LTC6268 in a 499kΩ TIA with extra Layout Effort to Reduce Feedback Capacitance Achieves 11.2MHz BW
**High Impedance Buffer**

The very high input impedance of the LTC6268 makes it ideal for buffering high impedance or capacitive sources. The circuit of Figure 10 shows the LTC6268 applied as a buffer, after a simple RC filter. The RLC network after the buffer acts as an absorptive filter to avoid excessive time domain reflections of the ADC glitches. The 2.048V reference establishes a midpoint input “zero” reference voltage. The LT1395 high speed current feedback amplifier and its associated resistor network attenuate the buffered signal and render it differential by forcing the common mode to virtual ground (the $V_{CM}$ voltage provided by the ADC).

![Circuit Diagram](image-url)

**Figure 10.** LTC6268 as a High-Z Buffer Driving an LT1395 as a Single-Ended to Differential Converter Into a 16-Bit ADC
APPLICATIONS INFORMATION

Figure 11 shows the time domain response of a 10.101MHz 3Vp-p input square wave, sampled at 10Msps, just 1ns slower than the waveform rate. At this rate, the waveform appears reconstructed at a rate of 1ns per sample, allowing for a more immediate view of the settling characteristics, even though each sample is really 100ns later.

Maintaining Ultralow Input Bias Current

Leakage currents into high impedance signal nodes can easily degrade measurement accuracy of fA signals. High temperature applications are especially susceptible to these issues. For humid environments, surface coating may be necessary to provide a moisture barrier.

There are several factors to consider in a low input bias current circuit. At the femtoamp level, leakage sources can come from unexpected sources including adjacent signals on the PCB, both on the same layer and from internal layers, any form of contamination on the board from the assembly process or the environment, other components on the signal path and even the plastic of the device package. Care taken in the design of the system can mitigate these sources and achieve excellent performance.

The choice of device package should be considered because although each has the same die internally, the pin spacing and adjacent signals influence the input bias current. The LTC6268/LTC6269 is available in SOIC, MSOP, DFN and SOT-23 packages. Of these, the SOIC has been designed as the best choice for low input bias current. It has the largest lead spacing which increases the impedance of the package plastic and the pinout is such that the two input pins are isolated on the far side of the package from the other signals. The gull-wing leads on this package also allow for better cleaning of the PCB and reduced contamination-induced leakage. The other packages have advantages in size and pin count but do so by reducing the input isolation. Leadless packages such as the DFN offer the minimum size but have the smallest pin spacing and may trap contaminants under the package.
APPLICATIONS INFORMATION

The material used in the construction of the PCB can sometimes influence the leakage characteristics of the design. Exotic materials such as Teflon can be used to improve leakage performance in specific cases but they are generally not necessary if some basic rules are applied in the design of conventional FR4 PCBs. It is important to keep the high impedance signal path as short as possible on the board. A node with high impedance is susceptible to picking up any stray signals in the system so keeping it as short as possible reduces this effect. In some cases, it may be necessary to have a metallic shield over this portion of the circuit. However, metallic shielding increases capacitance. Another technique for avoiding leakage paths is to cut slots in the PCB. High impedance circuits are also susceptible to electrostatic as well as electromagnetic effects. The static charge carried by a person walking by the circuit can induce an interference on the order of 100’s of femtoamps. A metallic shield can reduce this effect as well.

The layout of a high impedance input node is very important. Other signals should be routed well away from this signal path and there should be no internal power planes under it. The best defense from coupling signals is distance and this includes vertically as well as on the surface. In cases where the space is limited, slotting the board around the high impedance input nodes can provide additional isolation and reduce the effect of contamination. In electrically noisy environments the use of driven guard rings around these nodes can be effective (see Figure 12). Adding any additional components such as filters to the high impedance input node can increase leakage. The leakage current of a ceramic capacitor is orders of magnitude larger than the bias current of this device. Any filtering will need to be done after this first stage in the signal chain.

Low Input Offset Voltage

The LTC6268 has a maximum offset voltage of ±2.5mV (PNP region) over temperature. The low offset voltage is essential for precision applications. There are 2 different input stages that are used depending on the input common mode voltage. To increase the versatility of the LTC6268, the offset voltages are trimmed for both regions of operation.

Rail-to-Rail Output

The LTC6268 has a rail-to-rail output stage that has excellent output drive capability. It is capable of delivering over ±40mA of output drive current over temperature. Furthermore, the output can reach within 200mV of either rail while driving ±10mA. Attention must be paid to keep the junction temperature of the IC below 150°C.

Input Protection

To prevent breakdown of internal devices in the input stage, the two op amp inputs should NOT be separated by more than 2.0V. To help protect the input stage, internal circuitry will engage automatically if the inputs are separated by >2.0V and input currents will begin to flow. In all cases, care should be taken so that these currents remain less than 1mA. Additionally, if only one input is driven, internal circuitry will prevent any breakdown condition under transient conditions. The worst-case differential input voltage usually occurs when the +input is driven and the output is accidentally shorted to ground while in a unity gain configuration.
APPLICATIONS INFORMATION

ESD

ESD Protection devices can be seen in the simplified schematic. The +IN and –IN pins use a sophisticated method of ESD protection that incorporates a total of 4 reverse-biased diodes connected as 2 series diodes to each rail. To maintain extremely low input bias currents, the center node of each of these series diode chains is driven by a buffered copy of the input voltage. This maintains the two diodes connected directly to the input pins at low reverse bias, minimizing leakage current of these ESD diodes to the input pins.

The remaining pins have traditional ESD protection, using reverse-biased ESD diodes connected to each power supply rail. Care should be taken to make sure that the voltages on these pins do not exceed the supply voltages by more than 100mV or these diodes will begin to conduct large amounts of current.

Shutdown

The LTC6268S6, LTC6268S8, and LTC6269DD have SHDN pins that can shut down the amplifier to less than 1.2mA supply current per amplifier. The SHDN pin voltage needs to be within 0.75V of V– for the amplifier to shut down. During shutdown, the output will be in a high output resistance state, so the LTC6268 is suitable for multiplexer applications. The internal circuitry is kept in a low current active state for fast recovery. When left floating, the SHDN pin is internally pulled up to the positive supply and the amplifier is enabled.
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S6 Package
6-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1636)

NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

For more information www.linear.com/LTC6268
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

S8 Package
8-Lead Plastic Small Outline (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1610 Rev G)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN INCHES (MILLIMETERS)
2. DRAWING NOT TO SCALE
3. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .006" (0.15mm)
4. PIN 1 CAN BE BEVEL EDGE OR A DIMPLE.
LTC6268/LTC6269

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MS8E Package
8-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1662 Rev K)

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2). CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
### Typical Application

LTC6268 as a High-Z Buffer Driving an LT1395 as a Single-Ended to Differential Converter Into a 16-Bit ADC

Reconstructed Sampled Time Domain Response of Above Circuit

---

### Related Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Op Amps</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTC6244</td>
<td>Dual 50MHz, Low Noise, Rail-to-Rail, CMOS Op Amp</td>
<td>Unity Gain Stable, 1pA Input Bias Current, 100μV Max Offset.</td>
</tr>
<tr>
<td>LTC6240/LTC6241/</td>
<td>18MHz, Low Noise, Rail-to-Rail Output, CMOS Op Amp</td>
<td>18MHz GBW, 0.2pA Input Current, 125μV Max Offset.</td>
</tr>
<tr>
<td>LTC6242</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTC6252/LTC6253/</td>
<td>720MHz, 3.5mA Power Efficient Rail-to-Rail I/O Op Amp</td>
<td>720MHz GBW, Unity Gain Stable, Low Noise</td>
</tr>
<tr>
<td>LTC6254</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTC6246/LTC6247/</td>
<td>180MHz, 1mA Power Efficient Rail-to-Rail I/O Op Amps</td>
<td>180MHz GBW, Unity Gain Stable, Low Noise</td>
</tr>
<tr>
<td>LTC6248</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LT1818</td>
<td>400MHz, 2500V/μs, 9mA Single Operational Amplifier</td>
<td>Unity Gain Stable, 6nV/√Hz Unity Gain Stable</td>
</tr>
<tr>
<td>LT6230</td>
<td>215MHz, Rail-to-Rail Output, 1.1nV/√Hz, 3.5mA Op Amp Family</td>
<td>350μV Max Offset Voltage, 3V to 12.6V Supply</td>
</tr>
<tr>
<td>LT6411</td>
<td>650MHz Differential ADC Driver/Dual Selectable Amplifier</td>
<td>SR 3300V/μs, 6ns 0.1% Settling.</td>
</tr>
</tbody>
</table>

**SAR ADC**

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC2376-18/</td>
<td>18-Bit, 250ksps to 1.6Msps, Low Power SAR ADC, 102dB SNR</td>
<td>18mW at 1.6Msps, 3.4pW at 250sps, –126dB THD.</td>
</tr>
<tr>
<td>LTC2377-18/</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTC2378-18/</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTC2379-18</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>