LTC4370
Two-Supply Diode-OR Current Balancing Controller

FEATURES
- Shares Load Between Two Supplies
- Eliminates Need for Active Control of Input Supplies
- No Share Bus Required
- Blocks Reverse Current
- No Shoot-Through Current During Start-Up or Faults
- 0V to 18V High Side Operation
- Enable Inputs
- MOSFET On Status Outputs
- Dual Ideal Diode Mode
- 16-Lead DFN (4mm × 3mm) and MSOP Packages

APPLICATIONS
- Redundant Power Supplies
- High Availability Systems and Servers
- Telecom and Network Infrastructure

DESCRIPTION
The LTC®4370 is a two-supply current sharing controller which incorporates MOSFET ideal diodes. The diodes block reverse and shoot-through currents during start-up and fault conditions. Their forward voltage is adjusted to share the load currents between supplies. Unlike other sharing methods, neither a share bus nor trim pins on the supply are required.

The maximum MOSFET voltage drop can be set with a resistor. A fast gate turn-on reduces the load voltage droop during supply switchover. If the input supply fails or is shorted, a fast turn-off minimizes reverse current transients.

The controller operates with supplies from 2.9V to 18V. For lower rail voltages, an external supply is needed at the VCC pin. Enable inputs can be used to turn off the MOSFET and put the controller in a low current state. Status outputs indicate whether the MOSFETs are on or off. The load sharing function can be disabled to turn the LTC4370 into a dual ideal diode controller.

TYPICAL APPLICATION

12V, 10A Load Share

![Typical Application Diagram](Diagram.png)

Current Sharing Error vs Supply Difference

![Current Sharing Error Graph](Graph.png)
**LTC4370**

**ABSOLUTE MAXIMUM RATINGS** *(Notes 1, 2)*

- \( V_{IN1}, V_{IN2}, OUT1, OUT2 \) Voltages: \(-2\)V to 24V
- \( V_{CC} \) Voltage: \(-0.3\)V to 6.5V
- \( GATE1, GATE2 \) Voltages (Note 3): \(-0.3\)V to 34V
- \( CPO1, CPO2 \) Voltages (Note 3): \(-0.3\)V to 34V
- \( RANGE \) Voltage: \(-0.3\)V to \( V_{CC} + 0.3\)V
- \( COMP \) Voltage: \(-0.3\)V to 3V
- \( EN1, EN2, FETON1, FETON2 \) Voltages: \(-0.3\)V to 24V
- \( CPO1, CPO2 \) Average Current: 10mA
- \( FETON1, FETON2 \) Currents: 5mA

**Operating Ambient Temperature Range**
- LTC4370: 0°C to 70°C
- LTC4370I: -40°C to 85°C

**Storage Temperature Range**
- -65°C to 150°C

**Lead Temperature (Soldering, 10 sec)**
- MS Package: 305°C

**PIN CONFIGURATION**

**ORDER INFORMATION**

<table>
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<tr>
<th>LEAD FREE FINISH</th>
<th>TAPE AND REEL</th>
<th>PART MARKING*</th>
<th>PACKAGE DESCRIPTION</th>
<th>TEMPERATURE RANGE</th>
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<tbody>
<tr>
<td>LTC4370CDE#PBF</td>
<td>LTC4370CDE#TRPBF</td>
<td>4370</td>
<td>16-Lead (4mm × 3mm) Plastic DFN</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC4370IDE#PBF</td>
<td>LTC4370IDE#TRPBF</td>
<td>4370</td>
<td>16-Lead (4mm × 3mm) Plastic DFN</td>
<td>-40°C to 85°C</td>
</tr>
<tr>
<td>LTC4370CMS#PBF</td>
<td>LTC4370CMS#TRPBF</td>
<td>4370</td>
<td>16-Lead Plastic MSOP</td>
<td>0°C to 70°C</td>
</tr>
<tr>
<td>LTC4370IMS#PBF</td>
<td>LTC4370IMS#TRPBF</td>
<td>4370</td>
<td>16-Lead Plastic MSOP</td>
<td>-40°C to 85°C</td>
</tr>
</tbody>
</table>

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: [http://www.linear.com/leadfree/](http://www.linear.com/leadfree/)

For more information on tape and reel specifications, go to: [http://www.linear.com/tapeandreel/](http://www.linear.com/tapeandreel/)
**ELECTRICAL CHARACTERISTICS**

The ● denotes those specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ$C. $V_{IN1} = V_{IN2} = 12V$, $OUT = V_IN$, $V_{CC}$ open, unless otherwise noted.

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<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}$</td>
<td>$V_{IN1}, V_{IN2}$ Operating Range</td>
<td>With External $V_{CC}$ Supply</td>
<td>● 2.9</td>
<td>18</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$V_{CC(EXT)}$</td>
<td>$V_{CC}$ External Supply Operating Range</td>
<td>$V_{IN1}, V_{IN2} \leq V_{CC}$</td>
<td>● 2.9</td>
<td>6</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>$I_{IN}$</td>
<td>$V_{IN1}, V_{IN2}$ Current</td>
<td>Enabled, Higher Supply Other $V_{IN} = 11.7V$, Both $EN = 0V$</td>
<td>● 2.1</td>
<td>3</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Enabled, Lower Supply Other $V_{IN} = 12.3V$, Both $EN = 0V$</td>
<td>● 320</td>
<td>450</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Pull-Up Both $V_{IN} = 0V$, $V_{CC} = 5V$, Both $EN = 0V$</td>
<td>● –110</td>
<td>–180</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disabled Both $EN = 1V$</td>
<td>● 80</td>
<td>180</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{CC}$</td>
<td>$V_{CC}$ Current Enabled, Higher Supply $V_{CC} = 5V$, Both $V_{IN} = 1.2V$, Both $EN = 0V$</td>
<td>● 2</td>
<td>2.8</td>
<td>mA</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disabled $V_{CC} = 5V$, Both $V_{IN} = 1.2V$, Both $EN = 1V$</td>
<td>● 105</td>
<td>220</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$V_{CC(UVLO)}$</td>
<td>$V_{CC}$ Undervoltage Lockout Threshold</td>
<td>$V_{CC}$ Rising</td>
<td>● 2.3</td>
<td>2.55</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{CC(HYST)}$</td>
<td>$V_{CC}$ Undervoltage Lockout Hysteresis</td>
<td>$V_{CC}$ Rising</td>
<td>● 40</td>
<td>120</td>
<td>300</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{EA(OS)}$</td>
<td>Error Amplifier Input Offset</td>
<td></td>
<td>● 0</td>
<td>±2</td>
<td>mV</td>
<td></td>
</tr>
<tr>
<td>$\beta_{IN(EA)}$</td>
<td>Error Amplifier Gain ($-\Delta V_{COMP}/\Delta V_{OUT}$)</td>
<td></td>
<td>● 150</td>
<td>µS</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{FR(MIN)}$</td>
<td>Minimum Forward Regulation Voltage ($V_{IN} - OUT$)</td>
<td>$V_{IN} = 1.2V$, $V_{CC} = 5V$</td>
<td>● 2</td>
<td>12</td>
<td>25</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$V_{IN} = 12V$</td>
<td>● 2</td>
<td>25</td>
<td>50</td>
<td>mV</td>
</tr>
<tr>
<td>$V_{FR(MAX)}$</td>
<td>Maximum Forward Regulation Voltage ($V_{IN} - OUT$)</td>
<td>$R_{RANGE} = 4.99k$, $V_{IN} = 1.2V$, $V_{CC} = 5V$</td>
<td>● 40</td>
<td>62</td>
<td>82</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_{RANGE} = 4.99k$, $V_{IN} = 12V$</td>
<td>● 45</td>
<td>75</td>
<td>100</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_{RANGE} = 49.9k$, $V_{IN} = 1.2V$, $V_{CC} = 5V$</td>
<td>● 425</td>
<td>511</td>
<td>575</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$R_{RANGE} = 49.9k$, $V_{IN} = 12V$</td>
<td>● 440</td>
<td>524</td>
<td>590</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{RANGE}$</td>
<td>RANGE Pull-Up Current</td>
<td>RANGE = 0.2V</td>
<td>● –8.8</td>
<td>–10</td>
<td>–11.2</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{RANGE(TH)}$</td>
<td>RANGE Load Share Disable Threshold</td>
<td>Corresponding $EN = 1V$, $\Delta V_{GATE} = 2.5V$</td>
<td>● $V_{CC} - 0.5$</td>
<td>$V_{CC} - 0.3$</td>
<td>$V_{CC} - 0.1$</td>
<td>V</td>
</tr>
<tr>
<td>$\Delta V_{GATE}$</td>
<td>MOSFET Gate Drive ($GATE - V_{IN}$)</td>
<td></td>
<td>● 10</td>
<td>12</td>
<td>14</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>● 4.5</td>
<td>7</td>
<td>9</td>
<td>V</td>
</tr>
<tr>
<td>$t_{ON(GATE)}$</td>
<td>GATE1, GATE2 Turn-On Propagation Delay</td>
<td>$V_{FWD} = (V_{IN} - OUT)$ Step: $-0.3V \int 0.3V$</td>
<td>● 0.4</td>
<td>1</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$t_{OFF(GATE)}$</td>
<td>GATE1, GATE2 Turn-Off Propagation Delay</td>
<td>$V_{FWD}$ Step: $0.3V \int -0.3V$</td>
<td>● 0.4</td>
<td>1</td>
<td>µs</td>
<td></td>
</tr>
<tr>
<td>$R_{GATE(PK)}$</td>
<td>GATE1, GATE2 Peak Pull-Up Current</td>
<td></td>
<td>● –0.9</td>
<td>–1.4</td>
<td>–1.9</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td></td>
<td>GATE1, GATE2 Peak Pull-Down Current</td>
<td>Corresponding $EN = 1V$, $\Delta V_{GATE} = 2.5V$</td>
<td>● 0.9</td>
<td>1.4</td>
<td>1.9</td>
</tr>
<tr>
<td>$I_{GATE(OFF)}$</td>
<td>GATE1, GATE2 Off Pull-Down Current</td>
<td>Corresponding $EN = 1V$, $\Delta V_{GATE} = 2.5V$</td>
<td>● 65</td>
<td>110</td>
<td>160</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{EN(TH)}$</td>
<td>EN1, EN2 Threshold Voltage</td>
<td>EN Falling</td>
<td>● 580</td>
<td>600</td>
<td>620</td>
<td>mV</td>
</tr>
<tr>
<td>$\Delta V_{EN(TH)}$</td>
<td>EN1, EN2 Threshold Hysteresis</td>
<td></td>
<td>● 2</td>
<td>8</td>
<td>20</td>
<td>mV</td>
</tr>
<tr>
<td>$I_{EN}$</td>
<td>EN1, EN2 Current</td>
<td>At 0.6V</td>
<td>● 0</td>
<td>±1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>$I_{OUT}$</td>
<td>OUT1, OUT2 Current</td>
<td>Enabled</td>
<td>OUTn = 0V, 12V; Both $EN = 0V$</td>
<td>● –70</td>
<td>260</td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Disabled Both $EN = 1V$</td>
<td></td>
<td>● 16</td>
<td>40</td>
<td>µA</td>
</tr>
<tr>
<td>$I_{CPO(UP)}$</td>
<td>CPO1, CPO2 Pull-Up Current</td>
<td>$CPO = V_{IN}$</td>
<td>● –40</td>
<td>–70</td>
<td>–115</td>
<td>µA</td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>FETON1, FETON2 Output Low Voltage</td>
<td></td>
<td>● 1mA</td>
<td>0.12</td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>● 3mA</td>
<td>0.36</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>FETON1, FETON2 Output High Voltage</td>
<td></td>
<td>● $V_{CC} - 1.4$</td>
<td>$V_{CC} - 0.9$</td>
<td>$V_{CC} - 0.5$</td>
<td>V</td>
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</tbody>
</table>
### ELECTRICAL CHARACTERISTICS

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<th>MAX</th>
<th>UNITS</th>
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<tbody>
<tr>
<td>I_{FE(TON)}</td>
<td>FETON1, FETON2 Leakage Current</td>
<td>At 12V</td>
<td>±1 µA</td>
<td>±1 µA</td>
<td>±1 µA</td>
<td>µA</td>
</tr>
<tr>
<td>ΔV_{GATE(ON)}</td>
<td>MOSFET On Detect Threshold (GATE – V_{IN})</td>
<td>FETON Transitions High</td>
<td>0.28 V</td>
<td>0.7 V</td>
<td>1.1 V</td>
<td>V</td>
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</tbody>
</table>

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

**Note 3:** Internal clamps limit the GATE and CPO pins to a minimum of 10V above, and a diode below the corresponding V_{IN} pin. Driving these pins to voltages beyond the clamp may damage the device.

### TYPICAL PERFORMANCE CHARACTERISTICS

\( T_A = 25^\circ C, \ V_{IN1} = \ V_{IN2} = 12V, \ \text{OUT} = \ V_{IN}, \ \text{VCC} \ open, \) unless otherwise noted.

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**V\_IN Current vs Voltage**

- \( \text{OTHER V\_IN} = 0V \)
- \( \text{OTHER V\_IN} = 12V \)

**V\_IN Current vs Voltage with External V\_CC**

- \( \text{V\_CC} = 6V \)
- \( \text{V\_CC} = 6V, \ \text{OTHER V\_IN} = 0V \)

**V\_CC Current vs Voltage**

- \( \text{BOTH V\_IN} = 0V \)

**Minimum Forward Regulation Voltage vs V\_IN Voltage with External V\_CC**

- \( \text{V\_GC} = 3.3V \)
- \( \text{V\_GC} = 5V \)
TYPICAL PERFORMANCE CHARACTERISTICS

\( T_A = 25^\circ C, V_{IN1} = V_{IN2} = 12V, \) OUT = \( V_{IN} \), VCC open, unless otherwise noted.

1. **\( \Delta V_{GATE} \) Voltage vs Current**
   - Graph showing \( \Delta V_{GATE} \) voltage vs current.
   - Curves for \( V_{IN} = 18V \) and \( V_{IN} = 2.9V \).

2. **\( \Delta V_{GATE} \) and VCC Voltages vs \( V_{IN} \) Voltage**
   - Graph showing \( \Delta V_{GATE} \) and VCC voltages vs \( V_{IN} \).

3. **Maximum Forward Regulation Voltage vs RANGE Resistor**
   - Graph showing maximum forward regulation voltage vs RANGE resistor.

4. **Error Amplifier Transfer Characteristic**
   - Graph showing error amplifier transfer characteristic.

5. **FETON Output Low Voltage vs Current**
   - Graph showing FETON output low voltage vs current.

6. **FETON Output High Voltage vs Current**
   - Graph showing FETON output high voltage vs current.

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**Notes:**
- Graphs and data are provided for various electrical characteristics of the LTC4370.
- Technical parameters and specifications are detailed in the graphs and tables.
PIN FUNCTIONS

**COMP:** Error Amplifier Compensation. Connect a capacitor from this pin to GND. The value of this capacitor should be approximately 10 to 50 times the gate capacitance ($C_{ISS}$) of the MOSFET switch. Maintain low board leakage on this pin for best load sharing accuracy. For example, 100nA of leakage current (equal to 1V across 10MΩ) increases the error amplifier offset by 0.7mV. Leave this pin open if only using ideal diode mode.

**CPO1, CPO2:** Charge Pump Output. Connect a capacitor from this pin to the corresponding $V_{IN}$ pin. The value of this capacitor should be approximately 10× the gate capacitance ($C_{ISS}$) of the MOSFET switch. The charge stored on this capacitor is used to pull up the gate during a fast turn-on. Leave this pin open if fast turn-on is not needed.

**EN1, EN2:** Enable Input. Keep this pin below 0.6V to enable sharing and diode control on the corresponding supply. Driving this pin high shuts off the MOSFET gate (current can still flow through its body diode). The comparator has a built-in hysteresis of 8mV. Having both $EN$ pins high lowers the current consumption of the device.

**Exposed Pad (DE Package Only):** The exposed pad may be left open or connected to device ground.

**FETON1, FETON2:** MOSFET Status Output. This pin is pulled low by an internal switch when GATE is less than 0.7V above $V_{IN}$ to indicate an off MOSFET. Because of this, it may also signal off if small currents are flowing through a high-$g_m$ MOSFET with a large forward voltage across it. An internal 500k resistor pulls this pin up to a diode below $V_{CC}$. It may be pulled above $V_{CC}$ using an external pull-up. Tie to GND or leave open if unused.

**GATE1, GATE2:** MOSFET Gate Drive Output. Connect this pin to the gate of the external N-channel MOSFET switch. An internal clamp limits the gate voltage to 12V above, and a diode below the input supply. During fast turn-on, a 1.4A pull-up current charges GATE to CPO. During fast turn-off, a 1.4A pull-down current discharges GATE to $V_{IN}$.

**GND:** Device Ground.

**OUT1, OUT2:** Output Voltage and Current Sense Input. Connect this pin to the input side of the supply’s current sense resistor. A Kelvin connection is important for accurate current sharing. The voltage sensed at this pin is used to control the MOSFET gate.

**RANGE:** Supply Differential Voltage Load Sharing Range. Connect a resistor (below 60k) from this pin to GND. A 10μA internal pull-up current source into this resistor sets the pin voltage $V_{RANGE}$. The two supplies will typically share the load current if their voltage difference is within $\pm V_{RANGE}$. The maximum sharing range is $\pm 0.6V$, obtained by leaving RANGE open. Connecting this pin to $V_{CC}$ disables load share control and the device behaves as a dual ideal diode controller.

**$V_{CC}$:** Low Voltage Supply. Connect a 0.1μF capacitor from this pin to ground. For $V_{IN} \geq 2.9V$ this pin provides decoupling for an internal regulator that generates a 5V supply. For applications where both $V_{IN} < 2.9V$, also connect an external supply in the 2.9V to 6V range to this pin.

**$V_{IN1}, V_{IN2}$:** Voltage Sense and Supply Input. Connect this pin to the supply side of the MOSFET. The low-voltage supply $V_{CC}$ is generated from the higher of $V_{IN1}$ and $V_{IN2}$. The voltage sensed at this pin is used to control the MOSFET gate.
**LTC4370**

**FUNCTIONAL DIAGRAM**

Diagram showing the functional diagram of the LTC4370 with various components and connections labeled. The diagram includes labels for Vcc, Vcc low, SA1, SA2, GATE1, GATE2, CP4, CP6, and other related components and connections.
The LTC4370 controls N-channel MOSFETs, M1 and M2, to share the load between two supplies. Error amplifier EA compares OUT1 to OUT2 and sets the servo command voltages, $V_{FR1}$ and $V_{FR2}$, for servo amplifiers, SA1 and SA2. When enabled, each servo amplifier controls the gate of the external MOSFET to regulate its forward voltage drop ($V_{FWD} = V_{IN} - OUT$) to $V_{FR}$. The combined action of EA and SA forces OUT1 to equal OUT2. Having the power path resistance from OUT1 to the load (R1) equal that from OUT2 to the load (R2) forces each supply to source half of the load current.

The lower limit of $V_{FR}$ adjustment is 25mV at higher supply voltages (reducing to 12mV at lower voltages to conserve power and voltage drop). The upper limit is $V_{RANGE} + 25mV$ (or $V_{RANGE} + 12mV$). $V_{RANGE}$ itself is set by the 10µA pull-up current source into resistor R3. The servo adjust block ensures that only the higher supply’s $V_{FR}$ is adjusted up while the other is pinned to the minimum. Tying RANGE to VCC (CP5) forces both $V_{FR}$ to the minimum, transforming the device into a dual ideal diode controller.

The servo amplifier raises the gate voltage to enhance the MOSFET whenever the load current causes the drop to exceed $V_{FR}$. For large output currents the MOSFET gate is driven fully on and the voltage drop is equal to $I_{FET} \cdot R_{DS(ON)}$.

In the case of an input supply short-circuit, when the MOSFET is conducting, a large reverse current starts flowing from the load towards the input. SA detects this failure condition as soon as it appears and turns off the MOSFET by rapidly pulling down its gate.

SA quickly pulls up the gate whenever it senses a large forward voltage drop. An external capacitor (C1, C2) between the CPO and V IN pins is needed for fast gate pull-up. This capacitor is charged up, at device power-up, by the internal charge-pump. The stored charge is used for the fast gate pull-up.

The GATE pin sources current from the CPO pin and sinks current to the V IN and GND pins. Clamps limit the GATE and CPO voltages to 12V above and a diode below V IN. Internal switches pull the FETON pins low when the GATE to V IN voltage is below 0.7V to indicate that the external MOSFET is off (body diode could still conduct).

LDO is a low dropout regulator that generates a 5V supply at the VCC pin from the highest V IN input. When supplies below 2.9V are being shared, an external supply in the 2.9V to 6V range is required at the VCC pin.

$V_{CC}$ and $EN$ pin comparators, CP1 to CP3, control power passage. The MOSFET is held off whenever the $EN$ pin is above 0.6V, or the $V_{CC}$ pin is below 2.55V. A high on both $EN$ pins lowers the current consumption of the device.
High availability systems often employ parallel-connected power supplies or battery feeds to achieve redundancy and enhance system reliability. ORing diodes have been a popular means of connecting these supplies at the point of load. System uptime improves further if these paralleled supplies also share the load current.

Current Sharing Characteristic

The LTC4370 load shares the two supplies by dropping their voltage difference across the MOSFETs in series with them (see Figure 1). The MOSFET on the lower supply drops the minimum servo voltage \( V_{FR(MIN)} \) (12mV or 25mV depending on supply voltage levels), while the other MOSFET drops \( V_{FR(MIN)} + \) the supply voltage difference. This equalizes both the OUT pin voltages, and by Ohm’s law the current that flows through the sense resistors. Figure 2a illustrates this. It shows the higher supply’s MOSFET forward voltage drop, \( V_{FWD} \), increasing to compensate the supply difference up to ±500mV.

The upper limit of the servo command adjustment is the minimum servo plus the RANGE pin voltage (500mV in Figure 2). Hence, when the two supplies differ by a voltage equal to \( V_{RANGE} \), the higher supply’s \( V_{FWD} \) is pinned at the maximum servo voltage \( V_{FR(MAX)} \). If the supplies diverge by more than \( V_{RANGE} \), the OUT pin voltages start...
diverging, and so too, the supply currents. As the supply voltages separate, the entire load current is steered to the higher supply. Now, the servo command across the higher supply’s MOSFET is folded back from the maximum to the minimum servo to minimize power dissipated in the MOSFET. The sharing capture range, $\Delta V_{\text{IN(SH)}}$, in Figure 2a is ±500mV, set by $V_{\text{RANGE}}$. Figure 2b will be discussed later in the MOSFET Selection section.

**RANGE Pin Configuration**

The RANGE pin resistor is decided by the design trade-off between the sharing capture range and the power dissipated in the MOSFET. A larger $R_{\text{RANGE}}$ increases the capture range at the expense of enhanced power dissipation and reduced load voltage. On the other hand, supplies with tight tolerances can afford a smaller capture range and therefore cooler operation of the MOSFETs.

As mentioned, the upper limit of the servo command adjustment is $V_{\text{RANGE}}$ plus the minimum forward regulation voltage. Since an internal 10μA pull-up current flowing through the external resistor sets $V_{\text{RANGE}}$:

$$V_{\text{FR(MAX)}} = 10\mu\text{A} \cdot R_{\text{RANGE}} + V_{\text{FR(MIN)}}$$  \hspace{1cm} (1)

If $R_{\text{RANGE}}$ is larger than 60k (including the pin open state), the internal limit for the first term on the right-hand side of Equation 1 is 600mV, setting $V_{\text{FR(MAX)}}$ to 612mV or 625mV. Note that servo voltages nearing the MOSFET’s body diode voltage may divert some or all current to the diode especially at hot temperatures. This may either cause FETON to go low if $V_{\text{GS}}$ falls below 0.7V, or loss of sharing control. Also note that an open RANGE pin biases itself to a voltage greater than 600mV.

Connecting the RANGE pin to $V_{\text{CC}}$ disables the load sharing loop. The servo voltages for both MOSFETs are fixed at the minimum with no adjustment. The device now behaves as a dual ideal diode controller. This is handy for testing purposes. Use the LTC4353 if only a dual ideal diode controller is needed.

**Power Supply Configuration**

The LTC4370 can load share high side supplies down to 0V rail voltage. This requires powering the $V_{\text{CC}}$ pin with an early external supply in the 2.9V to 6V range. In this range of operation $V_{\text{IN}}$ should be lower than $V_{\text{CC}}$. If $V_{\text{CC}}$ powers up after $V_{\text{IN}}$, and backfeeding of $V_{\text{CC}}$ by the internal 5V LDO is a concern, then a series resistor (few 100Ω) or Schottky diode limits device power dissipation and backfeeding of a low $V_{\text{CC}}$ supply when any $V_{\text{IN}}$ is high. A 0.1μF bypass capacitor should also be connected between the $V_{\text{CC}}$ and GND pins, close to the device. Figure 3 illustrates this.

If either $V_{\text{IN}}$ operates above 2.9V, then the external supply at $V_{\text{CC}}$ is not needed. The 0.1μF capacitor is still required for bypassing.

**Start of Sharing**

When currents are not being shared either because the load current or one of the supplies is off, the COMP voltage is railed towards 0V or 2V depending on the input signal to the error amplifier and its offset. For example,
in the absence of load current the differential input voltage to the error amplifier is zero and the COMP current is $g_{m(EA)} \cdot V_{EA(OS)}$. Before sharing can start, the COMP voltage has to slew towards its operating point of 0.7V (when $V_{IN1} < V_{IN2}$) or 1.24V ($V_{IN1} > V_{IN2}$). This delay is determined by the differential input signal to the error amplifier (which is $\Delta V_{OUT} = OUT1 - OUT2 = (I1 - I2) \cdot R_S$), its $g_m$ and the COMP capacitor value. Depending on how the currents split before converging, the delay can vary from 1 to 5 times:

$$\frac{C_C \cdot \Delta V_{COMP}}{g_{m(EA)} \cdot I_L \cdot R_S}$$

Figure 4a shows the case where a 5.1V $V_{IN1}$ is turned on while $V_{IN2}$ is at 4.9V supplying 10A. Initially, COMP is railed low to 0.1V since $\Delta V_{OUT}$ ($-I2 \cdot R_S$) is negative, and needs to rise to 1.24V as the final $V_{IN1}$ is higher than $V_{IN2}$. With $V_{IN}$ off, $\Delta V_{IN}$ is large and negative, causing the forward regulation voltage of the second supply $V_{FR2}$ to be folded back to the minimum $V_{FR(MIN)}$ (travelling from left to right in Figure 2a). As the $\Delta V_{IN}$ magnitude decreases, $V_{FR2}$ rises to the maximum $V_{FR(MAX)}$, lowering $I_2$ and the load voltage. COMP is around 0.7V when $V_{FR2}$ is being adjusted. When COMP reaches 1.24V, $V_{FR2}$ is kept at the minimum and $V_{FR1}$ is adjusted appropriately to compensate for the 0.2V of $\Delta V_{IN}$. The sharing closure is smoother for the case where $V_{IN1} < V_{IN2}$ since COMP only has to slew to 0.7V to lower $V_{FR2}$ (Figure 4b).

**MOSFET Selection**

The LTC4370 drives N-channel MOSFETs to conduct the load current. The important parameters of the MOSFET are its maximum drain-source voltage $BV_{DSS}$, maximum gate-source voltage $V_{GS(MAX)}$, on-resistance $R_{DS(ON)}$, and maximum power dissipation $P_{D(MAX)}$.

If an input is connected to ground, the full supply voltage can appear across the MOSFET. To survive this, the $BV_{DSS}$ must be higher than the supply voltages. The $V_{GS(MAX)}$ rating of the MOSFET should exceed 14V since that is the upper limit of the internal GATE to $V_{IN}$ clamp.

To obtain the maximum sharing capture range, the $R_{DS(ON)}$ should be low enough for the servo amplifier to regulate the minimum forward regulation voltage across the MOSFET while it’s conducting half of the load current. If it cannot, the gate voltage will be railed high. Hence, the $R_{DS(ON)}$ value in the MOSFET data sheet should be looked up for 10V or 4.5V gate drive depending on the $V_{IN}$ voltage. Since the OUT voltages are equal, the breakpoint for exact sharing in the higher $R_{DS(ON)}$ case is:

$$\Delta V_{IN(SH)} = V_{FR(MAX)} - 0.5I_L \cdot R_{DS(ON)} \quad (2)$$

Figure 4. Start of Sharing at $V_{IN1}$ Turn-On

4370f

4370a
In Figure 2b, 0.5IL • RDS(ON) is 125mV. The higher RDS(ON) rails the servo amplifier high as it cannot regulate the 25mV VFR(MIN) across the lower supply’s MOSFET. Compared to Figure 2a, the sharing capture range shrinks by 100mV (125mV – 25mV) to ±400mV. However, the ΔVIN over which currents are shared partially stays the same at 500mV + IL • RSD. Even when not maximizing sharing range, IL • RDS(ON) should be kept below 75mV for optimum performance.

The peak power dissipation in the MOSFET occurs when the entire load current is being sourced by one supply with the maximum forward regulation voltage dropped across the MOSFET (as shown in Figure 2a). Therefore, the PD(MAX) rating of the MOSFET should satisfy:

\[ P_{D(MAX)} \geq I_L \cdot V_{FR(MAX)} \]  

Table 1 provides starting guidelines for the type of MOSFET package and heat sink required at various levels of power dissipation. These are typical ranges for a room temperature ambient with no air flow.

<table>
<thead>
<tr>
<th>MAXIMUM POWER DISSIPATED</th>
<th>MOSFET PACKAGE</th>
<th>HEAT SINK</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.5W to 1W</td>
<td>SO-8</td>
<td>PCB</td>
</tr>
<tr>
<td>1W to 2W</td>
<td>SO-8 With Exposed Pad, D-Pak (TO-252)</td>
<td>PCB</td>
</tr>
<tr>
<td></td>
<td>TO-220</td>
<td>Standing in Free Air</td>
</tr>
<tr>
<td>2W to 4W</td>
<td>DD-Pak (TO-263), TO-220</td>
<td>PCB</td>
</tr>
<tr>
<td>4W to 10W</td>
<td>TO-220</td>
<td>Stamping</td>
</tr>
<tr>
<td>10W to 20W</td>
<td>TO-220</td>
<td>Casting, Extrusion</td>
</tr>
<tr>
<td>20W to 50W</td>
<td>TO-247, TO-3P</td>
<td>Extrusion</td>
</tr>
</tbody>
</table>

### Sense Resistor Selection

The sense resistor voltage drop dictates the current sharing accuracy. Sharing error, due to the error amplifier input offset, decreases with increasing sense voltage as:

\[ \Delta I / I_L = |I_1 - I_2| / I_L = |V_{EA(OS)}| / (I_L \cdot R_S) = 2mV / (I_L \cdot R_S) \]  

I1 and I2 are the two supply currents, IL is the load current (I1 + I2 = IL), RS is the sense resistor value, and VEA(OS) is the input offset of the internal error amplifier. A 25mV sense resistor voltage drop with half of the load current flowing through it (i.e., IL • RS = 50mV) gives a 4% sharing error. A larger sense resistance may also be needed if there is a connector in between the OUT pins and the load to minimize the effect of its resistance. At larger sense voltages the accuracy will be limited by the sense resistor tolerance.

If sharing accuracy requirements can be relaxed, power dissipated in the sense resistor can be reduced by selecting a lower resistance. Worst-case power dissipation happens at full load, i.e., when load current is not being shared. While reducing the sense resistance, note that the sharing loop does not close for load currents below VEA(OS)/RS.

The two sense resistors can have different values if the application does not require the load current to be shared equally between the supplies. In such a case:

\[ \frac{R_{S1}}{R_{S2}} = \frac{I_2}{I_1} \]  

### CPO Capacitor Selection

The recommended value of the capacitor between the CPO and VIN pins is approximately 10× the input capacitance CISS of the MOSFET. A larger capacitor takes a correspondingly longer time to be charged by the internal charge pump. A smaller capacitor suffers more voltage drop during a fast gate turn-on event as it shares charge with the MOSFET gate capacitance.
APPLICATIONS INFORMATION

External CPO Supply
The internal charge pump takes milliseconds to charge up the CPO capacitor especially during device power-up. This time can be shortened by connecting an external supply to the CPO pin. A series resistor is needed to limit the current into the internal clamp between the CPO and \( V_{\text{IN}} \) pins. The CPO supply should also be higher than the main input supply to meet the gate drive requirements of the MOSFET. Figure 5 shows such a 3.3V load share application, where a 12V supply is connected to the CPO pins through a 1k resistor. The 1k limits the current into the CPO pin when the \( V_{\text{IN}} \) pin is grounded. For the 8.7V of gate drive (12V – 3.3V), logic-level MOSFETs would be an appropriate choice for M1 and M2.

Loop Stability
The servo amplifier loop is compensated by the gate capacitance of the N-channel power MOSFET. No further compensation components are normally required. In the case when a MOSFET with less than 1nF gate capacitance is chosen, a 1nF compensation capacitor connected across the gate and source might be required.

The load sharing control loop is compensated by the capacitor from the COMP pin to ground. This capacitor should be at least 50× the input capacitance \( C_{\text{ISS}} \) of the MOSFET. A larger capacitor improves stability at the expense of increased sharing closure delay, while a smaller capacitor can cause the two supply currents to switch back and forth before settling. The COMP capacitor can be just 10× \( C_{\text{ISS}} \) when a CPO capacitor is omitted, i.e., when fast gate turn-on is not used (see Figure 6).

Input and Output Capacitance for Pulsed Loads
For pulsed loads, the load current will be shared every cycle at frequencies below 100Hz. At higher frequencies, each cycle’s current may not be shared but the time average of the currents will be. Bypassing capacitance on the inputs should be provided to minimize glitches and ripple. This is important since the controller tries to compensate for the supply voltage differences to achieve load sharing. Sufficient load capacitance should also be provided to enhance the DC component of the load current presented to the load share circuit. It is also important to design \( I_{\text{L}} \bullet R_{\text{DS(ON)}} \) below 75mV, as mentioned earlier.

With very low duty cycle or very low frequency loads, the COMP voltage will rail whenever the load current falls below the sharing threshold of \( V_{\text{EA(OS)}} / R_{\text{S}} \) for hundreds of milliseconds. At the start of the next load cycle there will be a sharing closure delay as COMP slews to its operating point around 0.7V or 1.24V. To avoid this delay, maintain the load current above \( V_{\text{EA(OS)}} / R_{\text{S}} \).

Figure 5. 3.3V Load Share with External 12V Supply Powering CPO for Faster Start-Up and Refresh
Figure 6. Current Sharing 12V Supplies
Input Transient Protection
When the capacitances at the input and output are very small, rapid changes in current can cause transients that exceed the 24V absolute maximum rating of the VIN and OUT pins. In ORing applications, one surge suppressor connected from OUT to ground clamps all the inputs. In the absence of a surge suppressor, an output capacitance of 10μF is sufficient in most applications to prevent the transient from exceeding 24V.

12V Design Example
This design example demonstrates the selection of components in a 12V system with a 10A maximum load current and ±2% tolerance supplies (Figure 6). That is followed by the recalculations involved for a similar 5V system (Figure 1).

First, calculate the R_DS(ON) of the MOSFET to achieve the desired forward drop at full load. Assuming a V_FWD of 50mV:

\[ R_{DS(ON)} \leq \frac{V_{FWD}}{I_{LOAD}} = \frac{50\text{mV}}{10\text{A}} = 5\text{mΩ} \]

The SUM85N03-06P offers a good solution in a DD-Pak (TO-263) sized package with a 4.5mΩ R_DS(ON), 30V BV_{DSS} and 20V V_{GS(MAX)}. Since 0.5I_L • R_{DS(ON)} is 22.5mV, the servo amplifier will be able to regulate the 25mV minimum forward regulation voltage leading to the maximum possible sharing range set by V_RANGE.

2% of 12V is 240mV. The sharing capture range, ΔV_{IN(SH)}, needs to be about 2 • 240mV (±480mV) to work for most supply voltage differences. A 47.5k R3 sets V_RANGE to 475mV. Equation 1 is used to calculate the maximum forward regulation voltage:

\[ V_{FR(MAX)} = 10\text{µA} \cdot 47.5\text{k} + 25\text{mV} = 500\text{mV} \]

Equation 3 gives the maximum power dissipation in the MOSFET to be:

\[ P_{D(MAX)} = 10\text{A} \cdot 500\text{mV} = 5\text{W} \]

Sufficient PCB area with air flow needs to be provided around the MOSFET drain to keep its junction temperature below the 175°C maximum.

A 2.5mΩ sense resistor drops 25mV at full load and yields an error amplifier offset induced sharing error of 2mV/(10A • 2.5mΩ) or 8% (Equation 4). At full load, the sense resistor dissipates 10A^2 • 2.5mΩ or 250mW. Since a 12V supply is large enough to tolerate a diode drop, fast gate turn-on is not needed. Hence, the CPO capacitor is omitted. The input capacitance, C_{ISS}, of the MOSFET is about 3800pF. Since fast turn-on is not used, the COMP capacitor C_C can be just 10 x C_{ISS} at 0.039µF.

Red LED, D1, turns on when any one of the MOSFETs is off, indicating a break in sharing. It requires around 3mA for good luminous intensity. Accounting for a 2V diode drop and 0.6V V_{OL}, R4 is set to 2.7k.

5V Design Example
For a 5V, 10A system with ±3% tolerance supplies and fast gate turn-on (Figure 1), the following components need to be recalculated: R3, C1, C2, C_C, and R4. R3 is set to 30.1k to account for possible supply differences (2 • 3% • 5V yields ±300mV). C1 and C2 are set to 10 x C_{ISS} at 0.039µF. With fast turn-on, C_C is selected closer to 50 x C_{ISS} at 0.18µF. With the 5V supply, R4 needs to be 820Ω to allow 3mA into the LED.
 PCB Layout Considerations

Kelvin connection of the OUT pins to the sense resistors is important for accurate current sharing. Place the MOSFET as close as possible to the sense resistor. Keep the traces to the MOSFET wide and short to minimize resistive losses. The PCB traces associated with the power path through the MOSFET should have low resistance. Thermal management techniques such as sufficient drain copper area or heat sinks should be considered for optimal MOSFET power dissipation. See Figure 7.

It is also important to put CVCC, the bypass capacitor, as close as possible between VCC and GND. Place C1 and C2 near the CPO and VIN pins. The COMP pin may need a guard ring to maintain low board leakage.

Figure 7. Recommended PCB Layout for M1, M2, CVCC, R1, R2
Current Sharing 3.3V Supplies for 20A Output
TYPICAL APPLICATIONS

12V Ideal Diode-OR by Tying RANGE to \( V_{CC} \) (to Compare Against Load Share).
Use LTC4353 if Load Share Is Not Desired
PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DE Package
16-Lead Plastic DFN (4mm × 3mm)
(Reference LTC DWG # 05-08-1732 Rev 0)

NOTE:
1. DRAWING PROPOSED TO BE MADE VARIATION OF VERSION (WGED-3) IN JEDEC PACKAGE OUTLINE MO-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS
APPLY SOLDER MASK TO AREAS THAT ARE NOT SOLDERED
PACKAGE DESCRIPTION

MS Package
16-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1669 Rev Ø)

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
# LTC4370

## Typical Application

### Schematic Diagram

![Schematic Diagram](image)

### Related Parts

<table>
<thead>
<tr>
<th>Part Number</th>
<th>Description</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>LTC1473/</td>
<td>Dual PowerPath™ Switch Driver</td>
<td>N-Channel, 4.75V to 30V/3.3V to 10V, SSOP-16 Package</td>
</tr>
<tr>
<td>LTC1473L</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LTC4349</td>
<td>PowerPath Controller for Dual Battery Systems</td>
<td>Three N-Channel Drivers, 6V to 28V, SSOP-36 Package</td>
</tr>
<tr>
<td>LTC4353</td>
<td>Low Voltage Ideal Diode Controller with Monitoring</td>
<td>N-Channel, 0V to 18V, UV, OV, MSOP-12 and DFN-12 Packages</td>
</tr>
<tr>
<td>LTC4354</td>
<td>Dual Low Voltage Ideal Diode Controller</td>
<td>Dual N-Channel, 0V to 18V, MSOP-16 and DFN-16 Packages</td>
</tr>
<tr>
<td>LTC4355</td>
<td>Negative Voltage Diode-OR Controller and Monitor</td>
<td>Dual N-Channel, −4.5V to −80V, SO-8 and DFN-8 Packages</td>
</tr>
<tr>
<td>LTC4356</td>
<td>Positive High Voltage Diode-OR with Supply and</td>
<td>Dual N-Channel, 9V to 80V, SO-16 and DFN-14 Packages</td>
</tr>
<tr>
<td></td>
<td>Fuse Monitors</td>
<td></td>
</tr>
<tr>
<td>LTC4357</td>
<td>Positive High Voltage Ideal Diode Controller</td>
<td>N-Channel, 9V to 80V, MSOP-8 and DFN-6 Packages</td>
</tr>
<tr>
<td>LTC4358</td>
<td>5A Ideal Diode</td>
<td>Internal N-Channel, 9V to 26.5V, TSSOP-16 and DFN-14 Packages</td>
</tr>
<tr>
<td>LTC43411</td>
<td>2.6A Low Loss Ideal Diode in ThinSOT™</td>
<td>Internal P-Channel, 2.6V to 5.5V, 40μA Iq, SOT-23 Package</td>
</tr>
<tr>
<td>LTC43412/LTC43412HV</td>
<td>Low Loss PowerPath Controller in ThinSOT</td>
<td>P-Channel, 2.5V to 28V/36V, 11μA Iq, SOT-23 Package</td>
</tr>
<tr>
<td>LTC43413/LTC43413-1</td>
<td>Dual 2.6A, 2.5V to 5.5V, Ideal Diodes in DFN-10</td>
<td>Dual Internal P-Channel, 2.5V to 5.5V, DFN-10 Package</td>
</tr>
<tr>
<td>LTC43414</td>
<td>36V Low Loss PowerPath Controller for Large</td>
<td>P-Channel, 3V to 36V, 30μA Iq, MSOP-8 Package</td>
</tr>
<tr>
<td></td>
<td>P-Channel MOSFETs</td>
<td></td>
</tr>
<tr>
<td>LTC43415</td>
<td>Dual 4A Ideal Diodes with Adjustable Current</td>
<td>Dual P-Channel 50mΩ Ideal Diodes, 1.7V to 5.5V, 15mV Forward Drop,</td>
</tr>
<tr>
<td></td>
<td>Limit</td>
<td>MSOP-16 and DFN-16 Packages</td>
</tr>
<tr>
<td>LTC43416/LTC43416-1</td>
<td>36V Low Loss Dual PowerPath Controller for Large</td>
<td>Dual P-Channel, 3.6V to 36V, 70μA Iq, MSOP-10 Package</td>
</tr>
<tr>
<td></td>
<td>P-Channel MOSFETs</td>
<td></td>
</tr>
</tbody>
</table>