FEATURES

- Wide Operating Voltage Range: 2.5V to 34V
- Overvoltage Protection to 60V
- Reverse Supply Protection to –40V
- LTC4365: Blocks 50Hz and 60Hz AC Power
- LTC4365-1: Fast (1ms) Recovery from Fault
- No Input Capacitor or TVS Required for Most Applications
- Adjustable Undervoltage and Overvoltage Protection Range
- Charge Pump Enhances External N-Channel MOSFET
- Low Operating Current: 125µA
- Low Shutdown Current: 10µA
- Compact 8-Lead, 3mm × 2mm DFN and TSOT-23 (ThinSOT™) Packages

APPLICATIONS

- Portable Instrumentation
- Industrial Automation
- Laptops
- Automotive Surge Protection

DESCRIPTION

The LTC®4365 protects applications where power supply input voltages may be too high, too low or even negative. It does this by controlling the gate voltages of a pair of external N-channel MOSFETs to ensure that the output stays within a safe operating range.

The LTC4365 can withstand voltages between –40V and 60V and has an operating range of 2.5V to 34V, while consuming only 125µA in normal operation.

Two comparator inputs allow configuration of the overvoltage (OV) and undervoltage (UV) set points using an external resistive divider. A shutdown pin provides external control for enabling and disabling the MOSFETs as well as placing the device in a low current shutdown state. A fault output provides status of the gate pin pulling low. A fault is indicated when the part is in shutdown or the input voltage is outside the UV and OV set points.

The LTC4365 has a 36ms turn-on delay that debounces live connections and blocks 50Hz to 60Hz AC power. For fast recovery after faults, the LTC4365-1 has a reduced 1ms turn-on delay.

For more information visit www.linear.com/LTC4365
LTC4365

**ABSOLUTE MAXIMUM RATINGS**

Supply Voltage (Note 1)

\[ V_{IN} \] .................................................. \(-40V \) to \(60V \)

Input Voltages (Note 3)

\[ UV, SHDN \] .............................................. \(-0.3V \) to \(60V \)
\[ OV \] ............................................................ \(-0.3V \) to \(6V \)
\[ V_{OUT} \] ....................................................... \(-0.3V \) to \(40V \)

Output Voltages (Note 4)

\[ FAULT \] ..................................................... \(-0.3V \) to \(60V \)
\[ GATE \] ....................................................... \(-40V \) to \(45V \)

Input Currents

\[ UV, OV, SHDN \] ............................................. \(-1mA \)

Operating Ambient Temperature Range

LTC4365C .................................................. \(0°C \) to \(70°C \)
LTC4365I .................................................. \(-40°C \) to \(85°C \)
LTC4365H .................................................. \(-40°C \) to \(125°C \)

Storage Temperature Range .................. \(-65°C \) to \(150°C \)

Lead Temperature (Soldering, 10 sec) for TSOT Only .............................................. \(300°C \)

**PIN CONFIGURATION**

![Top View Diagram]

**DDB PACKAGE**

8-LEAD (3mm × 2mm) PLASTIC DFN

\[ T_{JMAX} = 150°C, \theta JA = 76°C/W \]

EXPOSED PAD (PIN 9) PCB GROUND CONNECTION OPTIONAL

**TS8 PACKAGE**

8-LEAD PLASTIC TSOT-23

\[ T_{JMAX} = 150°C, \theta JA = 195°C/W \]
## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = 2.5V$ to $34V$, unless otherwise noted. (Note 2)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{IN}, V_{OUT}$</td>
<td>Input Voltage Range</td>
<td>Operating Range Protection Range</td>
<td>●</td>
<td>2.5</td>
<td>34</td>
<td>V</td>
</tr>
<tr>
<td>$I_{VIN}$</td>
<td>Input Supply Current</td>
<td>$SHDN = 0V, V_{IN} = V_{OUT}, -40°C to 85°C$&lt;br&gt;$SHDN = 0V, V_{IN} = V_{OUT}, -40°C to 125°C$&lt;br&gt;$SHDN = 2.5V$</td>
<td>●</td>
<td>10</td>
<td>50</td>
<td>μA</td>
</tr>
<tr>
<td>$I_{VIN(R)}$</td>
<td>Reverse Input Supply Current</td>
<td>$V_{IN} = -40V, V_{OUT} = 0V$</td>
<td>●</td>
<td>–1.2</td>
<td>–1.8</td>
<td>mA</td>
</tr>
<tr>
<td>$V_{IN(UVLO)}$</td>
<td>Input Supply Undervoltage Lockout</td>
<td>$V_{IN}$ Rising</td>
<td>●</td>
<td>1.8</td>
<td>2.2</td>
<td>2.4</td>
</tr>
<tr>
<td>$I_{VOUT}$</td>
<td>$V_{OUT}$ Input Current</td>
<td>$SHDN = 0V, V_{IN} = V_{OUT}$&lt;br&gt;$SHDN = 2.5V, V_{IN} = V_{OUT}$&lt;br&gt;$V_{IN} = -40V, V_{OUT} = 0V$</td>
<td>●</td>
<td>6</td>
<td>30</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>100</td>
<td>250</td>
<td>μA</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>20</td>
<td>50</td>
<td>μA</td>
</tr>
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</table>

### GATE

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>$\Delta V_{GATE}$</td>
<td>N-Channel Gate Drive ($GATE-V_{OUT}$)</td>
<td>$V_{IN} = V_{OUT} = 5.0V$, $I_{GATE} = -1\mu A$&lt;br&gt;$V_{IN} = V_{OUT} = 12V$ to $34V$, $I_{GATE} = -1\mu A$</td>
<td>●</td>
<td>3</td>
<td>3.6</td>
<td>4.2</td>
</tr>
<tr>
<td>$I_{GATE(UP)}$</td>
<td>N-Channel Gate Pull Up Current</td>
<td>$GATE = V_{IN} = V_{OUT} = 12V$</td>
<td>●</td>
<td>–12</td>
<td>–20</td>
<td>–30</td>
</tr>
<tr>
<td>$I_{GATE(FAST)}$</td>
<td>N-Channel Gate Fast Pull Down Current</td>
<td>Fast Shutdown, $GATE = 20V$, $V_{IN} = V_{OUT} = 12V$</td>
<td>●</td>
<td>31</td>
<td>50</td>
<td>72</td>
</tr>
<tr>
<td>$I_{GATE(SLOW)}$</td>
<td>N-Channel Gate Gentle Pull Down Current</td>
<td>Gentle Shutdown, $GATE = 20V$, $V_{IN} = V_{OUT} = 12V$</td>
<td>●</td>
<td>50</td>
<td>90</td>
<td>150</td>
</tr>
<tr>
<td>$I_{GATE(FAST)}$</td>
<td>N-Channel Gate Fast Turn Off Delay</td>
<td>$C_{GATE} = 2.2nF$, UV or OV Fault</td>
<td>●</td>
<td>2</td>
<td>4</td>
<td>μs</td>
</tr>
<tr>
<td>$I_{GATE(SLOW)}$</td>
<td>N-Channel Gentle Turn Off Delay</td>
<td>$C_{GATE} = 2.2nF$, SHDN Falling, $V_{IN} = V_{OUT} = 12V$</td>
<td>●</td>
<td>150</td>
<td>250</td>
<td>350</td>
</tr>
</tbody>
</table>
## LTC4365

### ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A = 25^\circ\text{C}$, $V_{IN} = 2.5\text{V}$ to $34\text{V}$, unless otherwise noted. (Note 2)

<table>
<thead>
<tr>
<th>SYMBOL</th>
<th>PARAMETER</th>
<th>CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNITS</th>
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</thead>
<tbody>
<tr>
<td>$t_{RECOVERY}$</td>
<td>GATE Recovery Delay Time</td>
<td>$V_{IN} = 12\text{V}, \text{Power Good to } \Delta V_{GATE} &gt; 0\text{V}$ $\text{LTC4365}, C_{GATE} = 2.2\text{nF}$ $\text{LTC4365-1}, \text{C}_{GATE} = 2.2\text{nF}$</td>
<td>● 26</td>
<td>36</td>
<td>49</td>
<td>ms</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>● 0.6</td>
<td>1</td>
<td>1.5</td>
<td>ms</td>
</tr>
<tr>
<td>UV, OV</td>
<td>$V_{UV}$</td>
<td>UV Input Threshold Voltage</td>
<td>UV Falling $\rightarrow \Delta V_{GATE} = 0\text{V}$</td>
<td>● 492.5</td>
<td>500</td>
<td>507.5</td>
</tr>
<tr>
<td></td>
<td>$V_{OV}$</td>
<td>OV Input Threshold Voltage</td>
<td>OV Rising $\rightarrow \Delta V_{GATE} = 0\text{V}$</td>
<td>● 492.5</td>
<td>500</td>
<td>507.5</td>
</tr>
<tr>
<td></td>
<td>$V_{UVHYST}$</td>
<td>UV Input Hysteresis</td>
<td></td>
<td>● 20</td>
<td>25</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>$V_{OVHYST}$</td>
<td>OV Input Hysteresis</td>
<td></td>
<td>● 20</td>
<td>25</td>
<td>32</td>
</tr>
<tr>
<td></td>
<td>$I_{LEAK}$</td>
<td>UV, OV Leakage Current</td>
<td>$V = 0.5\text{V}, V_{IN} = 34\text{V}$</td>
<td>● ±10</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$t_{FAULT}$</td>
<td>UV, OV Fault Propagation Delay</td>
<td>Overdrive $= 50\text{mV}$ $V_{IN} = V_{OUT} = 12\text{V}$</td>
<td>● 1</td>
<td>2</td>
<td></td>
</tr>
<tr>
<td>SHDN</td>
<td>$V_{SHDN}$</td>
<td>SHDN Input Threshold</td>
<td>SHDN Falling to $\Delta V_{GATE} = 0\text{V}$</td>
<td>● 0.4</td>
<td>0.75</td>
<td>1.2</td>
</tr>
<tr>
<td></td>
<td>$I_{SHDN}$</td>
<td>SHDN Input Current</td>
<td>$SHDN = 0.75\text{V}, V_{IN} = 34\text{V}$</td>
<td>● ±10</td>
<td></td>
<td></td>
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<tr>
<td></td>
<td>$I_{START}$</td>
<td>Delay Coming Out of Shutdown Mode</td>
<td>$SHDN = 0.75\text{V}, V_{IN} = 34\text{V}$</td>
<td>● 400</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{SHDN(F)}$</td>
<td>SHDN to FAULT Asserted</td>
<td>$V_{IN} = V_{OUT} = 12\text{V}$</td>
<td>● 1.5</td>
<td>3</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{LOWPWR}$</td>
<td>Delay from Turn Off to Low Power Operation</td>
<td>$V_{IN} = V_{OUT} = 12\text{V}$</td>
<td>● 26</td>
<td>36</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>● 0.3</td>
<td>0.7</td>
<td>2</td>
<td>ms</td>
</tr>
<tr>
<td>FAULT</td>
<td>$V_{OL}$</td>
<td>FAULT Output Voltage Low</td>
<td>$I_{FAULT} = 500\mu\text{A}$</td>
<td>● 0.15</td>
<td>0.4</td>
<td></td>
</tr>
<tr>
<td></td>
<td>$I_{FAULT}$</td>
<td>FAULT Leakage Current</td>
<td>$FAULT = 5\text{V}, V_{IN} = 34\text{V}$</td>
<td>● ±20</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note 1.** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2.** All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

**Note 3.** These pins can be tied to voltages below –0.3V through a resistor that limits the current below 1mA.

**Note 4.** The GATE pin is referenced to $V_{OUT}$ and does not exceed 44V for the entire operating range.
LTC4365

TYPICAL PERFORMANCE CHARACTERISTICS

UV Threshold vs Temperature

OV Threshold vs Temperature

UV/OV Leakage vs Temperature

UV/OV Propagation Delay vs Overdrive

Recovery Delay Time vs Temperature

LTC4365 Recovery Delay Time vs VIN

UV Threshold vs Temperature

OV Threshold vs Temperature

UV/OV Leakage vs Temperature

UV Threshold vs Temperature

Typical performance characteristics for the LTC4365 include:

- **UV Threshold vs Temperature**: Showcases the UV threshold voltage for different temperatures. The graph indicates a linear increase in UV threshold voltage as temperature decreases.

- **OV Threshold vs Temperature**: Similarly, this graph illustrates the OV threshold voltage for varying temperatures, showing a linear increase as temperature rises.

- **UV/OV Leakage vs Temperature**: Displays the leakage current at different temperatures, with a noticeable increase at higher temperatures.

- **UV/OV Propagation Delay vs Overdrive**: The propagation delay changes as a function of overdrive, with a clear decrease as overdrive increases.

- **Recovery Delay Time vs Temperature**: Recovery delay time is depicted for different temperatures, showing a significant increase at higher temperatures.

- **LTC4365 Recovery Delay Time vs VIN**: Recovery delay time varies with the input voltage (VIN), increasing as VIN rises.

- **Turn-On Timing**: Demonstrates the transition from SHDN to VOUT as the gate voltage changes, with a clear rise in VOUT as the gate voltage increases.

- **Turn-Off Timing**: Illustrates the transition from VOUT to SHDN as the gate voltage decreases, showing a smooth fall in VOUT.

For more information, visit www.linear.com/LTC4365
PIN FUNCTIONS

Exposed Pad: Connect to device ground.

FAULT: Fault Indication Output. This high voltage open drain output is pulled low if UV is below its monitor threshold, if OV is above its monitor threshold, if SHDN is low, or if VIN has not risen above VIN(UVLO).

GATE: Gate Drive Output for External N-channel MOSFETs. An internal charge pump provides 20μA of pull-up current and up to 9.8V of enhancement to the gate of an external N-channel MOSFET.

When turned off, GATE is pulled just below the lower of VIN or VOUT. When VIN goes negative, GATE is automatically connected to VIN.

GND: Device Ground.

OV: Overvoltage Comparator Input. Connect this pin to an external resistive divider to set the desired VIN overvoltage fault threshold. Input to an accurate, fast (1μs) comparator with a 0.5V rising threshold and 25mV of hysteresis. When OV rises above its threshold, a 50mA current sink pulls down on the GATE output. When OV falls back below 0.475V, and after a 36ms recovery delay waiting period (1ms for LTC4365-1), the GATE charge pump is enabled. The low leakage current of the OV input allows the use of large valued resistors for the external resistive divider. Connect to GND if unused.

SHDN: Shutdown Control Input. SHDN high enables the GATE charge pump which in turn enhances the gate of an external N-channel MOSFET. A low on SHDN generates a pull down on the GATE output with a 90μA current sink and places the LTC4365 in low current mode (10μA). If unused, connect to VIN. If VIN goes below ground, or if VIN goes to 60V, use a current limiting resistor of at least 100k.

UV: Undervoltage Comparator Input. Connect this pin to an external resistive divider to set the desired VIN undervoltage fault threshold. Input to an accurate, fast (1μs) comparator with a 0.5V falling threshold and 25mV of hysteresis. When UV falls below its threshold, a 50mA current sink pulls down on the GATE output. When UV rises back above 0.525V, and after a 36ms recovery delay waiting period (1ms for LTC4365-1), the GATE charge pump is enabled. The low leakage current of the UV input allows the use of large valued resistors for the external resistive divider. If unused, connect to VIN. While connected to VIN, if VIN goes below ground, or if VIN rings to 60V, use a current limiting resistor of at least 100k.

VIN: Power Supply Input. Maximum protection range: −40V to 60V. Operating range: 2.5V to 34V.

VOUT: Output Voltage Sense Input. This pin senses the voltage at the output side of the external N-channel MOSFET. The GATE charge pump voltage is referenced to VOUT. It is used as the charge pump input when VOUT is greater than approximately 6.5V.
Many of today’s electronic systems get their power from external sources such as wall wart adapters, batteries and custom power supplies. A typical supply arrangement for a portable product is shown by the operational diagram in Figure 1. Power is supplied by an AC adaptor or, if the plug is withdrawn, by a removable battery. Trouble arises when any of the following occurs:

- The battery is installed backwards
- An AC adaptor of opposite polarity is attached
- An AC adaptor of excessive voltage is attached
- The battery is discharged below a safe level

This can lead to supply voltages that are too high, too low, or even negative. If these power sources are applied directly to the electronic systems, the systems could be subject to damage. The LTC4365 is an input voltage fault protection N-channel MOSFET controller. The part isolates an input supply from its load to protect the load from unexpected supply voltage conditions, while providing a low loss path for qualified power.

To protect electronic systems from improperly connected power supplies, system designers will often add discrete diodes, transistors and high voltage comparators. The high voltage comparators enable system power only if the input supply falls within a desired voltage window. A Schottky diode or P-channel MOSFET typically added in series with the supply protects against reverse supply connections.

The LTC4365 provides accurate overvoltage and under-voltage comparators to ensure that power is applied to
OPERATION

The LTC4365 is an N-channel MOSFET controller that protects a load from faulty supply connections. A basic application circuit using the LTC4365 is shown in Figure 2. The circuit provides a low loss connection from \( V_{IN} \) to \( V_{OUT} \) as long as the voltage at \( V_{IN} \) is between 3.5V and 18V. Voltages at \( V_{IN} \) outside of the 3.5V to 18V range are prevented from getting to the load and can be as high as 60V and as low as –40V. The circuit of Figure 2 protects against negative voltages at \( V_{IN} \) as shown. No other external components are needed.

During normal operation, the LTC4365 provides up to 9.8V of gate enhancement to the external back-to-back N-channel MOSFETs. This turns on the MOSFET, thus connecting the load at \( V_{OUT} \) to the supply at \( V_{IN} \).

GATE Drive

The LTC4365 turns on the external N-channel MOSFETs by driving the GATE pin above \( V_{OUT} \). The voltage difference between the GATE and \( V_{OUT} \) pins (gate drive) is a function of \( V_{IN} \) and \( V_{OUT} \).
APPLICATIONS INFORMATION

Figure 3 highlights the dependence of the gate drive on $V_{IN}$ and $V_{OUT}$. When system power is first turned on (SHDN low to high, $V_{OUT} = 0$V), gate drive is at a maximum for all values of $V_{IN}$. This helps prevent start-up problems into heavy loads by ensuring that there is enough gate drive to support the load.

As $V_{OUT}$ ramps up from 0V, the absolute value of the GATE voltage remains fixed until $V_{OUT}$ is greater than the lower of $(V_{IN} - 1V)$ or 6V. Once $V_{OUT}$ crosses this threshold, gate drive begins to increase up to a maximum of 9.8V (for $V_{IN} \geq 12V$). The curves of Figure 3 were taken with a GATE load of $-1\mu A$. If there were no load on GATE, the gate drive for each $V_{IN}$ would be slightly higher.

Note that when $V_{IN}$ is at the lower end of the operating range, the external N-channel MOSFET must be selected with a corresponding lower threshold voltage.

![Figure 3. Gate Drive (GATE – VOUT) vs VOUT](image)

Table 1 lists some external MOSFETs compatible with different $V_{IN}$ supply voltages.

<table>
<thead>
<tr>
<th>$V_{IN}$</th>
<th>MOSFET</th>
<th>$V_{TH(MAX)}$</th>
<th>$V_{GS(MAX)}$</th>
<th>$V_{DS(MAX)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5V</td>
<td>SIB914</td>
<td>0.8V</td>
<td>5V</td>
<td>8V</td>
</tr>
<tr>
<td>3.3V</td>
<td>SI5920</td>
<td>1.0V</td>
<td>5V</td>
<td>8V</td>
</tr>
<tr>
<td>5V</td>
<td>SI7940</td>
<td>1.5V</td>
<td>8V</td>
<td>12V</td>
</tr>
<tr>
<td>$\leq 30V$</td>
<td>S14214</td>
<td>3.0V</td>
<td>20V</td>
<td>30V</td>
</tr>
<tr>
<td>$\leq 60V$</td>
<td>S19945</td>
<td>3.0V</td>
<td>20V</td>
<td>60V</td>
</tr>
</tbody>
</table>

Overvoltage and Undervoltage Protection

The LTC4365 provides two accurate comparators to monitor for overvoltage (OV) and undervoltage (UV) conditions at $V_{IN}$. If the input supply rises above the user adjustable OV threshold, the gate of the external MOSFET is quickly turned off, thus disconnecting the load from the input. Similarly, if the input supply falls below the user adjustable UV threshold, the gate of the external MOSFET also is quickly turned off. Figure 4 shows a UV/OV application for an input supply of 12V.

![Figure 4. UV, OV Comparators Monitor 12V Supply](image)

The external resistive divider allows the user to select an input supply range that is compatible with the load at $V_{OUT}$. Furthermore, the UV and OV inputs have very low leakage currents (typically $< 1nA$ at 100°C), allowing for large values in the external resistive divider. In the application of Figure 4, the load is connected to the supply only if $V_{IN}$ lies between 3.5V and 18V. In the event that $V_{IN}$ goes above 18V or below 3.5V, the gate of the external N-channel MOSFET is immediately discharged with a 50mA current sink, thus isolating the load from the supply.
APPLICATIONS INFORMATION

Figure 5 shows the timing associated with the UV pin. Once a UV fault propagates through the UV comparator \((t_{FAULT})\), the FAULT output is asserted low and a 50mA current sink discharges the GATE pin. As \(V_{OUT}\) falls, the GATE pin tracks \(V_{OUT}\).

![Figure 5. UV Timing (OV < (OV - OVHYST), SHDN > 1.2V)](image)

Procedure for Selecting UV/OV External Resistor Values

The following 3-step procedure helps select the resistor values for the resistive divider of Figure 4. This procedure minimizes UV and OV offset errors caused by leakage currents at the respective pins.

1. Choose maximum tolerable offset at the UV pin, \(V_{OS(UV)}\). Divide by the worst case leakage current at the UV pin, \(I_{UV}\) (10nA). Set the sum of \(R_1 + R_2\) equal to \(V_{OS(UV)}\) divided by 10nA. Note that due to the presence of \(R_3\), the actual offset at UV will be slightly lower:

\[
R_1 + R_2 = \frac{V_{OS(UV)}}{I_{UV}}
\]

2. Select the desired \(V_{IN}\) UV trip threshold, \(UV_{TH}\). Find the value of \(R_3\):

\[
R_3 = \frac{V_{OS(UV)}}{I_{UV}} \left( \frac{UV_{TH} - 0.5V}{0.5V} \right)
\]

3. Select the desired \(V_{IN}\) OV trip threshold, \(OV_{TH}\). Find the values of \(R_1\) and \(R_2\):

\[
R_1 = \left( \frac{V_{OS(UV)}}{I_{UV}} \right) + R_3 - 0.5V
\]

\[
R_2 = \frac{V_{OS(UV)}}{I_{UV}} - R_1 - OV_{TH}
\]

The example of Figure 4 uses standard 1% resistor values. The following parameters were selected:

- \(V_{OS(UV)} = 3mV\)
- \(I_{UV} = 10nA\)
- \(UV_{TH} = 3.5V\)
- \(OV_{TH} = 18V\)

When both the UV and OV faults are removed, the external MOSFET is not immediately turned on. The input supply must remain within the user selected power good window for at least 36ms \((t_{RECOVERY})\) before the load is again connected to the supply. This recovery timeout period filters noise (including line noise) at the input supply and prevents chattering of power at the load. For applications that require faster turn-on after a fault, the LTC4365-1 provides a 1ms recovery timeout period.

![Figure 6. OV Timing (UV > (UV + UVHYST), SHDN > 1.2V)](image)
The resistor values can then be solved:

1. \( R_1 + R_2 = \frac{3\text{mV}}{10\text{nA}} = 300k \)

2. \( R_3 = 2 \cdot \frac{3\text{mV}}{10\text{nA}} \cdot (3.5V - 0.5V) = 1.8M \)

The closest 1% value: \( R_3 = 1.82M \):

3. \( R_1 = \frac{300k + 1.82M}{2 \cdot 18V} = 58.9k \)

The closest 1% value: \( R_1 = 59k \):

\( R_2 = 300k - 59k = 241k \)

The closest 1% value: \( R_2 = 243k \)

Therefore: \( OV = 17.93V, UV = 3.51V \).

Reverse \( V_{IN} \) Protection

The LTC4365’s rugged and hot-swappable \( V_{IN} \) input helps protect the more sensitive circuits at the output load. If the input supply is plugged in backwards, or a negative supply is inadvertently connected, the LTC4365 prevents this negative voltage from passing to the output load.

The LTC4365 employs a novel, high speed reverse supply voltage monitor. When the negative \( V_{IN} \) voltage is detected, an internal switch connects the gates of the external back-to-back N-channel MOSFETs to the negative input supply.

As shown in Figure 7, external back-to-back N-channel MOSFETs are required for reverse supply protection. When \( V_{IN} \) goes negative, the reverse \( V_{IN} \) comparator closes the internal switch, which in turn connects the gates of the external MOSFETs to the negative \( V_{IN} \) voltage. The body diode (D1) of M1 turns on, but the body diode (D2) of M2 remains in reverse blocking mode. This means that the common source connection of M1 and M2 remains about a diode drop higher than \( V_{IN} \). Since the gate voltage of M2 is shorted to \( V_{IN} \), M2 will be turned off and no current can flow from \( V_{IN} \) to the load at \( V_{OUT} \). Note that the voltage rating of M2 must withstand the reverse voltage excursion at \( V_{IN} \).

Figure 8 illustrates the waveforms that result when \( V_{IN} \) is hot plugged to –20V. \( V_{IN}, \text{ GATE and } V_{OUT} \) start out at ground just before the connection is made. Due to the parasitic inductance of the \( V_{IN} \) and GATE connections, the voltage at the \( V_{IN} \) and GATE pins ring significantly below –20V. Therefore, a 40V N-channel MOSFET was selected to survive the overshoot.

The speed of the LTC4365 reverse protection circuits is evident by how closely the GATE pin follows \( V_{IN} \) during the negative transients. The two waveforms are almost indistinguishable on the scale shown.

The trace at \( V_{OUT} \), on the other hand, does not respond to the negative voltage at \( V_{IN} \), demonstrating the desired reverse supply protection. The waveforms of Figure 8 were captured using a 40V dual N-channel MOSFET, a 10µF ceramic output capacitor and no load current on \( V_{OUT} \).
Recovery Timer

The LTC4365 has a recovery delay timer that filters noise at \( V_{IN} \) and helps prevent chatter at \( V_{OUT} \). After either an OV or UV fault has occurred, the input supply must return to the desired operating voltage window for at least 36ms (\( t_{RECOVERY} \)) in order to turn the external MOSFET back on as illustrated in Figure 5 and Figure 6. For applications that require faster turn-on after a fault, the LTC4365-1 provides a 1ms recovery timeout period.

Going out of and then back into fault in less than \( t_{RECOVERY} \) will keep the MOSFET off continuously. Similarly, coming out of shutdown (\( \text{SHDN} \) low to high) triggers an 800\( \mu \)s start-up delay timer (see Figure 11).

The recovery timer is also active while the part is powering up. The recovery timer starts once \( V_{IN} \) rises above \( V_{IN(UVLO)} \) and \( V_{IN} \) lies within the user selectable UV/OV power good window. See Figure 9.

Fault Status

The \( \text{FAULT} \) high voltage open drain output is driven low if \( \text{SHDN} \) is asserted low, if \( V_{IN} \) is outside the desired UV/OV voltage window, or if \( V_{IN} \) has not risen above \( V_{IN(UVLO)} \). Figure 5, Figure 6 and Figure 11 show the \( \text{FAULT} \) output timing.

Gentle Shutdown

The \( \text{SHDN} \) input turns off the external MOSFETs in a gentle, controlled manner. When \( \text{SHDN} \) is asserted low, a 90\( \mu \)A current sink slowly begins to turn off the external MOSFETs.

Once the voltage at the GATE pin falls below the voltage at the \( V_{OUT} \) pin, the current sink is throttled back and a feedback loop takes over. This loop forces the GATE voltage to track \( V_{OUT} \), thus keeping the external MOSFETs off as \( V_{OUT} \) decays. Note that when \( V_{OUT} < 4.5V \), the GATE pin is pulled to within 400mV of ground.

Gentle gate turn off reduces load current slew rates and mitigates voltage spikes due to parasitic inductances. To further decrease GATE pin slew rate, place a capacitor across the gate and source terminals of the external MOSFETs. The waveforms of Figure 10 were captured using the Si4214 dual N-channel MOSFETs, and a 2A load with 100\( \mu \)F output capacitor.

Select Between Two Input Supplies

With the part in shutdown, the \( V_{IN} \) and \( V_{OUT} \) pins can be driven by separate power supplies. The LTC4365 then automatically drives the GATE pin just below the lower of \( V_{IN} \) and \( V_{OUT} \). The LTC4365 has a recovery delay timer that filters noise at \( V_{IN} \) and helps prevent chatter at \( V_{OUT} \). After either an OV or UV fault has occurred, the input supply must return to the desired operating voltage window for at least 36ms (\( t_{RECOVERY} \)) in order to turn the external MOSFET back on as illustrated in Figure 5 and Figure 6. For applications that require faster turn-on after a fault, the LTC4365-1 provides a 1ms recovery timeout period.

Going out of and then back into fault in less than \( t_{RECOVERY} \) will keep the MOSFET off continuously. Similarly, coming out of shutdown (\( \text{SHDN} \) low to high) triggers an 800\( \mu \)s start-up delay timer (see Figure 11).

The recovery timer is also active while the part is powering up. The recovery timer starts once \( V_{IN} \) rises above \( V_{IN(UVLO)} \) and \( V_{IN} \) lies within the user selectable UV/OV power good window. See Figure 9.

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The \( \text{FAULT} \) high voltage open drain output is driven low if \( \text{SHDN} \) is asserted low, if \( V_{IN} \) is outside the desired UV/OV voltage window, or if \( V_{IN} \) has not risen above \( V_{IN(UVLO)} \). Figure 5, Figure 6 and Figure 11 show the \( \text{FAULT} \) output timing.

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Gentle gate turn off reduces load current slew rates and mitigates voltage spikes due to parasitic inductances. To further decrease GATE pin slew rate, place a capacitor across the gate and source terminals of the external MOSFETs. The waveforms of Figure 10 were captured using the Si4214 dual N-channel MOSFETs, and a 2A load with 100\( \mu \)F output capacitor.

Select Between Two Input Supplies

With the part in shutdown, the \( V_{IN} \) and \( V_{OUT} \) pins can be driven by separate power supplies. The LTC4365 then automatically drives the GATE pin just below the lower of \( V_{IN} \) and \( V_{OUT} \).
the two supplies, thus turning off the external back-to-back MOSFETs. The application of Figure 12 uses two LTC4365s to select between two power supplies. Care should be taken to ensure that only one of the two LTC4365s is enabled at any given time.

Limiting Inrush Current During Turn-On

The LTC4365 turns on the external N-channel MOSFET with a 20µA current source. The maximum slew rate at the GATE pin can be reduced by adding a capacitor on the GATE pin:

\[
\text{Slew Rate} = \frac{20\mu A}{C_{\text{GATE}}}
\]

Since the MOSFET acts like a source follower, the slew rate at V_OUT equals the slew rate at GATE.

Therefore, inrush current is given by:

\[
I_{\text{INRUSH}} = \frac{C_{\text{OUT}}}{C_{\text{GATE}}} \cdot 20\mu A
\]

For example, a 1A inrush current to a 330µF output capacitance requires a GATE capacitance of:

\[
C_{\text{GATE}} = \frac{20\mu A \cdot C_{\text{OUT}}}{I_{\text{INRUSH}}} = \frac{20\mu A \cdot 330\mu F}{1A} = 6.6nF
\]

The 6.8nF C_{\text{GATE}} capacitor in the application circuit of Figure 14 limits the inrush current to approximately 1A. R_{\text{GATE}} makes sure that C_{\text{GATE}} does not affect the fast GATE turn off characteristics during UV/OV faults, or during reverse V_IN connection. R4A and R4B help prevent high frequency oscillations with the external N-channel MOSFET and related board parasitics.

Single MOSFET Application

When reverse V_IN protection is not needed, only a single external N-channel MOSFET is necessary. The application circuit of Figure 13 connects the load to V_IN when V_IN is less than 30V, and uses the minimal set of external components.

Figure 12. Selecting One of Two Supplies

Figure 13. Small Footprint Single MOSFET Application Protects Against 60V

Figure 14. Limiting Inrush Current with C_{\text{GATE}}
**APPLICATIONS INFORMATION**

**Transients During OV Fault**

The circuit of Figure 15 was used to display transients during an overvoltage condition. The nominal input supply is 24V and it has an overvoltage threshold of 30V. The parasitic inductance is that of a 1 foot wire (roughly 300nH). Figure 16 shows the waveforms during an overvoltage condition at $V_{IN}$. These transients depend on the parasitic inductance and resistance of the wire along with the capacitance at the $V_{IN}$ node. D1 is an optional power clamp (TVS, Tranzorb) recommended for applications where the DC input voltage can exceed 24V and with large $V_{IN}$ parasitic inductance. No clamp was used to capture the waveforms of Figure 16. In order to maintain reverse supply protection, D1 must be a bi-directional clamp rated for at least 225W peak pulse power dissipation.

![Figure 15. OV Fault with Large $V_{IN}$ Inductance](image)

![Figure 16. Transients During OV Fault When No Tranzorb (TVS) Is Used](image)
Hysteretic Regulator

Built-in hysteresis and the availability of both inverting and noninverting control inputs (OV and UV) facilitate the design of hysteretic regulators. Figure 17 shows how the LTC4365-1 can protect a load from OV transients, while regulating the output voltage at a user-defined level. When the output voltage reaches its OV limit, the LTC4365-1 turns off the external MOSFETs. The load current then discharges the output capacitance until OV falls below the hysteresis voltage. The external MOSFETs are turned back on after a 1ms delay. Figure 18 shows the waveforms for the circuit of Figure 17. Note that the duration, magnitude and duty cycle of the VIN glitch must not exceed the SOA rating of the external MOSFETs.

Solar Charger

Figure 19 shows a series regulator for a solar charger. The LTC4365-1 connects the solar charger to the battery when the battery voltage falls below 13.9V (after a 1ms delay). Conversely, when the battery reaches 14.6V, the LTC4365-1 immediately (2µs) opens the charging path.

Regulation of the battery voltage is achieved by connecting a resistive divider from the battery to the accurate OV comparator input (with 5% hysteresis). The fast rising response of the OV comparator prevents the battery voltage from rising above the user-selected threshold.
APPLICATIONS INFORMATION

Note that during initial start-up, the LTC4365-1 will not turn on the external MOSFETs until a battery is first connected to the VIN pin. To begin operation, VIN must initially rise above the 2.2V UVLO lockout voltage. Connecting the battery ensures that the LTC4365-1 comes out of UVLO.

12V Application with 150V Transient Protection

Figure 20 shows a 12V application that withstands input supply transients up to 150V. When the input voltage exceeds 17.9V, the OV resistive divider turns off the external MOSFETs. As VIN rises to 150V, the gate of transistor M1 remains in the Off condition, thus preventing conduction from VIN to VOUT. Note that M1 must have an operating range above 150V.

Resistor R6 and diode D3 clamp the LTC4365 supply voltage to 50V. To prevent R6 from interfering with reverse operation, the recommended value is 1k or less. Note that the power handling capability of R6 must be considered in order to avoid overheating during transients. D3 is shown as a bidirectional clamp in order to achieve reverse-polarity protection at VIN. M2 is also required in order to protect VOUT from negative voltages at VIN and should have an operating range beyond the breakdown of D3. If reverse protection is not desired remove M2 and connect the source of M1 directly to VOUT.

MOSFET Selection

To protect against a negative voltage at VIN, the external N-channel MOSFETs must be configured in a back-to-back arrangement. Dual N-channel packages are thus the best choice. The MOSFET is selected based on its power handling capability, drain and gate breakdown voltages, and threshold voltage.

The drain to source breakdown voltage must be higher than the maximum voltage expected between VIN and VOUT. Note that if an application generates high energy transients during normal operation or during Hot Swap™, the external MOSFET must be able to withstand this transient voltage.

Due to the high impedance nature of the charge pump that drives the GATE pin, the total leakage on the GATE pin must be kept low. The gate drive curves of Figure 2 were measured with a 1µA load on the GATE pin. Therefore, the leakage on the GATE pin must be no greater than 1µA in order to match the curves of Figure 2. Higher leakage currents will result in lower gate drive. The dual N-channel MOSFETs shown in Table 1 all have a maximum GATE leakage current of 100nA. Additionally, Table 1 lists representative MOSFETs that would work at different values of VIN.

Layout Considerations

The trace length between the VIN pin and the drain of the external MOSFET should be minimized, as well as the trace length between the GATE pin of the LTC4365 and the gates of the external MOSFETs.

Place the bypass capacitors at VOUT as close as possible to the external MOSFET. Use high frequency ceramic capacitors in addition to bulk capacitors to mitigate Hot Swap ringing. Place the high frequency capacitors closest to the MOSFET. Note that bulk capacitors mitigate ringing by virtue of their ESR. Ceramic capacitors have low ESR and can thus ring near their resonant frequency.

Figure 20. 12V Application Protected from 150V Transients
LTC4365

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

**TS8 Package**

8-Lead Plastic TSOT-23

(Reference LTC DWG # 05-08-1637 Rev A)

**DDB Package**

8-Lead Plastic DFN (3mm × 2mm)

(Reference LTC DWG # 05-08-1702 Rev B)

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For more information www.linear.com/LTC4365
## REVISION HISTORY

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LTC4365 Protects Step Down Regulator from –30V to 30V VIN Faults

**PART NUMBER** | **DESCRIPTION** | **COMMENTS**
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LT4363 | Surge Stopper Overvoltage/Overcurrent Protection Regulator | Wide Operating Range: 4V to 80V, Reverse Protection to –60V, Adjustable Output Clamp Voltage
LTC4364 | Surge Stopper with Ideal Diode | 4V to 80V Operation, –40V Reverse Input, –20V Reverse Output
LTC4366 | Floating Surge Stopper | 9V to >500V Operation, 8-Pin TSOT and 3mm × 2mm DFN Packages
LTC4361 | Overvoltage/Overcurrent Protection Controllers | 5.8V Overvoltage Threshold, 85V Absolute Maximum
LTC2909 | Triple/Dual Inputs UV/OV Negative Monitor | Pin Selectable Input Polarity Allows Negative and OV Monitoring
LTC2912/LTC2913 | Single/Dual UV/OV Voltage Monitor | Ads UV and OV Trip Values, ±1.5% Threshold Accuracy
LTC2914 | Quad UV/OV Monitor | For Positive and Negative Supplies
LTC2955 | Pushbutton On/Off Controller | Automatic Turn-On, 1.5V to 36V Input, ±36V PB Input
LT4256 | Positive 48V Hot Swap Controller with Open-Circuit Detect | Foldback Current Limiting, Open-Circuit and Overcurrent Fault Output, Up to 80V Supply
LTC4260 | Positive High Voltage Hot Swap Controller with ADC and I²C | Wide Operating Range 8.5V to 80V
LTC4352 | Ideal MOSFET ORing Diode | External N-Channel MOSFETS Replace ORing Diodes, 0V to 18V
LTC4354 | Negative Voltage Diode-OR Controller | Controls Two N-Channel MOSFETS, 1.2µs Turn-Off, –80V Operation
LTC4355 | Positive Voltage Diode-OR Controller | Controls Two N-Channel MOSFETS, 0.4µs Turn-Off, 80V Operation
LT1913 | Step-Down Switching Regulator | 3.6V to 25V Input, 3.5A Maximum Current, 200kHz to 2.4MHz