**FEATURES**

- Bidirectional Buffer with Stuck Bus Recovery
- 60mV Buffer Offset Independent of Load
- 30ms Stuck Bus Timeout
- Compatible with Non-Compliant \( V_{OL} \) I²C Devices
- Prevents SDA and SCL Corruption During Live Board Insertion and Removal from Backplane
- ±5kV Human Body Model ESD Protection
- Isolates SDA and SCL Line from Output
- Compatible with I²C™, I²C Fast Mode and SMBus
- READY Open-Drain Output
- 1V Precharge on All SDA and SCL Lines
- High Impedance SDA, SCL Pins for \( V_{CC} = 0V \)
- Small 8-Lead (3mm × 3mm) DFN and 8-Lead MSOP Packages

**APPLICATIONS**

- Live Board Insertion
- Servers
- Capacitance Buffer/Bus Extender
- RAID Systems
- ATCA

**DESCRIPTION**

The LTC®4307 hot swappable, 2-wire bus buffer allows I/O card insertion into a live backplane without corruption of the data and clock busses. The LTC4307 provides bidirectional buffering, keeping the backplane and card capacitances isolated. Low offset and high \( V_{OL} \) tolerance allows multiple devices to be cascaded on the clock and data busses. If SDAOUT or SCLOUT are low for 30ms, the LTC4307 will automatically break the bus connection. At this time the LTC4307 automatically generates up to 16 clock pulses on SCLOUT in an attempt to free the bus. A connection will resume if the stuck bus is cleared.

During insertion, the SDA and SCL lines are pre-charged to 1V to minimize bus disturbances. When driven high, the ENABLE input allows the LTC4307 to connect after a stop bit or bus idle. Driving ENABLE low breaks the connection between SDAIN and SDAOUT, SCLIN and SCLOUT. READY is an open-drain output which indicates that the backplane and card sides are connected.

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**TYPICAL APPLICATION**

![Typical Application Diagram](image)

**Rising Edge from Asserted Low**

![Rising Edge Graph](image)
# LTC4307

## Absolute Maximum Ratings (Notes 1, 7)

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Conditions</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Units</th>
</tr>
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<tr>
<td>VCC Positive Supply Voltage</td>
<td></td>
<td>2.3</td>
<td>5.5</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>ICC Supply Current</td>
<td>VCC = 5.5V, VSDAOUT = 0V (Note 6)</td>
<td>8</td>
<td>11</td>
<td></td>
<td>mA</td>
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<tr>
<td>ISD Shutdown Supply Current</td>
<td>VCC = 5.5V, ENABLE = GND, SDA, SCL = 5.5V</td>
<td>900</td>
<td>1200</td>
<td></td>
<td>μA</td>
</tr>
<tr>
<td>VPRE Precharge Voltage</td>
<td>SDA, SCL Floating</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>VPRE Precharge Voltage</td>
<td>SDA, SCL Floating</td>
<td>0.8</td>
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<tr>
<td>VPRE Precharge Voltage</td>
<td>SDA, SCL Floating</td>
<td>0.8</td>
<td>1</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>VTH_ENABLE ENABLE Threshold</td>
<td></td>
<td>0.8</td>
<td>1.4</td>
<td>2</td>
<td>V</td>
</tr>
<tr>
<td>IENABLE ENABLE Input Current</td>
<td>ENABLE from 0V to VCC</td>
<td>0.1</td>
<td>±5</td>
<td></td>
<td>μA</td>
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<tr>
<td>tPLH_EN ENABLE Delay Off-On</td>
<td>VCC = 3.3V (Figure 1)</td>
<td></td>
<td></td>
<td>95</td>
<td>μs</td>
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<tr>
<td>tPHL_EN ENABLE Delay Off-On</td>
<td>VCC = 3.3V (Note 3) (Figure 1)</td>
<td>10</td>
<td></td>
<td>ns</td>
<td></td>
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<tr>
<td>tPLH_READY READY Delay Off-On</td>
<td>VCC = 3.3V (Note 3) (Figure 1)</td>
<td>10</td>
<td></td>
<td>ns</td>
<td></td>
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<tr>
<td>tPHL_READY READY Delay Off-On</td>
<td>VCC = 3.3V (Note 3) (Figure 1)</td>
<td>10</td>
<td></td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>VOL_READY READY Output Low Voltage</td>
<td>IPUllUp = 3mA, VCC = 2.3V</td>
<td></td>
<td></td>
<td>0.4</td>
<td>V</td>
</tr>
<tr>
<td>IOFF_READY READY Off Leakage Current</td>
<td>VCC = READY = 5.5V</td>
<td></td>
<td></td>
<td>0.1</td>
<td>μA</td>
</tr>
</tbody>
</table>

## Operating Temperature Range
- **LTC4307C**: 0°C to 70°C
- **LTC4307I**: -40°C to 85°C

## Electrical Characteristics

- **TJMAX = 125°C**, **θJA = 43°C/W**
- **TJMAX = 125°C**, **θJA = 200°C/W**

## Package/Order Information

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<tr>
<th>ORDER PART NUMBER</th>
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<td>LTC4307CDD</td>
<td>LTC4307CMS8</td>
</tr>
<tr>
<td>LTC4307IDD</td>
<td>LTC4307IMS8</td>
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Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.*
## Electrical Characteristics

The symbol denotes the specifications which apply over the full operating temperature range, otherwise specifications are at \( T_A = 25^\circ C \). \( V_{CC} = 3.3V \), unless otherwise noted.

### Symbol | Parameter | Conditions | Min | Typ | Max | Units
--- | --- | --- | --- | --- | --- | ---
| \( t_{PHL} \) | SDA/SCL Propagation Delay High to Low | \( C_{LOAD} = 50pF, 2.7k \) to \( V_{CC} \) on SDA, SCL, \( V_{CC} = 3.3V \) (Notes 2, 3) (Figure 1) | 70 | ns | | |
| \( t_{PLH} \) | SDA/SCL Propagation Delay Low to High | \( C_{LOAD} = 50pF, 2.7k \) to \( V_{CC} \) on SDA, SCL, \( V_{CC} = 3.3V \) (Notes 2, 3) (Figure 1) | 10 | ns | | |
| \( t_{RISE} \) | SDA/SCL Transition Time Low to High | \( C_{LOAD} = 100pF, 10k \) to \( V_{CC} \) on SDA, SCL, \( V_{CC} = 3.3V \) (See Notes 3, 4) (Figure 1) | 30 | 300 | ns | |
| \( t_{FALL} \) | SDA/SCL Transition Time High to Low | \( C_{LOAD} = 100pF, 10k \) to \( V_{CC} \) on SDA, SCL, \( V_{CC} = 3.3V \) (See Notes 3, 4) (Figure 1) | 30 | 300 | ns | |
| \( I_{PULLUPAC} \) | Transient Boosted Pull-Up Current | Positive Transition on SDA, SCL, \( V_{CC} = 3.3V \) (Note 5) | 5 | 8 | mA | |

### Input-Output Connection

- \( V_{OS} \): Input-Output Offset Voltage
  - \( 2.7k \) to \( V_{CC} \) on SDA, SCL, \( V_{CC} = 3.3V \), Driven SDA/SCL = 0.2V
  - \( \bullet \) 20 | 60 | 100 | mV |
- \( V_{THR} \): SDA, SCL Logic Input Threshold Voltage Rising Edge
  - \( 0.45V_{CC} \) | 0.55V_{CC} | 0.65V_{CC} | V |
- \( V_{HYS} \): SDA, SCL Logic Input Threshold Voltage Hysteresis
  - (Note 3)
  - 50 | mV |
- \( C_{IN} \): Digital Input Capacitance SDAIN, SDAOUT, SCLIN, SCLOUT
  - (Note 3)
  - 10 | pF |
- \( I_{LEAK} \): Input Leakage Current SDA, SCL, Pins
  - (Note 3)
  - ±5 | μA |
- \( V_{OL} \): Output Low Voltage
  - SDA, SCL Pins, \( I_{SINK} = 4mA \), Driven SDA/SCL = 0.2V, \( V_{CC} = 2.7V \)
  - (Note 3)
  - 0 | 0.4 | V |
  - 2.7k to \( V_{CC} \) on SDA, SCL, \( V_{CC} = 3.3V \), Driven SDA/SCL = 0.1V
  - 120 | 160 | 205 | mV |
- \( V_{IL\text{MAX}} \): Buffer Input Logic Low Voltage
  - \( V_{CC} = 3.3V \)
  - (Note 3)
  - 1.2 | V |

### Bus Stuck Low Timeout

- \( I_{\text{TIMEOUT}} \): Bus Stuck Low Timer
  - \( V_{CC} = 3.3V \), SDAOUT, SCLOUT = 0V
  - (Note 3)
  - 25 | 30 | 35 | ms |

### Timing Characteristics

- \( f_{I^2C,\text{MAX}} \): I2C Maximum Operating Frequency
  - (Note 3)
  - 400 | 600 | kHz |
- \( t_{BUF} \): Bus Free Time Between Stop and Start Condition
  - (Note 3)
  - 1.3 | μs |
- \( t_{HD,\text{STA}} \): Hold Time After (Repeated) Start Condition
  - (Note 3)
  - 100 | ns |
- \( t_{SUL,\text{STA}} \): Repeated Start Condition Set-Up Time
  - (Note 3)
  - 0 | ns |
- \( t_{SUL,\text{STO}} \): Stop Condition Set-Up Time
  - (Note 3)
  - 0 | ns |
- \( t_{HD,\text{DATI}} \): Data Hold Time Input
  - (Note 3)
  - 0 | ns |
- \( t_{SUL,\text{DAT}} \): Data Set-Up Time
  - (Note 3)
  - 100 | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** See “Propagation Delays” in the Operations section for a discussion of \( t_{PHL} \) and \( t_{PLH} \) as a function of pull-up resistance and bus capacitance.

**Note 3:** Determined by design, not tested in production.

**Note 4:** Measure points are 0.3 • \( V_{CC} \) and 0.7 • \( V_{CC} \). 

**Note 5:** \( I_{PULLUP} \) varies with temperature and \( V_{CC} \) voltage as shown in the Typical Performance Characteristics section.

**Note 6:** \( I_{CC} \) test performed with connection circuitry active.

**Note 7:** All currents into pins are positive; all voltages are referenced to GND unless otherwise specified.
ENABLE, CONNECT, READY Timing

Rising and Falling Propagation Delay and Rise and Fall Times for SDAIN, SDAOUT and SCLIN, SCLOUT

Figure 1. Timing Diagrams
**TYPICAL PERFORMANCE CHARACTERISTICS**  
$T_A = 25^\circ C$, $V_{CC} = 3.3V$, unless otherwise indicated.

- **$I_{CC}$ vs Temperature**
  
- **$I_{PULLUPAC}$ vs Temperature**
  
- **$I_{SD}$ vs Temperature**
  
- **Input-Output High to Low Propagation Delay vs Temperature**
  
- **Input-Output High to Low Propagation Delay vs $C_{OUT}$**
  
- **Connection Circuitry $V_{OUT} - V_{IN}$ ($V_{OS}$)**
  
- **Bus Stuck Low Timeout vs $V_{CC}$**
**PIN FUNCTIONS**

**ENABLE (Pin 1):** Connection Enable Input. This is a 1.4V digital threshold input pin. For normal operation pull or tie ENABLE high. Driving ENABLE below 0.8V isolates SDAIN from SDAOUT, SCLIN from SCLOUT and asserts READY low. A rising edge on ENABLE after a fault has occurred forces a connection between SDAIN, SDAOUT and SCLIN, SCLOUT. Connect to VCC if unused.

**SCLOUT (Pin 2):** Serial Clock Output. Connect this pin to an SCL bus segment where stuck bus recovery is needed. A pull-up resistor should be connected between this pin and VCC.

**SCLIN (Pin 3):** Serial Clock Input. Connect this pin to an SCL bus segment that needs to be isolated from stuck bus problems. A pull-up resistor should be connected between this pin and VCC.

**GND (Pin 4):** Device Ground. Connect this pin to a ground plane for best results.

**READY (Pin 5):** Connection READY Status Output. The READY pin is an open-drain N-channel MOSFET output that pulls low when ENABLE is low, or when the start-up and connection sequence described in the Operation section has not been completed. READY also goes low when the LTC4307 disconnects the inputs from the outputs due to the bus being stuck low for at least 30ms. READY goes high when ENABLE is high and a connection is made. Connect a pull-up resistor, typically 10k, from this pin to VCC to provide the pull-up. This pin can be floated if unused.

**SDAIN (Pin 6):** Serial Data Input. Connect this pin to an SDA bus segment that needs to be isolated from stuck bus problems. A pull-up resistor should be connected between this pin and VCC.

**SDAOUT (Pin 7):** Serial Data Output. Connect this pin to the SDA bus segment where stuck bus recovery is needed. A pull-up resistor should be connected between this pin and VCC.

**VCC (Pin 8):** Supply Voltage Input. Place a bypass capacitor of at least 0.01μF close to VCC for best results.

**Exposed Pad (Pin 9, DFN Package Only):** Exposed Pad may be left open or connected to device ground.
**OPERATION**

**Start-Up**

When the LTC4307 first receives power on its $V_{CC}$ pin, either during power-up or live insertion, it starts in an undervoltage lockout (UVLO) state, ignoring any activity on the SDA or SCL pins until $V_{CC}$ rises above 2V (typ). This is to ensure that the LTC4307 does not try to function until it has enough voltage to do so.

During this time, the 1V precharge circuitry is active and forces 1V through 100k nominal resistors to the SDA and SCL pins. Because the I/O card is being plugged into a live backplane, the voltage on the backplane SDA and SCL busses may be anywhere between 0V and $V_{CC}$. Precharging the SCL and SDA pins to 1V minimizes the worst-case voltage differential these pins will see at the
moment of connection, therefore minimizing the amount of disturbance caused by the I/O card.

Once the LTC4307 comes out of UVLO, it monitors both the backplane and card sides for either a stop bit or bus idle condition to indicate the completion of data transactions. When both sides are idle or one side has a stop bit condition while the other is idle, the input-to-output connection circuitry is activated, joining the SDA and SCL busses on the I/O card with those on the backplane. In addition, the precharge circuitry is deactivated and will not be reactivated unless the VCC voltage falls below the UVLO threshold.

Connection Circuitry

Once the connection circuitry is activated, the functionality of the SDAIN and SDAOUT pins is identical. A low forced on either pin at any time results in both pin voltages being low. The LTC4307 is tolerant of I2C bus DC logic low voltages up to the 0.3VCC VIL I2C specification.

When the LTC4307 senses a rising edge on the bus, it deactivates its pull-down devices for bus voltages as low as 0.48V and activates its accelerators. This methodology maximizes the effectiveness of the rise time accelerator circuitry and maintains compatibility with the other devices in the LTC4300 bus buffer family. Care must be taken to ensure that devices participating in clock stretching or arbitration force logic low voltages below 0.48V at the LTC4307 inputs.

SDAIN and SDAOUT enter a logic high state only when all devices on both SDAIN and SDAOUT release high. The same is true for SCLIN and SCLOUT. This important feature ensures that clock stretching, clock synchronization, arbitration and the acknowledge protocol always work, regardless of how the devices in the system are tied to the LTC4307.

Another key feature of the connection circuitry is that it provides bidirectional buffering, keeping the backplane and card capacitances isolated. Because of this isolation, the waveforms on the backplane busses look slightly different than the corresponding card bus waveforms as described here.

Input to Output Offset Voltage

When a logic low voltage, VLOW1, is driven on any of the LTC4307’s data or clock pins, the LTC4307 regulates the voltage on the opposite data or clock pins to a slightly higher voltage, typically 60mV above VLOW1. This offset is practically independent of pull-up current (see the Typical Performance curves).

Propagation Delays

During a rising edge, the rise time on each side is determined by the bus pull-up resistor and the equivalent capacitance on the line. If the pull-up resistors are the same, a difference in rise time occurs which is directly proportional to the difference in capacitance between the two sides. This effect is displayed in Figure 2 for VCC = 5.5V and a 10k pull-up resistor on each side (50pF on one side and 150pF on the other). Since the output side has less capacitance than the input, it rises faster and the effective propagation delay is negative.

There is a finite propagation delay through the connection circuitry for falling waveforms. Figure 3 shows the falling edge waveforms for the same pull-up resistors and equivalent capacitance conditions as used in Figure 2. An external N-channel MOSFET device pulls down the voltage on the side with 150pF capacitance; the LTC4307 pulls down the voltage on the opposite side with a delay of 80ns. This delay is always positive and is a function of supply voltage, temperature and the pull-up resistors and equivalent bus capacitances on both sides of the bus. The Typical Performance Characteristics section shows propagation delay as a function of temperature and voltage for 10k pull-up resistors and 50pF equivalent capacitance on both sides of the part. Also, the tPHL vs COUT curve for VCC = 5.5V shows that increasing the capacitance from 50pF to 150pF results in a tPHL increase from 81ns to 91ns. Larger output capacitances translate to longer delays (up to 125ns). Users must quantify the difference in propagation times for a rising edge versus a falling edge in their systems and adjust setup and hold times accordingly.
**OPERATION**

**Bus Stuck Low Timeout**

When SDAOUT or SCLOUT is low, an internal timer is started. The timer is only reset by that respective input going high. If it does not go high within 30ms (typical) the connection between SDAIN and SDAOUT, and between SCLIN and SCLOUT is broken. After at least 40µs, the LTC4307 automatically generates up to 16 clock pulses at 8.5kHz (typical) on SCLOUT in an attempt to unstick the bus. When the clock pulses are completed, a stop bit will be generated on SCLOUT and SDAOUT to reset any circuitry on that bus. When the low SDAOUT or SCLOUT pin goes high, a connection is enabled waiting for a stop bit or a bus idle to make a connection.

When powering up into a bus stuck low condition, the connection circuitry joining the SDA and SCL busses on the I/O card with those on the backplane is not activated and is only reset when SDAOUT and SCLOUT are high. 30ms after UVLO, automatic clocking takes place as described above.

**READY Digital Output**

This pin provides a digital flag which is low when either ENABLE is low, the start-up sequence described earlier in this section has not been completed, or the LTC4307 has disconnected due to a stuck bus condition. READY goes high when ENABLE is high and the backplane and card sides are connected. The pin is driven by an open-drain pull-down capable of sinking 3mA while holding 0.4V on the pin. Connect a resistor to $V_{CC}$ to provide the pull-up.

**ENABLE**

When the ENABLE pin is driven below 0.8V with respect to the LTC4307’s ground, the backplane side is disconnected from the card side and the READY pin is internally pulled low. When the pin is driven above 2V, the part waits for data transactions on both the backplane and card sides to be complete (as described in the Start-Up section) before connecting the two sides. At this time the internal pull-down on READY releases. When ENABLE is low, automatic clocking is disabled.

A rising edge on ENABLE after a bus stuck low condition has occurred forces a connection between SDAIN, SDAOUT, and SCLIN, SCLOUT even if the bus stuck low condition has not been cleared. At this time the 30ms timer is reset but not disabled.

**Rise Time Accelerators**

Once connection has been established, rise time accelerator circuits on all four SDA and SCL pins are enabled. During positive bus transitions, the rise time accelerators provide strong, slew-limited pull-up currents that make the bus voltage rise at a rate of 100V/µs. The rise time accelerators significantly improve system reliability in two ways. First, they provide smooth, controlled transitions during rising edges for both small and large systems. Because the accelerator pull-up impedance is significantly lower than the bus pull-up resistance, the system is much less susceptible to noise on rising edges. Second, the accelerators allow users to choose large bus pull-up resistors, reducing power consumption and improving logic low noise margin.

For these reasons, it is strongly recommended that users choose bus pull-up resistors so that the bus will rise on its own at a rate of at least 0.8V/µs to guarantee activation of the accelerators. The rise time accelerators are disabled until the sequence of events described in the start-up section has been completed. They are also disabled during automatic clocking.
**APPLICATIONS INFORMATION**

**Live Insertion and Capacitance Buffering Application**

Figures 4 and 5 illustrate applications of the LTC4307 that take advantage of the LTC4307’s Hot Swap™, capacitance buffering and precharge features. If the I/O cards were plugged directly into the backplane without the LTC4307 buffer, all of the backplane and card capacitances would add directly together, making rise-time and fall-time requirements difficult to meet. Placing an LTC4307 on the edge of each card, however, isolates the card capacitance from the backplane. For a given I/O card, the LTC4307 drives the capacitance of everything on the card and the backplane must drive only the capacitance of the LTC4307, which is less than 10pF.

In most applications the LTC4307 will be used with a staggered connector where VCC and GND will be long pins. SDA and SCL are medium length pins to ensure that the VCC and GND pins make contact first. This will allow the precharge circuitry to be activated on SDA and SCL before they make contact. ENABLE is a short pin that is pulled down when not connected. This is to ensure that the connection between the backplane and the card’s data and clock busses is not not enabled until the transients associated with live insertion have settled.

Figure 4 shows the LTC4307 in an application with a staggered connector. The LTC4307 receives its VCC voltage from one of the long “early power” pins. Establishing early power VCC ensures that the 1V precharge voltage is present at SDAIN and SCLIN before they make contact.

**Figure 4. The LTC4307 in an Application with a Staggered Connector**
The ENABLE pin is driven using a short pin. This is to ensure that a connection is not enabled until the transients associated with live insertion have settled.

Figure 5 shows the LTC4307 in an application where all of the pins have the same length. In this application a resistor is used to hold the ENABLE pin low during live insertion, until the backplane control circuitry can enable the device.

Repeater/Bus Extender Applications

Users who wish to connect two 2-wire systems separated by a distance can do so by connecting two LTC4307s back-to-back, as shown in Figure 6. The I²C specification allows for 400pF maximum bus capacitance, severely limiting the length of the bus. The SMBus specification places no restriction on bus capacitance, but the limited impedances of devices connected to the bus require systems to remain small if rise time and fall time specifications are to be met. In this situation, the differential ground voltage between the two systems may limit the allowed distance, because a valid logic-low voltage with respect to the ground at one end of the system may violate the allowed VOL specification with respect to the ground at the other end. In addition, the connection circuitry offset voltages of the back-to-back LTC4307s add together, directly contributing to the same problem.

Figure 7 further illustrates a repeater application. This circuit could be used in an AdvancedTCA system. In AdvancedTCA applications, the bus pull-up resistance on the backplane is quite small. Since there is no effect on the offset due to the pull-up impedance, multiple LTC4307 buffers can be used in a single system. This allows the user to divide the line and device capacitances into more sections with buffering and meet rise and fall times.

The LTC4307 disconnects when both bus I/Os are above 0.48V and rising. In systems with large ground bounce, if many devices are cascaded, the 0.48V threshold can be exceeded and the transients associated with the ground bounce can appear to be a rising edge. Under this condition, the LTC4307 with inputs above 0.48V may disconnect.
Systems with Supply Voltage Droop

In large 2-wire systems, the \(V_{CC}\) voltages seen by devices at various points in the system can differ by a few hundred millivolts or more. This situation is modeled by a series resistor in the \(V_{CC}\) line, as shown in Figure 8. For proper operation, make sure that the \(V_{CC(LTC4307)}\) is \(\geq 2.3\)V.

Figure 6. The LTC4307 in a Repeater/Bus Extender Application Where Two 2-Wire Systems are Separated by a Distance

Figure 7. The LTC4307 in a Repeater Application. The LTC4307's Low Offset Allows Cascading of Multiple Devices

Figure 8. System with Voltage Droop
TYPICAL APPLICATIONS

High VIL Application

Simplified ATCA IPMB Application
PACKAGE DESCRIPTION

DD Package
8-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1698)

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-1)
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON TOP AND BOTTOM OF PACKAGE

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

PACKAGE OUTLINE

BOTTOM VIEW—EXPOSED PAD

PIN 1 TOP MARK (NOTE 6)
MS8 Package
8-Lead Plastic MSOP
(Reference LTC DWG # 05-08-1660 Rev F)

RECOMMENDED SOLDER PAD LAYOUT

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.
**TYPICAL APPLICATION**

The LTC4307 in a Repeater Application. The LTC4307’s Low Offset Allows Cascading of Multiple Devices

**RELATED PARTS**

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<thead>
<tr>
<th>PART NUMBER</th>
<th>DESCRIPTION</th>
<th>COMMENTS</th>
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<tbody>
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<td>LTC1380/LTC1393</td>
<td>Single-Ended 8-Channel/Differential 4-Channel Analog MUX with SMBus Interface</td>
<td>Low RON: 35Ω Single Ended/70Ω Differential, Expandable to 32 Single or 16 Differential Channels</td>
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<tr>
<td>LTC1427-50</td>
<td>Micropower, 10-Bit Current Output DAC with SMBus Interface</td>
<td>Precision 50μA ±2.5% Tolerance Over Temperature, Four Selectable SMBus Addresses, DAC Powers Up at Zero or Midscale</td>
</tr>
<tr>
<td>LTC1623</td>
<td>Dual High Side Switch Controller with SMBus Interface</td>
<td>Eight Selectable Addresses/16-Channel Capability</td>
</tr>
<tr>
<td>LTC1663</td>
<td>SMBus Interface 10-Bit Rail-to-Rail Micropower DAC</td>
<td>DNL &lt; 0.75LSB Max, 5-Lead SOT-23 Package</td>
</tr>
<tr>
<td>LTC1694/LTC1694-1</td>
<td>SMBus Accelerator</td>
<td>Improved SMBus/I2C Rise Time, Ensures Data Integrity with Multiple SMBus/I2C Devices</td>
</tr>
<tr>
<td>LTC1695</td>
<td>SMBus/I2C Fan Speed Controller in ThinSOT™ Package</td>
<td>0.75Ω PMOS 180mA Regulator, 6-Bit DAC</td>
</tr>
<tr>
<td>LT1786F</td>
<td>SMBus Controlled CCFL Switching Regulator</td>
<td>1.25A, 200kHz Floating or Grounded Lamp Configurations</td>
</tr>
<tr>
<td>LTC1840</td>
<td>Dual I2C Fan Speed Controller</td>
<td>Two 100μA 8-Bit DACs, Two Tach Inputs, Four GPIO</td>
</tr>
<tr>
<td>LTC4301</td>
<td>Supply Independent Hot Swappable 2-Wire Bus Buffer</td>
<td>Supply Independent</td>
</tr>
<tr>
<td>LTC4301L</td>
<td>Hot Swappable 2-Wire Bus Buffer with Low Voltage Level Translation</td>
<td>Allows Bus Pull-Up Voltages as Low as 1V on SDAIN and SCLIN</td>
</tr>
<tr>
<td>LTC4302-1/LTC4302-2</td>
<td>Addressable 2-Wire Bus Buffer</td>
<td>Address Expansion, GPIO, Software Controlled</td>
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<tr>
<td>LTC4303/LTC4304</td>
<td>Hot Swappable 2-Wire Bus Buffers with Stuck Bus Recovery</td>
<td>Provides Automatic Clocking to Free Stuck I2C Busses</td>
</tr>
<tr>
<td>LTC4305/LTC4306</td>
<td>2-/4-Channel, 2-Wire Bus Multiplexers with Capacitance Buffering</td>
<td>2/4 Selectable Downstream Busses, Stuck Bus Disconnect, Rise Time Accelerators, Fault Reporting, ±10kV HBM ESD Tolerance</td>
</tr>
</tbody>
</table>

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